Sitronix

ST2203U

Integrated Microcontroller

P r e l i m i n a r y

Note: Sitronix Technology Corp. reserves the right to change the contents in this document without prior notice. This is not a final specification. Some parameters are subject to change.

Datasheet

Version 0.4

2006/12/22

Sitronix Technology Corporation

1 FEATURES

- **With 65C02, 8-bit CPU**
- **ROM:128K x 8-bit**
- **RAM: 2K x 8-bit**
- **Low Voltage Reset (LVR)**
- **Stack: Up to 128-level deep**
- **Operation voltage:**
  VDD: 2.4V ~ 3.6V
  VBTIN: 4.5V~6.8V(for internal regulator)
- **Operation frequency:**
  – 4/6MHz@2.4V(Min.),
  – 8.0Mhz@3.0V(Min.)
- **Low Voltage Detector (LVD)**
  –External battery level can be detected.
- **USB 2.0 full speed device (12Mbps)**
  – Integrate one PLL to produce 48Mhz clock
  – Built-in 3.3V regulator for transceiver
  – 4 endpoints with control, bulk in/out and interrupt in transfer
  – Double buffering mechanism
- **Memory configuration**
  – Internal RAM and ROM with bank switching mechanism
  – Support up to 28M bytes external memory
- **General-Purpose I/O (GPIO) ports**
  – 36 multiplexed CMOS bit programmable I/Os
  – Hardware de-bounce option for Port-A
  – Bit programmable pull-up/down or open-drain/CMOS
- **Watchdog Timer (WDT)**
  – Programmable WDT interrupt or reset
- **Four external Interrupt via I/O pin**
- **Timer/Counter**
  – Three 12-bit and one 8-bit timers
- **Clock output**
  – Four clock outputs
- **Prioritized interrupts with dedicated exception vectors**
  – External interrupt (edge triggered)
  – Port A interrupt (transition triggered)
  – Base timer interrupt (x8)
  – Timer0 ~2 interrupts (x3)
  – SPI interrupts (x2)
  – USB interrupts (x6)
  – RTC interrupts (x4)
- **Dual clock sources with warm-up timer**
  – Low frequency crystal oscillator (OSCX) …… 32768 Hz
  – High frequency crystal/resonator oscillator (OSC) …… 4/6/8M Hz
- **LCD Controller**
  – Programmable display size:
  – Share system memory with display buffer and with no loss of the CPU time
  – Support 1-bit/4-bit LCD data bus
  – Diverse functions including virtual screen, panning, scrolling, contrast control, alternating signal generator, buffer switching and fast graphic data manipulation
- **Serial Peripheral Interface (SPI)**
  – Master and slave modes
  – Five serial signals including enable and data-ready
  – Both transmitter and receiver buffers supported
  – Programmable data length from 7-bit to 16-bit
- **On-chip ICE debug interface**
- **Power management**
  – Auto switch to USB VCC when USB plug in
  – Less then 10uA stand-by current with 32K Xtal and RTC

2 BLOCK DIAGRAM

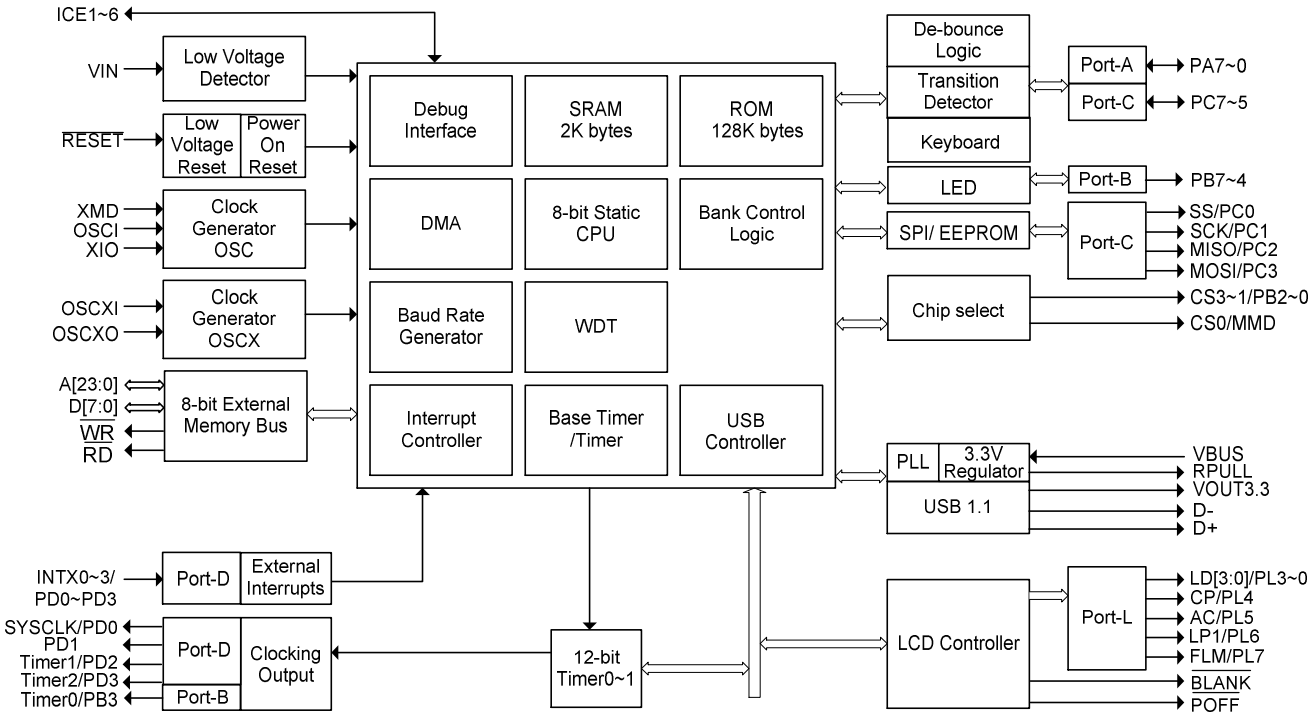


Figure 2-1 ST2203U Block Diagram

3 GENERAL DESCRIPTIONS

The ST2203U is an 8-bit integrated microcontroller designed with CMOS silicon gate technology. The true static CPU core, power down modes and dual oscillators design makes the ST2203U suitable for power saving and long battery life designs. The ST2203U integrates various logic to support functions on-chip which are needed by system designers. This is also important for lower system complexity, small board size and, of course, shorter time to market and less cost.

The ST2203U features the capacity of memory access of maximum 32M bytes which is needed by products with large data bases. Two chip selects are equipped for direct connection to external ROM, SRAM, or other devices. Maximum one single device of 8M bytes is possible.

One DMA channel makes fast data transfer possible and easy. Both source and destination pointers can refer to the whole memory space with 15-bit pointers and bank register.

The ST2203U has 36 I/Os grouped into 5 ports, Port-A ~ Port-D and Port-L. Each pin can be programmed to input or output. There are two options: pull-up/down for inputs of Port-C and only pull-up for inputs of the other ports. In case of output, there are open-drain/CMOS options for outputs of Port-C and only CMOS for other ports. Port-A is designed for keyboard scan with de-bounce and transition triggered interrupt, while Port-B/C/D are shared with other system functions. All the properties of I/O pins are still programmable when they are assigned to another function. This enlarges the flexibility of the usage of function signals.

The internal 2K bytes RAM helps to drive large LCD panels. The ST2203U can rich display

information and the diversity of contents as well. This is done with no need of external display RAM because of the special internal memory sharing design.

The ST2203U equips serial communication ports of one SPI to perform different communications. Communication via USB is becoming more and more popular. The ST2203U features one PLL, a 3.3V regulator, and a USB 2.0 full speed device engine to satisfy the strong demand of fast data transfer from market. Two classes of HID and Mass storage classes are supported as well as the firmware libraries and the Windows drivers.

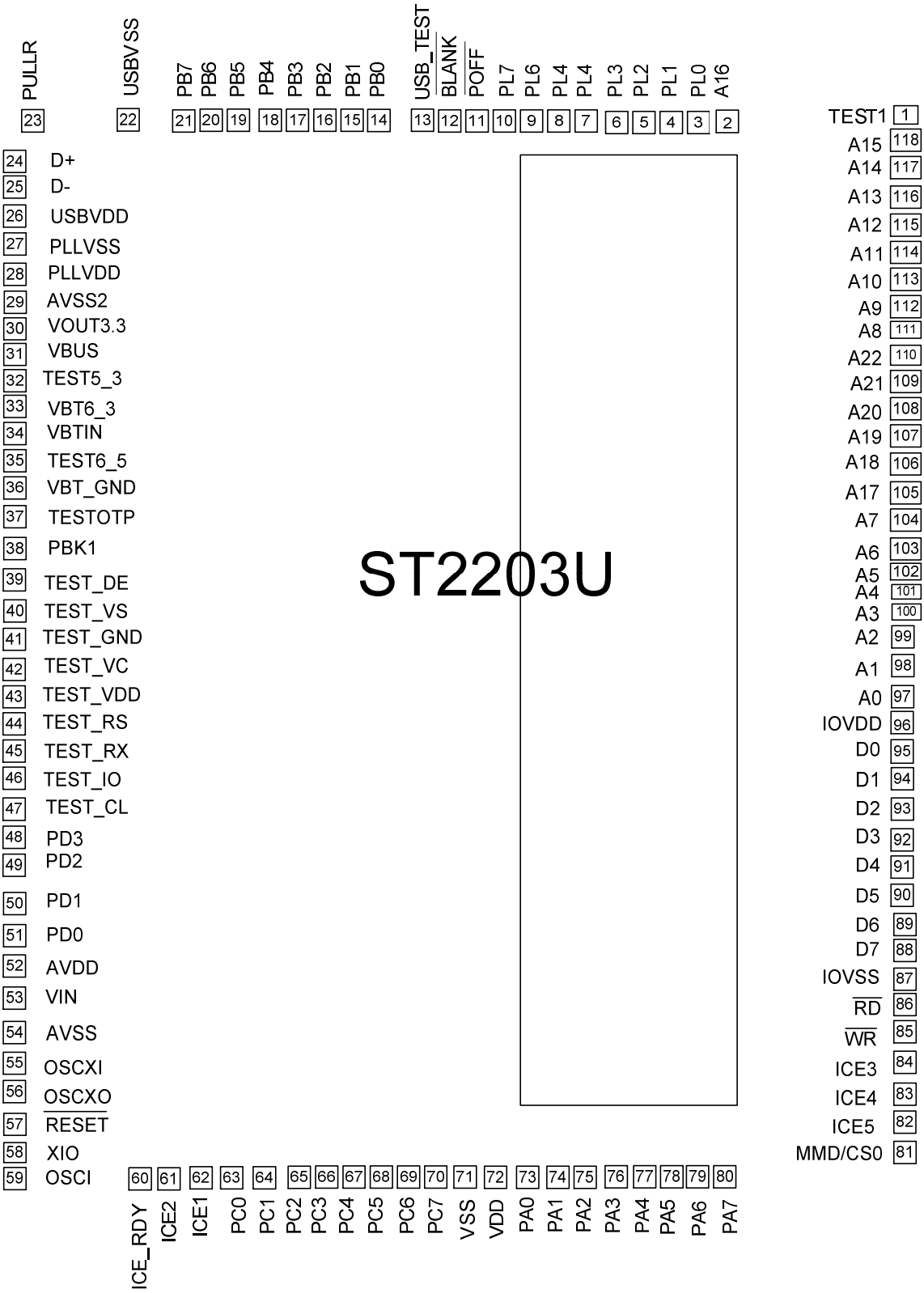
The ST2203U has one Low Voltage Detector (LVD) for power management. The status of external power can be detected and reported to the management software. Watch Dog Timer (WDT) is also built-in and is an essential function for a good design.

Power consumption is another big issue for a battery-powered device. The ST2203U has different power down modes and clock switch scheme to make the consuming power as low as possible.

The ST2203U equips an ICE debug interface for efficient development flow. Besides hardware emulator, a software simulator is also supported to save programmers setting up the system and makes programming be at anywhere.

With these integrated functions inside, the ST2203U single chip microcontroller is a right solution for PDA, translator, databank and other consumer products.

4 PAD DIGRAM


ST2203U
PULLR 23
USBVSS 22
PB7 21
PB6 20
PB5 19
PB4 18
PB3 17
PB2 16
PB1 15
PB0 14
USB_TEST 13
BLANK 12
POFF 11
PL7 10
PL6 9
PL4 8
PL4 7
PL3 6
PL2 5
PL1 4
PL0 3
A16 2
TEST1 1
A15 118
A14 117
A13 116
A12 115
A11 114
A10 113
A9 112
A8 111
A22 110
A21 109
A20 108
A19 107
A18 106
A17 105
A7 104
A6 103
A5 102
A4 101
A3 100
A2 99
A1 98
A0 97
IOVDD 96
D0 95
D1 94
D2 93
D3 92
D4 91
D5 90
D6 89
D7 88
IOVSS 87
RD 86
WR 85
ICE3 84
ICE4 83
ICE5 82
MMD/CS0 81
24 D+
25 D-
26 USBVDD
27 PLLVSS
28 PLLVDD
29 AVSS2
30 VOUT3.3
31 VBUS
32 TEST5_3
33 VBT6_3
34 VBTIN
35 TEST6_5
36 VBT_GND
37 TESTOTP
38 PBK1
39 TEST_DE
40 TEST_VS
41 TEST_GND
42 TEST_VC
43 TEST_VDD
44 TEST_RS
45 TEST_RX
46 TEST_IO
47 TEST_CL
48 PD3
49 PD2
50 PD1
51 PD0
52 AVDD
53 VIN
54 AVSS
55 OSCXI
56 OSCXO
57 RESET
58 XIO
59 OSCI
60 ICE_RDY
61 ICE2
62 ICE1
63 PC0
64 PC1
65 PC2
66 PC3
67 PC4
68 PC5
69 PC6
70 PC7
71 VSS
72 VDD
73 PA0
74 PA1
75 PA2
76 PA3
77 PA4
78 PA5
79 PA6
80 PA7

5 PAD DESCRIPTION

PAD #	Name	Description		
		Function1	Function2	Function3
1	TEST1	Test pin		
2	A16	Address[16]		
3	PL0	Port L[0]	d[0] of lcd driver	
4	PL1	Port L[1]	d[1] of lcd driver	
5	PL2	Port L[2]	d[2] of lcd driver	
6	PL3	Port L[3]	d[3] of lcd driver	
7	PL4	Port L[4]	cp of lcd dricer	
8	PL5	Port L[5]	ac of lcd driver	
9	PL6	Port L[6]	lp1 of lcd dricer	
10	PL7	Port L[7]	flm of lcd driver	
11	POFFB	Lcd pin, connect to the /POFF pin of LCD driver		
12	BLANKB	Lcd pin, connect to the /Blank pin of LCD driver		
13	USB_TEST	test pin		
14	PB0	Port B[0]	cs1	
15	PB1	Port B[1]	cs2	
16	PB2	Port B[2]	cs3	
17	PB3	Port B[3]	tco, timer0 output	
18	PB4	Port B[4]	led[0]	
19	PB5	Port B[5]	led[1]	
20	PB6	Port B[6]	led[2]	
21	PB7	Port B[7]	led[3]	
22	USBVSS	USB pins		
23	PULLR	D+ pull-up control; connect a 1.5K Ohm resistor to D+ pin		
24	D+	D+ pin of USB function		
25	D-	D- pin of USB function		
26	USBVDD	AVDD for USB		
27	PLLVSS	GND for USB VCO		
28	PLLVDD	VDD for USB VCO		
29	AVSS2	GND for USB		

30	VOUT3.3	3.3V regulator output pin; connect a Cap to AVSS2 pin		
31	VBUS	5V USB bus-power input pin		
32	TEST5_3	Reserved, NC		
33	VBT6_3	Internal regulator output		
34	VBTIN	Regulator input		
35	TEST6_5	Reserved, NC		
36	VBT_GND	Connected to GND		
37	TESTOTP	Reserved, must be connected to VSS		
38	PBK1	Reserved, must be connected to VSS		
39	TEST_DE	Reserved		
40	TEST_VS	Reserved, must be connected to GND		
41	TEST _GND	GND pin		
42	TEST _VC	Reserved, NC		
43	TEST _VD	Reserved ,NC		
44	TEST _RS	Reserved, NC		
45	TEST _RX	Reserved, NC		
46	TEST _IO	Reserved, NC		
47	TEST _CL	Reserved, NC		
48	PD3	Port D[3]	timer2 output	external edge trigger
49	PD2	Port D[2]	timer1 output	external edge trigger
50	PD1	Port D[1]	LCD Load2	external edge trigger
51	PD0	Port D[0]	system source clock	external edge trigger
52	AVDD	VDD pin of analog module		
53	VIN	Voltage input pin of low-voltage-detection function		
54	AVSS	GND pin of analog module		
55	OSCXI	32k crystal		
56	OSCXO	32k crystal		
57	RESETB	/RESET pin		
58	XIO	4,6,8MHz crystal connection pin		
59	OSCI	4,6,8MHz crystal connection pin		
60	ICE_RDY	(xmd)		

61	ICE2	Ice_pin(ice)		
62	ICE1	Ice_pin(rz)		
63	PC0	Port C[0]	SPI,ss pin	EEPROM, spin
64	PC1	Port C[1]	SPI, sck pin	EEPROM sck pin
65	PC2	Port C[2]	SPI, MISO pin	EEPROM di pin
66	PC3	Port C[3]	SPI, MOSI pin	EEPROM do pin
67	PC4	Port C[4]	SPI,readyb pin	
68	PC5	Port C[5]		
69	PC6	Port C[6]		
70	PC7	Port C[7]		
71	VSS	GND pin		
72	VDD	VDD pin		
73	PA0	Port A[0]		
74	PA1	Port A[1]		
75	PA2	Port A[2]		
76	PA3	Port A[3]		
77	PA4	Port A[4]		
78	PA5	Port A[5]		
79	PA6	Port A[6]		
80	PA7	Port A[7]		
81	MMD/CS0	Internal/external memory selection; connected to low to select internal ROM, connected to the /CS pin of a memory device to select an external memory.		
82	ICE5	Ice_pin(ice_mcsb)		
83	ICE4	Ice_pin(syncbpad)		
84	ICE3	Ice_pin (cpu_a15)		
85	WRB	/WR pin		
86	RDB	/RD pin		
87	IOVSS	GND pin of I/O function		
88	D7	Data[7]		
89	D6	Data[6]		
90	D5	Data[5]		
91	D4	Data[4]		
92	D3	Data[3]		
93	D2	Data[2]		
94	D1	Data[1]		
95	D0	Data[0]		

96	IOVDD	VDD pin of I/O function		
97	A0	Address[0]		
98	A1	Address[1]		
99	A2	Address[2]		
100	A3	Address[3]		
101	A4	Address[4]		
102	A5	Address[5]		
103	A6	Address[6]		
104	A7	Address[7]		
105	A17	Address[17]		
106	A18	Address[18]		
107	A19	Address[19]		
108	A20	Address[20]		
109	A21	Address[21]		
110	A22	Address[22]		
111	A8	Address[8]		
112	A9	Address[9]		
113	A10	Address[10]		
114	A11	Address[11]		
115	A12	Address[12]		
116	A13	Address[13]		
117	A14	Address[14]		
118	A15	Address[15]		

6 DEVICE INFORMATION

1. Pad size : 80um x 80um
2. Pad pitch : min: 100um corner: 110um
3. Chip size : 2720um x 4130um
4. Substrate: GND

PAD No.	Symbol	X	Y
1	TEST1	1290	1970
2	A16	1079.75	1995
3	PL0	959.75	1995
4	PL1	839.75	1995
5	PL2	739.75	1995
6	PL3	639.75	1995
7	PL4	539.75	1995
8	PL5	439.75	1995
9	PL6	339.75	1995
10	PL7	239.75	1995
11	POFFB	139.75	1995
12	BLANKB	39.75	1995
13	USB_TEST	-60.25	1995
14	PB0	-160.25	1995
15	PB1	-260.25	1995
16	PB2	-360.25	1995

PAD No.	Symbol	X	Y
29	AVSS2	-1290	1262.3
30	VOUT3.3	-1290	1101.88
31	VBUS	-1290	1001.88
32	TEST5_3	-1290	901.88
33	VBT6_3	-1290	801.87
34	VBTIN	-1290	701.87
35	TEST6_5	-1290	502.5
36	VBT_GND	-1290	402.5
37	TESTOTP	-1290	302.5
38	PBK1	-1290	202.5
39	TEST_DE	-1290	102.5
40	TEST_VS	-1290	2.5
41	TEST _GND	-1290	-97.5
42	TEST _VC	-1290	-197.5
43	TEST _VDD	-1290	-297.5
44	TEST _RS	-1290	-397.5

17	PB3	-460.25	1995
18	PB4	-560.25	1995
19	PB5	-660.25	1995
20	PB6	-760.25	1995
21	PB7	-860.25	1995
22	USBVSS	-1053	1995
23	PULLR	-1271.1	1995
24	D+	-1290	1794.7
25	D-	-1290	1674.7
26	USBVDD	-1290	1562.3
27	PLLVSS	-1290.2	1462.3
28	PLLVDD	-1290.2	1362.3
PAD No.	**Symbol**	**X**	**Y**
57	RESETB	-1290	-1730
58	XIO	-1290	-1850
59	OSCI	-1290	-1970
60	MMD/CS0	-1090	-1995
61	ICE2	-970	-1995
62	ICE1	-850	-1995
63	PC0	-750	-1995
64	PC1	-650	-1995
65	PC2	-550	-1995
66	PC3	-450	-1995
67	PC4	-350	-1995
68	PC5	-250	-1995
69	PC6	-150	-1995

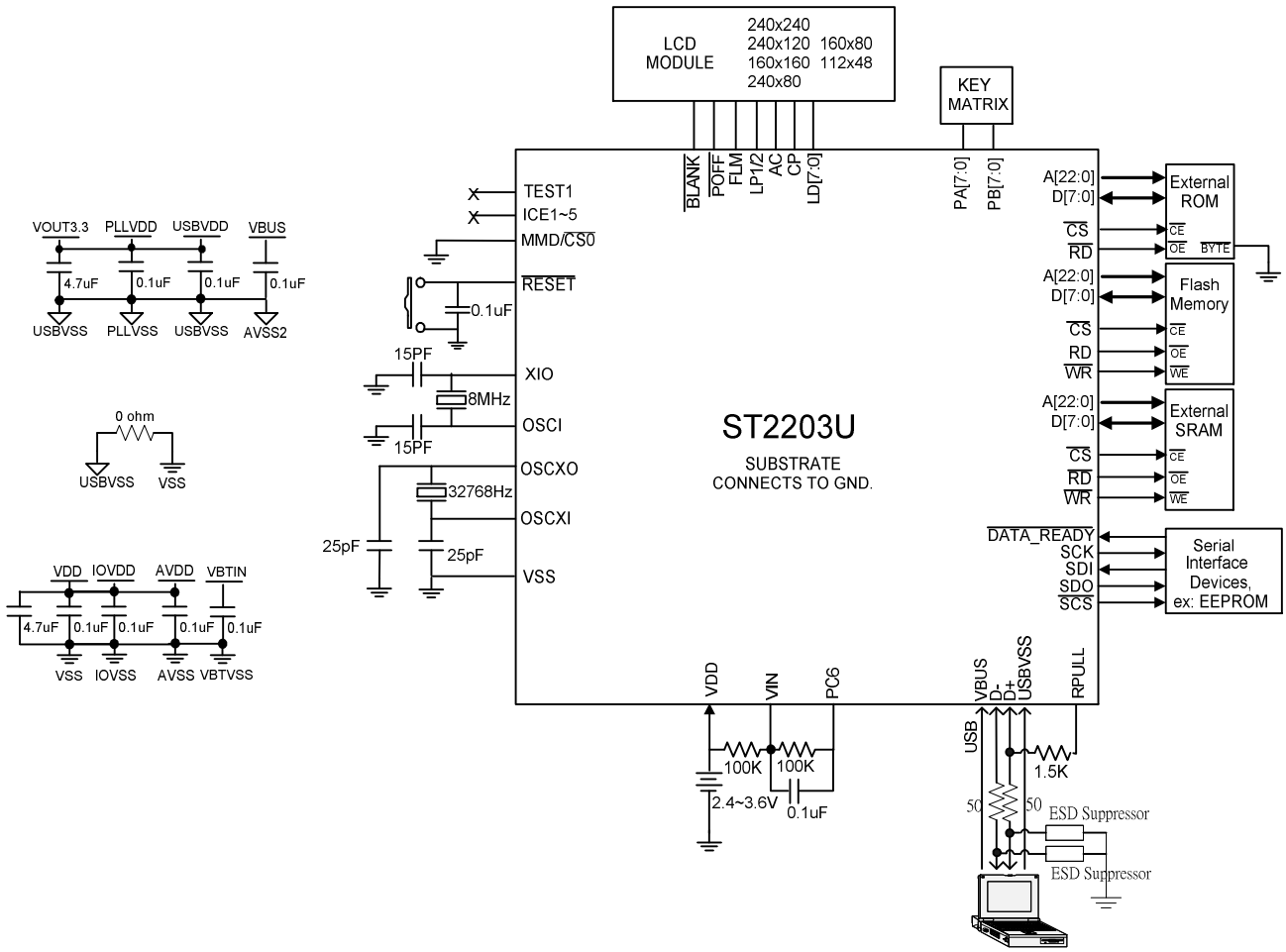
45	TEST _RX	-1290	-497.5
46	TEST _IO	-1290	-597.5
47	TEST _CL	-1290	-697.5
48	PD3	-1290	-807.4
49	PD2	-1290	-907.4
50	PD1	-1290	-1007.4
51	PD0	-1290	-1107.4
52	AVDD	-1290	-1207.4
53	VIN	-1290	-1320.1
54	AVSS	-1290	-1430
55	OSCXI	-1290	-1530
56	OSCXO	-1290	-1630
PAD No.	**Symbol**	**X**	**Y**
90	D5	1290	-1030
91	D4	1290	-930
92	D3	1290	-830
93	D2	1290	-730
94	D1	1290	-630
95	D0	1290	-530
96	IOVDD	1290	-370
97	A0	1290	-270
98	A1	1290	-170
99	A2	1290	-70
100	A3	1290	30
101	A4	1290	130
102	A5	1290	230

70	PC7	-50	-1995
71	VSS	50	-1995
72	VDD	250	-1995
73	PA0	350	-1995
74	PA1	450	-1995
75	PA2	550	-1995
76	PA3	650	-1995
77	PA4	750	-1995
78	PA5	850	-1995
79	PA6	970	-1995
80	PA7	1090	-1995
81	TEST2	1290	-1970
82	ICE5	1290	-1850
83	ICE4	1290	-1730
84	ICE3	1290	-1630
85	WRB	1290	-1530
86	RDB	1290	-1430
87	IOVSS	1290	-1330
88	D7	1290	-1230
89	D6	1290	-1130

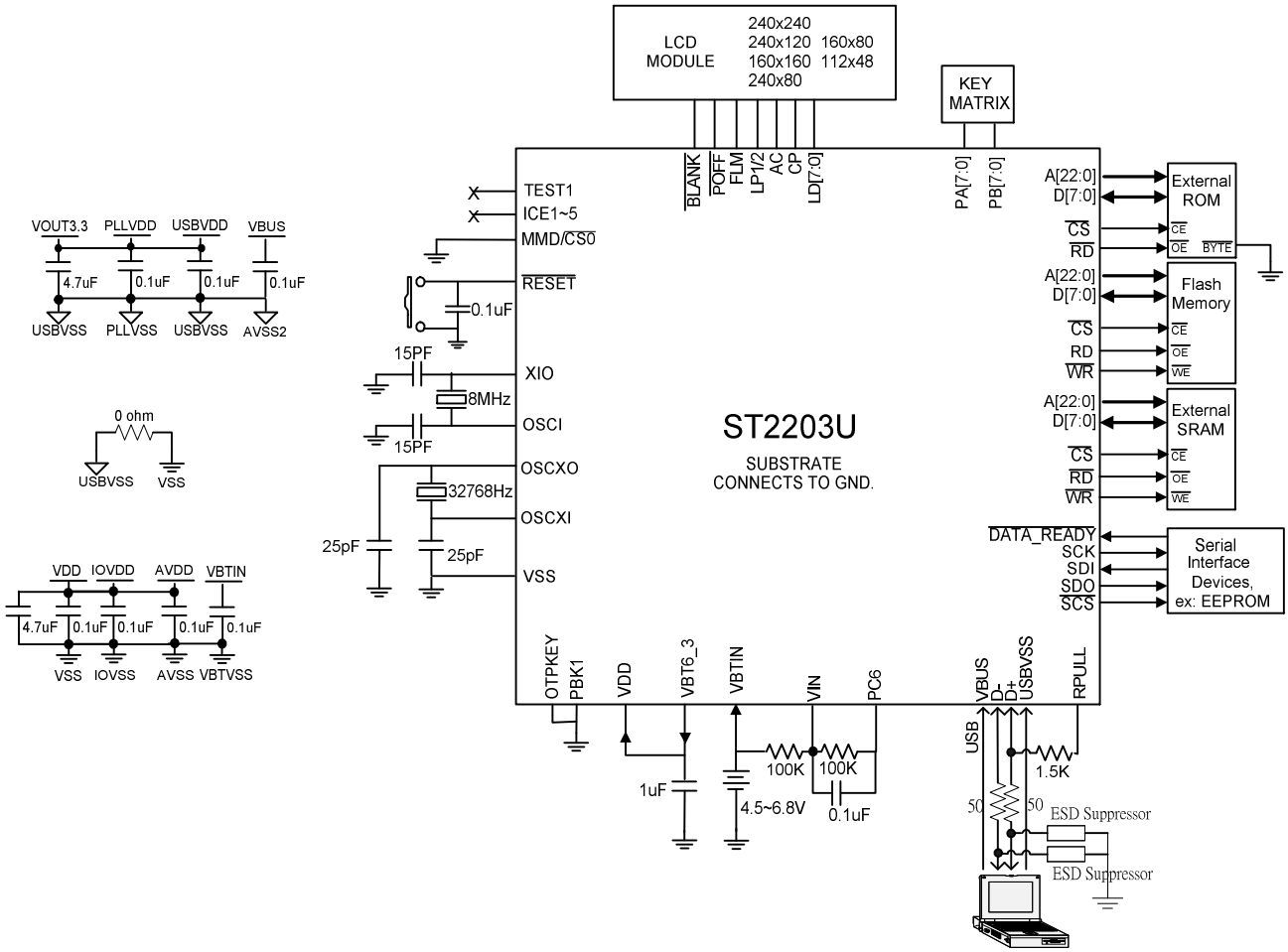
103	A6	1290	330
104	A7	1290	430
105	A17	1290	530
106	A18	1290	630
107	A19	1290	730
108	A20	1290	830
109	A21	1290	930
110	A22	1290	1030
111	A8	1290	1130
112	A9	1290	1230
113	A10	1290	1330
114	A11	1290	1430
115	A12	1290	1530
116	A13	1290	1630
117	A14	1290	1730
118	A15	1290	1850

7 APPLICATION CIRCUIT

The normal operation voltage range for ST2203U is 2.4~3.6V (VDD).



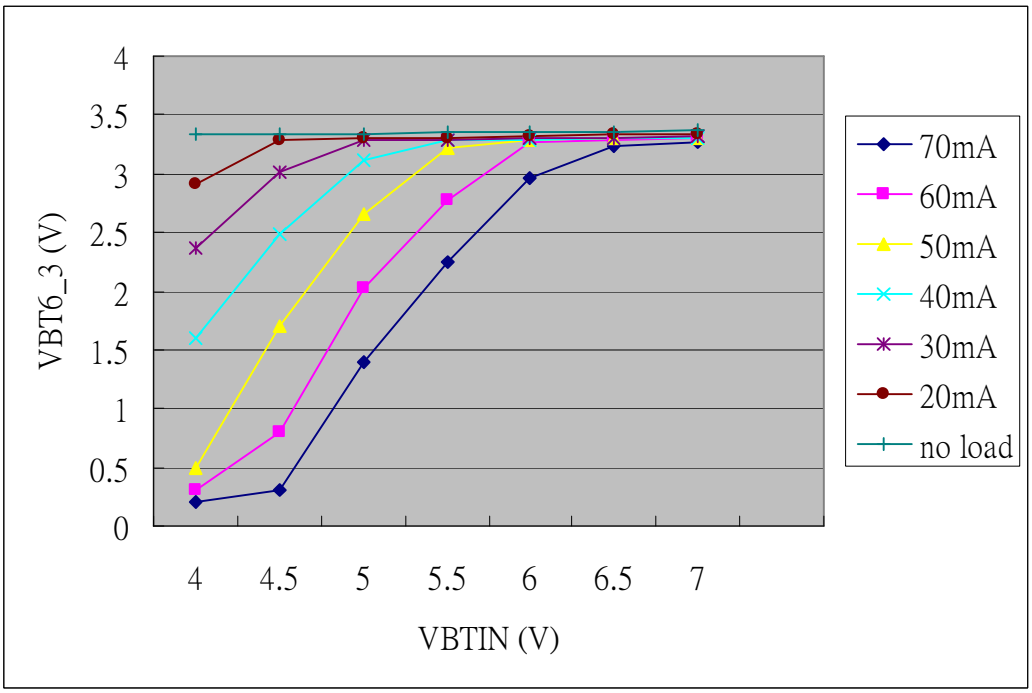
When using internal regulator output as system power, the application is shown below:



8 ELECTRICAL CHARACTERISTICS

8.1 Internal Regulator Load/Line Regulation

Standard operation conditions: T_A = 25°C, OSC =4MHz (system clock=4MHz), unless otherwise specified



VBTIN is the input of the regulator, and VBT6_3 is the output. One should notice the loading capability when using internal regulator.

8.2 DC Electrical Characteristics

Standard operation conditions: VCC = 3.0V, GND = 0V, T_A = 25°C, OSC =4MHz (system clock=4MHz), unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	VCC	2.4		3.6	V	
Operating Frequency(OSC)	F_1	4		8	MHz	VCC = 2.4V ~ 3.6V (system clock=8MHz)
Operating Current	I_{OP}		4	8	mA	All I/O port are input and pull-up, execute NOP instruction, LCDC on
Standby Current	I_{SB0}		800	1200	μA	All I/O port are input and pull-up, OSCX on, LCDC on (**WAIT0** mode) SEG=160, CP=SYS, LFRA=30
Standby Current	I_{SB1}		15	25	μA	All I/O port are input and pull-up, OSCX on, **heavy** load, LCDC off (**WAIT1** mode) LVR=1.9V
Standby Current	I_{SB2}		8	15	μA	All I/O port are input and pull-up, OSCX on, **normal** load, LCDC off (WAIT1 mode) LVR=1.9V
Standby Current	I_{SB3}		2	5	μA	All I/O port are input and pull-up, OSCX **off**, normal load LCDC off (WAIT1 mode) LVR=1.9V
Input High Voltage	V_{IH}	0.7Vcc			V	Port-A/B/C/D/E/L
Input Low Voltage	V_{IL}			0.3Vcc	V	Port-A/B/C/D/E/L
Pull-up resistance	R_{IH}	50	70	150	KΩ	Port-A/B/C/D/E/L (input Voltage=0.7VCC)
Output high voltage	V_{OH1}	0.7Vcc			V	Port-A/B/C/D/L (I_{OH} =-4.5mA)
Output low voltage	V_{OL1}			0.3Vcc	V	Port-A/B/C/D/E/L (I_{OL} =6.5mA)
Low Voltage Reset level	V_{LVR}	1.7	1.9	2.1	V	
Low Voltage Detect current	I_{LVR}		50	80	μA	Total LVD circuit current consumption
Warm up time	T_{WM1}		0.5	1	S	32768 Crystal Heavy mode.
			3	5	S	32768 Crystal Normal mode.
			15	30	mS	Main frequency crystal 32768 warm-up cycle

9 REVISION

REVISION	DESCRIPTION	PAGE	DATE
01	Original release		2006/10
02	Revise IC block diagram	3	2006/10/19
02a	Operating voltage	2	2006/11/01
03	Timer Section typing error	2	2006/11/2
	Pad diagram	5	2006/11/30
04	Pad diagram	5	2006/12/22
	Modify Application circuit	13, 14	
	Add section “Electrical characteristics”	15, 16	