Sitronix

ST7033

4 x 96 Dot Matrix LCD Controller/Driver

1. INTRODUCTION

The ST7033 is a driver & controller LSI for graphic dot-matrix liquid crystal display systems. It contains 96 segment and 4 common driver circuits. This chip is connected directly to a microprocessor, accepts 3-line serial peripheral interface (SPI), display data can stores in an on-chip display data RAM of 4 x 96 bits. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

Single-chip LCD controller & driver

Driver Output Circuits

- 4 common outputs / 96 segment. Output
- 96 segment drivers : up to forty-eight 8-segment numeric characters; up to twenty-five 15-segment alphanumeric characters; or any graphics of up to 384 elements

On-chip Display Data Ram

- Capacity: 4X96=384bits

Microprocessor Interface

- Parallel MPU interface: 8-bit parallel 6800-series or 8080-series
- Serial MPU interface: 4-line and 3-line SPI (serial peripheral interfaces) are available.

On-chip Low Power Analog Circuit

- Built-in Booster (x4 or x5) circuit generates LCD supply voltage (external V0/XV0 voltage supply is also supported).
- Built-in high-accuracy Regulator.
- Built-in voltage follower generates LCD bias voltages
- Built-in Oscillator requires no external components (external clock is also supported)

External RESB (reset) pin

Logic supply voltage range

- VDD1-VSS: 1.65V~3.4V
- VDD2-VSS: 2.5V~3.4V

Display supply voltage 4.0V

Temperature range: -30 to +80 degree

3. ST7033 PAD ARRANGEMENT (COG)

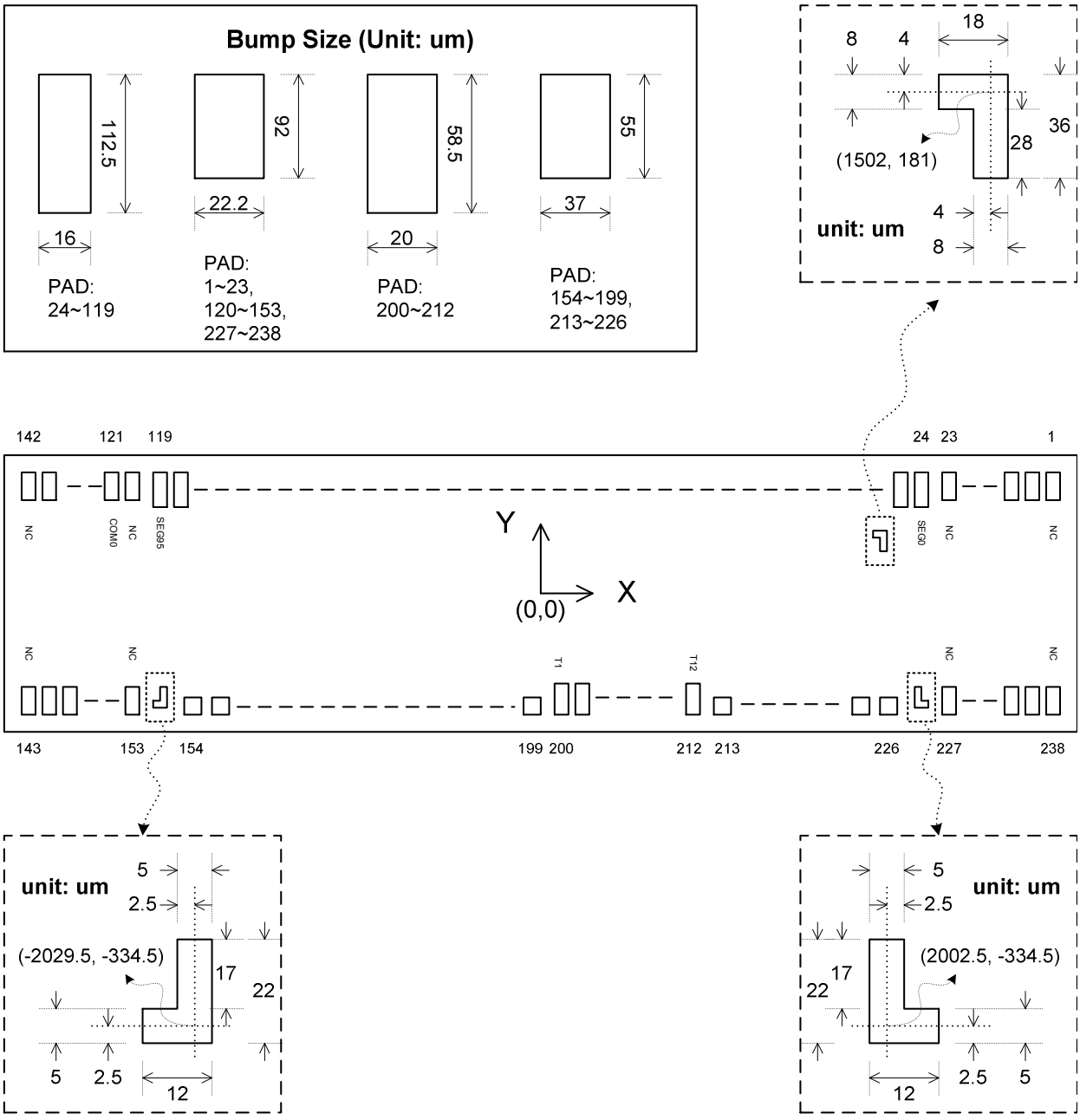
Dice Size: 5080um X 770um

Bump Height: 15um

Chip Thickness: 300um

Bump Pitch:

PAD Number	Pitch (um)	PAD Number	Pitch (um)
1~23, 120~142, 143~153, 227~238:	37.2	153-154:	86.97
24~119:	33	199-200	46.66
154~199, 213~226:	59.3	205-206, 206-207	38.8
200~205, 207~212:	33.3	212-213	53.44
23-24:	69.1	226-227	79.9
119-120:	60.70		



4-1. PAD CENTER COORDINATES

NO.	NAME	X	Y
1	NC	2450.80	293.00
2	NC	2413.60	293.00
3	NC	2376.40	293.00
4	NC	2339.20	293.00
5	NC	2302.00	293.00
6	NC	2264.80	293.00
7	NC	2227.60	293.00
8	NC	2190.40	293.00
9	NC	2153.20	293.00
10	NC	2116.00	293.00
11	NC	2078.80	293.00
12	NC	2041.60	293.00
13	NC	2004.40	293.00
14	NC	1967.20	293.00
15	NC	1930.00	293.00
16	NC	1892.80	293.00
17	NC	1855.60	293.00
18	NC	1818.40	293.00
19	NC	1781.20	293.00
20	NC	1744.00	293.00
21	NC	1706.80	293.00
22	NC	1669.60	293.00
23	NC	1632.40	293.00
24	SEG[0]	1563.30	282.75
25	SEG[1]	1530.30	282.75
26	SEG[2]	1497.30	282.75
27	SEG[3]	1464.30	282.75
28	SEG[4]	1431.30	282.75
29	SEG[5]	1398.30	282.75
30	SEG[6]	1365.30	282.75
31	SEG[7]	1332.30	282.75
32	SEG[8]	1299.30	282.75
33	SEG[9]	1266.30	282.75
34	SEG[10]	1233.30	282.75
35	SEG[11]	1200.30	282.75
36	SEG[12]	1167.30	282.75
37	SEG[13]	1134.30	282.75
38	SEG[14]	1101.30	282.75
39	SEG[15]	1068.30	282.75
40	SEG[16]	1035.30	282.75
41	SEG[17]	1002.30	282.75
42	SEG[18]	969.30	282.75
43	SEG[19]	936.30	282.75
44	SEG[20]	903.30	282.75
45	SEG[21]	870.30	282.75

NO.	NAME	X	Y
46	SEG[22]	837.30	282.75
47	SEG[23]	804.30	282.75
48	SEG[24]	771.30	282.75
49	SEG[25]	738.30	282.75
50	SEG[26]	705.30	282.75
51	SEG[27]	672.30	282.75
52	SEG[28]	639.30	282.75
53	SEG[29]	606.30	282.75
54	SEG[30]	573.30	282.75
55	SEG[31]	540.30	282.75
56	SEG[32]	507.30	282.75
57	SEG[33]	474.30	282.75
58	SEG[34]	441.30	282.75
59	SEG[35]	408.30	282.75
60	SEG[36]	375.30	282.75
61	SEG[37]	342.30	282.75
62	SEG[38]	309.30	282.75
63	SEG[39]	276.30	282.75
64	SEG[40]	243.30	282.75
65	SEG[41]	210.30	282.75
66	SEG[42]	177.30	282.75
67	SEG[43]	144.30	282.75
68	SEG[44]	111.30	282.75
69	SEG[45]	78.30	282.75
70	SEG[46]	45.30	282.75
71	SEG[47]	12.30	282.75
72	SEG[48]	-20.71	282.75
73	SEG[49]	-53.71	282.75
74	SEG[50]	-86.71	282.75
75	SEG[51]	-119.71	282.75
76	SEG[52]	-152.71	282.75
77	SEG[53]	-185.71	282.75
78	SEG[54]	-218.71	282.75
79	SEG[55]	-251.71	282.75
80	SEG[56]	-284.71	282.75
81	SEG[57]	-317.71	282.75
82	SEG[58]	-350.71	282.75
83	SEG[59]	-383.71	282.75
84	SEG[60]	-416.71	282.75
85	SEG[61]	-449.71	282.75
86	SEG[62]	-482.71	282.75
87	SEG[63]	-515.71	282.75
88	SEG[64]	-548.71	282.75
89	SEG[65]	-581.71	282.75
90	SEG[66]	-614.71	282.75

NO.	NAME	X	Y
91	SEG[67]	-647.71	282.75
92	SEG[68]	-680.71	282.75
93	SEG[69]	-713.71	282.75
94	SEG[70]	-746.71	282.75
95	SEG[71]	-779.71	282.75
96	SEG[72]	-812.71	282.75
97	SEG[73]	-845.71	282.75
98	SEG[74]	-878.71	282.75
99	SEG[75]	-911.71	282.75
100	SEG[76]	-944.71	282.75
101	SEG[77]	-977.71	282.75
102	SEG[78]	-1010.71	282.75
103	SEG[79]	-1043.71	282.75
104	SEG[80]	-1076.71	282.75
105	SEG[81]	-1109.71	282.75
106	SEG[82]	-1142.71	282.75
107	SEG[83]	-1175.71	282.75
108	SEG[84]	-1208.71	282.75
109	SEG[85]	-1241.71	282.75
110	SEG[86]	-1274.71	282.75
111	SEG[87]	-1307.71	282.75
112	SEG[88]	-1340.71	282.75
113	SEG[89]	-1373.71	282.75
114	SEG[90]	-1406.71	282.75
115	SEG[91]	-1439.71	282.75
116	SEG[92]	-1472.71	282.75
117	SEG[93]	-1505.71	282.75
118	SEG[94]	-1538.71	282.75
119	SEG[95]	-1571.71	282.75
120	NC	-1632.40	293.00
121	COM[0]	-1669.60	293.00
122	COM[1]	-1706.80	293.00
123	COM[2]	-1744.00	293.00
124	COM[3]	-1781.20	293.00
125	NC	-1818.40	293.00
126	NC	-1855.60	293.00
127	NC	-1892.80	293.00
128	NC	-1930.00	293.00
129	NC	-1967.20	293.00
130	NC	-2004.40	293.00
131	NC	-2041.60	293.00
132	NC	-2078.80	293.00
133	NC	-2116.00	293.00
134	NC	-2153.20	293.00
135	NC	-2190.40	293.00
136	NC	-2227.60	293.00
137	NC	-2264.80	293.00
138	NC	-2302.00	293.00

NO.	NAME	X	Y
139	NC	-2339.20	293.00
140	NC	-2376.40	293.00
141	NC	-2413.60	293.00
142	NC	-2450.80	293.00
143	NC	-2450.80	-293.00
144	NC	-2413.60	-293.00
145	NC	-2376.40	-293.00
146	NC	-2339.20	-293.00
147	NC	-2302.00	-293.00
148	NC	-2264.80	-293.00
149	NC	-2227.60	-293.00
150	NC	-2190.40	-293.00
151	NC	-2153.20	-293.00
152	NC	-2116.00	-293.00
153	NC	-2078.80	-293.00
154	VM	-1991.84	-311.50
155	VM	-1932.53	-311.50
156	VM	-1873.23	-311.50
157	VGO	-1813.92	-311.50
158	VGO	-1754.62	-311.50
159	VGI	-1695.31	-311.50
160	VGI	-1636.01	-311.50
161	VGI	-1576.70	-311.50
162	VGI	-1517.40	-311.50
163	VGS	-1458.09	-311.50
164	/RESB	-1398.79	-311.50
165	/CSB	-1339.49	-311.50
166	PS0	-1280.18	-311.50
167	PS1	-1220.88	-311.50
168	TMX	-1161.57	-311.50
169	TMY	-1102.27	-311.50
170	BR	-1042.96	-311.50
171	MODE	-983.66	-311.50
172	CP	-924.35	-311.50
173	VSS	-865.05	-311.50
174	VSS	-805.74	-311.50
175	VSS	-746.43	-311.50
176	VSS	-687.13	-311.50
177	VSS	-627.83	-311.50
178	RW_WR	-568.52	-311.50
179	E_RD	-509.22	-311.50
180	DA	-449.91	-311.50
181	A0	-390.61	-311.50
182	D[7]	-331.30	-311.50
183	D[6]	-272.00	-311.50
184	D[5]	-212.69	-311.50
185	D[4]	-153.39	-311.50
186	D[3]	-94.08	-311.50

NO.	NAME	X	Y
187	D[2]	-34.78	-311.50
188	D[1]	24.54	-311.50
189	D[0]	83.84	-311.50
190	OSC	143.15	-311.50
191	VDD1	202.45	-311.50
192	VDD1	261.75	-311.50
193	VDD1	321.06	-311.50
194	VDD1	380.37	-311.50
195	VDD2	439.67	-311.50
196	VDD2	498.97	-311.50
197	VDD2	558.28	-311.50
198	VDD2	617.59	-311.50
199	VRS	676.89	-311.50
200	T[1]	723.54	-307.75
201	T[2]	756.84	-307.75
202	T[3]	790.14	-307.75
203	T[4]	823.44	-307.75
204	T[5]	856.74	-307.75
205	T[6]	890.04	-307.75
206	T[0]	928.84	-307.75
207	T[7]	967.64	-307.75
208	T[8]	1000.94	-307.75
209	T[9]	1034.24	-307.75
210	T[10]	1067.54	-307.75
211	T[11]	1100.84	-307.75
212	T[12]	1134.14	-307.75
213	V0O	1187.58	-311.50
214	V0O	1246.89	-311.50
215	V0I	1306.20	-311.50
216	V0I	1365.50	-311.50
217	V0I	1424.80	-311.50
218	V0I	1484.11	-311.50
219	V0S	1543.42	-311.50
220	XV0O	1605.87	-311.50
221	XV0O	1665.17	-311.50
222	XV0I	1724.48	-311.50
223	XV0I	1783.79	-311.50
224	XV0I	1843.09	-311.50
225	XV0I	1902.39	-311.50
226	XV0S	1961.70	-311.50
227	NC	2041.60	-293.00
228	NC	2078.80	-293.00
229	NC	2116.00	-293.00
230	NC	2153.20	-293.00
231	NC	2190.40	-293.00
232	NC	2227.60	-293.00
233	NC	2264.80	-293.00

NO.	NAME	X	Y
234	NC	2302.00	-293.00
235	NC	2339.20	-293.00
236	NC	2376.40	-293.00
237	NC	2413.60	-293.00
238	NC	2450.80	-293.00

5. BLOCK DIAGRAM

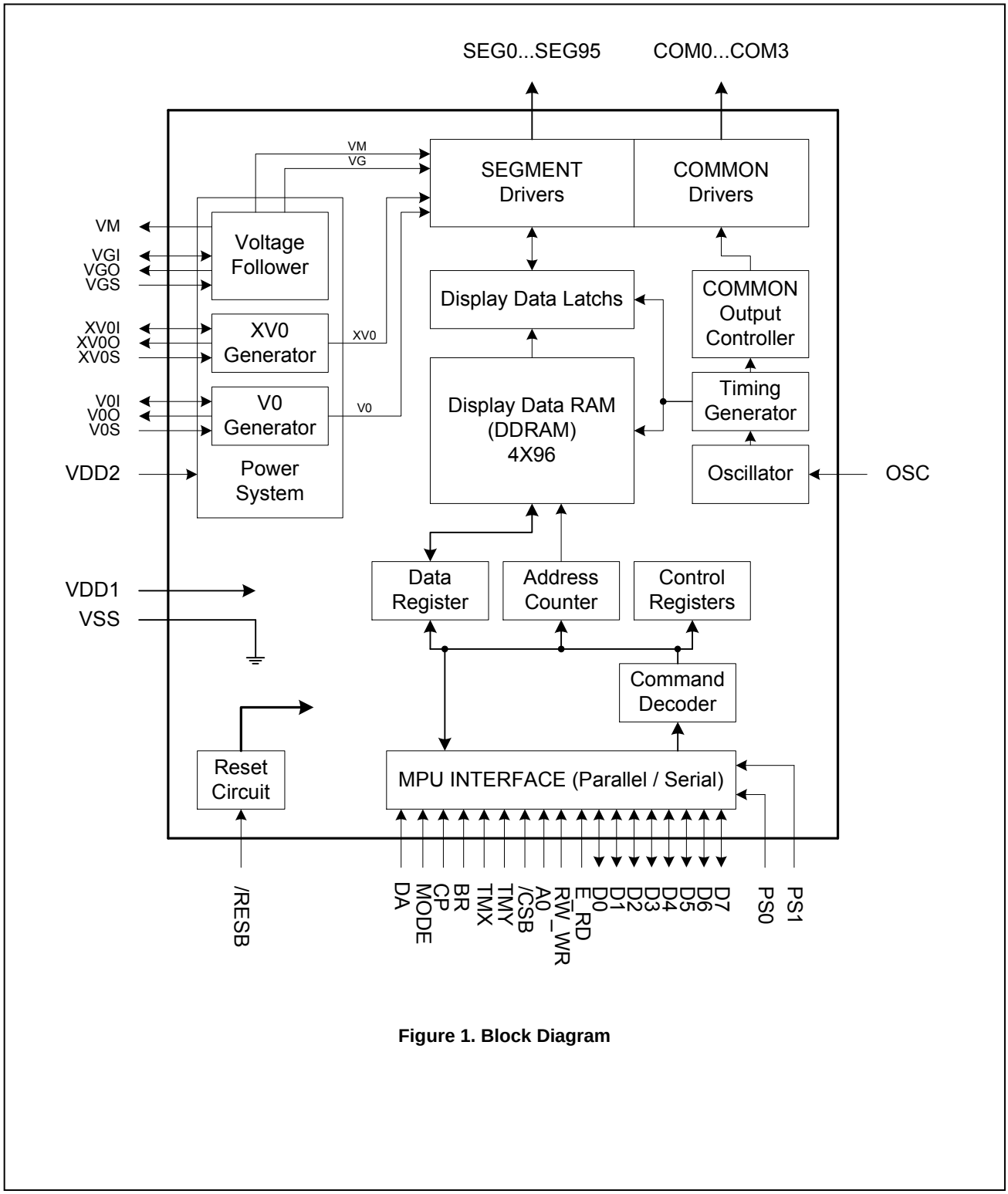


Figure 1. Block Diagram

6. PINNING DESCRIPTIONS

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Pin Count</th></tr>
<tr><td colspan="4">LCD driver outputs</td></tr>
<tr><td>SEG0 to SEG95</td><td>O</td><td>LCD segment driver outputs.
The display data and the M signal control the output voltage of segment driver.
<table>
<tr><th rowspan="2">Display data</th><th rowspan="2">Frame</th><th colspan="2">Segment drover output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>-</td><td>VG</td><td>VSS</td></tr>
<tr><td>H</td><td>+</td><td>VSS</td><td>VG</td></tr>
<tr><td>L</td><td>-</td><td>VSS</td><td>VG</td></tr>
<tr><td>L</td><td>+</td><td>VG</td><td>VSS</td></tr>
<tr><td colspan="2">Power save mode</td><td>VSS</td><td>VSS</td></tr>
</table></td><td>96</td></tr>
<tr><td>COM0 to COM3</td><td>O</td><td>LCD column driver outputs.
The internal scanning data and the M signal control the output voltage of common driver.
<table>
<tr><th rowspan="2">Display data</th><th rowspan="2">Frame</th><th colspan="2">Common drover output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>-</td><td colspan="2">XV0</td></tr>
<tr><td>H</td><td>+</td><td colspan="2">V0</td></tr>
<tr><td>L</td><td>-</td><td colspan="2">VM</td></tr>
<tr><td>L</td><td>+</td><td colspan="2">VM</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">VSS</td></tr>
</table></td><td>68</td></tr>
<tr><td colspan="4">MICROPROCESSOR INTERFACE</td></tr>
<tr><td>PS[1,0]</td><td>I</td><td>Microprocessor interface mode selection pins.
<table>
<tr><th>PS1</th><th>PS0</th><th>Interface Mode</th></tr>
<tr><td>1</td><td>1</td><td>8080-series parallel MPU interface</td></tr>
<tr><td>1</td><td>0</td><td>6800-series parallel MPU interface</td></tr>
<tr><td>0</td><td>1</td><td>4-line SPI MPU interface</td></tr>
<tr><td>0</td><td>0</td><td>3-line SPI MPU interface</td></tr>
</table></td><td>2</td></tr>
<tr><td>/CSB</td><td>I</td><td>Chip select input pin.
Data/instruction I/O is enabled only when /CSB is "L". When chip select is non-active, D7…D0 are high impedance.</td><td>1</td></tr>
<tr><td>/RESB</td><td>I</td><td>Reset input pin.
When /RESB is "L", initialization is executed.</td><td>1</td></tr>
<tr><td>A0</td><td>I</td><td>It determines whether the data bits are data or a command.
A0=" H “: Indicates that D0 to D7 are display data.
A0=" L “: Indicates that D0 to D7 are control data.
There is no A0 pin in three line , so this pin can fix to ” H”</td><td>1</td></tr>
<tr><td>RW_WR</td><td>I</td><td>Read/Write operation control pin (if using Parallel interface).
<table>
<tr><th>MPU Type</th><th>RW_WR</th><th>Interface Mode</th></tr>
<tr><td>6800-series</td><td>R/W</td><td>R/W=”H”: Read;
R/W=”L”: Write.</td></tr>
<tr><td>8080-series</td><td>/WR</td><td>Signals (Instruction or Data) on data bus will be latched at the raising edge of this signal.</td></tr>
</table></td><td>1</td></tr>
</table>

<table>
<tr><td>E_RD</td><td>I</td><td>Read/Write operation control pin (if using Parallel interface).<table><tr><th>MPU Type</th><th>E_RD</th><th>Interface Mode</th></tr><tr><td>6800-series</td><td>E</td><td>Signals (Instruction or Data) on data bus will be latched by MPU or this IC (depends on R/W) at the falling edge of this signal.</td></tr><tr><td>8080-series</td><td>/RD</td><td>Internal status (or display data) will be read out to data bus after the falling edge of this signal.</td></tr></table></td><td>1</td></tr>
<tr><td>D0…D7</td><td>I</td><td>Data Bus. If /CSB signal is not actived, D7…D0 are high impedance.
● Parallel interface (6800 or 8080):
I/O port which is connected to the standard 8-bit MPU data bus.
● Serial SPI interface (3 line or 4 line):
SCLK: D0;
SDA: D1~D3;
D4~D7 must connect to VDD1.</td><td>8</td></tr>
<tr><td colspan="4">LCD DRIVER SUPPLY</td></tr>
<tr><td>OSC</td><td>I</td><td>● OSC=”H”: Use the built-in oscillator.
● OSC=”L”: Both external clock and built-in oscillator are inhibited. And the display circuits will not be clocked and kept in a DC state. To avoid this, the chip should always be put into Power-Down Mode before stopping the clock.
● If using external clock, connect this pin to the external clock.</td><td>1</td></tr>
<tr><td colspan="4">POWER SUPPLY</td></tr>
<tr><td>VSS</td><td>Power</td><td>Ground.</td><td>5</td></tr>
<tr><td>VDD1</td><td>Power</td><td>Digital circuits supply voltage.
The 2 power supply rails, VDD1 and VDD2, could be connected together.
Use this power to be the high voltage level for the Option pins.</td><td>4</td></tr>
<tr><td>VDD2</td><td>Power</td><td>Analog circuits supply voltage.
The 2 power supply rails, VDD and VDD2, could be connected together.</td><td>4</td></tr>
<tr><td>XV0I, XV0O, XV0S</td><td>Power Supply</td><td>Negative LCD driver supply voltages.
XV0I, XV0O & XV0S should be separated in ITO layout.
XV0I, XV0O & XV0S should be connected together in FPC layout.</td><td>7</td></tr>
<tr><td>V0I, V0O, V0S;
VGI, VGO, VGS</td><td>Power Supply</td><td>This is a multi-level power supply for the liquid crystal.
V0 ≥ VG ≥ VM ≥ VSS ≥ XV0
V0I, V0O & V0S should be separated in ITO layout.
V0I, V0O & V0S should be connected together in FPC layout.
VGI, VGO & VGS should be separated in ITO layout.
VGI, VGO & VGS should be connected together in FPC layout.</td><td>6</td></tr>
<tr><td>VM</td><td>Power Supply</td><td>LCD driving voltage for commons.</td><td>3</td></tr>
<tr><td>VRS</td><td>Power</td><td>Reserved to monitor internal Voltage Regulator reference level, must be left open.</td><td>1</td></tr>
<tr><td colspan="4">Configuration Pins</td></tr>
<tr><td>MODE</td><td>I</td><td>Test pin.
<u>Must fix to “L”</u></td><td>1</td></tr>
<tr><td>CP</td><td>I</td><td>Set Booster stage.
VSS=4X;
VDD=5X.</td><td>1</td></tr>
</table>

BR	I	Test pin. **Must fix to "L"**	1
Test Pin			
T0~T12	---	Test pins. Do not use these pins.	13
TMX	I	Mirror X: SEG bi-direction selection (refer to pad center coordinates). TMX connect to VSS :MX mode1(refer to segment driver direction select) TMX connect to VDD1 :MX mode2(refer to segment driver direction select)	1
TMY	I	Mirror Y: COM bi-direction selection (refer to pad center coordinates). TMY connect to VSS: MY mode1(refer to common driver direction select) TMY connect to VDD1: MY mode2(refer to common driver direction select)	1
DA	I	Test pin. **Must fix to "L"**	1

Recommended I/O PIN ITO Resistance Limitation

PIN Name	ITO Resister
PS[1:0],OSC,CP,BR	<5KΩ
T0~T12,VRS	Floating
VDD1, VDD2, VSS	<100Ω
V0, VG , VM , XV0	<500Ω
A0,/WR,/RD,/CSB, D0 …D7	<1KΩ
/RESB	RESB<10KΩ

7. FUNCTIONS DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

There is /CSB pin for chip selection. The ST7033 can interface with an MPU when /CSB is "L". When /CSB is “H”, the internal shift register and the counter are reset.

Parallel / Serial Interface

ST7033 has five types of interface with an MPU, which are three serial and two parallel interfaces. This parallel or serial interface is determined by PS [1:0] pin as shown in Table 1.

PS1	PS0	/CSB	A0	State
H	H	/CSB	A0	8080-series parallel MPU interface
H	L	/CSB	A0	6800-series parallel MPU interface
L	H	/CSB	A0	4 Pin-SPI MPU interface
L	L	/CSB	" * "	3 Pin-SPI MPU interface

Table 1. Parallel/Serial Interface Mode

Parallel Interface

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by PS1~PS0 as shown in Table 2. The type of data transfer is determined by signals at A0, /RD (E) and /WR(R/W) as shown in Table 3.

PS1	PS0	/CSB	A0	/RD (E)	/WR (R/W)	DB0 to DB7	MPU bus
H	H	/CSB	A0	/RD	/WR	DB0 to DB7	8080-series
H	L	/CSB	A0	E	R/W	DB0 to DB7	6800-series

Table 2. Microprocessor Selection for Parallel Interface

Common	6800-series		8080-series		Description
A0	E	R/W	/RD	/WR	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

Table 3. Parallel Data Transfer

NOTE: By fixing /RD (E) pin at high (VDD1) in 6800-series interface mode, /CSB can be used as enable signal. In this case, interface data is latched at the rising edge of /CSB and the access type is determined by signals on A0, /WR(R/W) just same as 6800-series mode.

Serial Interface

Serial Mode	PS1	PS0	/CSB	A0
4-line SPI interface	L	H	/CSB	Used
3-line SPI interface	L	L	/CSB	Not Used Fix to “H”

Table 4. Microprocessor Selection for Serial Interface

PS1= “L”, PS0= “H”: 4-line SPI interface

When the ST7033 is active (/CSB=”L”), serial data (D1) and serial clock (D0) inputs are enabled. When /CSB is “High”, the internal 8-bit shift register and the 3-bit counter are reset. The display data/command indication is controlled by the register selection pin (A0). The signals transferred on data bus will be display data when A0 is high and will be instruction when A0 is low. The read feature is not supported in this mode. Serial data on SDA (D1) is latched at the rising edge of serial clock on SCLK (D0). After the eighth serial clock, the serial data will be processed as 8-bit parallel data. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access.

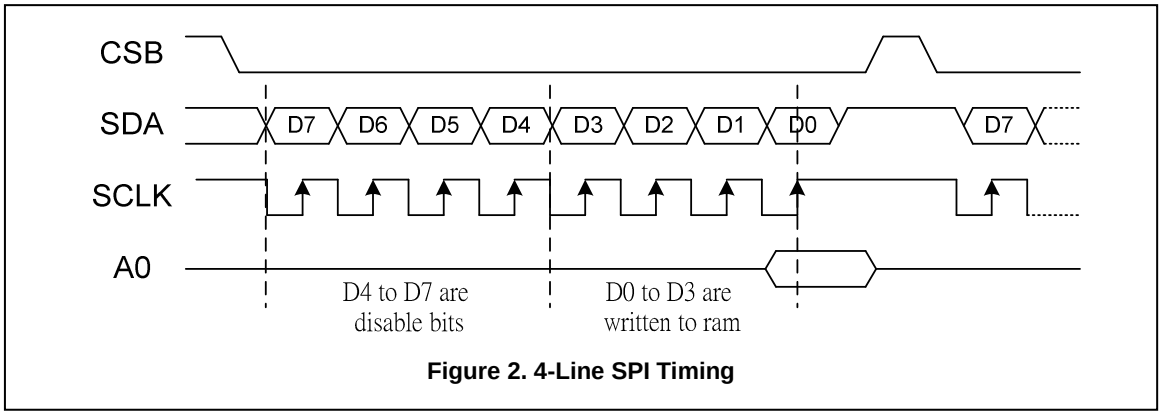


Figure 2. 4-Line SPI Timing

3-line SPI interface

When ST7033 is active (/CSB=”L”), SDA-out, SDA-in and SCL inputs are enabled. When ST7033 is not active (/CSB=”H”), the internal 8-bit shift register and the 3-bit counter are reset. The A0 pin is not available in this mode. Before issuing serial data, an A0 bit is required to indicate the access is data or instruction. The read feature is not supported in this mode except ID code read feature. Serial data on SDA (D1) is latched at the rising edge of serial clock on SCLK (D0). After the eighth serial clock, the serial data will be processed as 8-bit parallel data. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access.

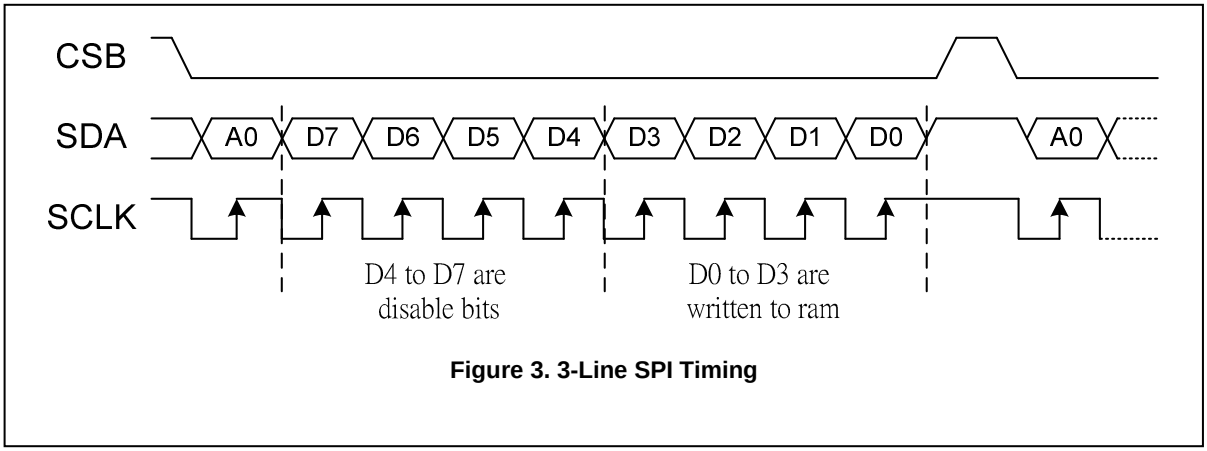


Figure 3. 3-Line SPI Timing

DISPLAY DATA RAM (DDRAM)

The ST7033 contains a 4x96 bit static RAM that stores the display data. The display data RAM store the dot data for the LCD.It is 4-row by 96-column addressable array. Each pixel can be selected when the column addresses are specified.Data are written to ram directly through D0 to D3 and D4 to D7 are disabled bits. The display data from the microprocessor correspond to the LCD common lines. The microprocessor can write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting Line Address repeatedly.At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the line address for transferring the 96-bit RAM data to the display data latch circuit.

Column Address Circuit

Column Address Circuit has an 8-bit preset counter that provides Column Address to the Display Data RAM. The display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data write command. This allows the MPU display data to be accessed continuously.

ADDRESSING

Data is downloaded in bytes into the RAM matrix of ST7033 as indicated in Figure 4. The display RAM has a matrix of 4 by 96 bits. The address pointer addresses the columns. The column address ranges are: 0 to 95 (1011111), .Addresses outside these ranges are not allowed. After the last column address (95) wraps around to 0 .

Data Structure

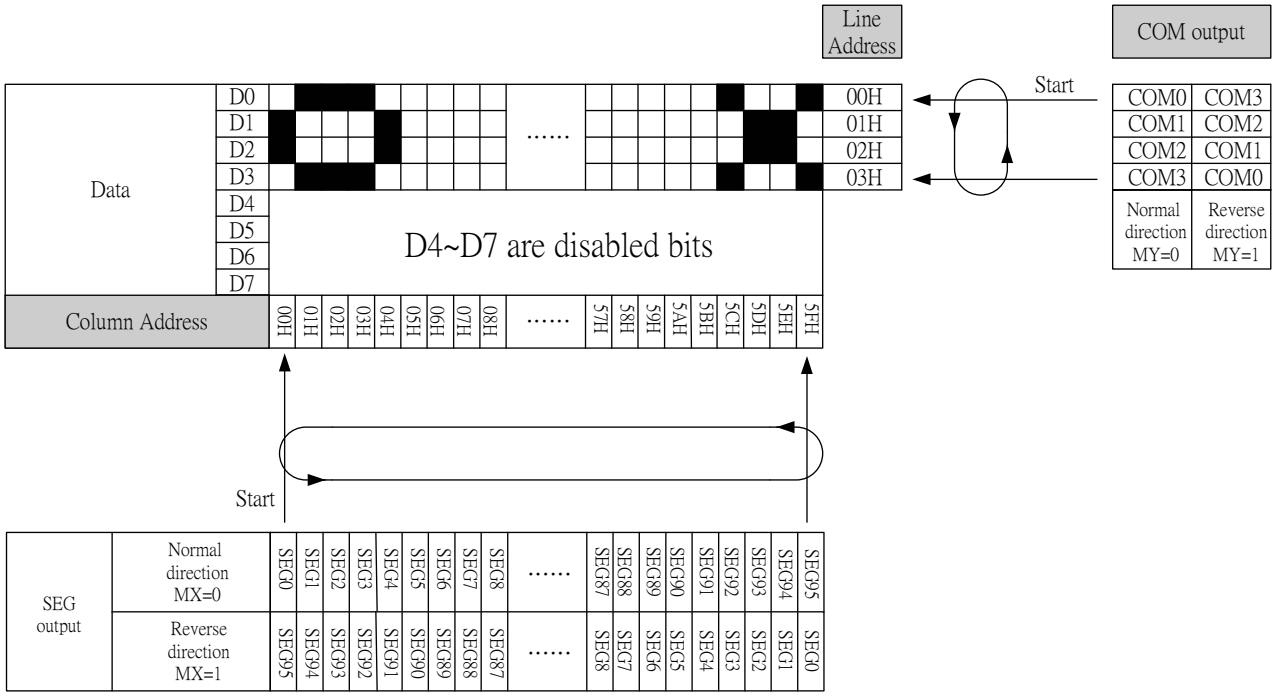
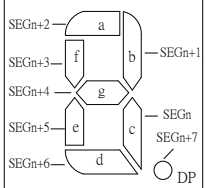


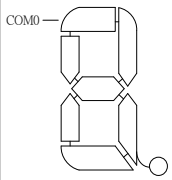
Figure 4. Display Data RAM Map (1/4 Duty)

LCD layout reference

Layout method	LCD SEG	LCD COM	Display RAM filling order

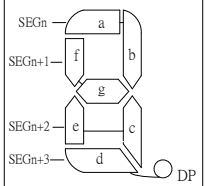
Method 1

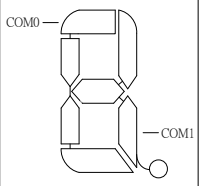




	SEGn	SEGn+1	SEGn+2	SEGn+3	SEGn+4	SEGn+5	SEGn+6	SEGn+7
COM0	c	b	a	f	g	e	d	DP
COM1	x	x	x	x	x	x	x	x
COM2	x	x	x	x	x	x	x	x
COM3	x	x	x	x	x	x	x	x

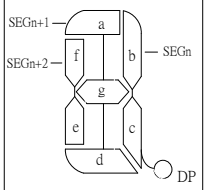
Method 2

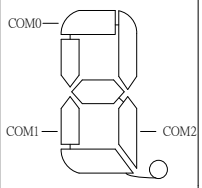




	SEGn	SEGn+1	SEGn+2	SEGn+3
COM0	a	f	e	d
COM1	b	g	c	DP
COM2	x	x	x	x
COM3	x	x	x	x

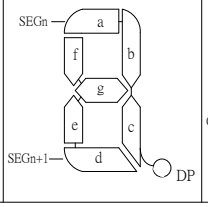
Method 3

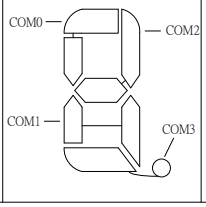




	SEGn	SEGn+1	SEGn+2
COM0	b	a	f
COM1	DP	d	e
COM2	c	g	x
COM3	x	x	x

Method 4





	SEGn	SEGn+1
COM0	a	f
COM1	c	e
COM2	b	g
COM3	DP	d

Figure 5. Relationships between LCD layout and display RAM filling order and display data

Notes 1：' x '= data bit unchanged.

Notes 2：ST7033 is always operating in 1/4 duty.

LCD DRIVER CIRCUIT

4-channel common drivers and 96-channel segment drivers configure this driver circuit. This LCD panel driver voltage depends on the combination of display data and frame (positive or negative).

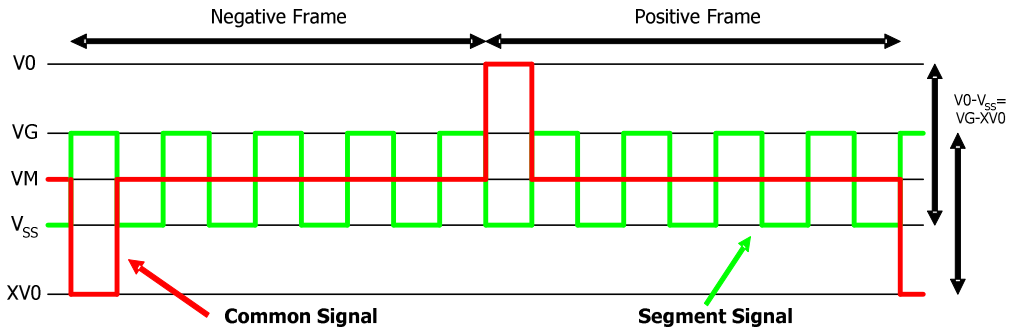


Figure 6. LCD Driver Waveforms

Liquid Crystal Driver Power Circuit

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction.

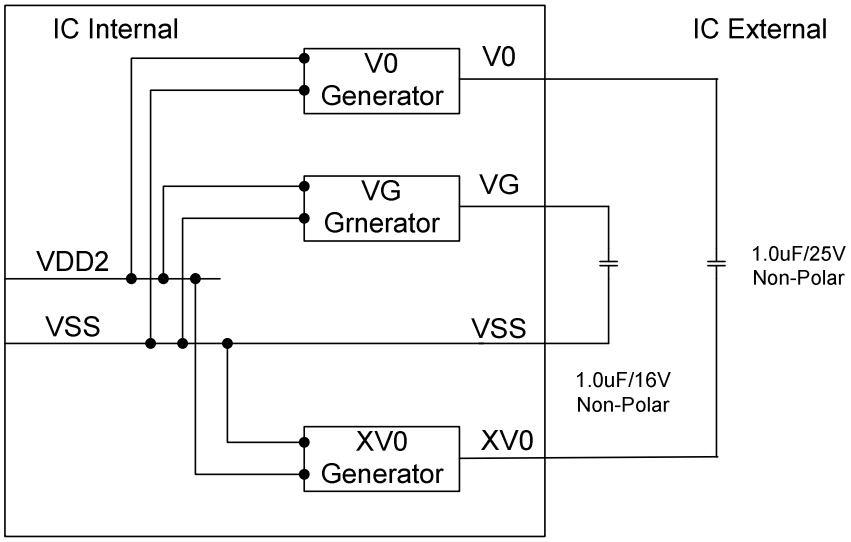


Figure 7. External Components on V0, XV0 and VG

8. RESET CIRCUIT

Setting /RESB to “L” or Reset instruction can initialize internal function.
When /RESB becomes “L”, following procedure is occurred.
Power save mode is entered
--Oscillator circuit is stopped
--The LCD power supply circuit is stopped
--Display OFF
--Display all point ON
--Segment/Common output go to the VSS level
Display normal
Column address: 0
Common scan direction : MY=0
Segment scan direction : MX=0
Power control [VB VR VF]=0
Booster: CP pad

9-1. INSTRUCTION TABLE

COMMAND	CODE									DESCRIPTION
	A0	D7	D6	D5	D4	D3	D2	D1	D0	
Display data write	1	D7	D6	D5	D4	D3	D2	D1	D0	Write data to RAM
Display ON/OFF	0	1	0	1	0	1	1	1	0 1	LCD display 0:OFF,1:ON
Display normal/reverse	0	1	0	1	0	0	1	1	0 1	LCD display 0:normal;1:reverse
Display all points ON/OFF	0	1	0	1	0	0	1	0	0 1	LCD display 0:normal;1:all points ON
Page address set	0	1	0	1	1	0	0	0	0	Set the DDRAM page address
Column address set Upper 3-bit address	0	0	0	0	1	*	X6	X5	X4	Set the DDRAM column address
Column address set Lower 4-bit address	0	0	0	0	0	X3	X2	X1	X0	
Segment driver direction select	0	1	0	1	0	0	0	0	MX	Sets the correspondence between the DDRAM column address and the SEG driver output
Common driver direction select	0	1	1	0	0	MY	*	*	*	Sets the correspondence between the DDRAM line address and the COM driver output
Power control set	0	0	0	1	0	1	VB	VR	VF	Set the on-chip power supply circuit operation mode
Power save mode	-	-	-	-	-	-	-	-	-	Compound command of Display OFF and Display-all-points-ON
Reset	0	1	1	1	0	0	0	1	0	Software reset
NOP	0	1	1	1	0	0	0	1	1	No operation
Enter mode set	0	1	1	1	1	0	0	0	1	Enter mode set
Duty mode set	0	1	0	1	0	1	1	0	0	Set 1/4 duty
Finish mode set	0	1	1	1	1	0	0	0	0	Finish mode set

Notes: “*” = Disabled bit

9-2. INSTRUCTION DESCRIPTION

Display data Write

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address . The column address is increased by 1 automatically so that the microprocessor can continuously write data . During auto-increment, the column address wraps to 0 after the last column is written.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
1	Write data								Write to the DDRAM

Display ON/OFF

This command turns the display ON and OFF.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	0	1	0	1	1	1	0	Display OFF
								1	Display ON

Display Normal/Reverse

This command can reserve the lit and unlit without overwriting the content of the DDRAM.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	0	1	0	0	1	1	0	LCD ON Voltage
								1	LCD OFF Voltage

Display All Points ON/OFF

The command makes it possible to force all display points ON regardless of the content of the DDRAM. Even when this is done, the DDRAM contents are maintained. This command takes priority over the Display normal/reverse command.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	0	1	0	0	1	0	0	Normal Display Mode
								1	Display All Points ON

When the Display all points ON command is executed when in the Display OFF mode, Power Save mode is entered. See the “Power Save mode” for detail.

Page Address Set

This command specifies the start page address of the DDRAM.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	0	1	1	0	0	0	0	Ser page address

Column Address Set

This command specifies the column address of the DDRAM. The column address is split into two sections (the upper 3-bits and lower 4-bits) when it is set.

Each time the DDRAM is accessed, the column address automatically increments by +1, imaging it possible for the MCU to continuously access to the display data. After the last column address (5FH), column address returns to 00H.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	*	X6	X5	X4	Upper bit address
				0	X3	X2	X1	X0	Lower bit address

Notes:’ * ‘Disabled bit

X6	X5	X4	X3	X2	X1	X0	Column Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:
1	0	1	1	1	1	0	94
1	0	1	1	1	1	1	95

Segment Driver Direction Select

This command can reverse the correspondence between the DDRAM column address and the segment driver output

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description	
0	1	0	1	0	0	0	0	MX	TMX=VSS MX mode 1	MX=0 SEG95→ SEG0 MX=1 SEG0→ SEG95
									TMX=VDD1 MX mode 2	MX=0 SEG0 → SEG95 MX=1 SEG95 → SEG0

Common Driver Direction Select

This command can reverse the correspondence between the DDRAM line address and the common driver output

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description	
0	1	1	0	0	MY	*	*	*	TMY=VSS MY mode 1	MY=0 COM0→ COM67 MY=1 COM67→ COM0
									TMY=VDD1 MY mode 2	MY=0 COM67→ COM0 MY=1 COM0→ COM67

Notes1:' * 'Disabled bit

Power control set

This command sets the on-chip power supply function ON/OFF.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	1	0	0	0	Booster: OFF Voltage Regulator: OFF Voltage Follower: OFF
						1	1	1	Booster: ON Voltage Regulator: ON Voltage Follower: ON

(D2 : Booster, D1 : Voltage Regulator, D0 : Voltage Follower)

Set 1/4 duty mode (Combinative instructions)

These combinative instructions set the driver into 1/4 duty mode.

Enter mode set

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	1	1	1	0	0	0	1	Enter mode set

Duty mode set

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	0	1	0	1	1	0	0	Set 1/4 duty

Finish mode set

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	1	1	1	0	0	0	0	Finish mode set

Power Save Mode

If the display all points ON command is executed when the display is in display OFF mode, power saver mode is entered. This mode stops every operation of the LCD display system.

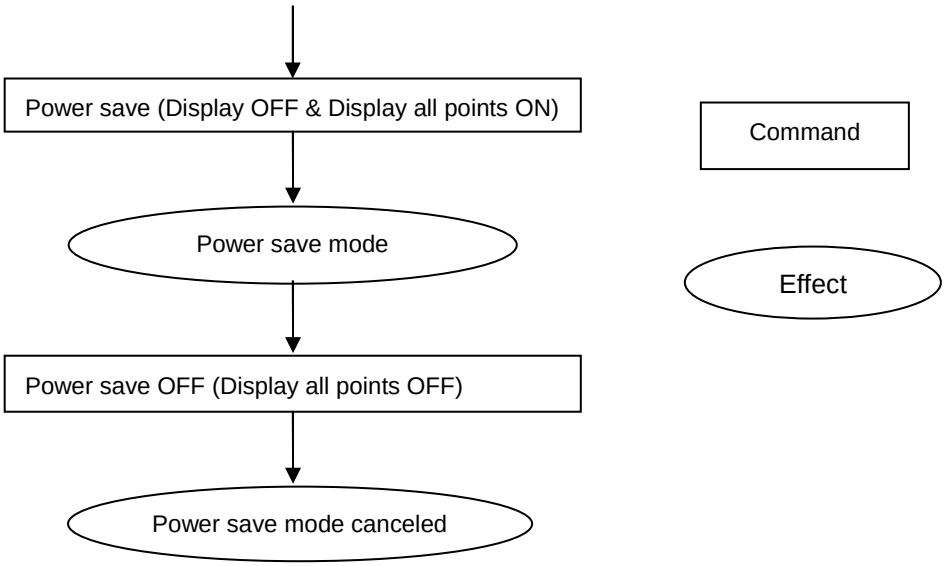


Figure 8. Power Save Mode

The internal states in power save mode are as follows:

-The oscillator circuit is stopped

-The LCD driver circuit is stopped

-The LCD driver circuit is stopped and segment/common driver output s to VSS level

-The display data and operation mode before execution of the Power save are held, and the MCU can access to the DDRAM and internal registers.

Reset

When this command is issued, the driver is initialized. This command doesn't change DDRAM content.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	1	1	0	0	0	1	0	Software reset

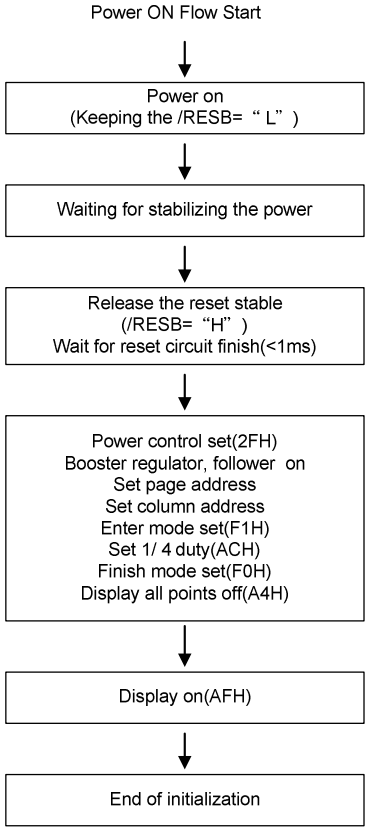
NOP

Non-operation command

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	1	1	0	0	0	1	1	No operation

Command Description

Referential instruction setup flow for power on:



Referential instruction setup flow for power down:

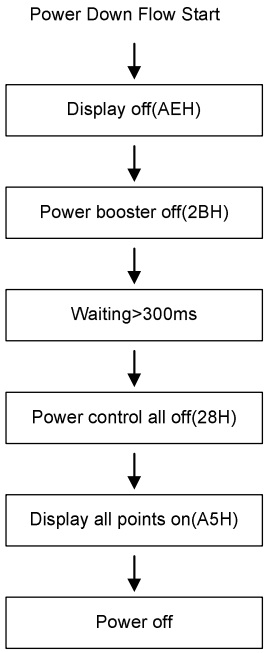


Figure 9. Power On and Power Down Sequence

10. LIMITING VALUES

In accordance with the Absolute Maximum Rating System; see notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Power supply voltage	VDD1	-0.3 ~ 3.6	V
Power supply voltage	VDD2	-0.3 ~ 3.6	V
Power supply voltage (VDD2 standard)	V0, |XV0|	-0.3 ~ 13.5	V
Power supply voltage (VDD2 standard)	VG, VM	0.3 to V0	V
Operating temperature	TOPR	–30 to +80	℃
Storage temperature	TSTR	–65 to +150	℃

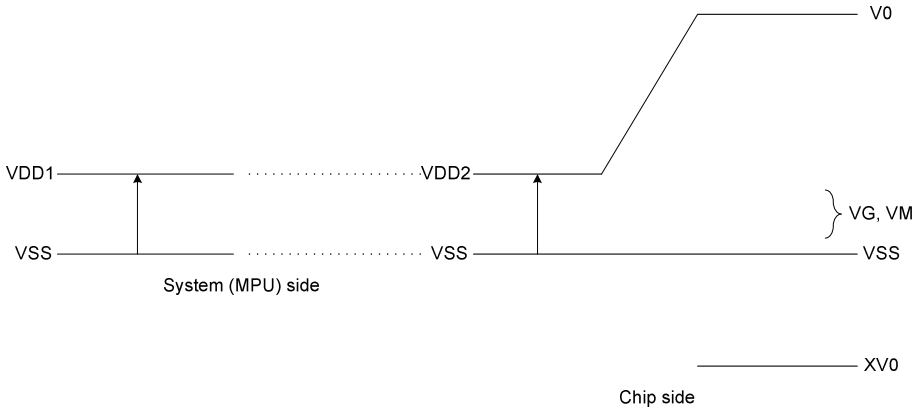


Figure 10.

Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.
3. Insure that the voltage levels of VG, VM, VSS, and XV0 are always such that
   V0 ≧ VG ≧ VM ≧ VSS ≧ XV0

11. HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices

12. DC CHARACTERISTICS

VSS = 0 V; Ta = -30℃ to +80℃; unless otherwise specified.

Item		Symbol	Condition		Rating			Units	Applicable Pin
					Min.	Typ.	Max.		
Operating Voltage (1)		VDD1			1.65	—	3.4	V	VSS
Operating Voltage (2)		VDD2	(Relative to VSS)		2.5	—	3.4	V	VSS
High-level Input Voltage		VIHC			0.7 x VDD1	—	VDD1	V	
Low-level Input Voltage		VILC			VSS	—	0.3 x VDD1	V	
High-level Output Voltage		VOHC	IOH=1mA		0.8 x VDD1	—	VDD1	V	
Low-level Output Voltage		VOLC	IOL1mA		VSS	—	0.2 x VDD1	V	
Input leakage current		ILI			–1.0	—	1.0	μA	
Output leakage current		ILO			–3.0	—	3.0	μA	
Liquid Crystal Driver ON Resistance		RON	Ta= 25℃ △V=10%	V0 =9.0 V	—	0.8	—	KΩ	SEGn COMn
				VG = 2.0 V	—	0.9	—		
Frame frequency		FR			—	70	—	Hz	
Internal Power	Supply Step-up output voltage Circuit	V0	(V0 To VSS)		—	4	—	V	V0
	Voltage regulator Circuit Operating Voltage	XV0	(VG To XV0)		—	-4	—	V	XV0

Dynamic Consumption Current :

During Display, with the Internal Power Supply ON Current consumed by total ICs(bare die)

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Power Down	ISS	Ta = 25℃	—	1.0	10	μA	

Notes to the DC characteristics

1. The maximum possible V0 oltage that may be generated is dependent on voltage, temperature and (display) load.
2. During power down all static currents are switched off.

13. TIMING CHARACTERISTICS

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

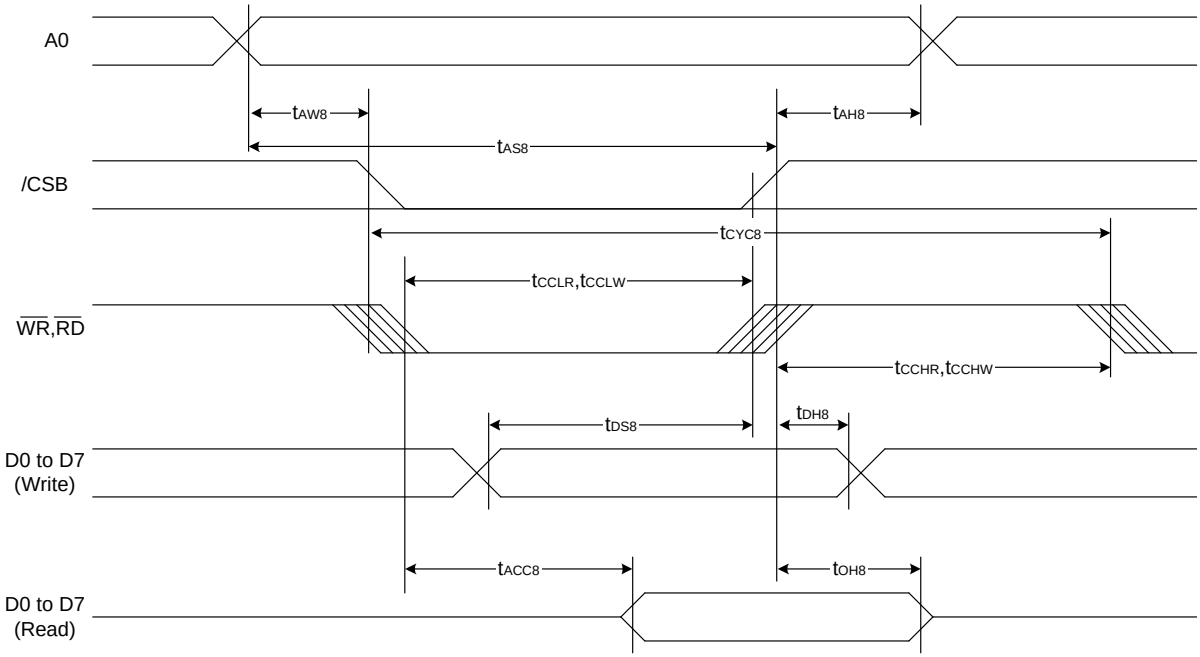


Figure 11. Parallel 8080 Series Interface Characteristics

(VDD1 = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		10	—	ns
Address setup time		tAW8		80	—	
Address setup time		tAS8		60	—	
System cycle time		tCYC8		350	—	
Enable L pulse width (WRITE)	/WR	tCCLW		70	—	
Enable H pulse width (WRITE)		tCCHW		50	—	
WRITE Data setup time	D0 to D7	tDS8		60	—	
WRITE Address hold time		tDH8		50	—	

(VDD1 = 2.8V , Ta =25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		15	—	ns
Address setup time		tAW8		120	—	
Address setup time		tAS8		80	—	
System cycle time		tCYC8		450	—	
Enable L pulse width (WRITE)	/WR	tCCLW		120	—	
Enable H pulse width (WRITE)		tCCHW		100	—	
WRITE Data setup time	D0 to D7	tDS8		90	—	
WRITE Address hold time		tDH8		60	—	

(VDD1 = 1.8V , Ta =25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		30	—	ns
Address setup time		tAW8		150	—	
Address setup time		tAS8		100	—	
System cycle time		tCYC8		550	—	
Enable L pulse width (WRITE)	/WR	tCCLW		170	—	
Enable H pulse width (WRITE)		tCCHW		150	—	
WRITE Data setup time	D0 to D7	tDS8		120	—	
WRITE Address hold time		tDH8		70	—	

Notes1:The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast,(tr +tf) ≦ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≦ (tCYC8 – tCCLR – tCCHR) are specified.

Notes2: All timing is specified using 20% and 80% of VDD1 as the reference.

Notes3: tCCLW and tCCLR are specified as the overlap between /CSB being “L” and /WR and /RD being at the “L” level.

System Bus Read/Write Characteristics 1 (For the 6800 Series MPU)

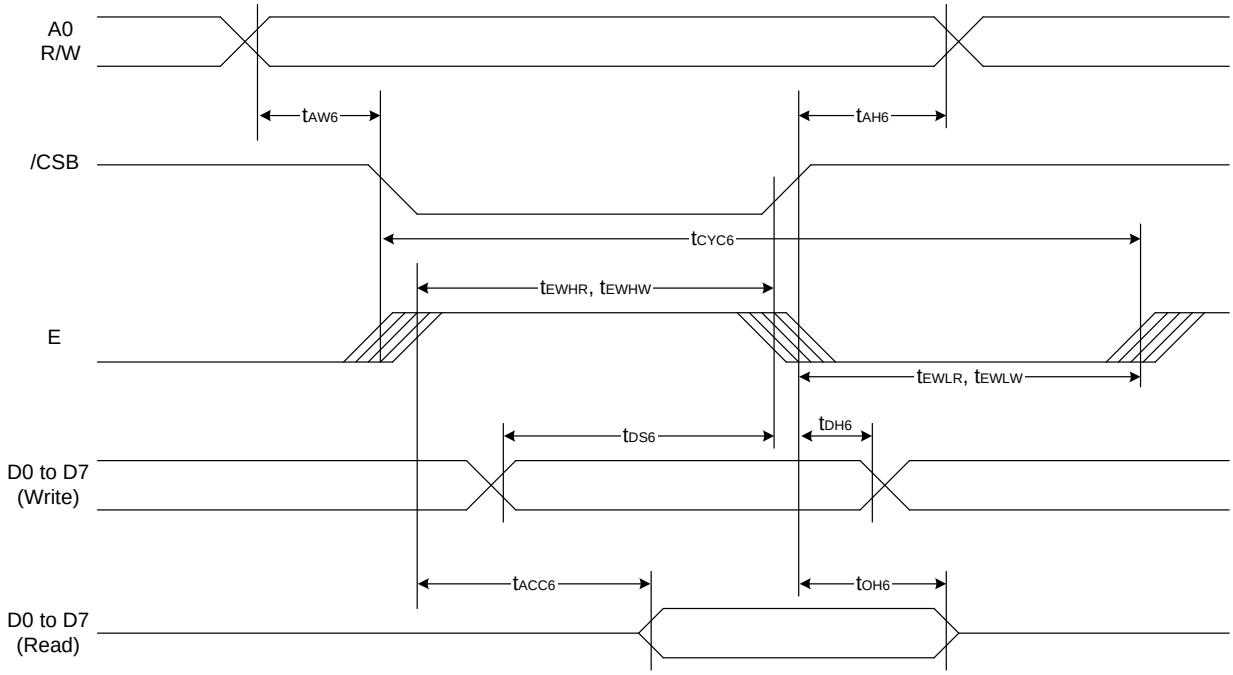


Figure 12. Parallel 6800 Series Interface Characteristics

(VDD1 = 3.3V , Ta =25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0 R/W	tAH6		10	—	ns
Address setup time		tAW6		80	—	
System cycle time		tCYC6		240	—	
Enable L pulse width (WRITE)	E	tEWLW		70	—	
Enable H pulse width (WRITE)		tEWHW		50	—	
WRITE Data setup time	D0 to D7	tDS6		60	—	
WRITE Address hold time		tDH6		50	—	

(VDD1 = 2.8V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0 R/W	tAH6		15	—	ns
Address setup time		tAW6		100	—	
System cycle time		tCYC6		340	—	
Enable L pulse width (WRITE)	E	tEWLW		120	—	
Enable H pulse width (WRITE)		tEWHW		100	—	
WRITE Data setup time	D0 to D7	tDS6		120	—	
WRITE Address hold time		tDH6		60	—	

(VDD1 = 1.8V , Ta =25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0 R/W	tAH6		30	—	ns
Address setup time		tAW6		150	—	
System cycle time		tCYC6		440	—	
Enable L pulse width (WRITE)	E	tEWLW		170	—	
Enable H pulse width (WRITE)		tEWHW		150	—	
WRITE Data setup time	D0 to D7	tDS6		180	—	
WRITE Address hold time		tDH6		70	—	

Notes1:The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast,(tr +tf) ≦ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≦ (tCYC6 – tEWLR – tEWHR) are specified.

Notes2:All timing is specified using 20% and 80% of VDD1 as the reference.

Notes3:tEWLW and tEWLR are specified as the overlap between /CSB being “L” and E.

SERIAL INTERFACE (4-Line Interface)

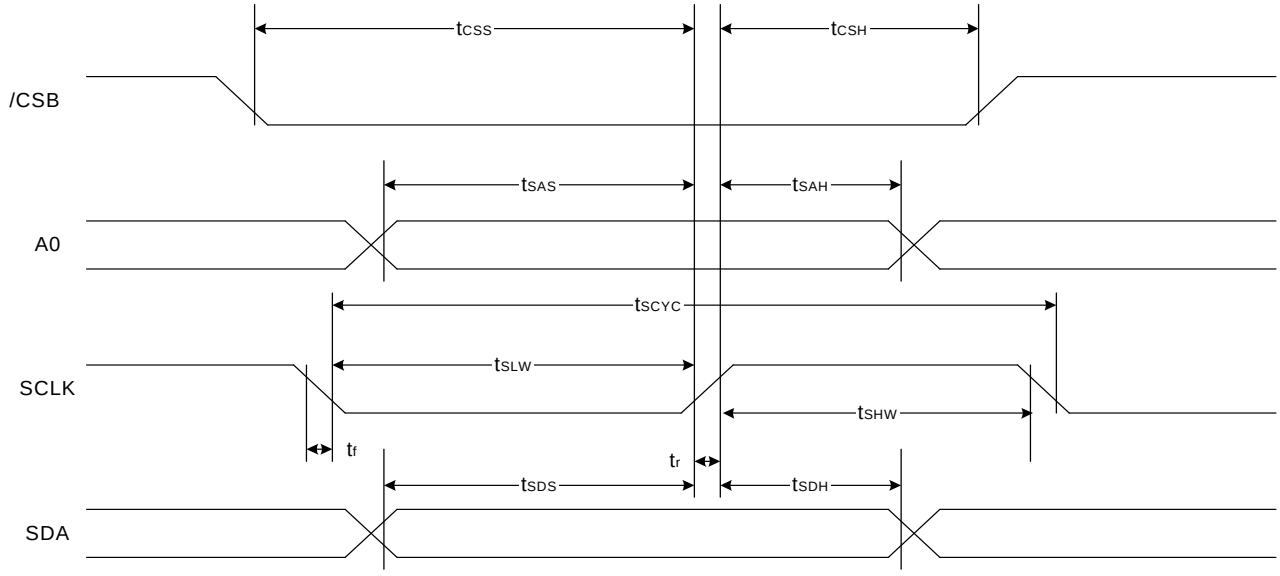


Figure 13. 4- Line Serial Interface Characteristics

(VDD1 = 3.3V , Ta =25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCLK	tSCYC		120	—	ns
SCL “H” pulse width		tSHW		60	—	
SCL “L” pulse width		tSLW		60	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		90	—	
Data setup time	SDA	tSDS		20	—	
Data hold time		tSDH		10	—	
CS-SCL time	/CSB	tCSS		20	—	
CS-SCL time		tCSH		120	—	

(VDD1 = 2.8V , Ta =-25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCLK	tSCYC		200	—	ns
SCL “H” pulse width		tSHW		100	—	
SCL “L” pulse width		tSLW		100	—	
Address setup time	A0	tSAS		30	—	
Address hold time		tSAH		120	—	
Data setup time	SDA	tSDS		30	—	
Data hold time		tSDH		20	—	
CS-SCL time	/CSB	tCSS		30	—	
CS-SCL time		tCSH		150	—	

(VDD1 = 1.8V , Ta =25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCLK	tSCYC		280	—	ns
SCL “H” pulse width		tSHW		140	—	
SCL “L” pulse width		tSLW		140	—	
Address setup time	A0	tSAS		50	—	
Address hold time		tSAH		150	—	
Data setup time	SDA	tSDS		50	—	
Data hold time		tSDH		50	—	
CS-SCL time	/CSB	tCSS		40	—	
CS-SCL time		tCSH		180	—	

Notes1: The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

Notes2: All timing is specified using 20% and 80% of VDD1 as the standard.

SERIAL INTERFACE (3-Line Interface)

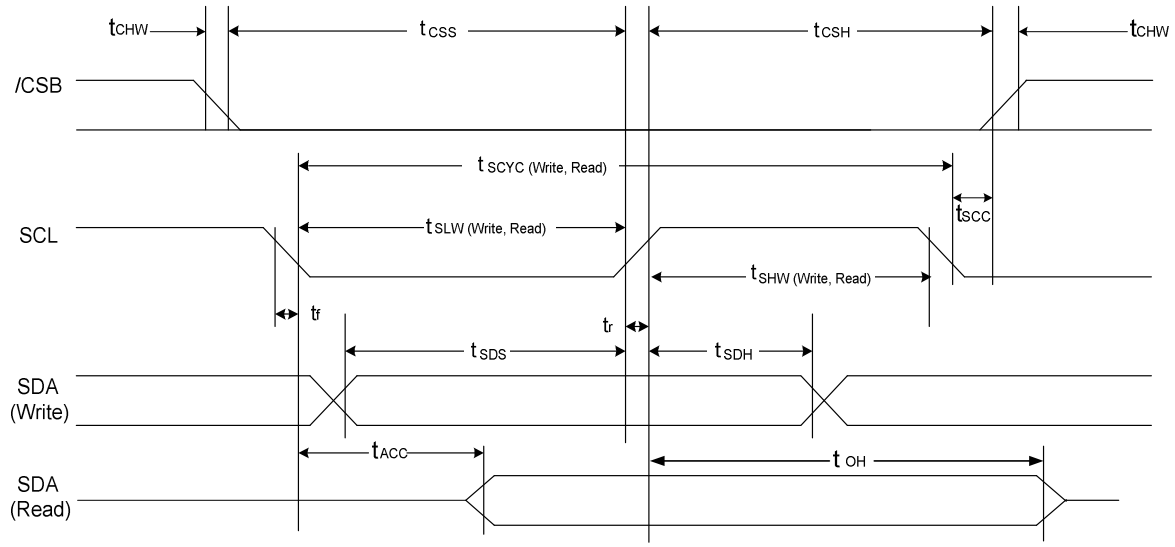


Figure 14. 3- Line Serial Interface Characteristics

(VDD1=3.3V ,Ta=25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period(Write)	SCLK	tSCYC		120	—	ns
SCL “H” pulse width(Write)		tSHW		60	—	
SCL “L” pulse width(Write)		tSLW		60	—	
Data setup time	SDAIN	tSDS		30	—	
Data hold time		tSDH		30	—	
CS-SCL time	/CSB	tCSS		30	—	
CS-SCL time		tCSH		30	—	
SCL-CS	/CSB	tSCC		10	—	
CS “H” pulse width	/CSB	tCHW		30	—	

(VDD1=2.8V ,Ta=25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period(Write)	SCLK	tSCYC		180	—	ns
SCL “H” pulse width(Write)		tSHW		90	—	
SCL “L” pulse width(Write)		tSLW		90	—	
Data setup time	SDAIN	tSDS		40	—	
Data hold time		tSDH		40	—	
CS-SCL time	/CSB	tCSS		40	—	
CS-SCL time		tCSH		40	—	
SCL-CS	/CSB	tSCC		15	—	
CS “H” pulse width	/CSB	tCHW		35	—	

(VDD1=1.8V ,Ta=25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period(Write)	SCLK	tSCYC		250	—	ns
SCL “H” pulse width(Write)		tSHW		100	—	
SCL “L” pulse width(Write)		tSLW		100	—	
Data setup time	SDAIN	tSDS		60	—	
Data hold time		tSDH		60	—	
CS-SCL time	/CSB	tCSS		60	—	
CS-SCL time		tCSH		65	—	
SCL-CS	/CSB	tSCC		20	—	
CS “H” pulse width	/CSB	tCHW		45	—	

Notes1:The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

Notes2:All timing is specified using 30% and 70% of VDD1 as the standard.

14. RESET TIMING

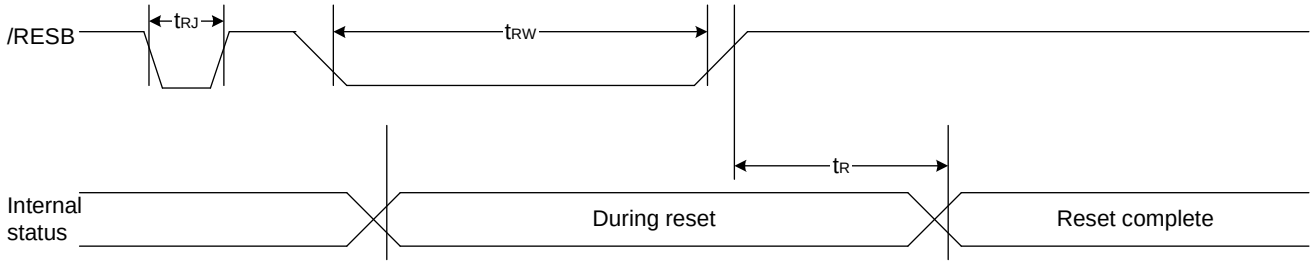


Figure 15. Reset Timing Characteristics

(VDD1 = 3.3V , Ta = 25℃)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time	/RESB	tR		20	—	—	us
Reset “L” pulse width	/RESB	tRW		2	—	—	us
Reset rejection (for noise spike)	/RESB	tRJ		—	—	1	us

(VDD1 = 2.8V , Ta =25℃)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time	/RESB	tR		20	—	—	us
Reset “L” pulse width	/RESB	tRW		2	—	—	us
Reset rejection (for noise spike)	/RESB	tRJ		—	—	1	us

(VDD1 =1.8V , Ta = 25℃)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time	/RESB	tR		30	—	—	us
Reset “L” pulse width	/RESB	tRW		3	—	—	us
Reset rejection (for noise spike)	/RESB	tRJ		—	—	1	us

15. APPLICATION NOTE

ST7033 (1/4 duty)

Resolution 4COM*96SEG
Interface : 6800
Internal analog circuit
Internal OSC
Booster : X4
Bias ratio default : 1/4
Vop : 4.0V
C=1.0 uF

PS0 : VSS
PS1 : VDD1
OSC : VDD1
CP : VSS
DA : VSS
MODE : VSS
TMX:VDD1
TMY:VSS

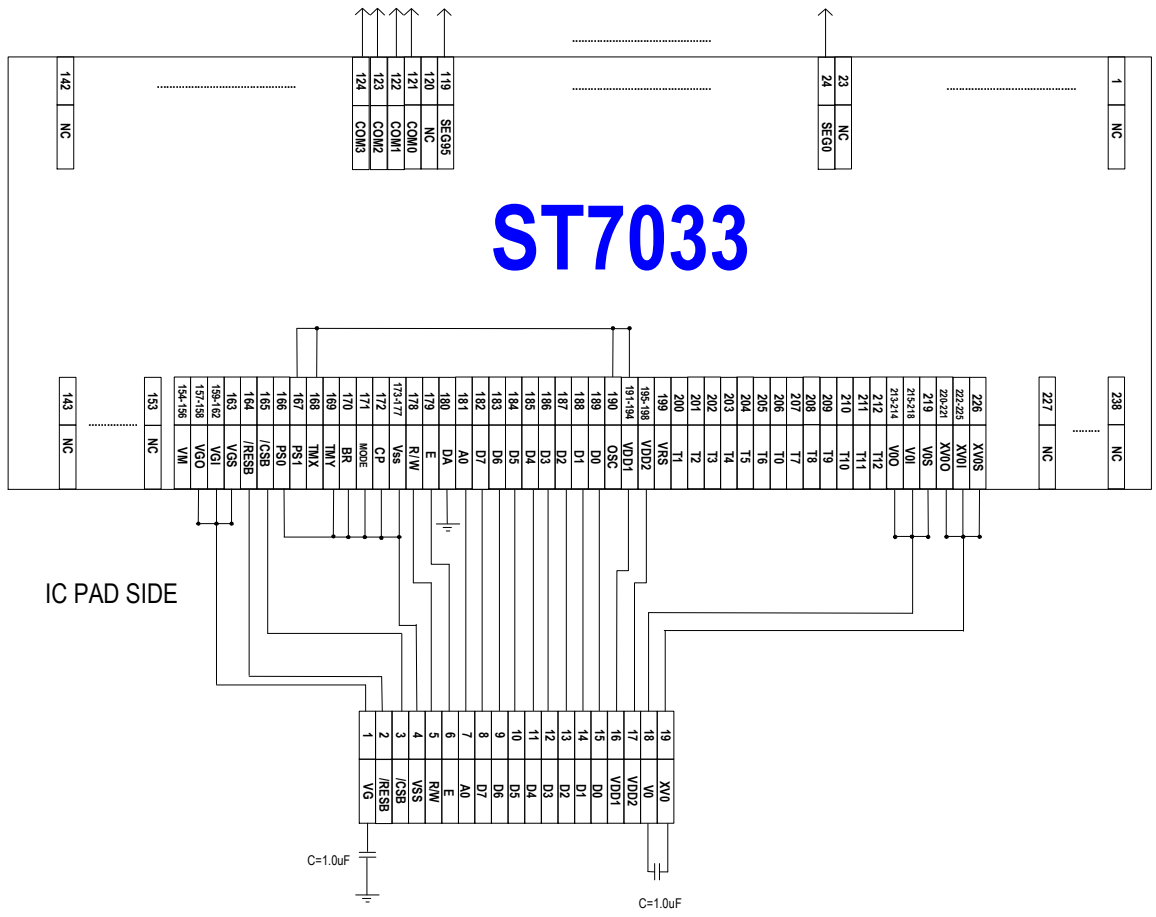


Figure 16. 6800 Parallel Application

ST7033 (1/4 duty)

Resolution : 4COM*96SEG
Interface : 8080
Internal analog circuit
Internal OSC
Booster : X4
Bias ratio default : 1/4
Vop : 4.0V
C=1.0 uF

PS0 : VDD1
PS1 : VDD1
OSC : VDD1
CP : VSS
DA : VSS
MODE : VSS
TMX:VDD1
TMY:VSS

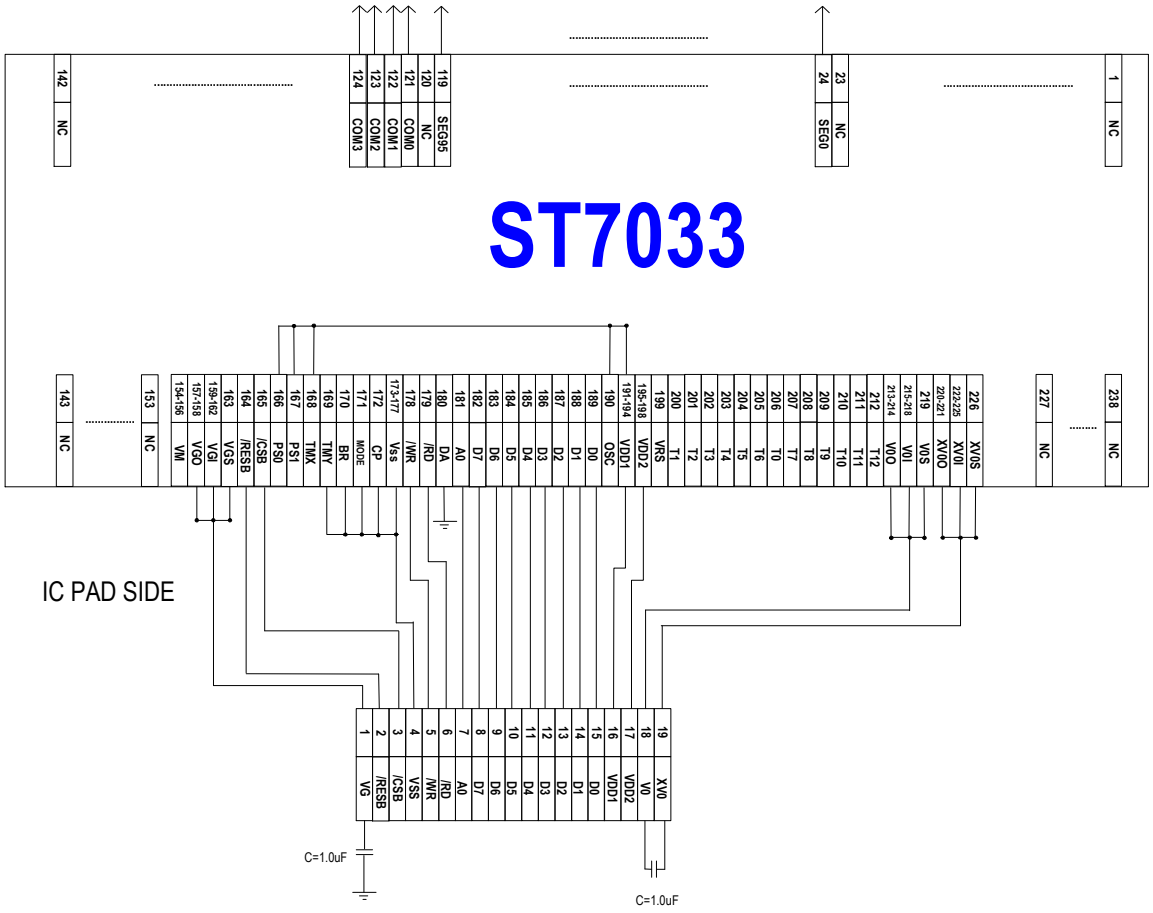


Figure 17. 8080 Parallel Applicaiton

ST7033 (1/4 duty)

Resolution : 4COM*96SEG
Interface : 3-line
Internal analog circuit
Internal OSC
Booster : X4
Bias ratio default : 1/4
Vop : 4.0V
C=1.0 uF

PS0 : VSS
PS1 : VSS
OSC : VDD1
CP : VSS
DA : VSS
MODE : VSS
TMX:VDD1
TMY:VSS

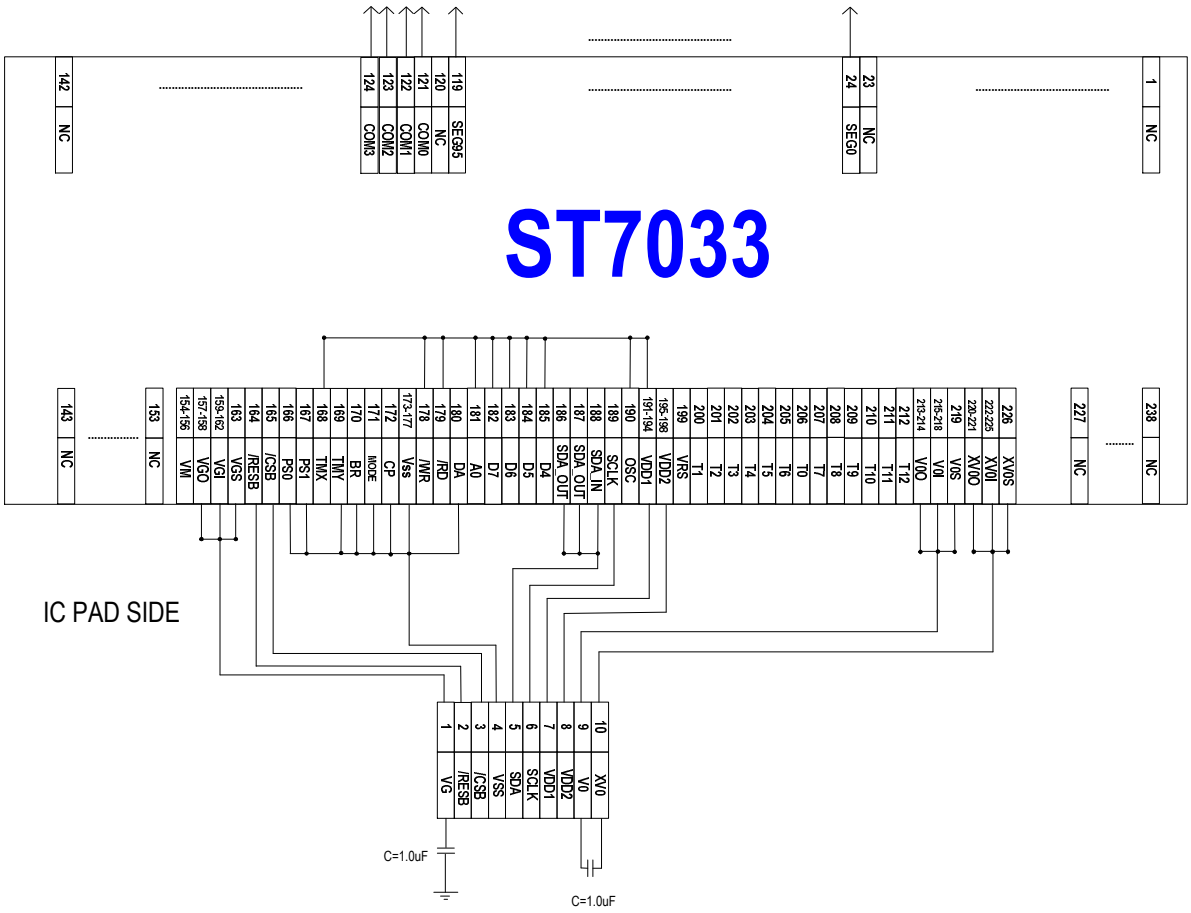


Figure 18. 3-Line Serial Application

ST7033 (1/4 duty)

Resolution : 4COM*96SEG
Interface : 4-line
Internal analog circuit
Internal OSC
Booster : X4
Bias ratio default : 1/4
Vop : 4.0V
C=1.0 uF

PS0 : VDD1
PS1 : VSS
OSC : VDD1
CP : VSS
DA : VSS
MODE : VSS
TMX:VDD1
TMY:VSS

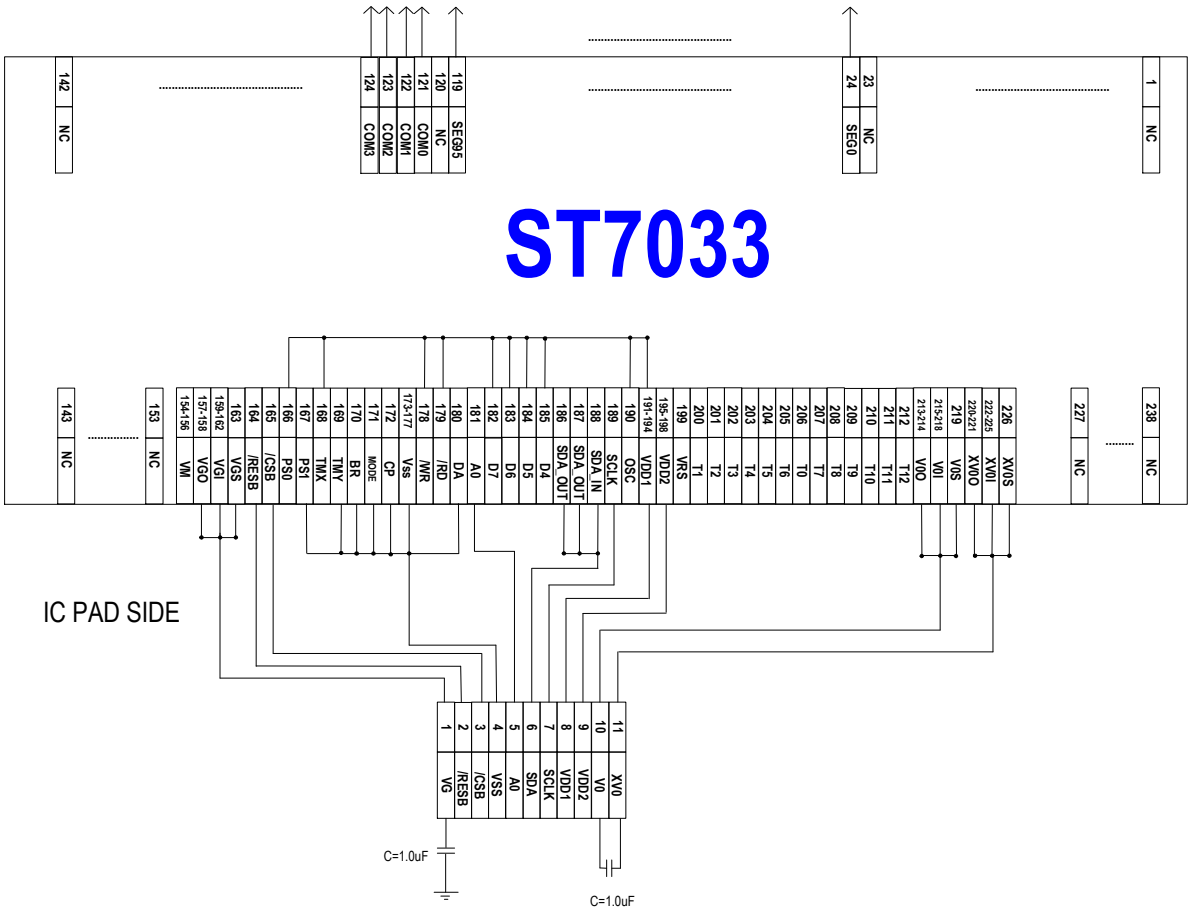
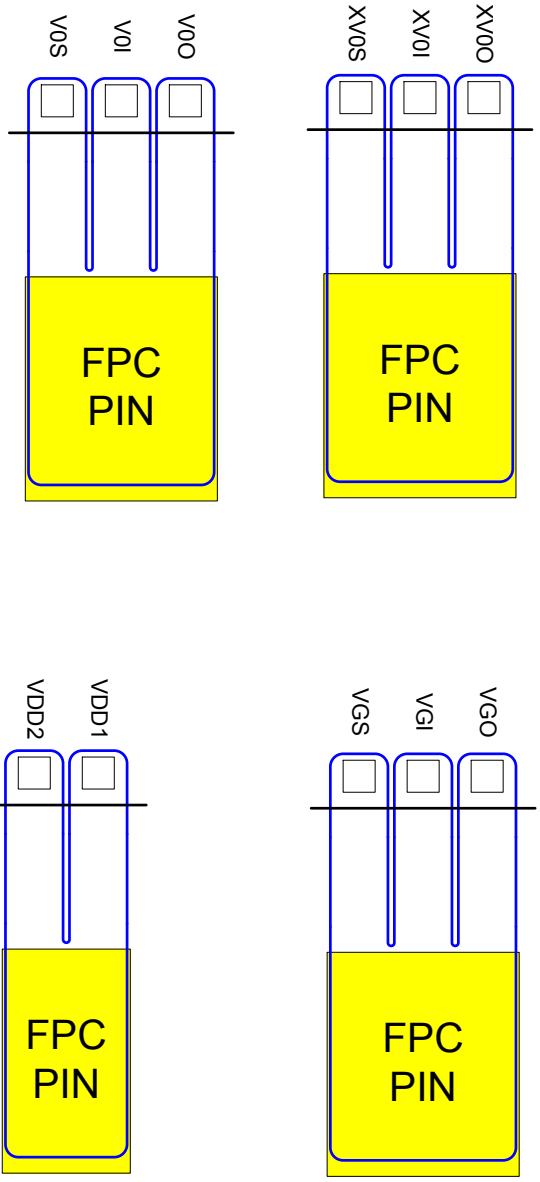


Figure 19. 4-Line Serial Application

ITO Layout Reference

About ITO layout, please refer the following pictures：



ST7033 Serial Specification Revision History		
Version	**Date**	**Description**
1.0	2008/04/18	First Issue Version
1.1	2009/07/15	Modify application note