Sitronix

ST7093

26 COM / 80 SEG LCD CONTROLLER/DRIVER

FEATURES

- CGROM :10240 bits(256chars 5 x 8 dots)
  CGRAM :320 bits(8 chars 5 x 8 dots)
  DDRAM :64 bytes(16 x 4)
  ICONRAM :80 bits
- Low power operation support:
  -- 2.4 to 3.6V
- Wide range of LCD driver power
  -- 3.0 to 7.0V
- 4-bit or 8-bit MPU interface for both 68 and 80 series
- 4 pin clock synchronized serial interface
- COM/SEG bi-directional setting
- Voltage converter/regulator/follower/bias circuit built in
- 26 common x 80 segment liquid crystal display driver
- 32 steps electronic volume control
- Wide range of instruction functions:
  return home, display on/off, cursor on/off, display character blink, double height, line shift, function set, power and bias control
- Hardware reset pin available
- Internal oscillator or external clock
- Power save mode for low power consumption
- Bare Chip available

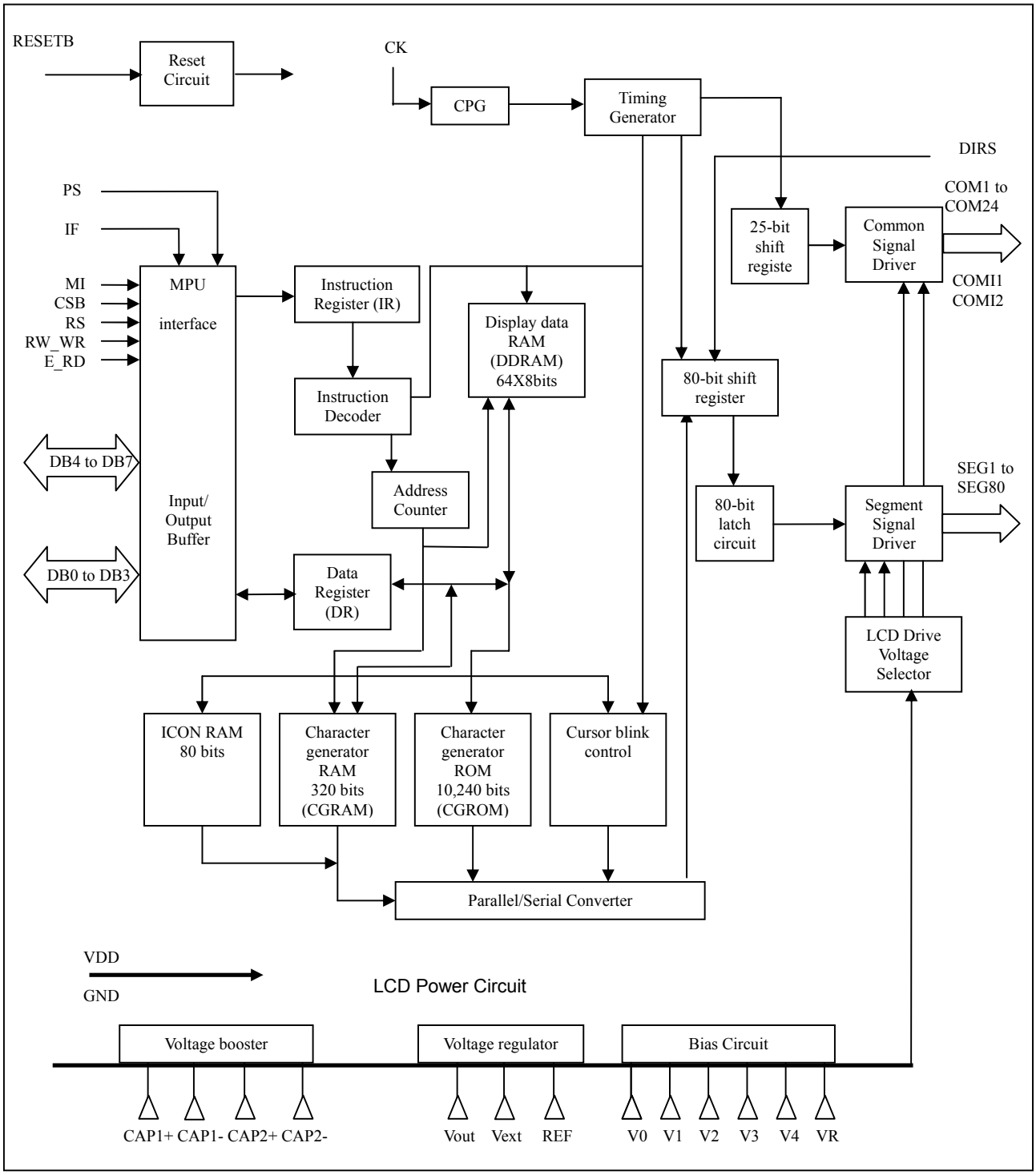
GENERAL DESCRIPTION

The ST7093 dot-matrix liquid crystal display controller can drive LSI displays alphanumeric, Japanese kana characters, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4bit, 8 bit or 4 pin clock synchronized serial bus interface. For 4 bit and 8 bit bus interface both 68 series and 80 series type are available. Since all the functions such as display RAM, character generator, liquid crystal driver, oscillator and voltage control functions required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimal system can be interfaced with this controller/driver.

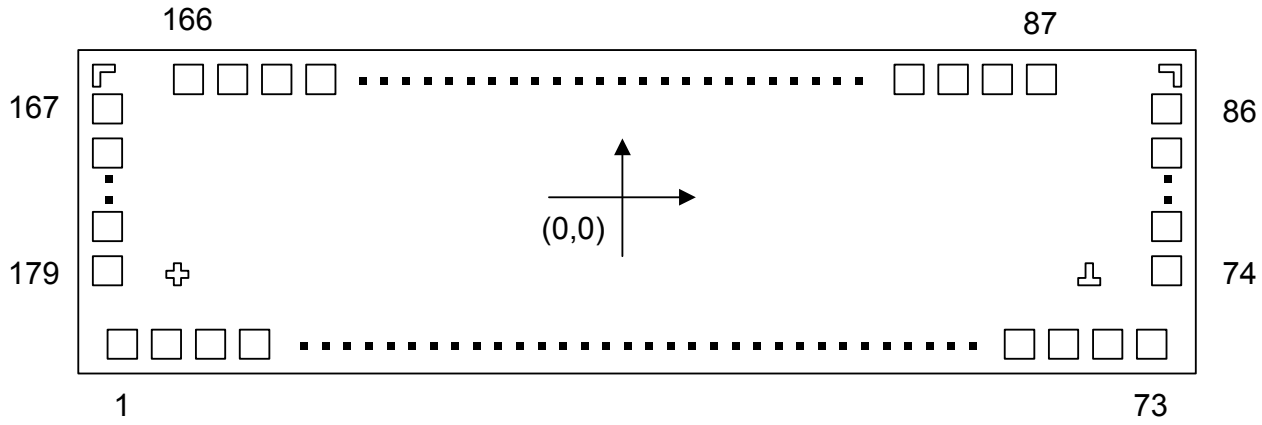
The ST7093 character generator ROM is extended to generate 256 5 x 8 dot character fonts. The low power supply (2.4V to 3.6V) of the ST7093 is suitable for any portable battery-driven product requiring low power dissipation.

The ST7093 LCD driver consists of 26 common signal drivers and 80 segment signal drivers with COG gold bump available.

BLOCK DIAGRAM

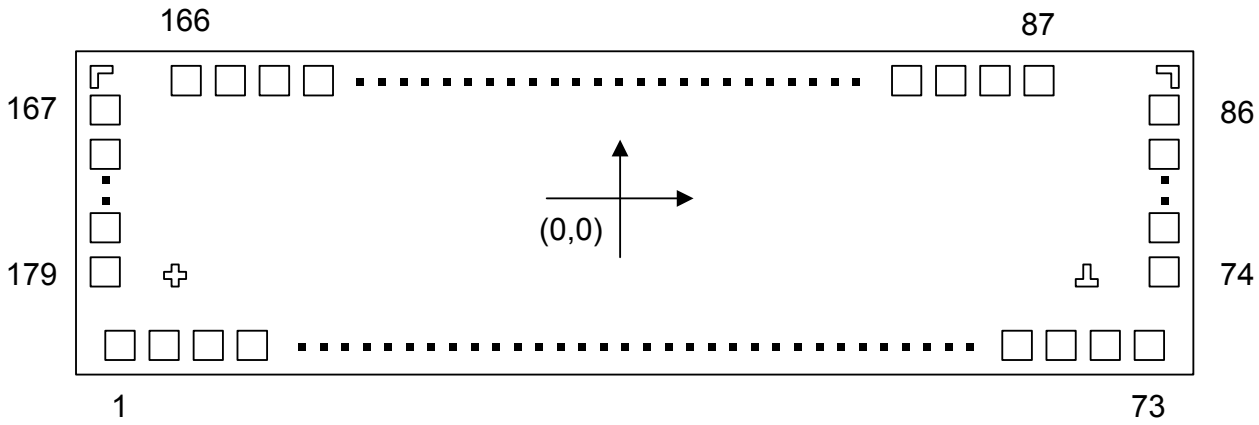


PAD DIMENSIONS (COB)



Chip Size	: 6775 X 1872 μm		
Min Pitch	: 72 μm (Seg.)		
Pad Size	: PAD No.	1~73	81.0 μm x 64.8 μm
	: PAD No.	74~86	64.8 μm x 81.0 μm
	: PAD No.	87~166	63.0 μm x 84.6 μm
	: PAD No.	167~179	64.8 μm x 81.0 μm

PAD DIMENSIONS (COG)



Chip Size : 6775 X 1872 μm

Min Pitch : 72 μm (Seg.)

Bump Size : PAD No. 1~73 68.4 μm x 52.2 μm

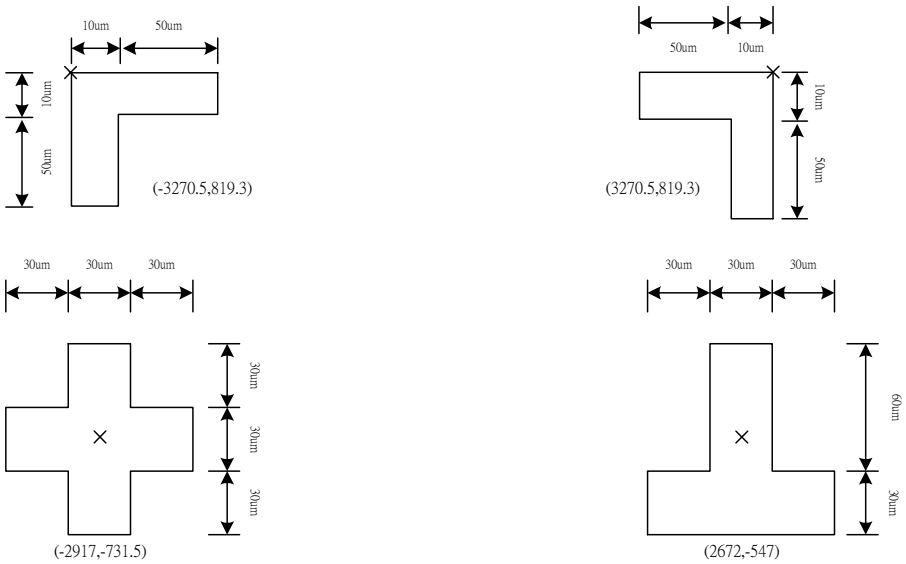
: PAD No. 74~86 52.2 μm x 68.4 μm

: PAD No. 87~166 50.4 μm x 72 μm

: PAD No. 167~179 52.2 μm x 68.4 μm

Bump Height : 18 μm (Typ.)

COG Align Key Coordinate



PAD LOCATION

Table 2. PAD Center Coordinates

NO. PAD	PAD NAME	X	Y	NO. PAD	PAD NAME	X	Y	NO. PAD	PAD NAME	X	Y
1	DUMMY	-3249	-821	61	CK	2151	-821	121	SEG[35]	420	811
2	DUMMY	-3159	-821	62	VSS	2241	-821	122	SEG[36]	348	811
3	DUMMY	-3069	-821	63	PSB	2331	-821	123	SEG[37]	276	811
4	DUMMY	-2979	-821	64	VDD	2421	-821	124	SEG[38]	204	811
5	DUMMY	-2889	-821	65	IF	2511	-821	125	SEG[39]	132	811
6	RS	-2799	-821	66	VSS	2601	-821	126	SEG[40]	60	811
7	VSS	-2709	-821	67	MI	2691	-821	127	SEG[41]	-12	811
8	RW	-2619	-821	68	VDD	2781	-821	128	SEG[42]	-84	811
9	VDD	-2529	-821	69	RESETB	2871	-821	129	SEG[43]	-156	811
10	E	-2439	-821	70	TEST3	2961	-821	130	SEG[44]	-228	811
11	CSB	-2349	-821	71	TEST2	3051	-821	131	SEG[45]	-300	811
12	D7	-2259	-821	72	TEST1	3141	-821	132	SEG[46]	-372	811
13	D6	-2169	-821	73	TEST0	3231	-821	133	SEG[47]	-444	811
14	D5	-2079	-821	74	COMI1	3272	-454	134	SEG[48]	-516	811
15	D4	-1989	-821	75	COM[1]	3272	-364	135	SEG[49]	-588	811
16	D3	-1899	-821	76	COM[2]	3272	-274	136	SEG[50]	-660	811
17	D2	-1809	-821	77	COM[3]	3272	-184	137	SEG[51]	-732	811
18	D1	-1719	-821	78	COM[4]	3272	-94	138	SEG[52]	-804	811
19	D0	-1629	-821	79	COM[5]	3272	-4	139	SEG[53]	-876	811
20	VDD	-1539	-821	80	COM[6]	3272	86	140	SEG[54]	-948	811
21	VDD	-1449	-821	81	COM[7]	3272	176	141	SEG[55]	-1020	811
22	VDD	-1359	-821	82	COM[8]	3272	266	142	SEG[56]	-1092	811
23	VSS	-1269	-821	83	COM[17]	3272	356	143	SEG[57]	-1164	811
24	VSS	-1179	-821	84	COM[18]	3272	446	144	SEG[58]	-1236	811
25	VSS	-1089	-821	85	COM[19]	3272	536	145	SEG[59]	-1308	811
26	V4	-999	-821	86	COM[20]	3272	626	146	SEG[60]	-1380	811
27	V4	-909	-821	87	SEG[1]	2868	811	147	SEG[61]	-1452	811
28	V3	-819	-821	88	SEG[2]	2796	811	148	SEG[62]	-1524	811
29	V3	-729	-821	89	SEG[3]	2724	811	149	SEG[63]	-1596	811
30	V2	-639	-821	90	SEG[4]	2652	811	150	SEG[64]	-1668	811
31	V2	-549	-821	91	SEG[5]	2580	811	151	SEG[65]	-1740	811
32	V1	-459	-821	92	SEG[6]	2508	811	152	SEG[66]	-1812	811
33	V1	-369	-821	93	SEG[7]	2436	811	153	SEG[67]	-1884	811
34	V0	-279	-821	94	SEG[8]	2364	811	154	SEG[68]	-1956	811
35	V0	-189	-821	95	SEG[9]	2292	811	155	SEG[69]	-2028	811
36	V0	-99	-821	96	SEG[10]	2220	811	156	SEG[70]	-2100	811
37	V0	-9	-821	97	SEG[11]	2148	811	157	SEG[71]	-2172	811
38	VR	81	-821	98	SEG[12]	2076	811	158	SEG[72]	-2244	811
39	VR	171	-821	99	SEG[13]	2004	811	159	SEG[73]	-2316	811
40	VOUT	261	-821	100	SEG[14]	1932	811	160	SEG[74]	-2388	811
41	VOUT	351	-821	101	SEG[15]	1860	811	161	SEG[75]	-2460	811
42	CAP2N	441	-821	102	SEG[16]	1788	811	162	SEG[76]	-2532	811
43	CAP2N	531	-821	103	SEG[17]	1716	811	163	SEG[77]	-2604	811
44	CAP2P	621	-821	104	SEG[18]	1644	811	164	SEG[78]	-2676	811
45	CAP2P	711	-821	105	SEG[19]	1572	811	165	SEG[79]	-2748	811
46	CAP1N	801	-821	106	SEG[20]	1500	811	166	SEG[80]	-2820	811
47	CAP1N	891	-821	107	SEG[21]	1428	811	167	COMI2	-3272	626
48	CAP1P	981	-821	108	SEG[22]	1356	811	168	COM[24]	-3272	536
49	CAP1P	1071	-821	109	SEG[23]	1284	811	169	COM[23]	-3272	446
50	VEXT	1161	-821	110	SEG[24]	1212	811	170	COM[22]	-3272	356
51	VSS	1251	-821	111	SEG[25]	1140	811	171	COM[21]	-3272	266
52	VSS	1341	-821	112	SEG[26]	1068	811	172	COM[16]	-3272	176
53	VSS	1431	-821	113	SEG[27]	996	811	173	COM[15]	-3272	86
54	VR	1521	-821	114	SEG[28]	924	811	174	COM[14]	-3272	-4
55	DUMMY	1611	-821	115	SEG[29]	852	811	175	COM[13]	-3272	-94
56	REF	1701	-821	116	SEG[30]	780	811	176	COM[12]	-3272	-184
57	DIRS	1791	-821	117	SEG[31]	708	811	177	COM[11]	-3272	-274
58	VDD	1881	-821	118	SEG[32]	636	811	178	COM[10]	-3272	-364
59	VDD	1971	-821	119	SEG[33]	564	811	179	COM[9]	-3272	-454
60	VDD	2061	-821	120	SEG[34]	492	811				

PIN DESCRIPTION

NAME	I/O	Interfaced	FUNCTION
RS	I	MPU	Select registers. 0: Instruction register (for write) address counter (for read) 1: Data register (for write and read)
RW_WR	I	MPU	Select read or write. In 68 mode In 80 mode 0: Write 0: Write 1: Read 1: Not active
E_RD	I	MPU	Starts data read/write. In 68 mode In 80 mode 0: Not active 0: Read 1: Enable 1: Not active
DB4 to DB7	I/O	MPU	Four high order bi-directional tristate data bus pins. Used for data transfer and receive between the MPU and the ST7093. In serial interface mode DB7 is SI (input data), DB6 is SCL (serial clock).
DB0 to DB3	I/O	MPU	Four low order bi-directional tristate data bus pins. Used for data transfer and receive between the MPU and the ST7093. These pins are not used during 4-bit operation. (Fixed high)
CSB	I	MPU	Chip select signal. Active low.
RESETB	I	MPU	Reset signal. Active low.
CK	I	MPU	External clock input pin. it must be fixed to “Vss” , when the internal oscillator circuit is used. In case of the external clock mode, CK is used as the clock and OS bit should be turn off.
MI	I	MPU	Interface selection 0: 80 mode interface 1: 68 mode interface
DIRS	I	MPU	SEG direction selection 0: SEG1 → SEG80 1: SEG80 → SEG1
IF	I	MPU	Interface selection valid when PS=1 0: 4 bit bus mode 1: 8 bit bus mode
PS	I	MPU	Interface selection 0: serial mode 1: 4bit/ 8bit bus mode
COM1 to COM24 COMI1,COMI2	O	LCD	Common signals. COMI1 and COMI2 are the same signal
SEG1 to SEG80	O	LCD	Segment signals
CAP1+, CAP1- CAP2+, CAP2-	O		Capacitor connection pins for voltage booster
Vout	I/O		Voltage booster output pin
VR	I		Voltage adjust pin between V0 and VSS
REF	I	MPU	Reference voltage selection pin 0: internal regulator is selected 1: external reference voltage input to Vext
Vext	I/O		External reference voltage input
V0 to V4	-	Power supply	Power supply for LCD drive V_0 - Vss = 7 V (Max)
VDD , GND	-	Power supply	VDD : 2.4V to 3.6V, GND: 0V
Test 0 to Test3	I		Test pin. open

Note: 1. V0>=V1>=V2>=V3>=V4>=VSS must be maintained

FUNCTION DESCRIPTION

System Interface

This chip has all two kinds of parallel interface type with MPU : 4-bit bus and 8-bit bus. 4-bit bus or 8-bit bus is selected by IF pin.
During read or write operation, two 8-bit registers are used. One is data register (DR), the other is instruction register(IR).

The data register(DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically. So to speak, after MPU reads DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically.

The Instruction register(IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data.

To select register, use RS input pin in 4-bit/8-bit bus mode and serial mode.

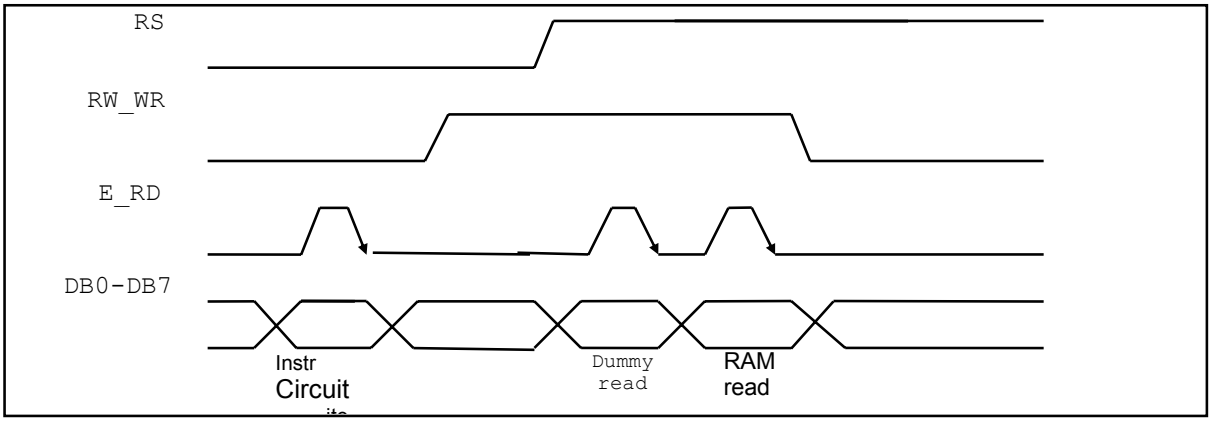
Table 1. Various kinds of operations according to RS and R/W bits for 68 interface.

RS	RW_WR	Operation
L	L	Instruction Write operation (MPU writes Instruction code into IR)
L	H	Read address counter (DB0 ~ DB6)
H	L	Data Write operation (MPU writes data into DR)
H	H	Data Read operation (MPU reads data from DR)

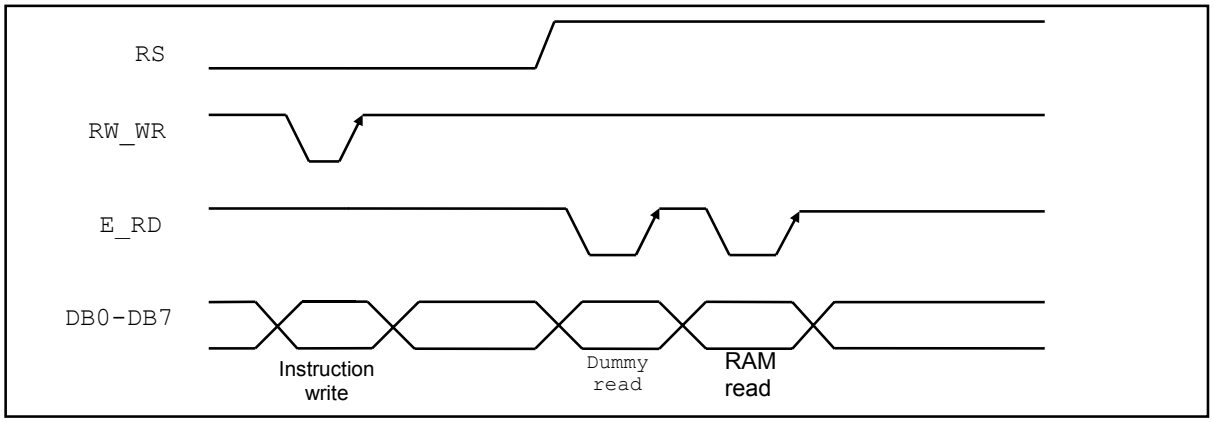
Table 1.1. Various kinds of operations according to RS and R/W bits for 80 interface.

RS	RW_WR E_RD	Operation
L	L H	Instruction Write operation (MPU writes Instruction code into IR)
L	H L	Read address counter (DB0 ~ DB6)
H	L H	Data Write operation (MPU writes data into DR)
H	H L	Data Read operation (MPU reads data from DR)

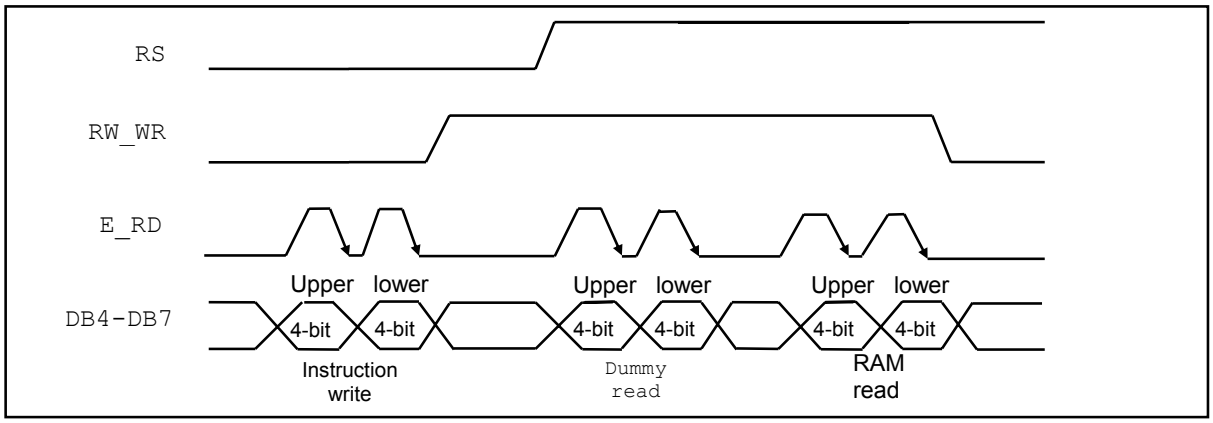
Address Counter (AC)
Address Counter(AC) stores DDRAM/CGRAM address, transferred from IR.
After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1.
When RS = "Low" and R/W = "High", AC can be read through DB0 ~ DB6 ports.



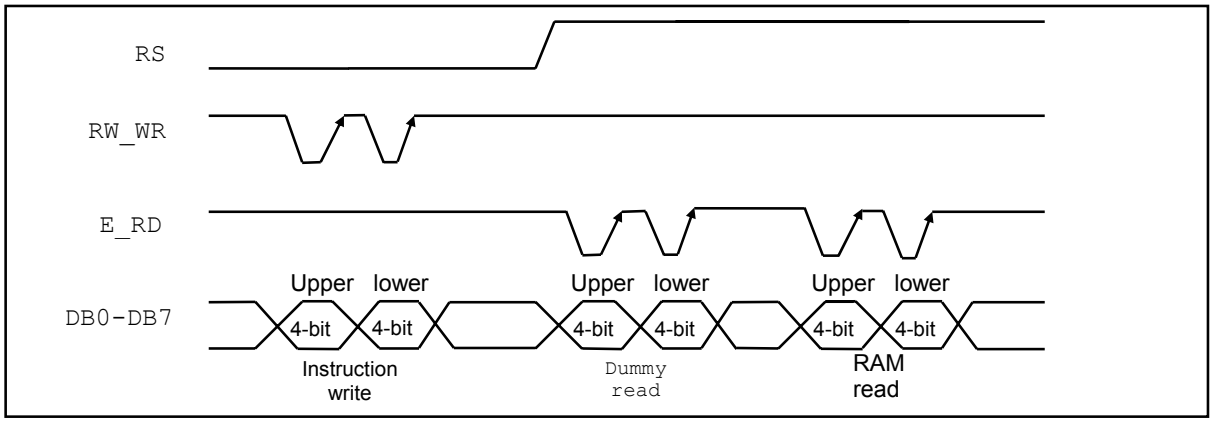
Timing Diagram of 8-bit Parallel Bus Mode Data Transfer (68 Series MPU Mode)



Timing Diagram of 8-bit Parallel Bus Mode Data Transfer (80 Series MPU Mode)



Timing Diagram of 4-bit Parallel Bus Mode Data Transfer (68 Series MPU Mode)



Timing Diagram of 4-bit Parallel Bus Mode Data Transfer (80 Series MPU Mode)

Display Data RAM (DDRAM)

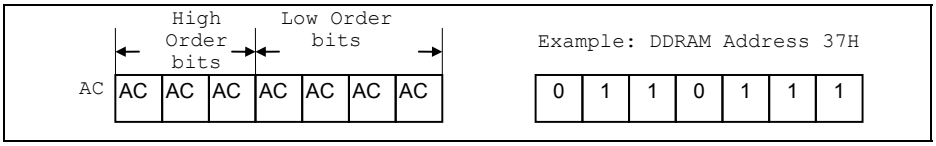
Display data RAM (DDRAM) stores display data represented in 8-bit character codes. Its extended capacity is 64 x 8 bits, or 64 characters. The area in display data RAM (DDRAM) that is not used for display can be used as general data RAM. See Figure 1 for the relationships between DDRAM addresses and positions on the liquid crystal display.

The DDRAM address (A_{DD}) is set in the address counter (AC) as hexadecimal.

- DDRAM address and corresponding display position

  There is 4 line display data stored in DDRAM but only 2 lines are shown at a time. (2 line mode)
  Hidden lines can be displayed by issuing line shift instruction.

Figure 1 DDRAM Address



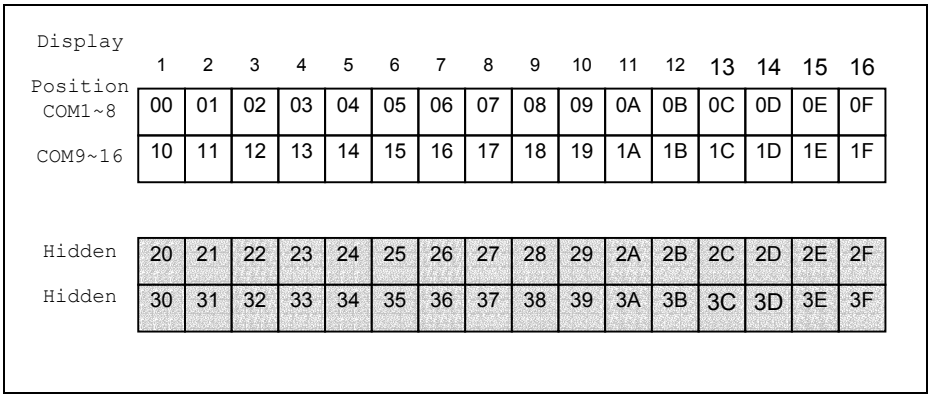


Figure 2 2-Line Mode by 16-Character Display Example

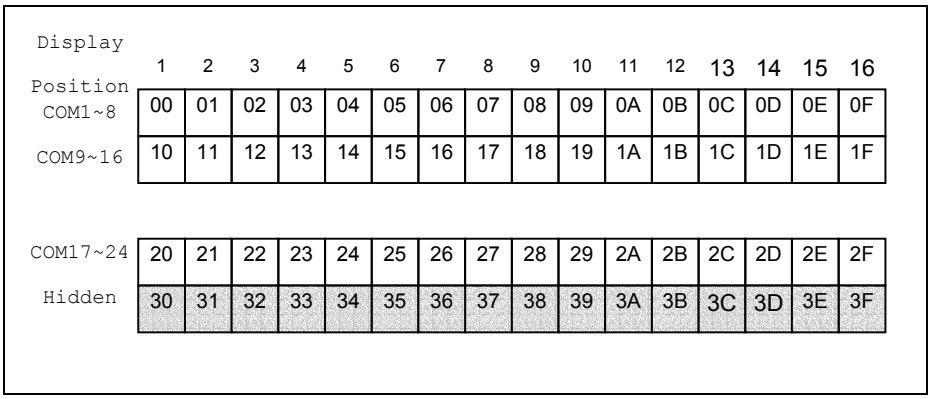


Figure 3 3-Line Mode by 16-Character Display Example

Character Generator ROM (CGROM)
The character generator ROM generates 5 x 8 dot character patterns from 8-bit character codes. It can generate 256 5 x 8 dot character patterns. User-defined character patterns are also available by mask-programmed ROM.

Character Generator RAM (CGRAM)
In the character generator RAM, the user can rewrite character patterns by program. For 5 x 8 dots, eight character patterns can be written.

Write into DDRAM the character codes at the addresses shown as the left column of Table 4 to show the character patterns stored in CGRAM.

See Table 5 for the relationship between CGRAM addresses and data and display patterns. Areas that are not used for display can be used as general data RAM.

Timing Generation Circuit
The timing generation circuit generates timing signals for the operation of internal circuits such as DDRAM, CGROM and CGRAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DDRAM, for example, there will be no undesirable interference, such as flickering, in areas other than the display area.

LCD Driver Circuit
LCD Driver circuit has 26 common and 80 segment signals for LCD driving. Data from CGRAM/CGROM is transferred to 80 bit segment latch serially, and then it is stored to 80 bit shift latch. When each common is selected by 26 bit common register, segment data also output through segment driver from 80 bit segment latch.

Cursor/Blink Control Circuit
It can generate the cursor or blink in the cursor/blink control circuit. The cursor or the blink appears in the digit at the display data RAM address set in the address counter.

Applicable Panel Size

Font	Display	Duty	Contents of outputs
5X8	2 Line X 16 Char	1/17	2x16 characters + 80icons
	3 Line x 16 Char	1/25	3x16 characters + 80icons

Correspondence between Character Codes and Character Patterns

NO.7093-0B

Table 4-1

NO.7093-C0A

b7-b4 / b3-b0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CG RAM (1)															
0001	(2)															
0010	(3)															
0011	(4)															
0100	(5)															
0101	(6)															
0110	(7)															
0111	(8)															
1000	CG RAM (1)															
1001	(2)															
1010	(3)															
1011	(4)															
1100	(5)															
1101	(6)															
1110	(7)															
1111	(8)															

Table 4-2

NO.7093-0C

b7-b4 / b3-b0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CG RAM (1)															
0001	(2)															
0010	(3)															
0011	(4)															
0100	(5)															
0101	(6)															
0110	(7)															
0111	(8)															
1000	(1)															
1001	(2)															
1010	(3)															
1011	(4)															
1100	(5)															
1101	(6)															
1110	(7)															
1111	(8)															

Character Code (DDRAM Data)								CGRAM Address						Character Patterns (CGRAM Data)							
b7	b6	b5	b4	b3	b2	b1	b0	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	-	0	0	0	0	0	0	0	0	0	-	-	-	1	1	1	1	1
					0	0	0				0	0	1				0	0	1	0	0
					0	0	0				0	1	0				0	0	1	0	0
					0	0	0				0	1	1				0	0	1	0	0
					0	0	0				1	0	0				0	0	1	0	0
					0	0	0				1	0	1				0	0	1	0	0
					0	0	0				1	1	0				0	0	1	0	0
					0	0	0				1	1	1				0	0	0	0	0
0	0	0	0	-	0	0	1	0	0	1	0	0	0	-	-	-	1	1	1	1	0
					0	0	1				0	0	1				1	0	0	0	1
					0	0	1				0	1	0				1	0	0	0	1
					0	0	1				0	1	1				1	1	1	1	0
					0	0	1				1	0	0				1	0	1	0	0
					0	0	1				1	0	1				1	0	0	1	0
					0	0	1				1	1	0				1	0	0	0	1
					0	0	1				1	1	1				0	0	0	0	0

Table 5

Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character patterns (CGRAM Data)

Notes:

1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).
2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line CGRAM address (b2,b1,b0) = (1,1,1) is the cursor line. Should the cursor position is displayed with CGRAM character the 8th line output data will become (1,1,1,1,1).
3. Character pattern row positions correspond to CGRAM data bits 0 to 4 (bit 4 being at the left).
4. 1 for CGRAM data corresponds to display selection and 0 to non-selection.

"-": Indicates no effect.

Relationship between ICONRAM address and display pattern

When ICONRAM data is filled the corresponding position displayed is described as the following table.

ICONRAM address	ICONRAM bits							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	-	-	-	S1	S2	S3	S4	S5
01H	-	-	-	S6	S7	S8	S9	S10
02H	-	-	-	S11	S12	S13	S14	S15
:	:	:	:	:	:	:	:	:
0DH	-	-	-	S66	S67	S68	S69	S70
0EH	-	-	-	S71	S72	S73	S74	S75
0FH	-	-	-	S76	S77	S78	S79	S80

Notes : S1~S80 corresponds to display position of SEG1 ~ SEG80.

Segment data shift direction corresponding to DIRS pin setting

Segment data shift direction can be altered by setting values to the DIRS pin described as the following table.

DIRS	Segment data shift direction
Low	S1 → S2 → S3 → S4 → S5 → ..... S78 → S79 → S80
High	S80 → S79 → S78 → S77 → S76 → ..... S3 → S2 → S1

Common data shift direction corresponding to S

Common data shift direction can be altered by setting the S value through function set instruction. The directions corresponding to S value is described as the following table.

S	Common data shift direction
Low	COM1 → COM2 → COM3 → ..... COM15 → COM24 → COMI1(COMI2)
High	COMI1(COMI2) → COM24 → COM15 → ..... COM3 → COM2 → COM1

Instructions

There are four categories of instructions that:

- Designate ST7093 functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Others

Instruction Table:

Instruction	Instruction Code										Description	Execution Time
	RS	RW	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0		
Return Home	0	0	0	0	0	0	0	0	1	x	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	80us
Double height Mode Set	0	0	0	0	0	0	1	0	DH2	DH1	Set double height mode (DH2, DH1) = (0,0) : normal (default) (0,1) :1)2-line mode COM1..COM16 is a double height COM17..COM24 is no use 2) 3-line mode COM1..COM16 is a double height COM17..COM24 is normal (1,0) : 1) 2-line mode normal display 2) 3-line mode COM1..COM8 is normal COM9..COM24 is a double height l (1,1) : normal	80us
Display control	0	0	0	0	1	0	1	C	B	D	C=0 : cursor off(default) C=1: cursor on B=0 : blink off (default) B=1: blink on D=0 : display off(default) D=1: display on	80us
Power save control	0	0	0	0	0	0	1	1	OS	PS	OS=0 : OSC off(default) OS=1 : OSC on PS=0 : save off(default) PS=1 : save on	80us
Function Set	0	0	0	0	0	1	0	N	S	CG	(Display line mode) N=0 : 2 line display(default) N=1 : 3 line display (Shifting direction of COM) S=0 : 1) 2-line mode COM1→COM16(default) 2) 3-line mode COM1→COM24(default) S=1 : 1) 2-line mode COM16 → COM1 2) 3-line mode COM24 → COM1 (Select CGRAM or CGROM) CG=0 : CGROM(default) CG=1 : CGRAM	80us

Instruction	Instruction Code										Description	Execution Time
	RS	RW	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0		
Line shift mode	0	0	0	0	0	1	1	0	LS2	LS1	(LS2,LS1) = (0,0) : DDRAM line 1 on top (0,1) : DDRAM line 2 on top (1,0) : DDRAM line 3 on top (1,1) : DDRAM line 4 on top	80us
Bias control	0	0	0	0	0	1	1	1	x	BS	BS=0 : 1/5 bias(default) BS=1 : 1/4 bias	80us
Power control	0	0	0	0	1	0	0	VC	VR	VF	VC=0 : voltage booster off(default) =1 : voltage booster on VR=0 : voltage regulator off(default) =1 : voltage regulator on VF =0 : voltage follower off(default) =1 : voltage follower on	80us
ICONRAM address	0	0	0	1	0	AC 4	AC 3	AC 2	AC 1	AC 0	Set ICONRAM address in address counter EV addr : 10H	80us
CGRAM/ DDRAM address	0	0	1	AC 6	AC 5	AC 4	AC 3	AC 2	AC 1	AC 0	Set CGRAM/DDRAM address DDRAM : 00H ~ 3FH CGRAM : 40H ~ 7FH	80us
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM)	80us
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM)	80us

Note:
1. “x” Don’t care
2. Make sure to use enough delay time(100us) between instruction

INSTRUCTION DESCRIPTION

- **Return Home**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	1	x

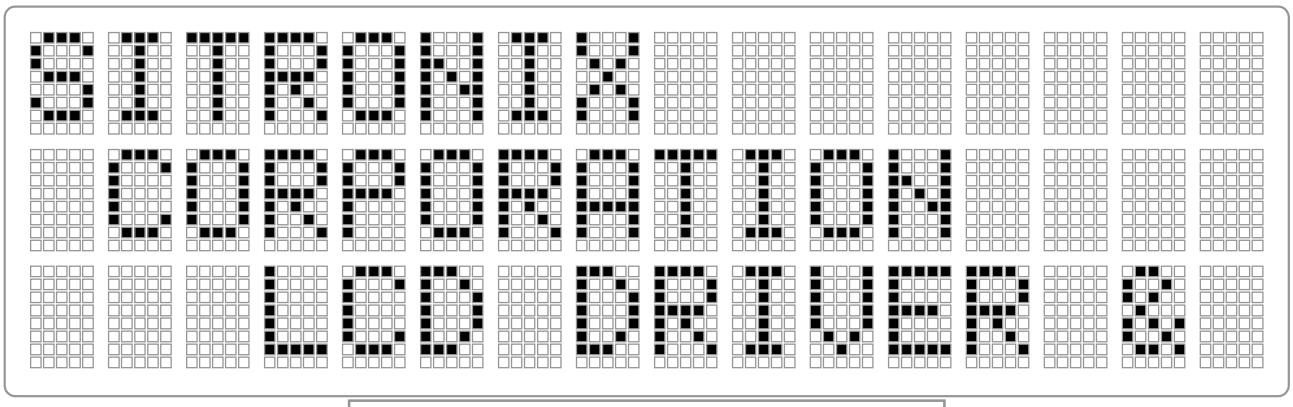
Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to the left edge on first line of display.

- **Double height mode**

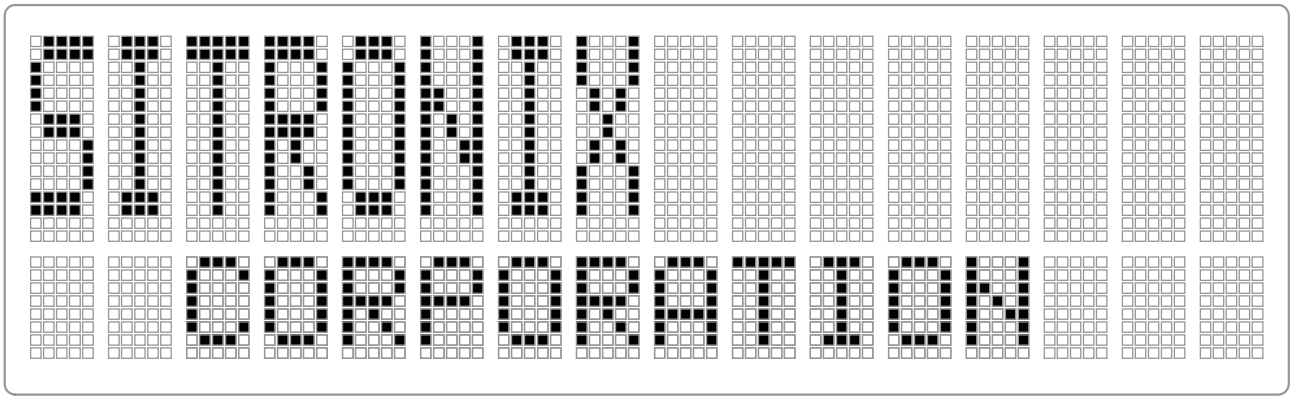
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	1	0	DH2	DH1

Set double height mode

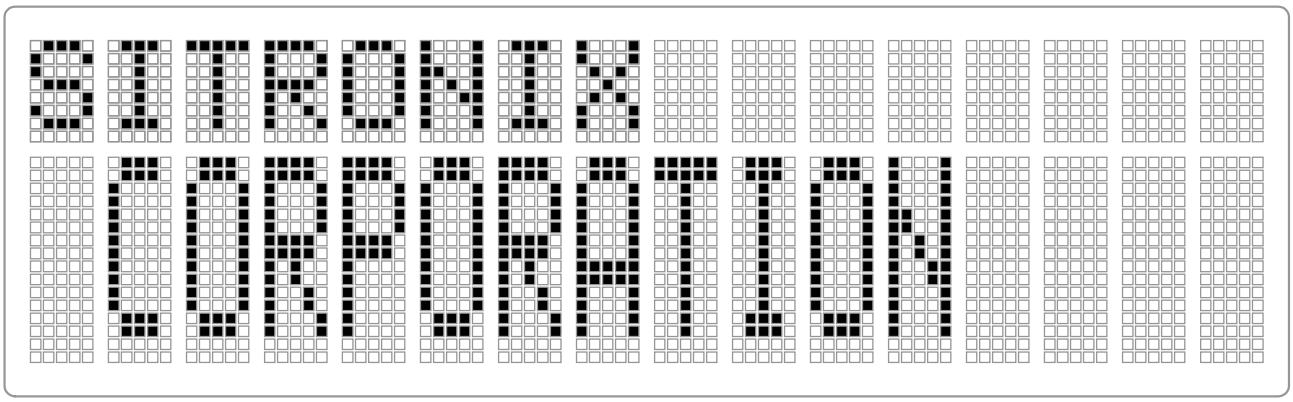
DH2	DH1	Action
Low	Low	Normal display (default)
Low	High	1) 2-line mode COM1..COM16 is a double height COM17..COM24 is no use 2) 3-line mode COM1..COM16 is a double height COM17..COM24 is normal
High	Low	1) 2-line mode normal display 2) 3-line mode COM1..COM8 is normal COM9..COM24 is a double height
High	High	Normal display



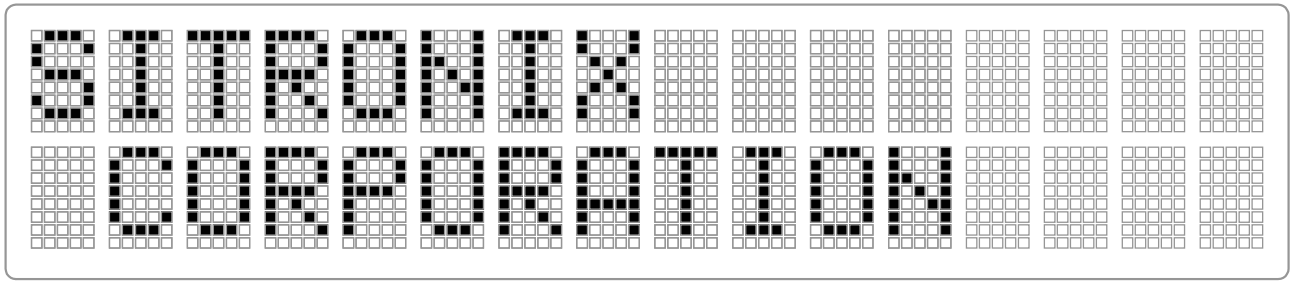
3 Line mode normal display (DH2,DH1=0,0)



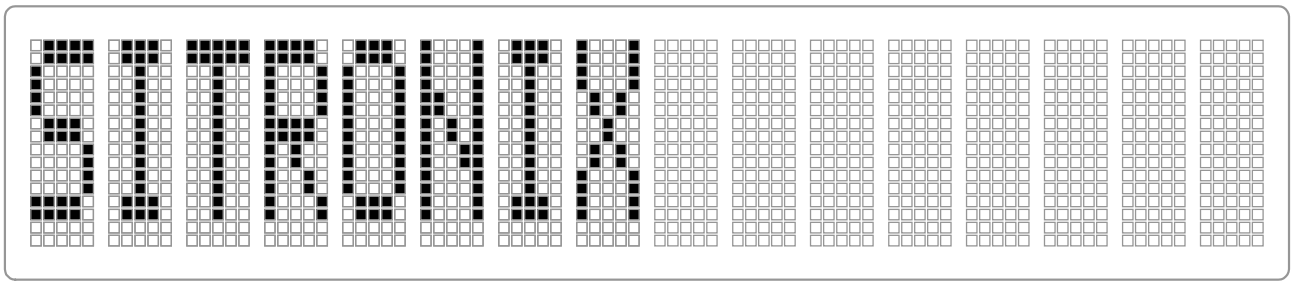
3 Line mode COM1 ..16 is a double height line, COM17 .. 24 is normal (DH2,DH1=0,1)



COM1 ..8 is normal , COM9 .. 24 is a double height line (DH2.DH1 = 1,0)



2 line mode normal display (DH2,DH1=0,0)



2 line mode COM1 ..16 is a double height line (DH2,DH1=0,1)

- **Bias Control**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	1	1	1	*	BS

Bias control instruction will set the internal bias level generator
BS = “Low” (default) : 1/5 bias
= ”High” : 1/4 bias

- **Display control**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	0	1	C	B	D

Control display/cursor/blink ON/OFF 1 bit register.
C : Cursor ON/OFF control bit

When C = "High", cursor is turned on.

When C = "Low", cursor is disappeared in current display.

The cursor data performs exclusive OR with any display data on the cursor line.

B : Cursor Blink ON/OFF control bit

When B = "High", C=”High” then performs alternate between reverse display character and display character at the cursor position. If C=”Low” then display is normal regardless of B.

When B = "Low", blink is off.

D : Display ON/OFF control bit

When D = "High", entire display is turned on.

When D = "Low", display is turned off, but display data is remained in DDRAM.

- **Function set**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	1	0	N	S	CG

(Display line mode)

N : Number of display lines

=”Low” (default) : 2 lines COM1~COM16 are displayed
=”High” : 3 lines COM1~COM24 are displayed

(Shifting direction of COM)
S : Common data shift direction
=”Low” (default) : 1) 2-line mode COM1→COM16(default)
2) 3-line mode COM1→COM24(default)
=”High” : 1) 2-line mode COM16 → COM1
2) 3-line mode COM24 → COM1

(Select CGRAM or CGROM)
CG: CGRAM enable bit
=”Low” (default) : CGRAM is disabled, CGROM data pattern will appear on the display instead.
=”High” : CGRAM enabled.

- **Power save set**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	1	1	OS	PS

OS : Oscillator on/off bit

When OS = "High", internal oscillator is enabled.

When OS = "Low" (default), internal oscillator is disabled

PS : Power save mode

When PS = "Low" (default) Power save mode is disabled.

When PS = "High" , Power save mode is enabled.

- **Set ICONRAM Address**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	0	AC	AC	AC	AC	AC

Set ICONRAM address to AC.

Before writing or reading data, set ICONRAM address should be performed. After each write or read the address counter will increase 1 automatically. 5 bit ICON is stored in each data byte. If (C,B) = (1,1) then ICON display will blink. ICONRAM address is from 00H to 0FH. Address 10H is reserved for electronic volume level setting.

- **Set CGRAM/DDRAM Address**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	AC	AC	AC	AC	AC	AC	AC

Set CGRAM /DDRAM address to AC.

CGRAM and DDRAM share the same address space. Before accessing CGRAM/DDRAM, set CGRAM/DDRAM address should be performed. Address counter will automatically increase by 1 after each write or read operation. After accessing 7FH the address will reset to 00H.

Addr	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00H	DDRAM LINE 1 (00H~0FH)															
10H	DDRAM LINE 2 (10H~1FH)															
20H	DDRAM LINE 3 (20H~2FH)															
30H	DDRAM LINE 4 (30H~3FH)															
40H	CGRAM (pattern 0)								CGRAM (pattern1)							
50H	CGRAM (pattern 2)								CGRAM (pattern 3)							
60H	CGRAM (pattern 4)								CGRAM (pattern5)							
70H	CGRAM (pattern 6)								CGRAM (pattern 7)							

- **Read Data from CGRAM/DDRAM or ICONRAM**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	1	D7	D6	D5	D4	D3	D2	D1	D0

Before RAM data read, address set of either CGRAM/DDRAM or ICONRAM should be performed. The first read is a dummy read. The data is invalid. The correct data is obtain from the second read. After read data the address counter will increase by 1 automatically. If multiple read in succession only the first read data is dummy.

- **Line shift mode**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	1	1	0	LS2	LS1

Set Line Shift mode

LS2	LS1	Action
Low	Low	DDRAM Line1 shows at the first line of LCD (default)
Low	High	DDRAM Line2 shows at the first line of LCD
High	Low	DDRAM Line3 shows at the first line of LCD
High	High	DDRAM Line4 shows at the first line of LCD

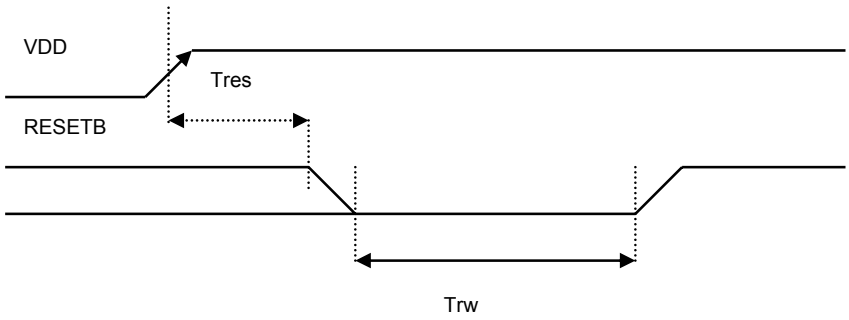
Reset Function

Initializing by Internal Reset Circuit

External reset can be achieved by pulling low RESETB pin.

1. Function set:
   S = 0; COM left shift
   CG = 0; CGRAM disable
2. Display on/off control:
   D = 0; Display off
   C = 0; Cursor off
   B = 0; Blinking off
3. Power control & bias
   BS = 0 ; 1/5 bias
   OS = 0 ; oscillator off
   PS = 0 ; power save off
   VC = 0; voltage booster off
   VR = 0; voltage regulator off
   VF = 0; voltage follower off
4. Line shift mode
   (LS2,LS1) = (0,0) ; DDRAM line 1 shown at the first line of LCD display
5. Electronic contrast control register
   (E4,E3,E2,E1,E0) = (0,0,0,0,0)

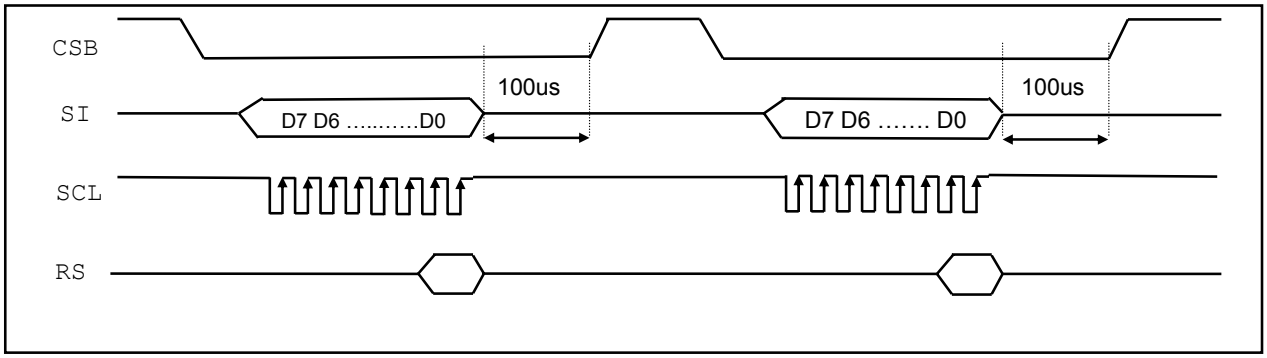
RESETB pulse width	Trw	10us
RESET start time	Tres	50ns


VDD
Tres
RESETB
Trw

Interfacing to the MPU

The ST7093 can send data in either two 4-bit operations or one 8-bit operation, or 4 pin clock synchronous serial interface is used.

- For 4-bit interface data, only four bus lines (DB4 to DB7) are used for transfer. Bus lines DB0 to DB3 are disabled. The data transfer between the ST7093 and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB4 to DB7) are transferred before the four low order bits (for 8-bit operation, DB0 to DB3).
- For 8-bit interface data, all eight bus lines (DB0 to DB7) are used.
- For serial interface, by setting PS = "Low" DB7 become SI (serial in data), DB6 become SCL (serial clock). Each bit of data transfer is at the rising edge of SCL. At the rising edge of 8th SCL the data is converted into 8 bit parallel data and RS bit is read in to select whether write data or write instruction. Read operation is not supported.



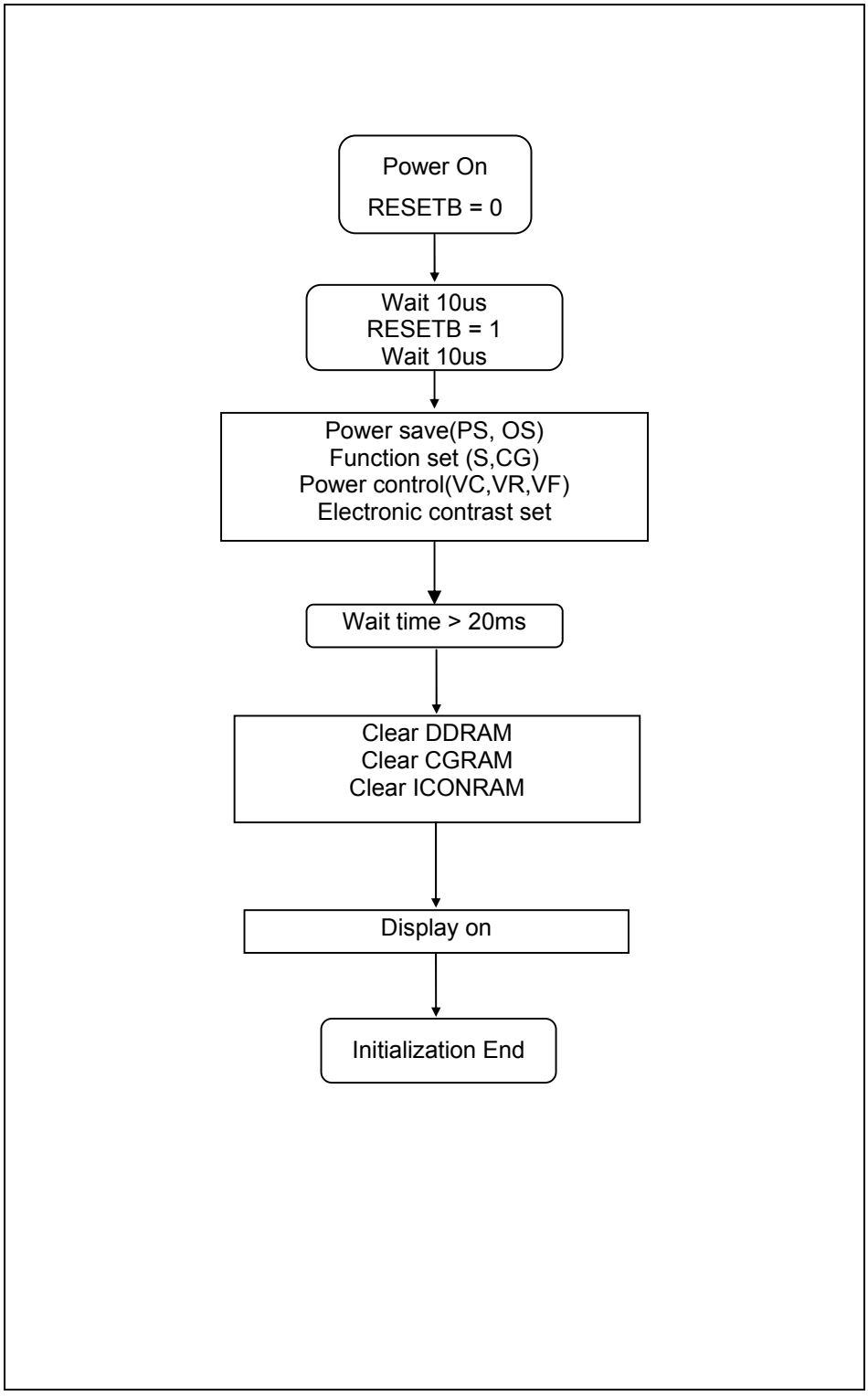
Timing Diagram of Serial Mode Data Transfer (serial Mode)

Supply Voltage for LCD Drive

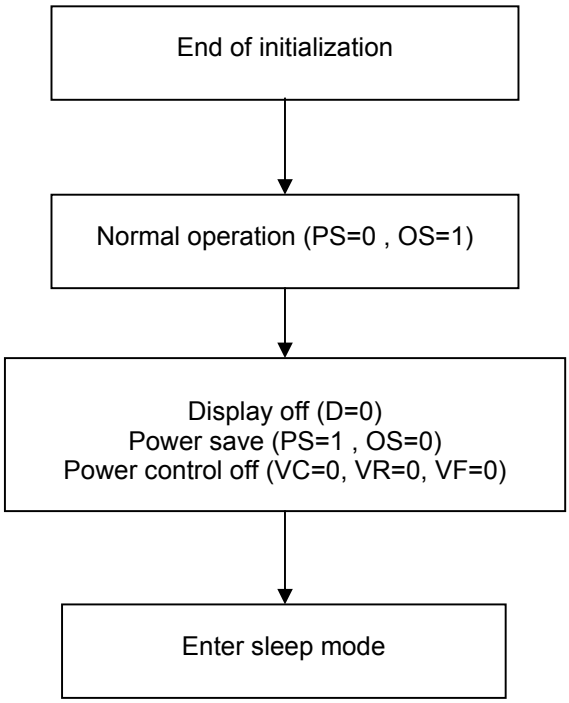
There are different voltages that supply to ST7093's pin (V0 – V4) to obtain LCD drive waveform. The relations of the bias, duty factor and supply voltages are shown as below:

	Duty Factor 1/17	
	Bias	
Supply Voltage	1/4	1/5
V0	V_{LCD}	V_{LCD}
V1	3/4 V_{LCD}	4/5 V_{LCD}
V2	1/2V_{LCD}	3/5 V_{LCD}
V3	1/2V_{LCD}	2/5 V_{LCD}
V4	1/4 V_{LCD}	1/5 V_{LCD}

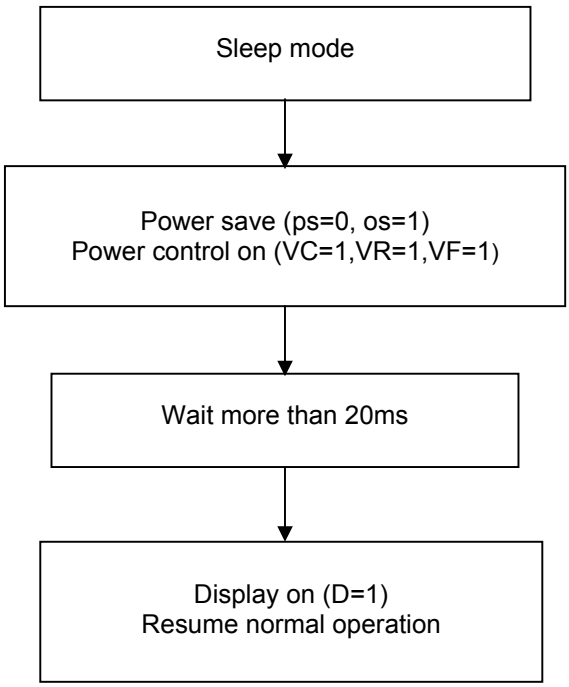
Initialization sequence



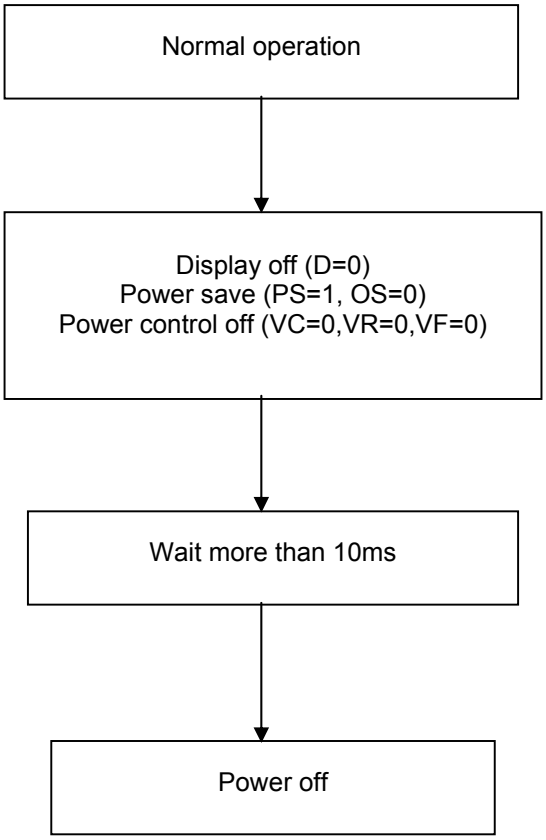
Sleep mode set



Sleep mode release

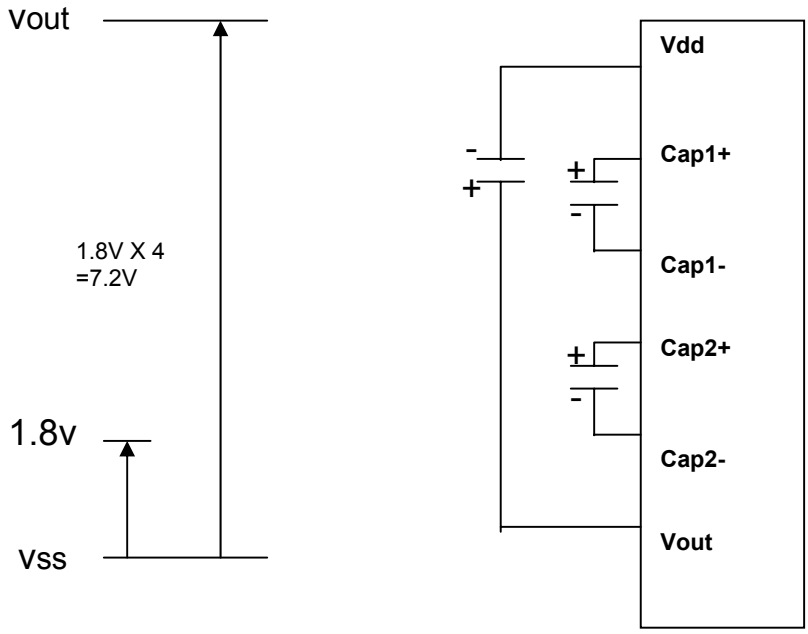


Power off sequence



Voltage booster

The voltage booster use internal generates reference voltage 1.8V to boost 4 times to produce Vout as 7.2V.



Voltage regulator

The voltage regulator circuit is used to obtain an appropriate LCD panel driving voltage. This voltage is obtained By adjusting resistors Ra and Rb as shown in equation (1) or (2) ,and by setting Electronic Contrast Control data Bits, see this equation (3) or (4).

The potential of V0 Pin can be adjusted within Vout – Vref, Vref is the internal constant voltage source of the Chip and this value is 2.0V in the condition vdd ≧ 2.4V

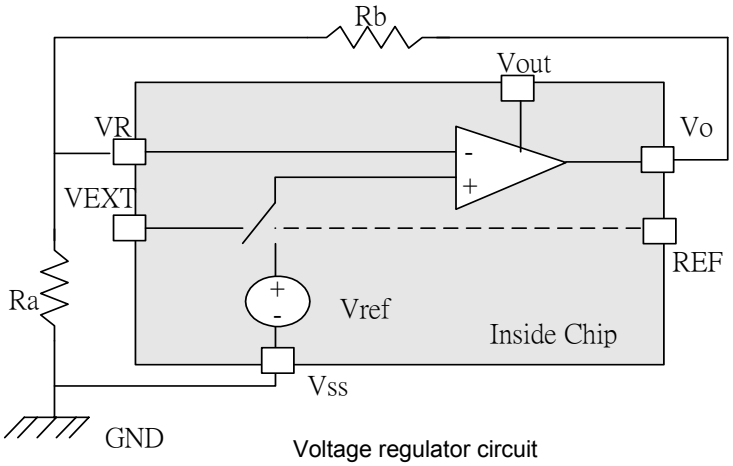
The REF selects which voltage is used for voltage regulator between the ecternal VEXT and internal Vref.

■ Voltage regulation by adjusting resistors Ra, Rb

When REF is “Low”
V0 = (1 + Rb / Ra) x Vref……..(1)

When REF is “High”
V0 = (1 + Rb / Ra) x VEXT …..(2)

Reference set value
Ra = 1MΩ Rb = 1.5MΩ



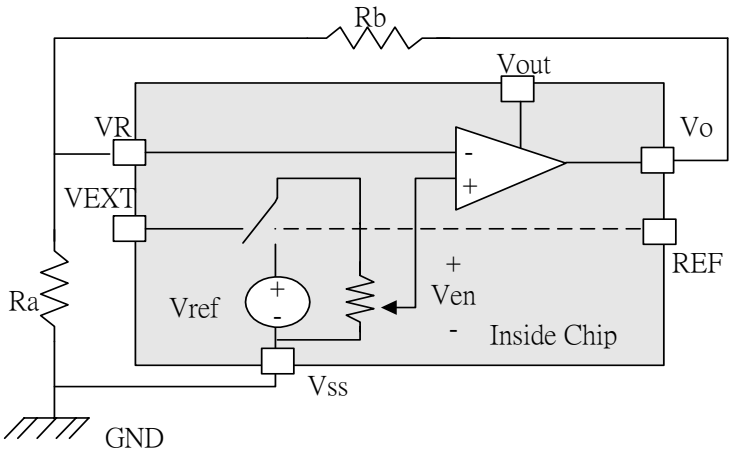
Voltage regulator circuit

Electronic contrast control (32 steps)

Electronic contrast control data bits is 10H = (C4, C3, C2, C1, C0), Voltage regulation is adjusted as 32-contrast step According to the value of Electronic contrast control data bits. LCD drive voltage V0 has one of 32 voltage values if 5-bit data is set to the electronic contrast control register (ICONRAM address 10H). When using the electronic contrast control function, you need to turn the voltage regulators on using power control instruction.

When REF is “Low”
V0 = (1 + Rb / Ra) x Ven ….. (3)
Ven = Vref - nα
(n = 0, 1, 2, ….. 30, 31)
α = Vref / 150

When REF is “High”
V0 = (1 + Rb / Ra) x Ven ….. (4)
Ven = Vext - nα
(n = 0, 1, 2, ….. 30, 31)
α = Vext / 150

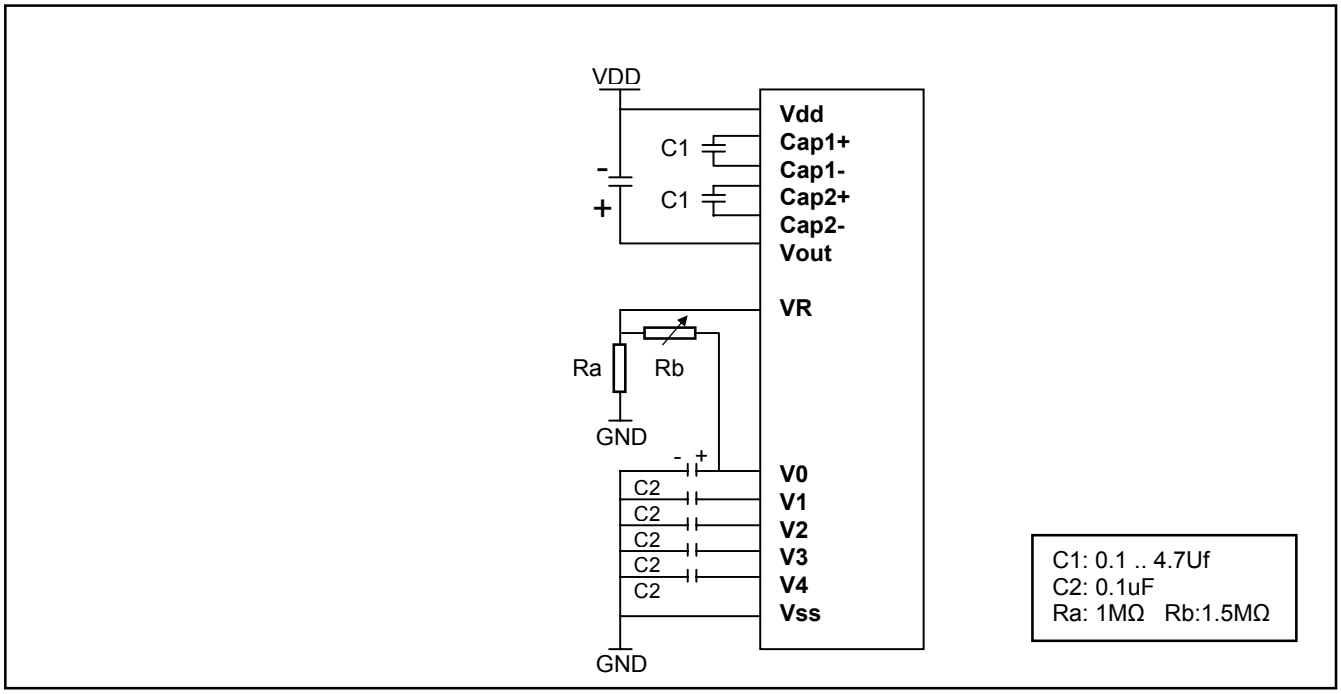


Electronic contrast control circuit

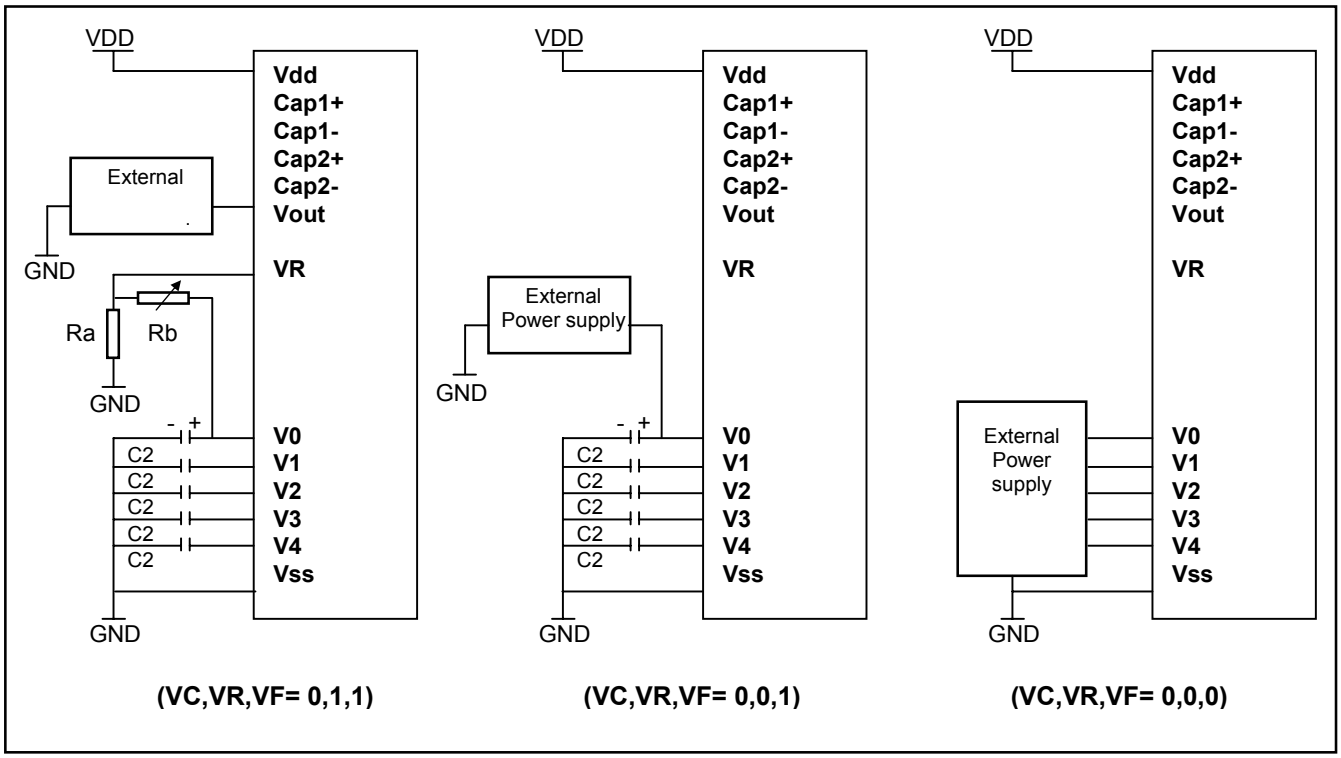
No.	C7	C6	C5	C4	C3	C2	C1	C0	n	V0	Contrast
1	-	-	-	0	0	0	0	0	0 (default)	Maximum	High
2	-	-	-	0	0	0	0	1	1	.	.
3	-	-	-	0	0	0	1	0	2	.	.
4	-	-	-	0	0	0	1	1	3	.	.
. . .									. . .	. . .	. . .
31	-	-	-	1	1	1	1	0	30	.	.
32	-	-	-	1	1	1	1	1	31	Minimum	Low

Electronic contrast control register (“-“ don’t care)

Voltage generator circuit

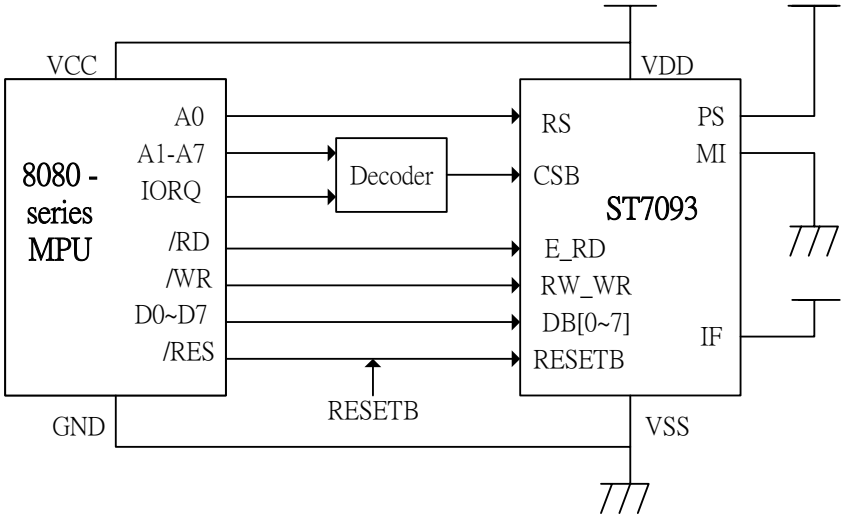


When built-in power supply is used (VC,VR,VF = 1,1,1)

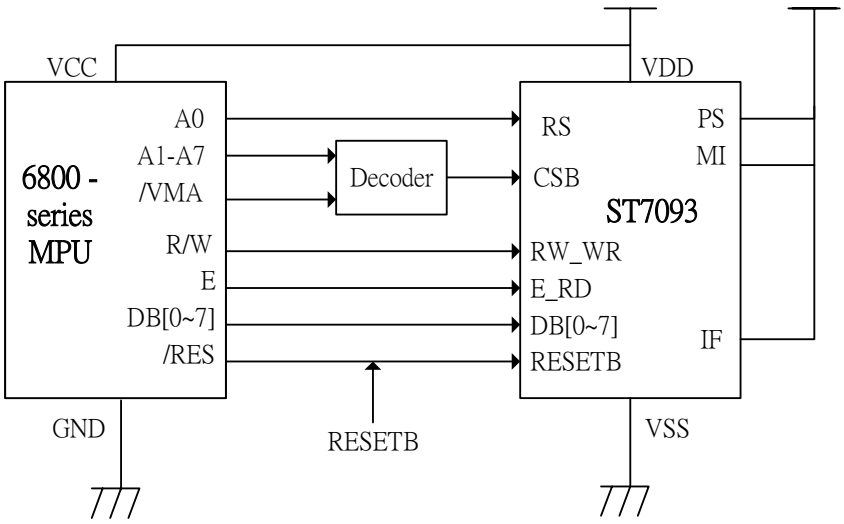


When external power supply is used **(C2:01 to 4.7uF)**

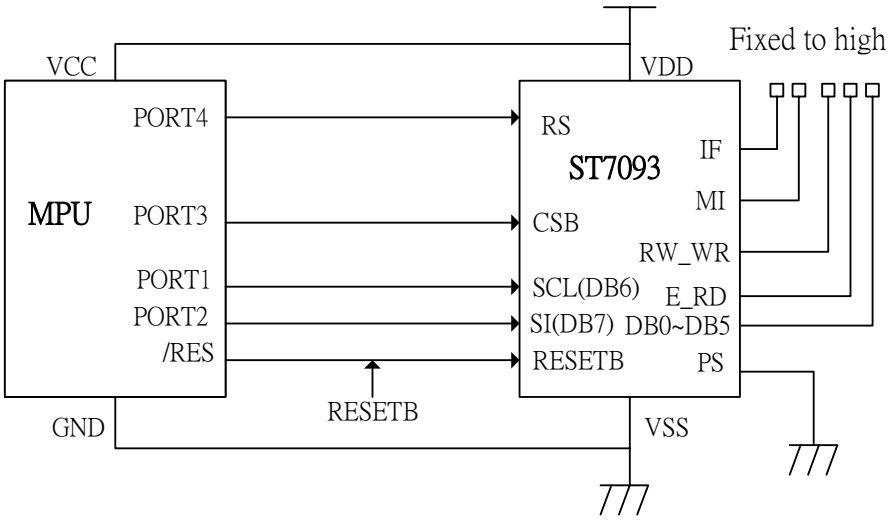
MPU Interface



Parallel interfacing with 8080-series microprocessors.



Parallel interfacing with 6800-series microprocessors.



Clock synchronized serial interfacing with any microprocessors.

- **Absolute Maximum Ratings**

Characteristics	Symbol	Value
Power Supply Voltage	V_{DD}	-0.3V to +7.0V
LCD Driver Voltage	V_{LCD}	-0.3V to +10.0V
Input Voltage	V_{IN}	-0.3V to V_{DD}+0.3V
Operating Temperature	T_A	-40°C to + 85°C
Storage Temperature	T_{STO}	-55°C to + 125°C

DC CHARACTERISTICS (T_A = 25°C , VDD =2.4V – 3.6V)

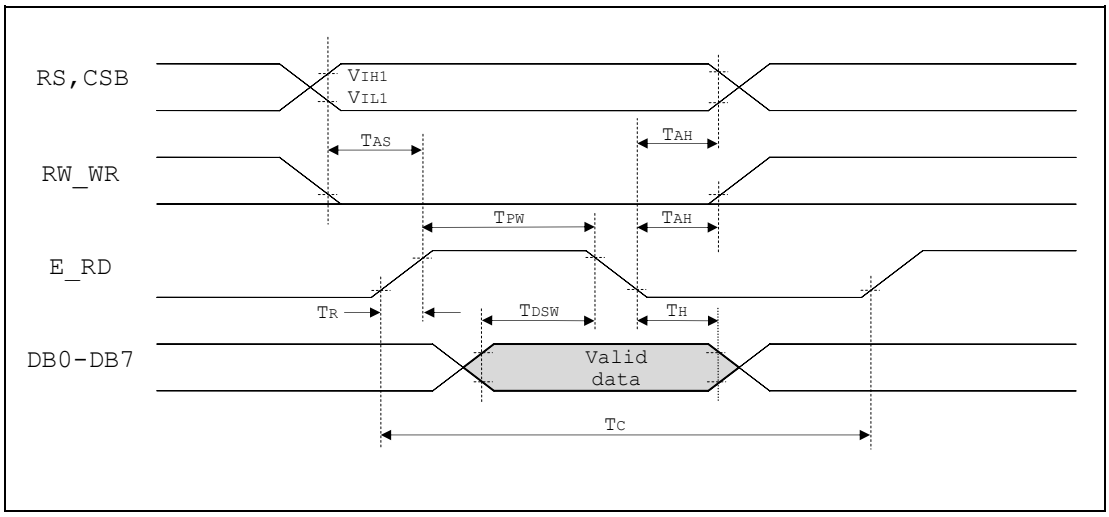
Symbol	Characteristics	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	-	2.4	-	3.6	V
V_{LCD}	LCD Voltage	V_0- V_{SS}	3.0	-	7.0	V
I_{DD}	Power Supply Current	f_{OSC} = 160KHz, V_{DD} =3.0V checker pattern no CPU access	-	90	115	uA
V_{IH1}	Input High Voltage (Except OSC1)	-	0.7V_{DD}	-	V_{DD}	V
V_{IL1}	Input Low Voltage (Except OSC1)	-	- 0.3	-	0.6	V
V_{IH2}	Input High Voltage (OSC1)	-	V_{DD} – 1	-	V_{DD}	V
V_{IL2}	Input Low Voltage (OSC1)	-	-	-	1.0	V
V_{OH1}	Output High Voltage (DB0 - DB7)	I_{OH} = -0.1mA	0.8V_{DD}	-	V_{DD}	V
V_{OL1}	Output Low Voltage (DB0 - DB7)	I_{OL} = 0.1mA	-	-	0.4	V
V_{OH2}	Output High Voltage (Except DB0 - DB7)	I_{OH} = -0.04mA	0.8V_{DD}	-	V_{DD}	V
V_{OL2}	Output Low Voltage (Except DB0 - DB7)	I_{OL} = 0.04mA	-	-	0.2 V_{DD}	V
R_{COM}	Common Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	20	KΩ
R_{SEG}	Segment Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	30	KΩ
I_{LEAK}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-1	-	1	μA

AC CHARACTERISTICS (T_A = 25°C, VDD = 2.7 V - 3.6 V)

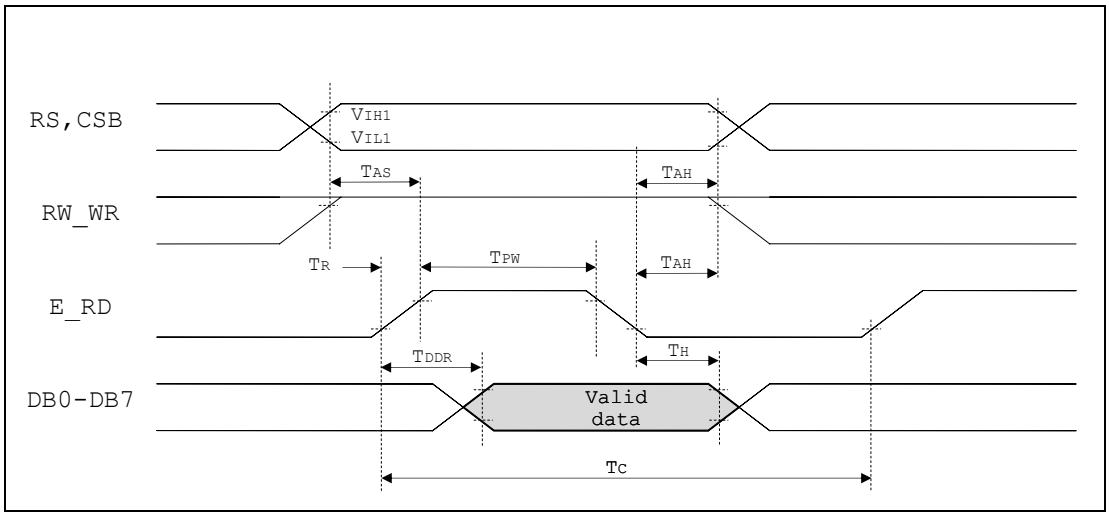
Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	OSC Frequency	-	112	160	208	KHz
External Clock Operation						
f_{EX}	External Frequency	-	112	160	208	KHz
	Duty Cycle	-	45	50	55	%
T_R,T_F	Rise/Fall Time	-			0.2	μs

TIMING CHARACTERISTICS

- **Writing data from MPU TO ST7093 by 68 mode parallel interface**



- **Reading data from ST7093 TO MCU by 68 mode parallel interface**



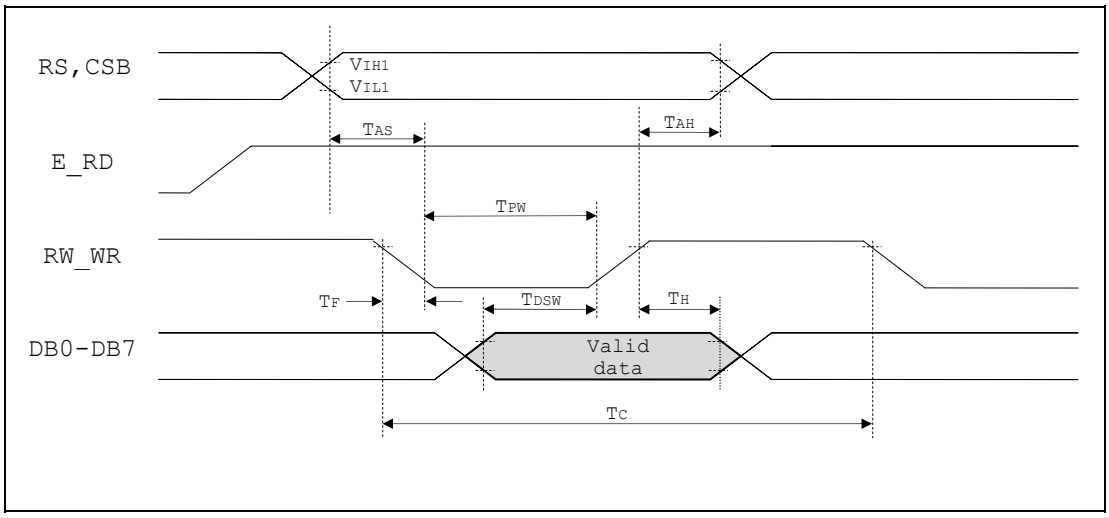
68 INTERFACE READ/WRITE TIMING(T_A = 25°C, VDD =3.6V)

	Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
WRITE MODE	T_C	Enable Cycle Time	Pin E	100	-	-	us
	T_{PW}	Enable Pulse Width	Pin E	300	-	-	ns
	T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
	T_{AS}	Address Setup Time	Pins: RS,RW,CSB	100	-	-	ns
	T_{AH}	Address Hold Time	Pins: RS,RW,CSB	20	-	-	ns
	T_{DSW}	Data Setup Time	Pins: DB0 - DB7	150	-	-	ns
	T_H	Data Hold Time	Pins: DB0 - DB7	20	-	-	ns
READ MODE	T_C	Enable Cycle Time	Pin E	100	-	-	us
	T_{PW}	Enable Pulse Width	Pin E	300	-	-	ns
	T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
	T_{AS}	Address Setup Time	Pins: RS,RW,CSB	360	-	-	ns
	T_{AH}	Address Hold Time	Pins: RS,RW,CSB	20	-	-	ns
	T_{DDR}	DB output ready Time	Pins: DB0 - DB7	-	-	300	ns
	T_H	DB output Hold Time	Pins: DB0 - DB7	50	-	-	ns

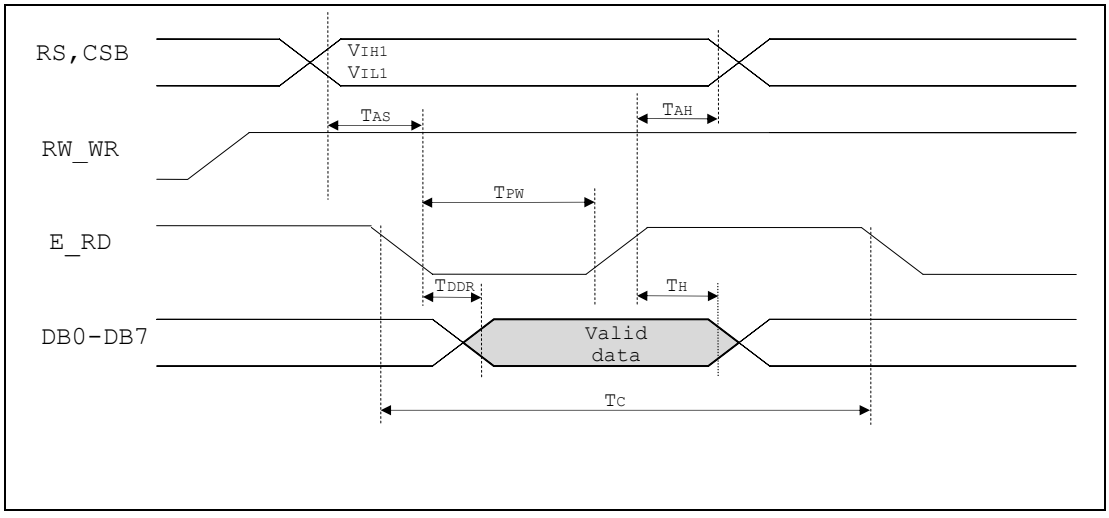
68 INTERFACE READ/WRITE TIMING (T_A = 25°C, VDD = 2.7V)

	Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
WRITE MODE	T_C	Enable Cycle Time	Pin E	100	-	-	us
	T_{PW}	Enable Pulse Width	Pin E	300	-	-	ns
	T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
	T_{AS}	Address Setup Time	Pins: RS,RW,CSB	500	-	-	ns
	T_{AH}	Address Hold Time	Pins: RS,RW,CSB	20	-	-	ns
	T_{DSW}	Data Setup Time	Pins: DB0 - DB7	300	-	-	ns
	T_H	Data Hold Time	Pins: DB0 - DB7	20	-	-	ns
READ MODE	T_C	Enable Cycle Time	Pin E	100	-	-	us
	T_{PW}	Enable Pulse Width	Pin E	300	-	-	ns
	T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
	T_{AS}	Address Setup Time	Pins: RS,RW,CSB	580	-	-	ns
	T_{AH}	Address Hold Time	Pins: RS,RW,CSB	20	-	-	ns
	T_{DDR}	DB output ready Time	Pins: DB0 - DB7	-	-	340	ns
	T_H	DB output Hold Time	Pins: DB0 - DB7	50	-	-	ns

- **Writing data from MPU to ST7093 by 80 mode parallel interface**



- **Reading data from ST7093 to MPU by 80 mode parallel interface**



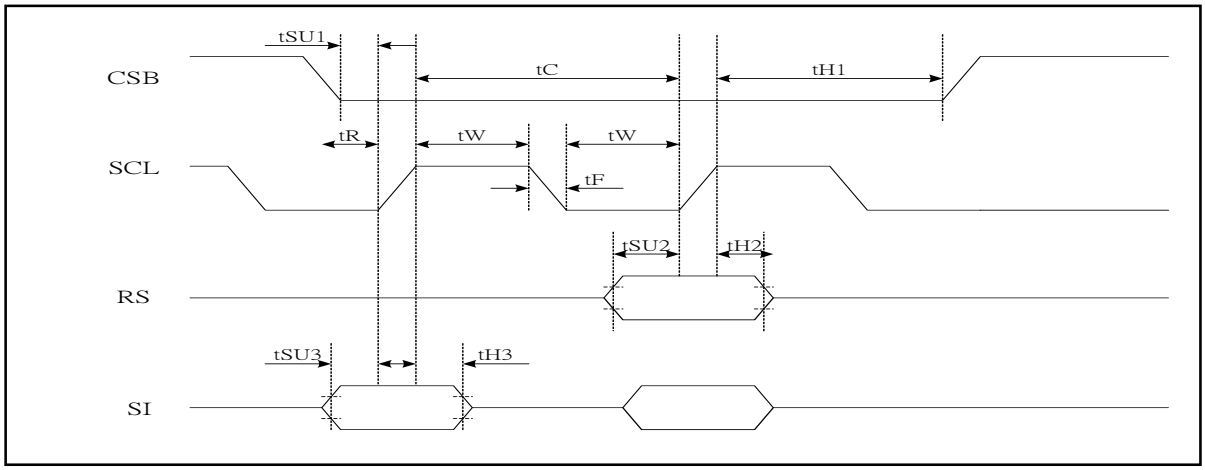
80 INTERFACE READ/WRITE TIMING (TA = 25oC, VDD = 3.6V)

	Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
WRITE MODE	T_C	Enable Cycle Time	Pin E	100	-	-	us
	T_{PW}	Enable Pulse Width	Pin E	300	-	-	ns
	T_R, T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
	T_{AS}	Address Setup Time	Pins: RS,RW,CSB	40	-	-	ns
	T_{AH}	Address Hold Time	Pins: RS,RW,CSB	200	-	-	ns
	T_{DSW}	Data Setup Time	Pins: DB0 - DB7	180	-	-	ns
	T_H	Data Hold Time	Pins: DB0 - DB7	40	-	-	ns
READ MODE	T_C	Enable Cycle Time	Pin E	100	-	-	us
	T_{PW}	Enable Pulse Width	Pin E	300	-	-	ns
	T_R, T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
	T_{AS}	Address Setup Time	Pins: RS,RW,CSB	360	-	-	ns
	T_{AH}	Address Hold Time	Pins: RS,RW,CSB	20	-	-	ns
	T_{DDR}	DB output ready Time	Pins: DB0 - DB7	-	-	300	ns
	T_H	DB output Hold Time	Pins: DB0 - DB7	50	-	-	ns

80 INTERFACE READ/WRITE TIMING (T_A = 25°C, VDD = 2.7V)

	Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
WRITE MODE	T_C	Enable Cycle Time	Pin E	100	-	-	us
	T_{PW}	Enable Pulse Width	Pin E	300	-	-	ns
	T_R, T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
	T_{AS}	Address Setup Time	Pins: RS,RW,CSB	40	-	-	ns
	T_{AH}	Address Hold Time	Pins: RS,RW,CSB	380	-	-	ns
	T_{DSW}	Data Setup Time	Pins: DB0 - DB7	280	-	-	ns
	T_H	Data Hold Time	Pins: DB0 - DB7	40	-	-	ns
READ MODE	T_C	Enable Cycle Time	Pin E	100	-	-	us
	T_{PW}	Enable Pulse Width	Pin E	300	-	-	ns
	T_R, T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
	T_{AS}	Address Setup Time	Pins: RS,RW,CSB	440	-	-	ns
	T_{AH}	Address Hold Time	Pins: RS,RW,CSB	40	-	-	ns
	T_{DDR}	DB output ready Time	Pins: DB0 - DB7	-	-	340	ns
	T_H	DB output Hold Time	Pins: DB0 - DB7	50	-	-	ns

- **Writing data from MPU TO ST7093 by Serial mode interface**



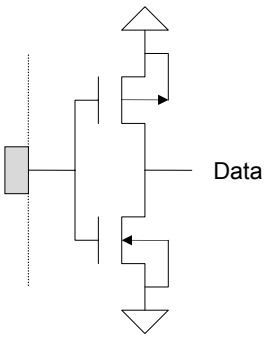
SERIAL INTERFACE WRITE TIMING (T_A = 25°C, VDD = 3.6V)

	Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
WRITE MODE	T_C	Enable Cycle Time	Pin SCL	3.0			us
	T_W	Enable Pulse Width	Pin SCL	1.5			us
	T_R,T_F	Enable Rise/Fall Time	Pin SCL			25	ns
	T_{SU1}	CSB Setup Time	Pin CSB	20			ns
	T_{H1}	CSB Hold Time	Pin CSB	100			us
	T_{SU2}	Rs Data Setup Time	Pin RS	40			ns
	T_{H2}	Rs Data Hold Time	Pin RS	40			ns
	T_{SU3}	SI Data Setup Time	Pin SI	40			ns
	T_{H3}	SI Data Hold Time	Pin SI	40			ns

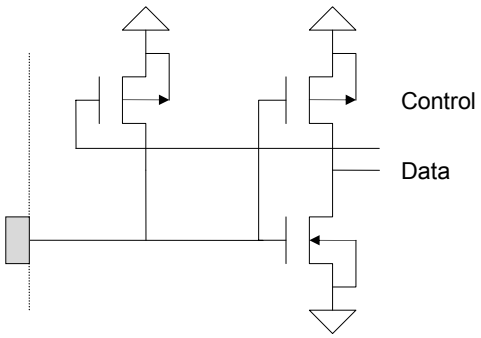
SERIAL INTERFACE WRITE TIMING (T_A = 25°C, VDD = 2.7V)

	Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
WRITE MODE	T_C	Enable Cycle Time	Pin SCL	5.0			us
	T_W	Enable Pulse Width	Pin SCL	2.5			us
	T_R,T_F	Enable Rise/Fall Time	Pin SCL			25	ns
	T_{SU1}	CSB Setup Time	Pin CSB	20			ns
	T_{H1}	CSB Hold Time	Pin CSB	100			us
	T_{SU2}	Rs Data Setup Time	Pin RS	40			ns
	T_{H2}	Rs Data Hold Time	Pin RS	40			ns
	T_{SU3}	SI Data Setup Time	Pin SI	40			ns
	T_{H3}	SI Data Hold Time	Pin SI	40			ns

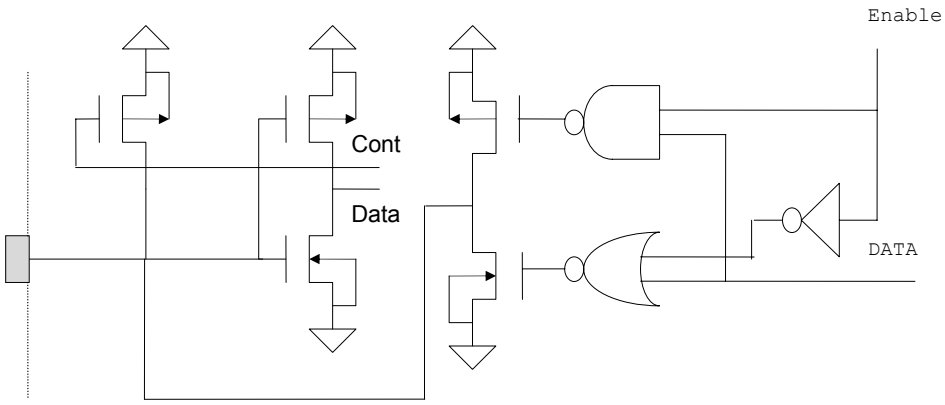
I/O PAD Configuration



Input PADs without pull up PMOS



Input PADs with pull up PMOS

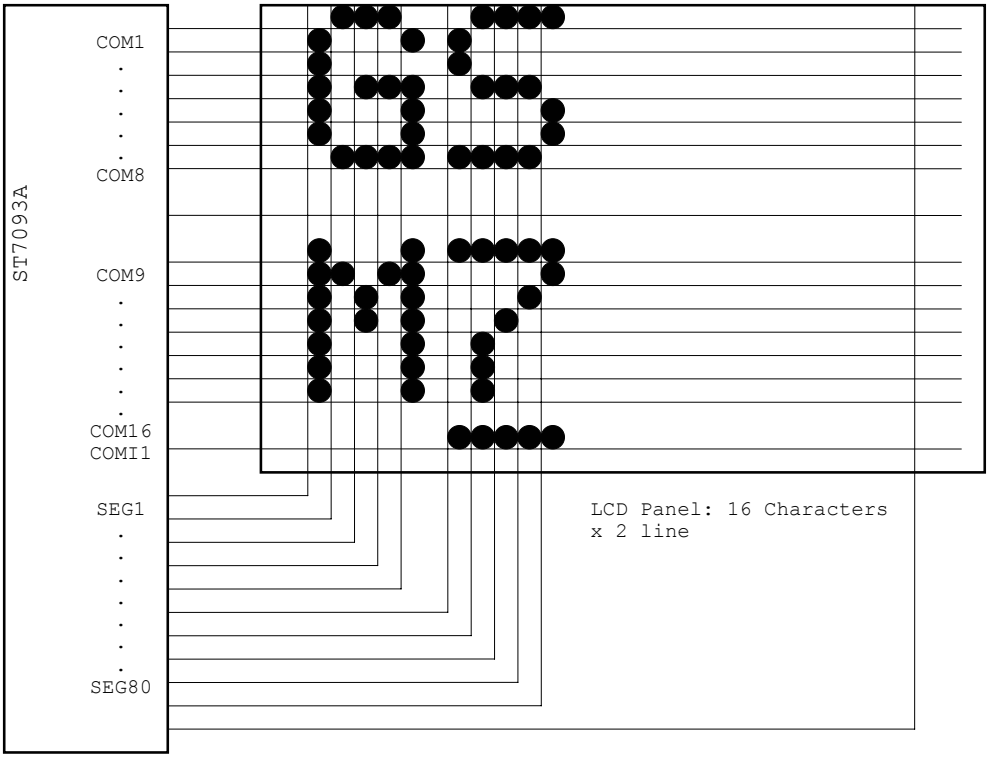


I/O PADs with pull up PMOS

When PS=1 all inputs and I/O pins are without PMOS pull up.
When PS=0 since only CSB, RS and DB6, DB7 is used for data transmission therefore RW_WR, E_RD and DB0~DB5 has internal pull up PMOS.
All system configuration pins such as CK,MI,PS,IF and DIRS are without pull up.

Typical application

5x8 dots, 16 characters x 2 line (1/5 bias, 1/17 duty)



ST7093 Specification Revision History		
Version	**Date**	**Description**
0.1A	2000/06/12	1. 17com*60segment (Original)
0.2A	2000/10/01	1. 26com*80segment
0.3	2001/01/08	1. Changed DC characteristics VLCD=V0-VSS 2. CGROM standard font 0B&C0A 3. Modify 3-Line mode double height instruction 4. Modify AC characteristics
0.3B	2001/03/12	1. Modify Booster 2.4Vx4 → 1.8Vx4 (page 27) 2. 2line17duty,3line25duty (Page 10) 3. COG Align Key Coordinate (page 4) 4.Reference Ra,Rb value (page 27,29) 5. Modify pin description CK , D0..D3 , TEST pin
0.4	2001/04/17	1. Modify AC characteristics
0.4b	2002/02/07	1. Add COB Pad Dimensions
1.0	2002/05/23	1. Modify double height mode instruction (P16 & P18) 2. Add illustration of electronic contrast control circuit (P30) 3. Add illustration of voltage regulator circuit (P29) 4. Add illustration of MPU interface (P32 & P33)
2.0	2002/08/29	1. Modify Operating Voltage 2.4V .. 3.6V
2.0b	2002/09/05	1. Modify CK pin must fixed “Vss” 2. CGROM standard font 0C
2.1	2003/09/23	1. Modify product number to ST7093