ST7272A

480x480 System-On-Chip Driver

for 320RGBx240 Dual Gate TFT LCD

Datasheet

Version 0.3
2018/01

Sitronix Technology Corporation

LIST OF CONTENT

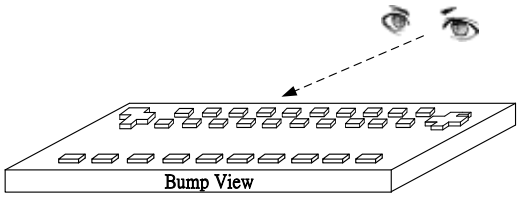
1. GENERAL DESCRIPTION

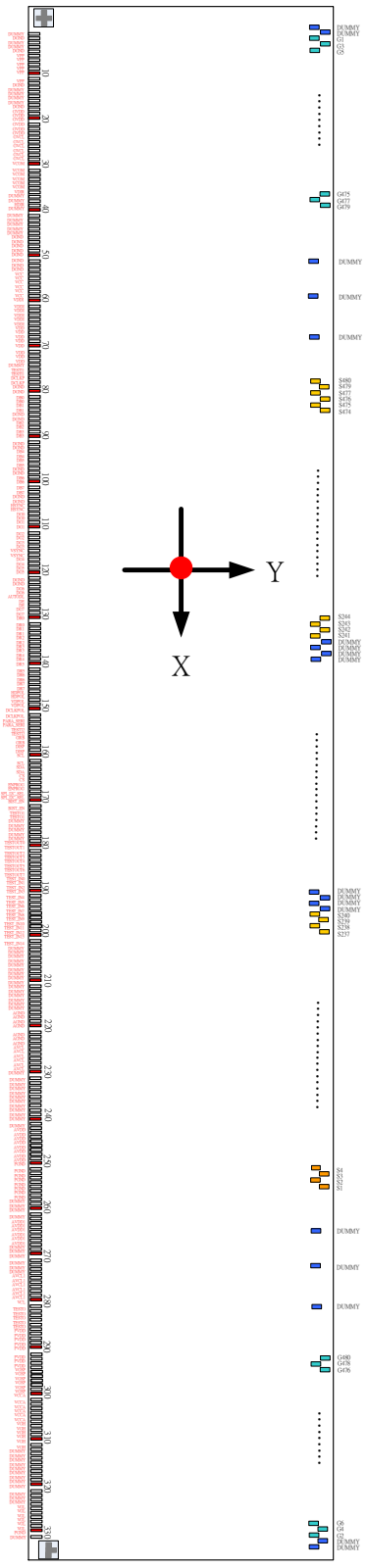
ST7272A offers all-in-one chip solution of 320RGBx240 for dual gate color TFT-LCD panel. The driver IC output ports consists of 480 source channels and 480 gate channels. This chip incorporated with digital timing generator, source and gate driver, power supply circuit and embedded serial communication interface for function setting. This chip can support parallel 24-bit RGB and serial 8-bit RGB interface. The source output support real 8-bit resolution and 256-gray scale with small output deviation are designed to support higher color resolution. The power supply circuit incorporated with step-up circuit, regulators and operational amplifiers to generate power supply voltages to drive TFT LCD.

2. FEATURES

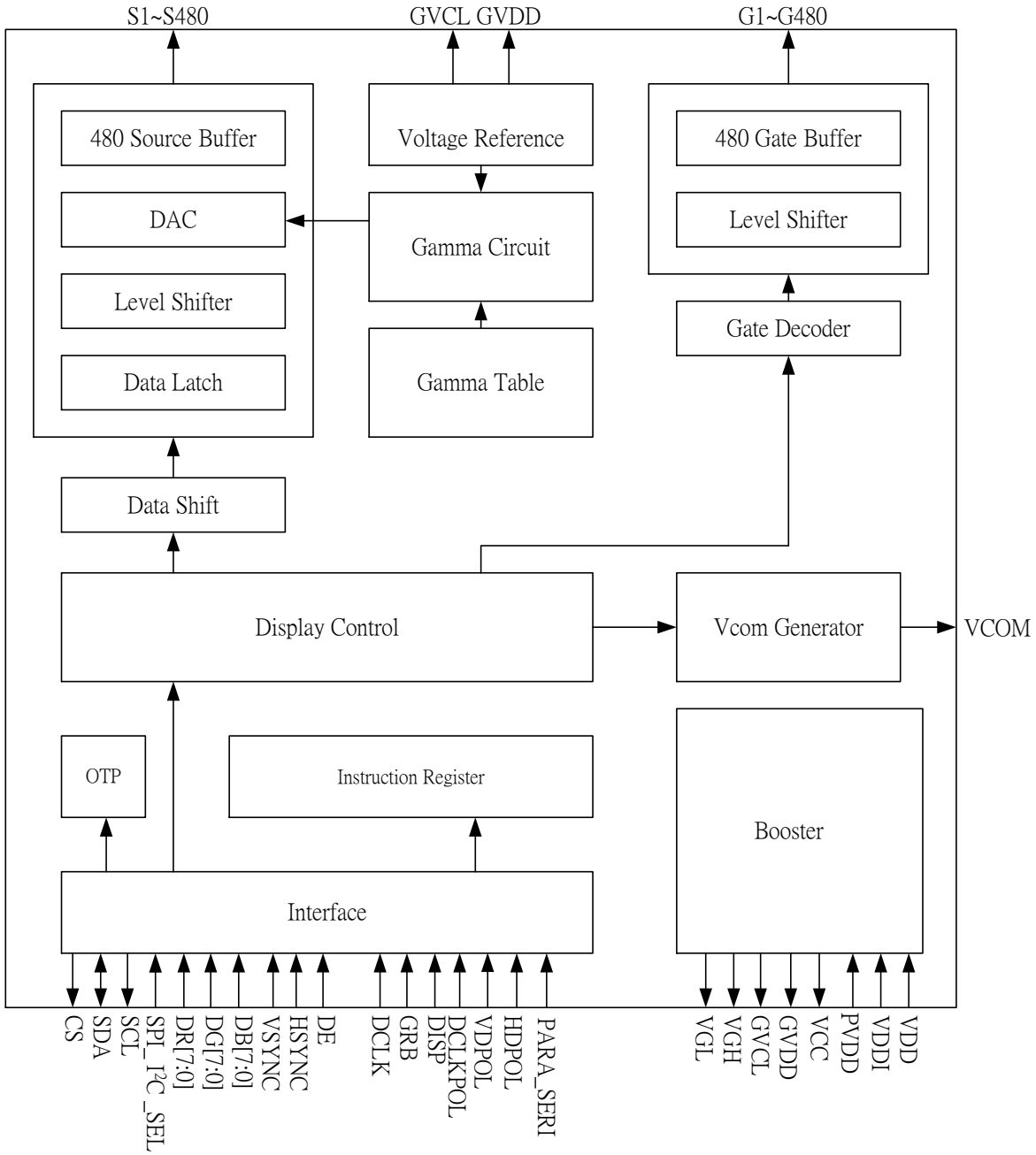
- Display Maximum Resolution:
  - support dual gate panel resolution: 320RGB * 240
- LCD Driver Output Circuits
  - source outputs: 480 channels
  - gate outputs: 480 channels
  - common electrode output
- 256 Gray Scale with True 8-bit DAC
- Microprocessor Interface
  - 8-bit and 24-bit RGB interface support: SYNC, SYNC-DE and DE mode
  - 3-wire SPI and I^2C interface
- On Chip Build-In Circuits
  - DC/DC converter
  - multi-OTP circuit (3 times)
  - timing controller
- Wide Supply Voltage Range
  - I/O voltage (VDDI to DGND): 3.0V ~ 3.6V
  - analog voltage (VDD to AGND): 3.0V ~ 3.6V
  - charge pump voltage (PVDD to PGND): 3.0V ~ 3.6V
- On-Chip Power System
  - GVDD: 4.960V ~ 5.968V
  - GVCL: -2.960V ~ -3.380V
  - VCOM: -0.24V ~ -1.504V (VCOM = (GVDD - |GVCL|) / 2, the VCOM voltage is set by panel characteristics)
  - gate high level (VGH to AGND): 13V ~ 16.5V
  - gate low level (VGL to AGND): -7V ~ -11V
- Optimized Layout for COG Assembly
- Built-in Multi-OTP Programming Circuit
  - internal VPP power supply
- Multi-OTP Adjustable Parameters
  - 7-bit for VCOM offset adjustment
  - 7-bit ID1/ ID2/ ID3 for end user use

3. PAD ARRANGEMENT





5. BLOCK DIAGRAM



6. PIN DESCRIPTION

6.1 Pin Function

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="3">3-Wire SPI / I²C Interface Pins</td></tr>
<tr><td>SPI_ I²C _SEL</td><td>I</td><td>3-wire SPI and I²C interface control.
<table>
<tr><th>SPI_ I²C _SEL</th><th>Function Description</th></tr>
<tr><td>L</td><td>I²C interface</td></tr>
<tr><td>H</td><td>3-wire SPI interface</td></tr>
</table></td></tr>
<tr><td>CS</td><td>I</td><td>Serial communication chip selection.
CS is not used in I²C interface and should be connected to “H”.</td></tr>
<tr><td>SDA</td><td>I/O</td><td>Serial communication data input and output.</td></tr>
<tr><td>SCL</td><td>I</td><td>Serial communication clock input.</td></tr>
<tr><td colspan="3">Control Pins</td></tr>
<tr><td>PARA_SERI</td><td>I</td><td>Set parallel or serial RGB interface.
<table>
<tr><th>PARA_SERI</th><th>Function Description</th></tr>
<tr><td>L</td><td>Serial 8 bit RGB interface</td></tr>
<tr><td>H</td><td>Parallel 24 bit RGB interface</td></tr>
</table></td></tr>
<tr><td>HDIR</td><td>I</td><td>Horizontal scan direction control pin. This pin must be connected to “H” or “L” according to system application.
<table>
<tr><th>HDIR</th><th>Function Description</th></tr>
<tr><td>L</td><td>From right to left</td></tr>
<tr><td>H</td><td>From left to right</td></tr>
</table></td></tr>
<tr><td>VDIR</td><td>I</td><td>Vertical scan direction control pin. This pin must be connected to “H” or “L” according to system application.
<table>
<tr><th>VDIR</th><th>Function Description</th></tr>
<tr><td>L</td><td>From down to up.</td></tr>
<tr><td>H</td><td>From up to down.</td></tr>
</table></td></tr>
<tr><td>VDPOL</td><td>I</td><td>VDPOL sets VSYNCC polarity in RGB interface.
<table>
<tr><th>DCLKPOL</th><th>Function Description</th></tr>
<tr><td>L</td><td>HSYNC polarity: positive</td></tr>
<tr><td>H</td><td>HSYNC polarity: negative</td></tr>
</table></td></tr>
<tr><td>HDPOL</td><td>I</td><td>HDPOL sets HSYNC polarity in RGB interface.
<table>
<tr><th>HDLKPOL</th><th>Function Description</th></tr>
<tr><td>L</td><td>HSYNC polarity: positive</td></tr>
<tr><td>H</td><td>HSYNC polarity: negative</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>DCLKPOL</td><td>I</td><td>VDPOL sets DCLK polarity in RGB interface.<table><tr><th>VDLKPOL</th><th>Function Description</th></tr><tr><td>L</td><td>VSYNC polarity: positive</td></tr><tr><td>H</td><td>YSNC polarity: negative</td></tr></table></td></tr>
<tr><td>GRB</td><td>I</td><td>Global reset pin. When GRB is “L”, internal initialization procedure is executed.</td></tr>
<tr><td>DISP</td><td>I</td><td>DISP sets the display mode.<table><tr><th>DISP</th><th>Function Description</th></tr><tr><td>L</td><td>Standby mode</td></tr><tr><td>H</td><td>Normal display mode</td></tr></table></td></tr>
<tr><td>AUTODL</td><td>I</td><td>OTP trim function control pin.<table><tr><th>AUTODL</th><th>Function Description</th></tr><tr><td>L</td><td>Disable auto-refresh function</td></tr><tr><td>H</td><td>Enable auto-refresh function</td></tr></table></td></tr>
<tr><td>ENPROG</td><td>I</td><td>OTP program control pin.<table><tr><th>ENPROG</th><th>Function Description</th></tr><tr><td>L</td><td>Disable OTP program function</td></tr><tr><td>H</td><td>Enable OTP program function</td></tr></table></td></tr>
<tr><td>BIST_EN</td><td>I</td><td>BIST function control pin.<table><tr><th>BIST_EN</th><th>Function Description</th></tr><tr><td>L</td><td>Disable BIST function</td></tr><tr><td>H</td><td>Enable BIST function</td></tr></table></td></tr>
<tr><td colspan="3">Input Interface Pins</td></tr>
<tr><td>DR[7:0]
DG[7:0]
DB[7:0]</td><td>I</td><td>RGB interface data input pins.<table><tr><th colspan="2">Function Description</th></tr><tr><td>DR[7:0]</td><td>8 bit data bus display red data. DR[7:0] are not used in 8-bit RGB interface and should be connected to “L” .</td></tr><tr><td>DG[7:0]</td><td>8 bit data bus display green data. DG[7:0] are used in 8-bit RGB interface.</td></tr><tr><td>DB[7:0]</td><td>8 bit data bus display blue data. DB[7:0] are not used in 8-bit RGB interface and should be connected to “L”.</td></tr></table></td></tr>
<tr><td>DCLK</td><td>I</td><td>Pixel clock input pin</td></tr>
<tr><td>HSYNC</td><td>I</td><td>Horizontal sync signal, default is negative polarity.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>Vertical sync signal, default is negative polarity.</td></tr>
<tr><td>DE</td><td>I</td><td>Data input enable. Display access is enabled when DE is “H”.</td></tr>
<tr><td colspan="3">Source / Gate Driver Pins</td></tr>
</table>

Name	Type	Description
S1~S480	O	Source driver output signals.
G1~G480	O	Gate driver output signals.
VCOM Generator Pin		
VCOM	O	Power supply for the TFT-LCD common electrode.
Power Supply Pins		
VDD	P	Power supply for analog circuit.
VDDI	P	Power supply for digital I/O pins.
PVDD	P	Power supply for charge pump circuit.
DGND	P	Ground pin for digital circuit.
AGND	P	Ground pin for analog circuit.
PGND	P	Ground pin for charge pump circuit.
Power Circuit Pins		
AVDD	C	DC/DC converter for positive source OP-AMP driver.
AVCL	C	DC/DC converter for negative source OP-AMP driver.
VGH	C	Positive power supply for gate driver.
VGL	C	Negative power supply for gate driver.
GVDD	PO	Positive voltage output of grayscale power.
GVCL	PO	Negative voltage output of grayscale power.
Test Pins		
VGSP	T	Monitor pin of internal VCOM offset.
VCC	T	Reserved for testing only, please leave those pins open
VCCA	T	Reserved for testing only, please leave those pins open
AVDD1	T	Reserved for testing only, please leave those pins open
AVCL1	T	Reserved for testing only, please leave those pins open
VPP	T	Reserved for testing only, please leave this pin open.
TEST_IN[14:0]	T	Reserved for testing only, please leave those pins open
TESTI[2:1]	T	Reserved for testing only, please leave those pins connect to “L”
TESTOUT[7:0]	T	Reserved for testing only, please leave those pins open.
TESTO[2:1]	T	Reserved for testing only, please leave it open.

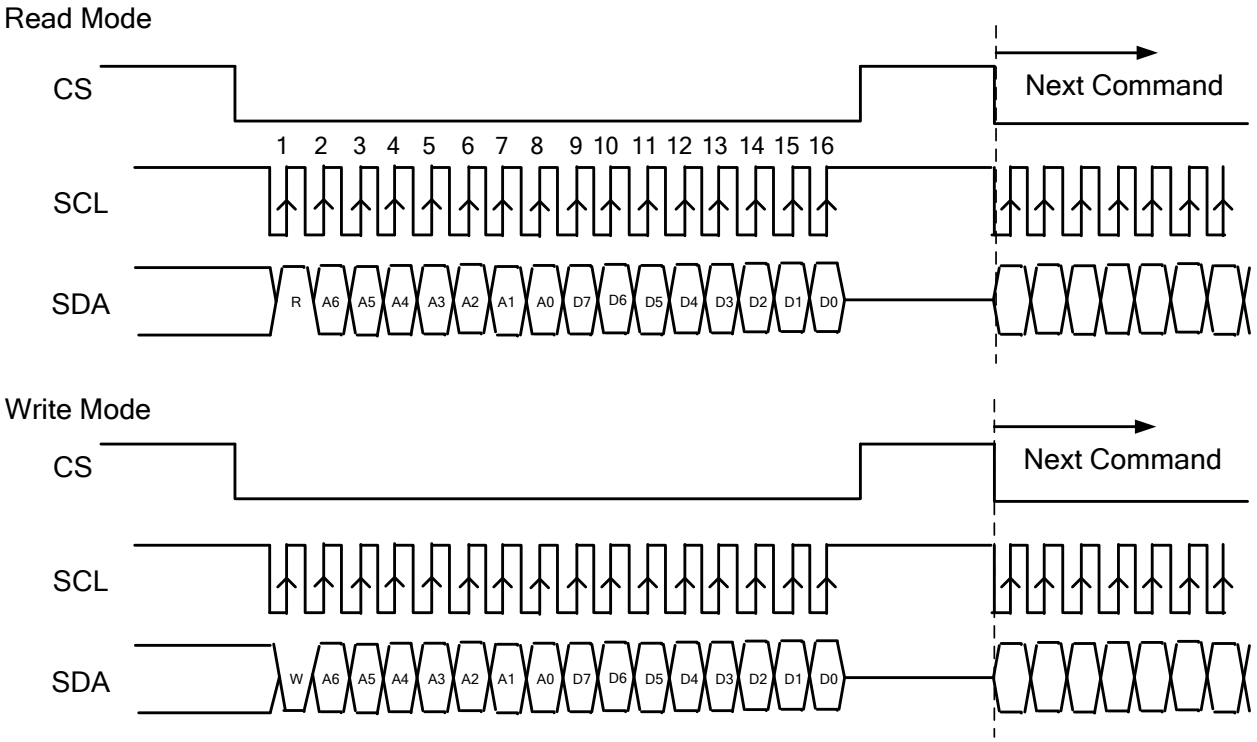
Note: 1. I: input, O: output, I/O: input/output, P: power input, PO: power out, D: dummy, T: test pin, C: capacitor pin

2. If hardware pin is not used, please fix to “H” by VDDI or “L” by DGND

7. COMMUNICATION INTERFACE

7.1 3-wire Serial Interface

R/W: Read/Write mode control bit.
R/W=1: Read mode
R/W=0: Write mode



a. Each serial command consists of 16 bits of data which is loaded one bit a time at the rising edge of serial clock SCL.

b. Command loading operation starts from the falling edge of CS and is completed at the next rising edge of CS.

c. The serial control block is operational after power on reset, but commands are established by the VSYNC signal. If command is transferred multiple times for the same register, the last command before the VSYNC signal is valid.

d. If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.

e. If 16 bits or more of SCL are input while CS is low, the previous 16 bits of transferred data before then rising edge of CS pulse are valid data.

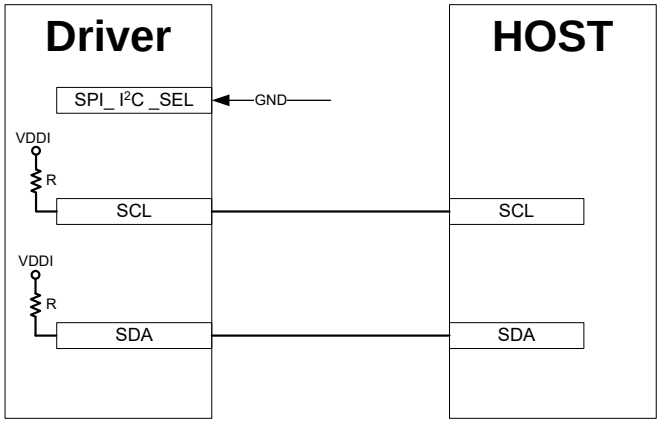
f. Serial block operates with the SCL clock

g. Serial data can be accepted in the power save mode.

h. After power on reset or GRB reset, it is required 100ms delay to begin SPI communication.

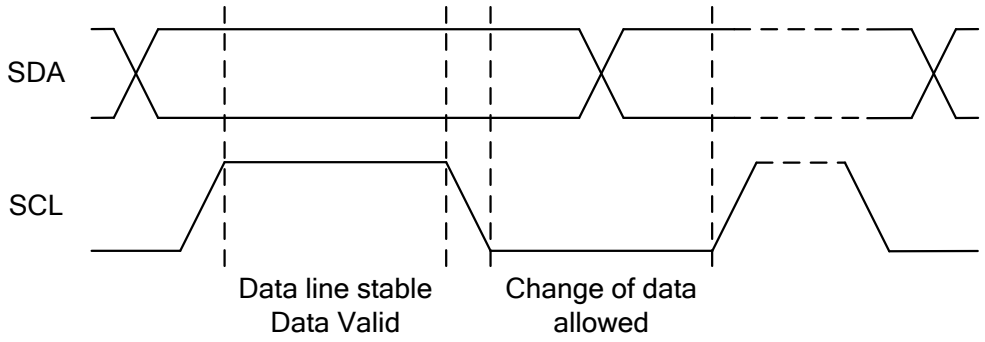
7.2 I²C Interface

The I²C Interface is bi-directional two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines have built-in pull up resistor which drives SDA and SCL to high when the bus is not busy. Data transfer can be initiated only when the bus is not busy.



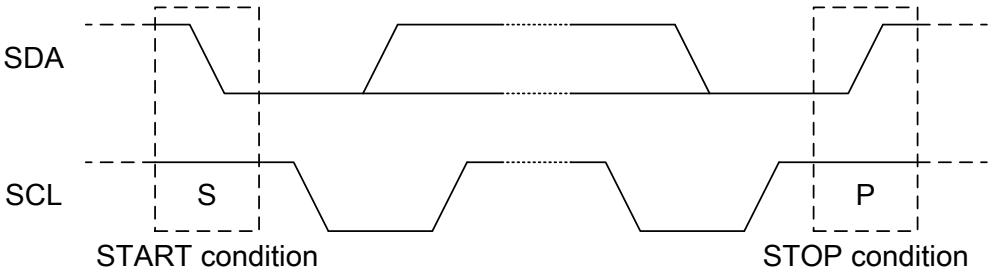
7.2.1 Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes of SDA line at this time will be interpreted as START or STOP. Bit transfer is illustrated as follows.

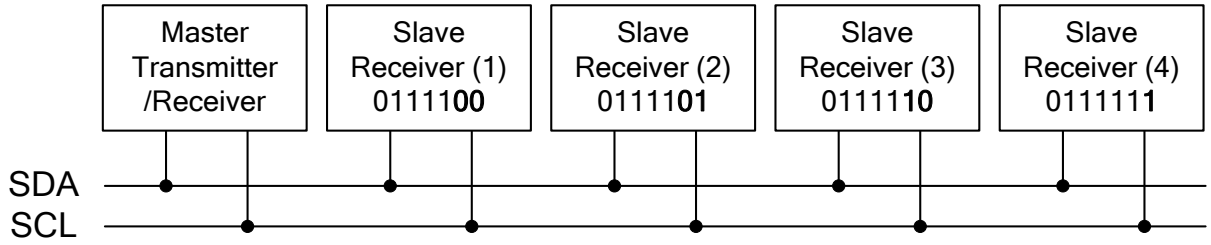


7.2.2 START and STOP Conditions

Both SDA and SCL lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of SDA, while SCL is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated as follows.



7.2.3 System Configuration



The system configuration is illustrated above and some word-definitions are explained below:

a. Transmitter: the device which sends the data to the bus.

b. Receiver: the device which receives the data from the bus.

c. Master: the device which initiates a transfer generates clock signals and terminates a transfer.

d. Slave: the device which is addressed by a master.

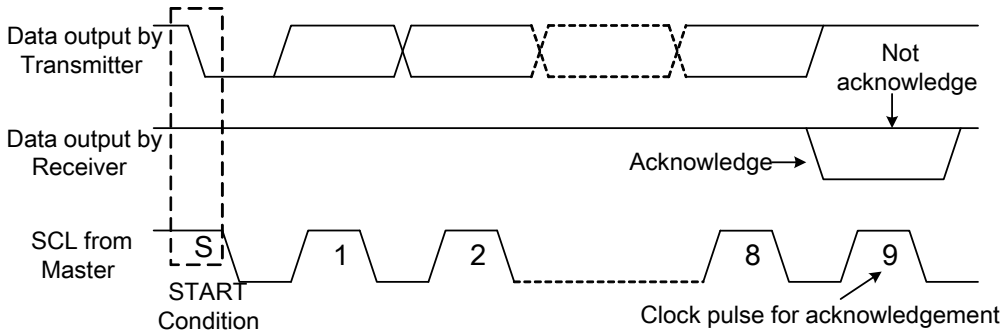
e. Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.

f. Arbitration: the procedure to ensure that, if more than one master tries to control the bus simultaneously, only one is allowed to do so and the message is not corrupted.

g. Synchronization: procedure to synchronize the clock signals of two or more devices.

7.2.4 Acknowledgment

Each byte of eight bits is followed by an acknowledge-bit. The acknowledge-bit is a HIGH signal put on SDA by the transmitter during the time when the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge-bit after the reception of each byte. A master receiver must also generate an acknowledge-bit after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge-clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge-bit on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I^2C Interface is illustrated as follows.



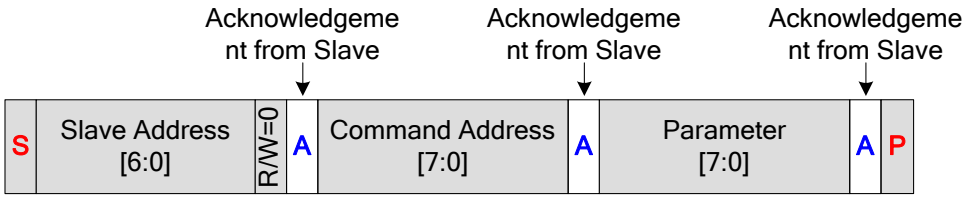
7.2.5 I²C Interface Protocol

The driver supports command/data write to addressed slaves on the bus. Before any data is transmitted on the I²C Interface, the device which should respond is addressed first. The default slave address is 0111100b and the three times I²C address could be OTP programing.

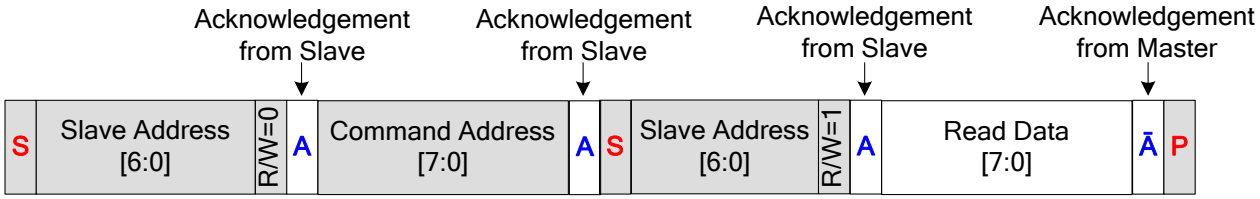
The sequence is initiated with a START condition (S) from the I²C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C Interface transfer. After acknowledgement, one or more command or data words are followed and define the status of the addressed slaves.

Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master. The register write/ read transference sequence are described as follows.

Write Mode (R/W="0")



Read Mode (R/W="1")



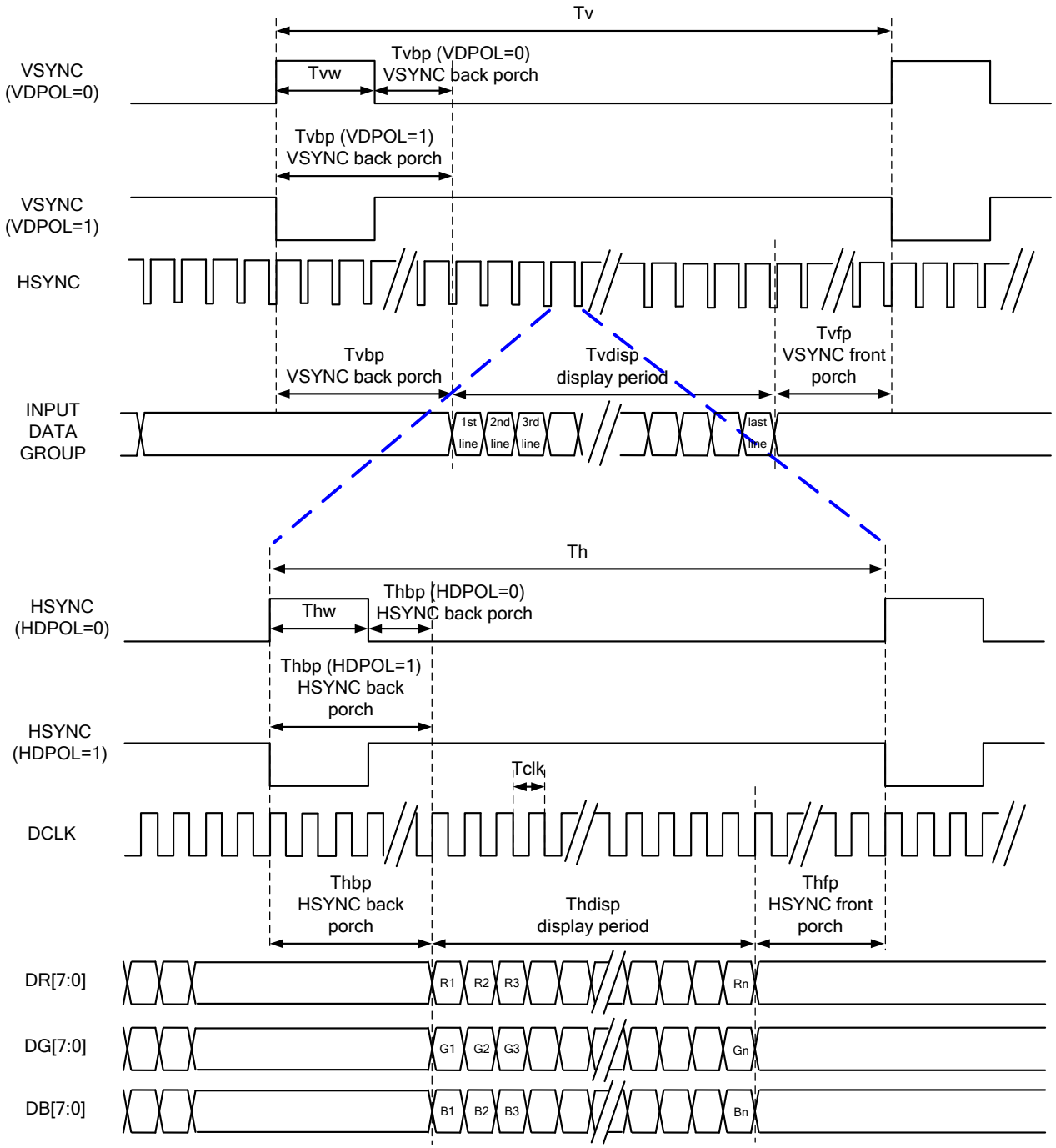
S: start condition
P: stop condition
A: acknowledge
Ā: no-acknowledge

master to slave

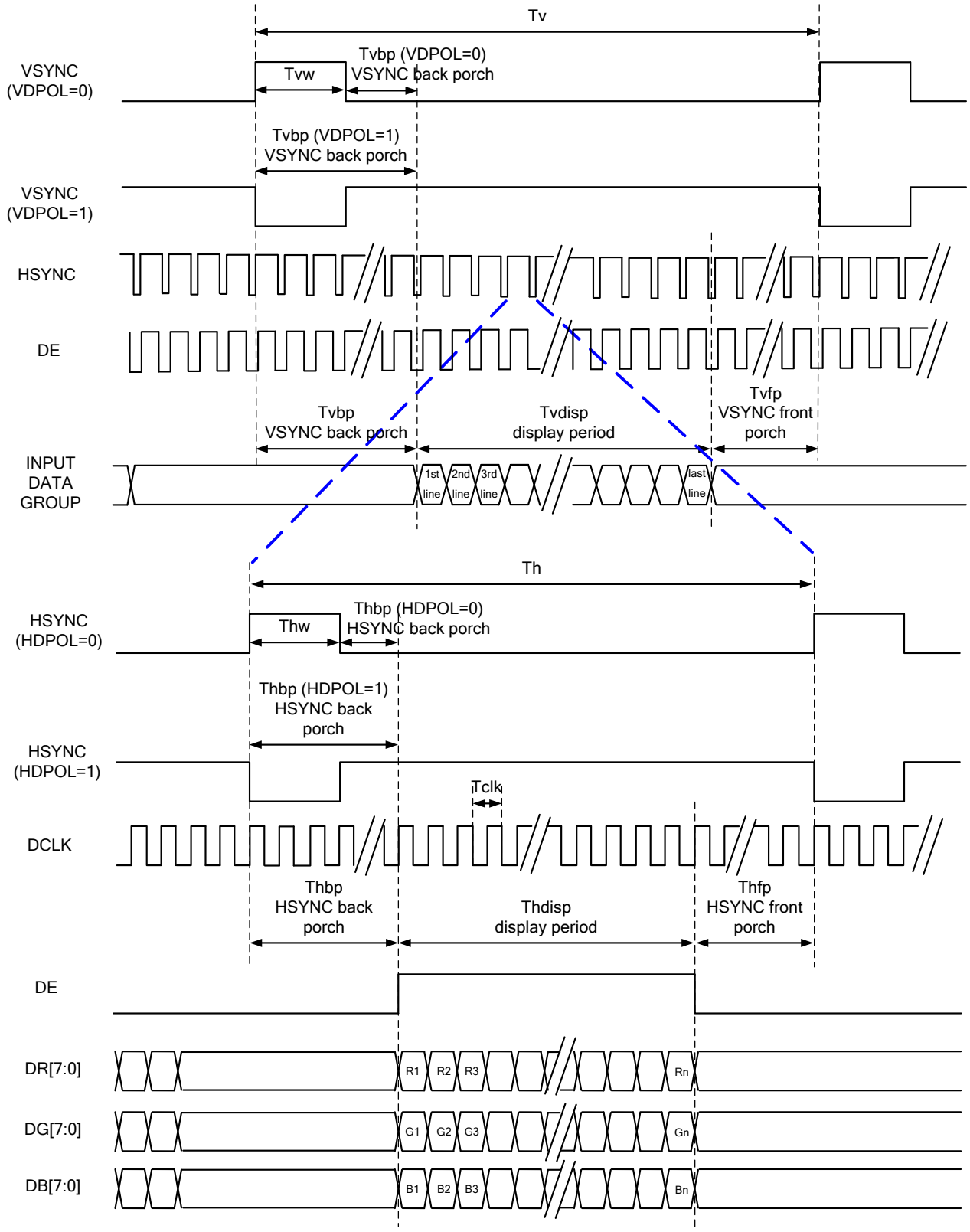
slave to master

7.3 RGB Interface

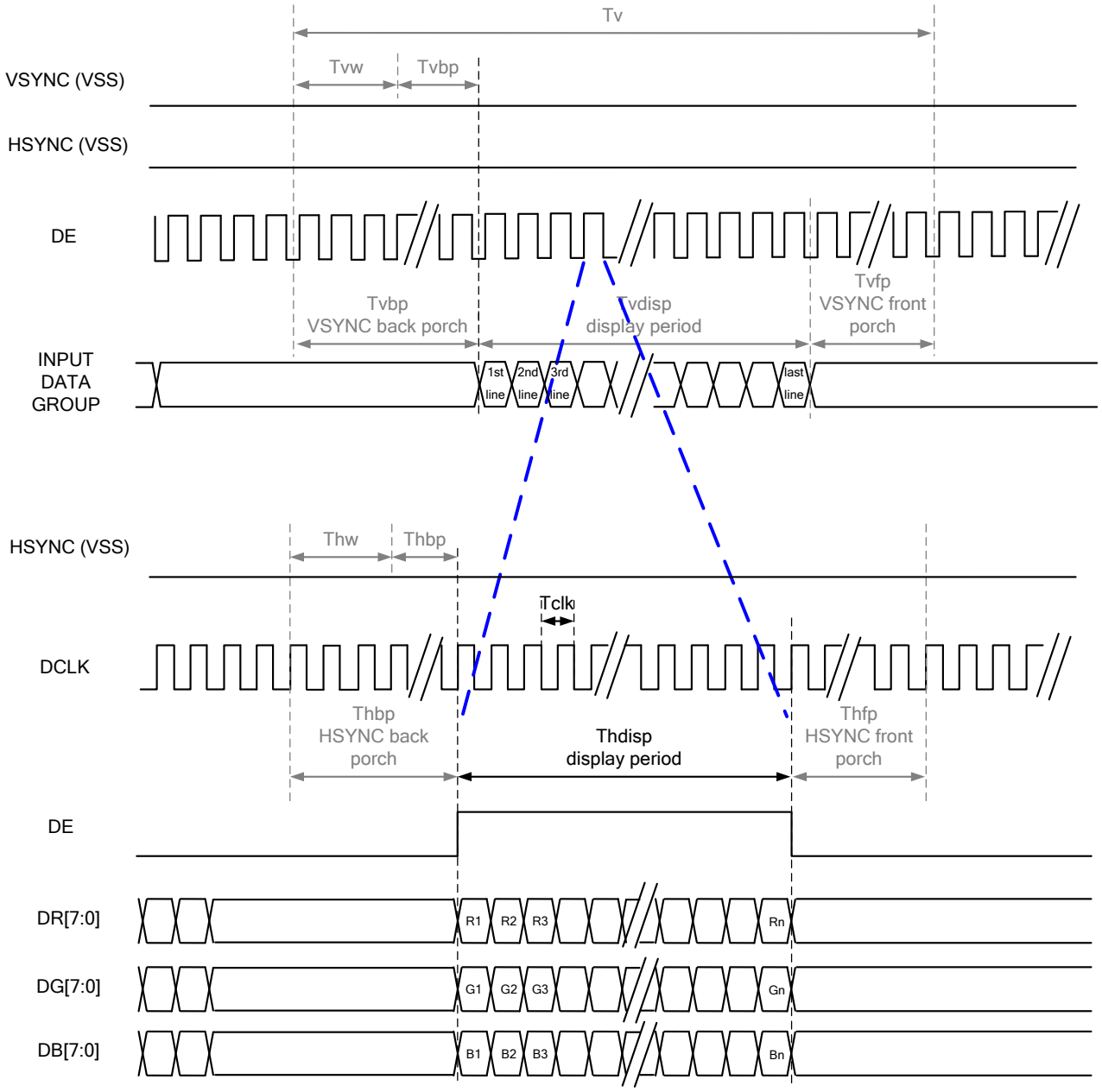
7.3.1 SYNC Mode



7.3.2 SYNC-DE Mode



7.3.3 DE Mode



RGB Mode Selection Table	DCLK	HSYNC	VSYNC	DE
SYNC - DE Mode	Input	Input	Input	Input
SYNC Mode	Input	Input	Input	GND
DE Mode	Input	GND	GND	Input

Note: "Input" means these signals are driven by host side.

7.3.4 Parallel 24-bit RGB Input Timing Table

Parallel 24-bit RGB Input Timing (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C)

Parallel 24-bit RGB Input Timing Table							
Item		**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Remark**
DCLK Frequency		Fclk	5	6	8	MHz	
DCLK Period		Tclk	125	167	200	ns	
HSYNC	Period Time	Th	325	371	438	DCLK	
	Display Period	Thdisp		320		DCLK	
	Back Porch	Thbp	3	43	43	DCLK	By H_BLANKING setting
	Front Porch	Thfp	2	8	75	DCLK	
	Pulse Width	Thw	2	4	43	DCLK	
VSYNC	Period Time	Tv	244	260	289	HSYNC	
	Display Period	Tvdisp		240		HSYNC	
	Back Porch	Tvbp	2	12	12	HSYNC	By V_BLANKING setting
	Front Porch	Tvfp	2	8	37	HSYNC	
	Pulse Width	Tvw	2	4	12	HSYNC	

Note: It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.

7.3.5 Serial 8-bit RGB Input Timing Table

Serial 8-bit RGB Input Timing (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C)

Serial 8-bit RGB Input Timing Table							
Item		**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Remark**
DCLK Frequency		Fclk	15	18	21	MHz	
DCLK Period		Tclk	47	55	66	ns	
HSYNC	Period Time	Th	965	1011	1078	DCLK	
	Display Period	Thdisp		960		DCLK	
	Back Porch	Thbp	3	43	43	DCLK	By H_BLANKING setting
	Front Porch	Thfp	2	8	75	DCLK	
	Pulse Width	Thw	2	4	43	DCLK	
VSYNC	Period Time	Tv	244	260	289	HSYNC	
	Display Period	Tvdisp		240		HSYNC	
	Back Porch	Tvbp	2	12	12	HSYNC	By V_BLANKING setting
	Front Porch	Tvfp	2	8	37	HSYNC	
	Pulse Width	Tvw	2	4	12	HSYNC	

Note: It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.

E mode is unnecessary to keep it.

8. REGISTER LIST

8.1 Register Summary

COMMAND TABLE 1									
Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
10h	0	0	0	0	GRB	0	0	DISP	08h
11h	CONTRAST[7:0]								40h
12h	0	SUB_CONTRAST_R[6:0]							40h
13h	0	SUB_CONTRAST_B[6:0]							40h
14h	BRIGHTNESS[7:0]								40h
15h	0	SUB_BRIGHTNESS_R[6:0]							40h
16h	0	SUB_BRIGHTNESS_B[6:0]							40h
17h	H_BLANKING[7:0]								2Bh
18h	V_BLANKING[7:0]								0Ch
19h	MVA_TN	VDIR	HDIR	SBGR	VDPOL	HDPOL	DEPOL	DCLKPOL	6Dh
1Ah	1	1	1	1	0	RGBSWAP	RGBMODE[1:0]		F7h
1Bh	0	0	0	0	1	AUTODL	0	0	0Ch
1Ch	0	0	PICSEC[1:0]		AUTOBIST	PICSEL [2:0]			38h
COMMAND TABLE 2									
Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
40h	0	1	VRHP[5:0]						--
41h	0	VRHN[6:0]							--
44h	0	1	MODE[1:0]		AVCLS[1:0]		AVDDS[1:0]		--
45h	0	0	0	0	VGLSEL[1:0]		VGHSEL[1:0]		--
46h	T4T[1:0]		T3T[1:0]		T2T[1:0]		T1T[1:0]		--
47h	0	0	0	0	0	SOURCE_AP[2:0]			--
49h	0	NO[2:0]			0	Reserved[2:0]			--
4Ah	0	PRGB_GWIDTH[2:0]			0	SRGB_GWIDTH[2:0]			--

Note:

1. When GRB is "Low", all registers reset to default values.

2. Symbol "--" means this value is OTP setting according to parameters of system application, panel loading and display quality.

3. Do not use instructions not listed in these tables.

GAMMA COMMAND TABLE									
Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
20h	0	0	0	VRF0P[4:0]					--
21h	0	0	0	VOS0P[4:0]					--
22h	PFP0[2:0]			PKP0[4:0]					--
23h	PFP1[2:0]			PKP1[4:0]					--
24h	PFP2[2:0]			PKP2[4:0]					--
25h	PFP3[2:0]			PKP3[4:0]					--
26h	PFP4[2:0]			PKP4[4:0]					--
27h	PFP5[2:0]			PKP5[4:0]					--
28h	PFP6[2:0]			PKP6[4:0]					--
29h	0	0	0	PKP7[4:0]					--
30h	0	0	0	VRF0N[4:0]					--
31h	0	0	0	VOS0N[4:0]					--
32h	PFN0[2:0]			PKN0[4:0]					--
33h	PFN1[2:0]			PKN1[4:0]					--
34h	PFN2[2:0]			PKN2[4:0]					--
35h	PFN3[2:0]			PKN3[4:0]					--
36h	PFN4[2:0]			PKN4[4:0]					--
37h	PFN5[2:0]			PKN5[4:0]					--
38h	PFN6[2:0]			PKN6[4:0]					--
39h	0	0	0	PKN7[4:0]					--

Note:

1. When GRB is “Low”, all registers reset to default values.

2. Symbol “--” means this value is OTP setting according to parameters of system application, panel loading and display quality.

3. Do not use instructions not listed in these tables.

OTP COMMAND TABLE									
Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
01h	0	ID1[6:0]							7Fh
02h	0	ID2[6:0]							7Fh
03h	0	ID3[6:0]							7Fh
04h	0	I^2CID[6:0]							78h
05h	0	VMF[6:0]							40h
60h	0	1	0	0	0	INTVPP	OTPEN	0	00h
65h	OTPACK[7:0]								00h
66h	0	0	0	0	0	VMF OTP TIME[2:0]			03h
67h	0	0	0	0	0	CMD2 OTP TIME[2:0]			03h
68h	0	0	0	0	0	GAMMA OTP TIME[2:0]			03h
69h	0	0	0	0	0	ID1 OTP TIME[2:0]			03h
6Ah	0	0	0	0	0	ID2 OTP TIME[2:0]			03h
6Bh	0	0	0	0	0	ID3 OTP TIME[2:0]			03h
6Ch	0	0	0	0	0	I^2CID OTP TIME[2:0]			03h

Note:

1. When GRB is "Low", all registers reset to default values.

2. Symbol "--" means this value is OTP setting according to parameters of system application, panel loading and display quality.

3. Do not use instructions not listed in these tables.

8.2 Command Table1 Register Description

8.2.1 GRB、DISP CONTROL (10h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
10h	R/W	0	0	0	0	GRB	0	0	DISP	08h

Designation	Description
GRB	Reset register setting GRB=0: reset all registers to default value GRB=1: normal operation
DISP	Standby (power saving) mode setting DISP=0: standby mode DISP=1: normal mode

8.2.2 CONTRAST (11h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
11h	R/W	CONTRAST[7:0]								40h

Designation	Description
CONTRAST[7:0]	Set RGB contrast level, the range of gain is 0~3.984 CONTRAST=00h: contrast gain=0 CONTRAST=40h: contrast gain=1 CONTRAST=FFh: contrast gain=3.984

8.2.3 SUB_CONTRAST_R (12h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
12h	R/W	0	SUB_CONTRAST_R[6:0]							40h

Designation	Description
SUB_CONTRAST_R[6:0]	Set red color sub-contrast level, the range of gain is 0.75~1.246 SUB_CONTRAST_R=00h: contrast gain=0.75 SUB_CONTRAST_R=40h: contrast gain=1 SUB_CONTRAST_R=7Fh: contrast gain=1.246

8.2.4 SUB_CONTRAST_B (13h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
13h	R/W	0	SUB_CONTRAST_B[6:0]							40h

Designation	Description
SUB_CONTRAST_B[6:0]	Set blue color sub-contrast level, the range of gain is 0.75~1.246 SUB_CONTRAST_B=00h: contrast gain=0.75 SUB_CONTRAST_B=40h: contrast gain=1 SUB_CONTRAST_B=7Fh: contrast gain=1.246

8.2.5 BRIGHTNESS (14h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
14h	R/W	BRIGHTNESS[7:0]								40h

Designation	Description
BRIGHTNESS[7:0]	Set RGB brightness level, the range of brightness is -64~+191 BRIGHTNESS=00h: -64 BRIGHTNESS=40h: 0 BRIGHTNESS=FFh: +191

8.2.6 SUB-BRIGHTNESS_R (15h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
15h	R/W	0	SUB_BRIGHTNESS_R[6:0]							40h

Designation	Description
SUB_BRIGHTNESS_R [6:0]	Set red color sub-brightness level, the range of brightness is -64~+63 SUB_BRIGHTNESS_R=00h: -64 SUB_BRIGHTNESS_R=40h: 0 SUB_BRIGHTNESS_R=7Fh: +63

8.2.7 SUB-BRIGHTNESS_B (16h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
16h	R/W	0	SUB_BRIGHTNESS_B[6:0]							40h

Designation	Description
SUB_BRIGHTNESS_B [6:0]	Set blue color sub-brightness level, the range of brightness is -64~+63 SUB_BRIGHTNESS_B=00h: -64 SUB_BRIGHTNESS_B=40h: 0 SUB_BRIGHTNESS_B=7Fh: +63

8.2.8 H_BLANKING (17h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
17h	R/W	H_BLANKING[7:0]								2Bh

Designation	Description
H_BLANKING[7:0]	The HSYNC back porch setting of RGB interface

8.2.9 V_BLANKING (18h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
18h	R/W	V_BLANKING[7:0]								0Ch

Designation	Description
V_BLANKING[7:0]	The VSYNC back porch setting of RGB interface

8.2.10 DISPLAY MODE SETTING (19h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
19h	R/W	MVA_TN	VDIR	HDIR	SBGR	VDPOL	HDPOL	DEPOL	DCLKPOL	6Dh

Designation	Description
MVA_TN	MVA_TN=0: TN mode for panel display. MVA_TN=1: VA mode for panel display.
VDIR	Vertical scan direction setting VDIR= 0: from bottom to top, L544(first line) → L543 →…→ L2 → L1(last line) VDIR= 1: from top to bottom, L1(first line) → L2 →…→ L543 → L544(last line)
HDIR	Horizontal scan direction setting HDIR= 0: from right to left, Y720(first data) → Y719 →…→ Y2 → Y1(last data) HDIR= 1: from left to right, Y1(first data) → Y2 →…→ Y719 → Y720(last data)
SBGR	Data of red and blue exchange SBGR= 0: normal, DR[7:0]→DR[7:0] and DB[7:0]→DB[7:0] SBGR= 1: exchange, DR[7:0]→DB[7:0] and DB[7:0]→DR[7:0]
VDPOL	VSYNC polarity setting VDPOL= 0: positive polarity VDPOL= 1: negative polarity
HDPOL	HSYNC polarity setting HDPOL= 0: positive polarity HDPOL= 1: negative polarity
DEPOL	DE polarity setting DEPOL= 0: positive polarity DEPOL= 1: negative polarity
DCLKPOL	DCLK polarity setting DCLKPOL= 0: positive Polarity DCLKPOL= 1: negative Polarity

8.2.11 RGB INTERFACE MODE SETTING (1Ah)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ah	R/W	1	1	1	1	0	RGBSWAP	RGBMODE[1:0]		F7h

<table>
<tr><th>Designation</th><th>Description</th></tr>
<tr><td>RGBSWAP</td><td>Set data format sequence of RGB interface
<table>
<tr><th>Pin Name</th><th>Internal Data</th><th>RGBSWAP=0</th><th>RGBSWAP=1</th></tr>
<tr><td>DR0</td><td>r0’</td><td>r0’</td><td>r7’</td></tr>
<tr><td>DR1</td><td>r1’</td><td>r1’</td><td>r6’</td></tr>
<tr><td>DR2</td><td>r2’</td><td>r2’</td><td>r5’</td></tr>
<tr><td>DR3</td><td>r3’</td><td>r3’</td><td>r4’</td></tr>
<tr><td>DR4</td><td>r4’</td><td>r4’</td><td>r3’</td></tr>
<tr><td>DR5</td><td>r5’</td><td>r5’</td><td>r2’</td></tr>
<tr><td>DR6</td><td>r6’</td><td>r6’</td><td>r1’</td></tr>
<tr><td>DR7</td><td>r7’</td><td>r7’</td><td>r0’</td></tr>
<tr><td>DG0</td><td>g0’</td><td>g0’</td><td>g7’</td></tr>
<tr><td>DG1</td><td>g1’</td><td>g1’</td><td>g6’</td></tr>
<tr><td>DG2</td><td>g2’</td><td>g2’</td><td>g5’</td></tr>
<tr><td>DG3</td><td>g3’</td><td>g3’</td><td>g4’</td></tr>
<tr><td>DG4</td><td>g4’</td><td>g4’</td><td>g3’</td></tr>
<tr><td>DG5</td><td>g5’</td><td>g5’</td><td>g2’</td></tr>
<tr><td>DG6</td><td>g6’</td><td>g6’</td><td>g1’</td></tr>
<tr><td>DG7</td><td>g7’</td><td>g7’</td><td>g0’</td></tr>
<tr><td>DB0</td><td>b0’</td><td>b0’</td><td>b7’</td></tr>
<tr><td>DB1</td><td>b1’</td><td>b1’</td><td>b6’</td></tr>
<tr><td>DB2</td><td>b2’</td><td>b2’</td><td>b5’</td></tr>
<tr><td>DB3</td><td>b3’</td><td>b3’</td><td>b4</td></tr>
<tr><td>DB4</td><td>b4’</td><td>b4’</td><td>b3’</td></tr>
<tr><td>DB5</td><td>b5’</td><td>b5’</td><td>b2’</td></tr>
<tr><td>DB6</td><td>b6’</td><td>b6’</td><td>b1’</td></tr>
<tr><td>DB7</td><td>b7’</td><td>b7’</td><td>b0’</td></tr>
</table></td></tr>
<tr><td>RGBMODE[1:0]</td><td>Set color format of RGB interface
<table>
<tr><th>RGBMODE [1:0]</th><th>Color Format</th></tr>
<tr><td>00</td><td>256-gray mono display</td></tr>
<tr><td>01</td><td>64K</td></tr>
<tr><td>10</td><td>262K</td></tr>
<tr><td>11</td><td>16.7M</td></tr>
</table></td></tr>
</table>

8.2.12 ERROR REPORT AND OTP AUTO DOWNLOAD CONTROL (1Bh)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Bh	R/W	0	0	0	0	1	AUTODL	0	0	0Ch

Designation	Description
AUTODL	Multi-OTP auto-refresh function control AUTODL= 0: disable auto-refresh function AUTODL= 1: enable auto-refresh function

8.2.13 BIST FUNCTION SETTING (1Ch)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ch	R/W	0	0	PICSEC[1:0]		AUTOBIST	PICSEL[2:0]			38h

Designation	Description
PICSEC[1:0]	The time interval of test pattern in the BIST mode PICSEC[1:0] / Time(sec): 00 / 0.5; 01 / 1; 10 / 1.5; 11 / 2
AUTOBIST	Auto display pattern control in the BIST mode AUTOBIST=0: Disable auto display mode AUTOBIST=1: Enable auto display mode
PICSEL[2:0]	BIST pattern selection PICSEL [2:0] / Display Pattern: 000 / Black; 001 / White; 010 / Red; 011 / Green; 100 / Blue; 101 / Black; 110 / Black; 111 / Black

8.3 Command Table2 Register Description

8.3.1 GVDD SETTING (40h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
40h	R/W	0	1	VRHP[5:0]						--

Designation	Description
VRHP[5:0]	GVDD level setting

VRHP[5:0]	GVDD	VRHP[5:0]	GVDD	VRHP[5:0]	GVDD	VRHP[5:0]	GVDD
000000	5.9680	010000	5.7120	100000	5.4560	110000	5.2000
000001	5.9520	010001	5.6960	100001	5.4400	110001	5.1840
000010	5.9360	010010	5.6800	100010	5.4240	110010	5.1680
000011	5.9200	010011	5.6640	100011	5.4080	110011	5.1520
000100	5.9040	010100	5.6480	100100	5.3920	110100	5.1360
000101	5.8880	010101	5.6320	100101	5.3760	110101	5.1200
000110	5.8720	010110	5.6160	100110	5.3600	110110	5.1040
000111	5.8560	010111	5.6000	100111	5.3440	110111	5.0880
001000	5.8400	011000	5.5840	101000	5.3280	111000	5.0720
001001	5.8240	011001	5.5680	101001	5.3120	111001	5.0560
001010	5.8080	011010	5.5520	101010	5.2960	111010	5.0400
001011	5.7920	011011	5.5360	101011	5.2800	111011	5.0240
001100	5.7760	011100	5.5200	101100	5.2640	111100	5.0080
001101	5.7600	011101	5.5040	101101	5.2480	111101	4.9920
001110	5.7440	011110	5.4880	101110	5.2320	111110	4.9760
001111	5.7280	011111	5.4720	101111	5.2160	111111	4.9600

8.3.2 GVCL SETTING (41h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
41h	R/W	0	VRHN[6:0]							--

Designation	Description
VRHN[6:0]	GVCL level setting

VRHN[6:0]	GVCL	VRHN[6:0]	GVCL	VRHN[6:0]	GVCL	VRHN[6:0]	GVCL
0100000	-4.4800	0111000	-4.0960	1010000	-3.7120	1101000	-3.3280
0100001	-4.4640	0111001	-4.0800	1010001	-3.6960	1101001	-3.3120
0100010	-4.448	0111010	-4.0640	1010010	-3.6800	1101010	-3.2960
0100011	-4.4320	0111011	-4.0480	1010011	-3.6640	1101011	-3.2800
0100100	-4.4160	0111100	-4.0320	1010100	-3.6480	1101100	-3.2640
0100101	-4.4000	0111101	-4.0160	1010101	-3.6320	1101101	-3.2480
0100110	-4.3840	0111110	-4.0000	1010110	-3.6160	1101110	-3.2320
0100111	-4.3680	0111111	-3.9840	1010111	-3.6000	1101111	-3.2160
0101000	-4.3520	1000000	-3.9680	1011000	-3.5840	1110000	-3.2000
0101001	-4.3360	1000001	-3.9520	1011001	-3.5680	1110001	-3.1840
0101010	-4.3200	1000010	-3.9360	1011010	-3.5520	1110010	-3.1680
0101011	-4.3040	1000011	-3.9200	1011011	-3.5360	1110011	-3.1520
0101100	-4.2880	1000100	-3.9040	1011100	-3.5200	1110100	-3.1360
0101101	-4.2720	1000101	-3.8880	1011101	-3.5040	1110101	-3.1200
0101110	-4.2560	1000110	-3.8720	1011110	-3.4880	1110110	-3.1040
0101111	-4.2400	1000111	-3.8560	1011111	-3.4720	1110111	-3.0880
0110000	-4.2240	1001000	-3.8400	1100000	-3.4560	1111000	-3.0720
0110001	-4.2080	1001001	-3.8240	1100001	-3.4400	1111001	-3.0560
0110010	-4.1920	1001010	-3.8080	1100010	-3.4240	1111010	-3.0400
0110011	-4.1760	1001011	-3.7920	1100011	-3.4080	1111011	-3.0240
0110100	-4.1600	1001100	-3.7760	1100100	-3.3920	1111100	-3.0080
0110101	-4.1440	1001101	-3.7600	1100101	-3.3760	1111101	-2.9920
0110110	-4.1280	1001110	-3.7440	1100110	-3.3600	1111110	-2.9760
0110111	-4.1120	1001111	-3.7280	1100111	-3.3440	1111111	-2.9600

8.3.3 AVDD, AVCL SETTING (44h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
44h	R/W	0	1	MODE[1:0]		AVCLS[1:0]		AVDDS[1:0]		--

Designation	Description
MODE[1:0]	AVDD booster mode setting MODE[1:0] / AVDD Booster Setting 00 / booster: x3 01 / booster: x2 10 / booster auto-detect, reference voltage: VDD:3.0V 11 / booster auto-detect, reference voltage: VDD:3.1V
AVCLS[1:0]	AVCL level setting AVCLS[1:0] / AVCL (V) 00 / -4.2 01 / -4.6 10 / Reserved 11 / Reserved
AVDDS[1:0]	AVDD level setting AVDDS[1:0] / AVDD (V) 00 / 6.2 01 / 6.4 10 / Reserved 11 / Reserved

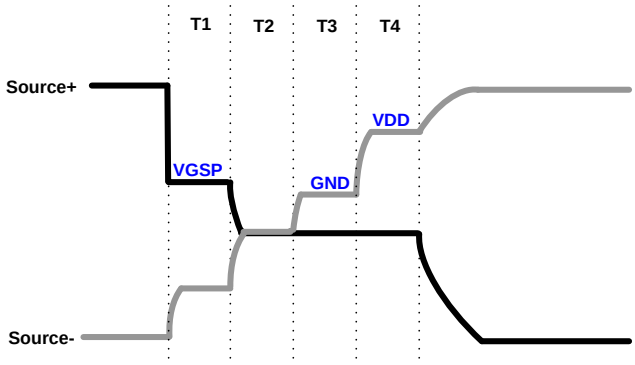
8.3.4 VGH, VGL SETTING (45h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
45h	R/W	0	0	0	0	VGLSEL[1:0]		VGHSEL[1:0]		--

Designation	Description
VGLSEL[1:0]	VGL level setting VGLSEL[1:0] / VGL (V) 00 / -7 01 / -8 10 / -10 11 / -11
VGHSEL[1:0]	VGH level setting VGHSEL[1:0] / VGH (V) 00 / 13 01 / 15 10 / 16 11 / 16.5

8.3.5 SOURCE EQUALIZE TIME SETTING (46h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
46h	R/W	T4T[1:0]		T3T[1:0]		T2T[1:0]		T1T[1:0]		--

Designation	Description
T4T[1:0] T3T[1:0] T2T[1:0] T1T[1:0]	

Source equalizing T4 timing setting

T4T[1:0]	T4 (DCLK)
00	4
01	8
10	17
11	26

Source equalizing T3 timing setting

T3T[1:0]	T3 (DCLK)
00	0.5
01	8
10	17
11	26

Source equalizing T2 timing setting

T2T[1:0]	T2 (DCLK)
00	0.5
01	8
10	17
11	26

Source equalizing T1 timing setting

T1T[1:0]	T1 (DCLK)
00	OFF
01	8
10	17
11	26

Note: The above source equalize timing table is only for 480RGB X 272 resolution application.

8.3.6 SOURCE OP-AMP POWER SETTING (47h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
47h	R/W	0	0	0	0	0	SOURCE_AP[2:0]			--

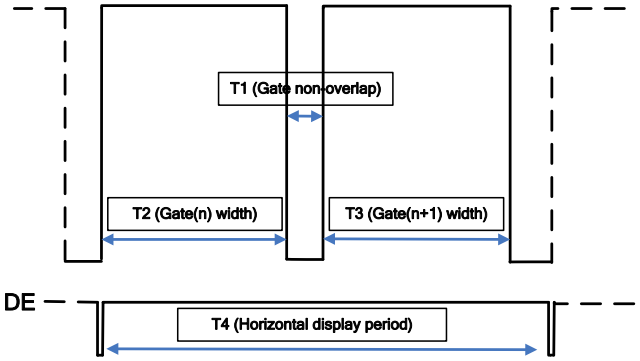
Designation	Description
SOURCE_AP[2:0]	Source driving ability setting. When value is higher, the source output current will increase.

SOURCE_AP[2:0]	Source Power
000	Level 1 (lowest)
001	Level 2 (minimal)
010	Level 3 (minimal to medium)
011	Level 4 (medium)
100	Level 5 (medium to large)
101	Level 6 (large)
110	Level 7 (large to highest)
111	Level 8 (highest)

Note: The setting value needs to be adjusted according to the display performance.

8.3.7 GATE TIMING SETTING 1 (49h)

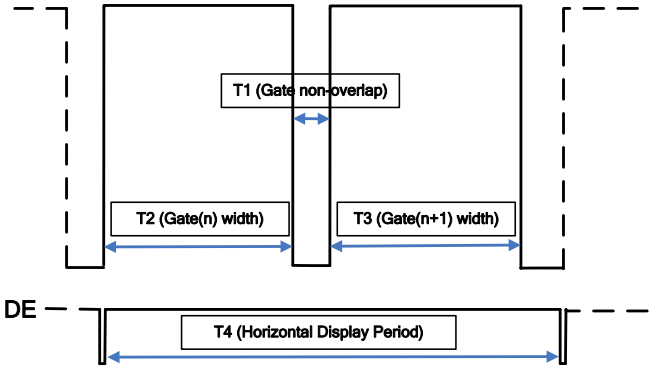
Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
49h	R/W	0	NO[2:0]			0	Reserved[2:0]			--

Designation	Description
NO[2:0]	 Gate (n) and Gate (n+1) non-overlap timing setting

NO[2:0]	Gate non-overlap (DCLK)
000	9
001	19
010	38
011	57
100	76
101	96
110	115
111	134

8.3.8 GATE TIMING SETTING 2 (4Ah)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
4Ah	R/W	0		PRGB_GWIDTH[2:0]		0		SRGB _GWIDTH[2:0]		--

Designation	Description
PRGB_GWIDTH[2:0] SRGB_GWIDTH[2:0]	

Set gate pulse width of parallel RGB interface.

PRGB _GWIDTH[2:0]	T2 Gate (n) width (DCLK)	T3 Gate (n+1) width (DCLK)
000	GT1	GT2
001	GT1 + 19	GT2 - 19
010	GT1 + 38	GT2 - 38
011	GT1 + 57	GT2 - 57
100	GT1 + 76	GT2 - 76
101	GT1 + 96	GT2 - 96
110	GT1 + 115	GT2 -115
111	GT1 +134	GT2 - 134

Set gate pulse width of serial RGB interface.

SRGB_GWIDTH[2:0]	T2 Gate (n) width (DCLK)	T3 Gate (n+1) width (DCLK)
000	GT1	GT2
001	GT1 + 19	GT2 - 19
010	GT1 + 38	GT2 - 38
011	GT1 + 57	GT2 - 57
100	GT1 + 76	GT2 - 76
101	GT1 + 96	GT2 - 96
110	GT1 + 115	GT2 -115
111	GT1 +134	GT2 - 134

8.4 Gamma Table Register Description

8.4.1 GAMMA SETTING (20h~29h, 30h~39h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
20h	R/W	0	0	0	VRF0P[4:0]					--
21h	R/W	0	0	0	VOS0P[4:0]					--
22h	R/W	PFP0[2:0]			PKP0[4:0]					--
23h	R/W	PFP1[2:0]			PKP1[4:0]					--
24h	R/W	PFP2[2:0]			PKP2[4:0]					--
25h	R/W	PFP3[2:0]			PKP3[4:0]					--
26h	R/W	PFP4[2:0]			PKP4[4:0]					--
27h	R/W	PFP5[2:0]			PKP5[4:0]					--
28h	R/W	PFP6[2:0]			PKP6[4:0]					--
29h	R/W	0	0	0	PKP7[4:0]					--
30h	R/W	0	0	0	VRF0N[4:0]					--
31h	R/W	0	0	0	VOS0N[4:0]					--
32h	R/W	PFN0[2:0]			PKN0[4:0]					--
33h	R/W	PFN1[2:0]			PKN1[4:0]					--
34h	R/W	PFN2[2:0]			PKN2[4:0]					--
35h	R/W	PFN3[2:0]			PKN3[4:0]					--
36h	R/W	PFN4[2:0]			PKN4[4:0]					--
37h	R/W	PFN5[2:0]			PKN5[4:0]					--
38h	R/W	PFN6[2:0]			PKN6[4:0]					--
39h	R/W	0	0	0	PKN7[4:0]					--

Designation	Description
PKP0[4:0]	V16 gamma selection
PKN0[4:0]	
PKP1[4:0]	V32 gamma selection
PKN1[4:0]	
PKP2[4:0]	V48 gamma selection
PKN2[4:0]	
PKP3[4:0]	V80 gamma selection
PKN3[4:0]	
PKP4[4:0]	V176 gamma selection
PKPN4[4:0]	
PKP5[4:0]	V208 gamma selection
PKN5[4:0]	

PKP6[4:0]	V224 gamma selection
PKN6[4:0]	
PKP7[4:0]	V240 gamma selection
PKN7[4:0]	
VRFOP[4:0]	V8 gamma selection
VRFON[4:0]	
VOS0P[4:0]	V248 gamma selection
VOS0N [4:0]	
PFP0[2:0]	V12 gamma selection
PFN0[2:0]	
PFP1[2:0]	V64 gamma selection
PFN1[2:0]	
PFP2[2:0]	V104 gamma selection
PFN2[2:0]	
PFP3[2:0]	V128 gamma selection
PFN3[2:0]	
PFP4[2:0]	V152 gamma selection
PFN4[2:0]	
PFP5[2:0]	V192 gamma selection
PFN5[2:0]	
PFP6[2:0]	V244 gamma selection
PFN6[2:0]	

8.5 OTP Table Register Description

8.5.1 ID1 SETTING (01h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
01h	R/W	0	ID1[6:0]							7Fh

Designation	Description
ID1[6:0]	Built-in OTP for ID1 setting. The OTP supports 3 times programming

8.5.2 ID2 SETTING (02h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
02h	R/W	0	ID2[6:0]							7Fh

Designation	Description
ID2[6:0]	Built-in OTP for ID2 setting. The OTP supports 3 times programming

8.5.3 ID3 SETTING (03h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
03h	R/W	0	ID3[6:0]							7Fh

Designation	Description
ID3[6:0]	Built-in OTP for ID3 setting. The OTP supports 3 times programming

8.5.4 2C ID CODE SETTING (04h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
04h	R/W	0	I^2CID[6:0]							78h

Designation	Description
I^2CID[6:0]	Built-in OTP for I^2C interface ID setting. The OTP supports 3 times programming

8.5.5 VCOM OFFSET SETTING (05h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
05h	R/W	0	VMF[6:0]							40h

Designation	Description
VMF[6:0]	VCOM offset setting

VMF[6]	VMF[5:0]	VGSP	GVDD	GVCL
0	000000	VMF[6:0]+64d	VRHP[5:0]+64d	VRHN[6:0]+64d
0	000001	VMF[6:0]+63d	VRHP[5:0]+63d	VRHN[6:0]+63d
0	000010	VMF[6:0]+62d	VRHP[5:0]+62d	VRHN[6:0]+62d
0	|	|	|	|
0	111110	VMF[6:0]+2d	VRHP[5:0]+2d	VRHN[6:0]+2d
0	111111	VMF[6:0]+1d	VRHP[5:0]+1d	VRHN[6:0]+1d
1	000000	VMF[6:0]	VRHP[5:0]	VRHN[6:0]
1	000001	VMF[6:0]-1d	VRHP[5:0]-1d	VRHN[6:0]-1d
1	000010	VMF[6:0]-2d	VRHP[5:0]-2d	VRHN[6:0]-2d
1	|	|	|	|
1	111110	VMF[6:0]-62d	VRHP[5:0]-62d	VRHN[6:0]-62d
1	111111	VMF[6:0]-63d	VRHP[5:0]-63d	VRHN[6:0]-63d

Note: d=16mV

8.5.6 OTP FUNCTION CONTROL (60h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
60h	R/W	0	0	0	0	1	INTVPP	OTPEN	1	09h

Designation	Description
INTVPP	Internal VPP function control INTVPP = 0: disable internal VPP function INTVPP = 1: enable internal VPP function
OTPEN	OTP function control OTPEN = 0: disable OTP function OTPEN = 1: enable OTP function

8.5.7 OTP ACKNOWLEDGEMENT CONTROL (65h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
65h	R/W	OTPACK[7:0]								00h

Designation	Description
OTPACK[7:0]	OTP active control

OTPACK[7:0]	Description
31h	ID1 program
32h	ID2 program
33h	ID3 program
34h	I^2C I/F ID program
3Ah	VCOM offset program
4Bh	Command 2 program
5Ch	Gamma program

8.5.8 VCOM OFFSET OTP PROGRAM TIMES (66h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
66h	R	0	0	0	0	0	VMF OTP TIME[2:0]			03h

Designation	Description
VMF OTP TIME[2:0]	Read VCOM offset programmable times

8.5.9 COMMAND 2 PROGRAM TIMES (67h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
67h	R	0	0	0	0	0	CMD2 OTP TIME[2:0]			03h

Designation	Description
CMD2 OTP TIME[2:0]	Read COMMAND 2 programmable times

8.5.10 GAMMA OTP PROGRAM TIMES (68h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
68h	R	0	0	0	0	0	GAMMA OTP TIME[2:0]			03h

Designation	Description
GAMMA OTP TIME[2:0]	Read GAMMA programmable times

8.5.11 ID1 OTP PROGRAM TIMES (69h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
69h	R	0	0	0	0	0	ID1 OTP TIME[2:0]			03h

Designation	Description
ID1 OTP TIME[2:0]	Read ID1 programmable times

8.5.12 ID2 OTP PROGRAM TIMES (6Ah)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
6Ah	R	0	0	0	0	0	ID2 OTP TIME[2:0]			03h

Designation	Description
ID2 OTP TIME[2:0]	Read ID2 programmable times

8.5.13 ID3 OTP PROGRAM TIMES (6Bh)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
6Bh	R	0	0	0	0	0	ID3 OTP TIME[2:0]			03h

Designation	Description
ID3 OTP TIME[2:0]	Read ID2 programmable times

8.5.14 I²C ID OTP PROGRAM TIMES (6Ch)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
6Ch	R	0	0	0	0	0	I²CID OTP TIME[2:0]			03h

Designation	Description
I²CID OTPTIME[2:0]	Read I²CID programmable times

9. ELECTRICAL SPECIFICATIONS

9.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power Supply Voltage	VDD	- 0.3 ~ +4.0	V
IO Supply Voltage	VDDI	- 0.3 ~ +4.0	V
Charge Pump Supply Voltage	PVDD	- 0.3 ~ +4.0	V
Logic Input Voltage Range	VIN	-0.3 ~ VDDI + 0.3	V
Logic Output Voltage Range	VOUT	-0.3 ~ VDDI + 0.3	V
Operating Temperature Range	TOPR	-30 ~ +85	℃
Storage Temperature Range	TSTG	-40 ~ +125	℃

Note:

1. That the stress exceeds the Limiting Value listed above it may cause the driver IC permanent damage. These values are for stress only. IC should be operated under the DC/AC Characteristic conditions for normal operation. If these conditions are not met, IC operation may be error and the reliability may be deteriorated.

2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.

3. VIN should be less than or equal to 3.6V. (VIN ≤ 3.6V)

9.2 DC Characteristics

DC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip)

9.2.1 Recommended Operating Range

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	VDD	3.0	3.3	3.6	V	
IO Supply Voltage	VDDI	3.0	-	3.6	V	
Charge Pump Supply Voltage	PVDD	3.0	3.3	3.6	V	

9.2.2 DC Characteristics for Digital Circuit

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Logic-High Input Voltage	Vih	0.7VDDI	-	VDDI	V	
Logic-Low Input Voltage	Vil	DGND	-	0.3VDDI	V	
Logic-High Output Voltage	Voh	VDDI-0.4	-	VDDI	V	
Logic-Low Output Voltage	Vol	DGND	-	DGND+0.4	V	

9.2.3 DC Characteristics for Analog Circuit

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Positive High-Voltage Power	VGH	13	15	16.5	V	No Load@ FR=60Hz
Negative High-Voltage Power	VGL	-7	-10	-11	V	
Output Voltage Deviation	Vod	-	±35	±45	mV	
Standby Current	Isc	-		50	uA	
Operation Current	Ioc	-	20		mA	

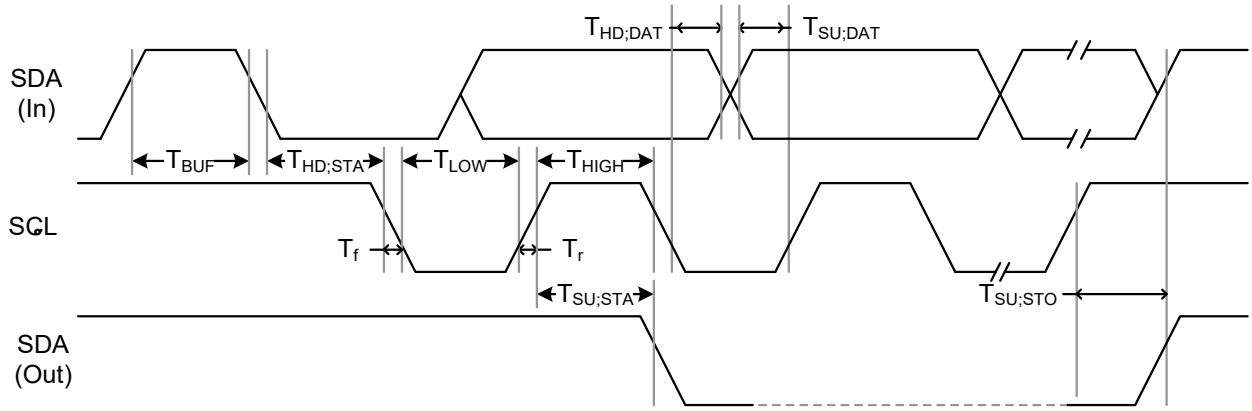
9.3 AC Characteristics

AC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip)

9.3.1 System Operation AC Characteristics

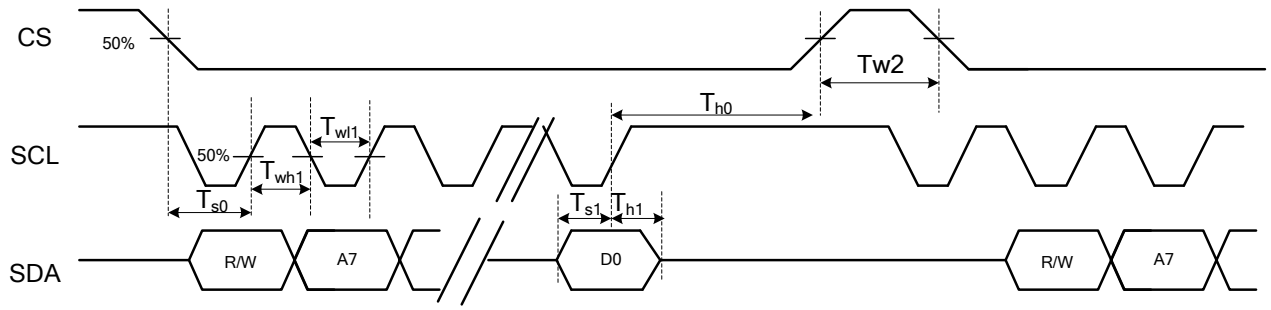
Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
VDD Power Source Slew Time	TPOR	-	-	20	ms	From 0V to 99% VDD
GRB Pulse Width	tRSTW	10	50	-	us	R=10Kohm, C=1uF
SD Output Stable Time	Tst	-	-	12	us	Output settled within +20mV Loading = 6.8k+28.2pF.
GD Output Rise and Fall Time	Tgst	-	-	6	us	Output settled (5%~95%), Loading = 4.7k+29.8pF

9.3.2 System Bus Timing for I²C Interface



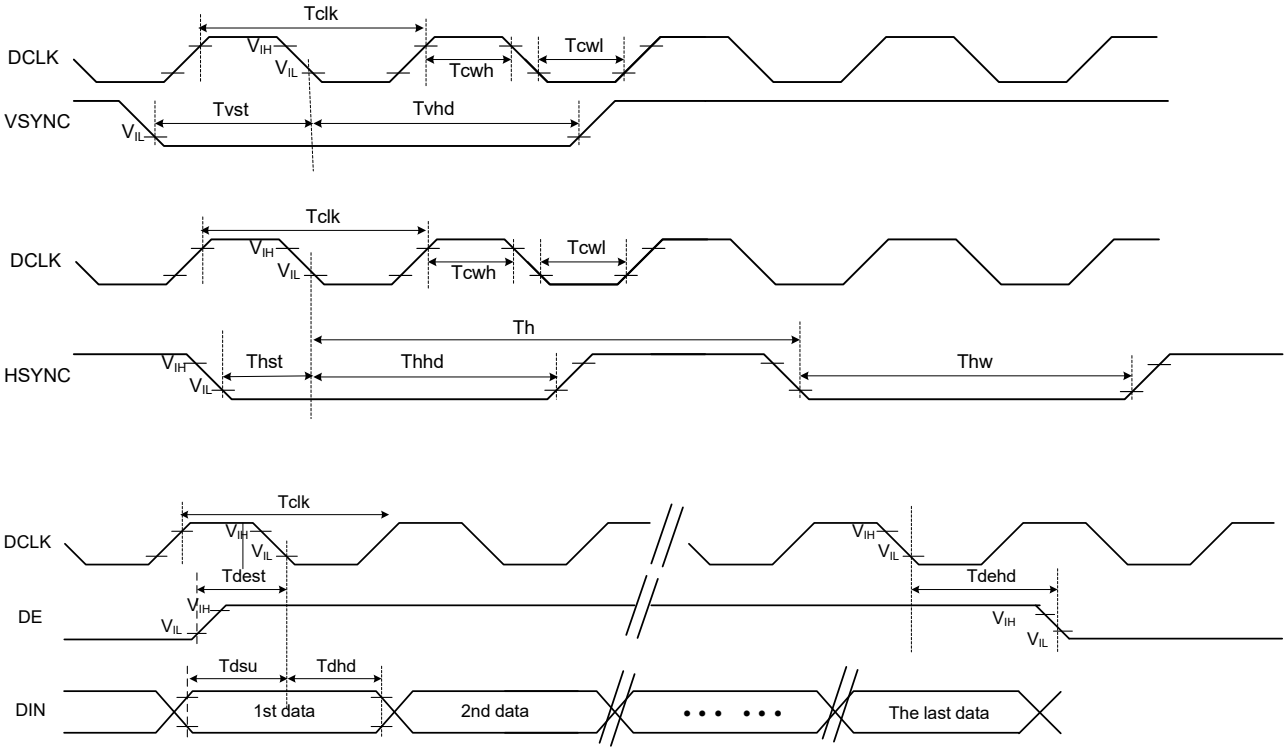
Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
SCL Clock Frequency	FSCL	-	-	400	KHz	
SCL Clock Low Period	TLOW	1300	-	-	ns	
SCL Clock High Period	THIGH	600	-	-	ns	
Signal Rise Time	Tr	20+0.1Cb	-	300	ns	
Signal Fall Time	Tf	20+0.1Cb	-	300	ns	
Start Condition Setup Time	TSU;STA	600	-	-	ns	
Start Condition Hold Time	THD;STA	600	-	-	ns	
Data Setup Time	TSU;DAT	100	-	-	ns	
Data Hold Time	THD;DAT	0	-	900	ns	
Setup Time for STOP Condition	TSU;STO	600	-	-	ns	
Bus Free Time Between a STOP and START	TBUF	100	-	-	ns	
Capacitive load represented by each bus line		Cb		400	pF	
Tolerable Spike Width on Bus	TSW	-	-	50	ns	

9.3.3 System Bus Timing for 3-Wire SPI Interface



Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
CS Input Setup Time	Ts0	50	-	-	ns	
Serial Data Input Setup Time	Ts1	50	-	-	ns	
CS Input Hold Time	Th0	50	-	-	ns	
Serial Data Input Hold Time	Th1	50	-	-	ns	
SCL Write Pulse High Width	Twh1	50	-	-	ns	
SCL Write Pulse Low Width	Twl1	50	-	-	ns	
SCL Read Pulse High Width	Trh1	300			ns	
SCL Read Pulse Low Width	Trl1	300			ns	
CS Pulse High Width	Tw2	400	-	-	ns	

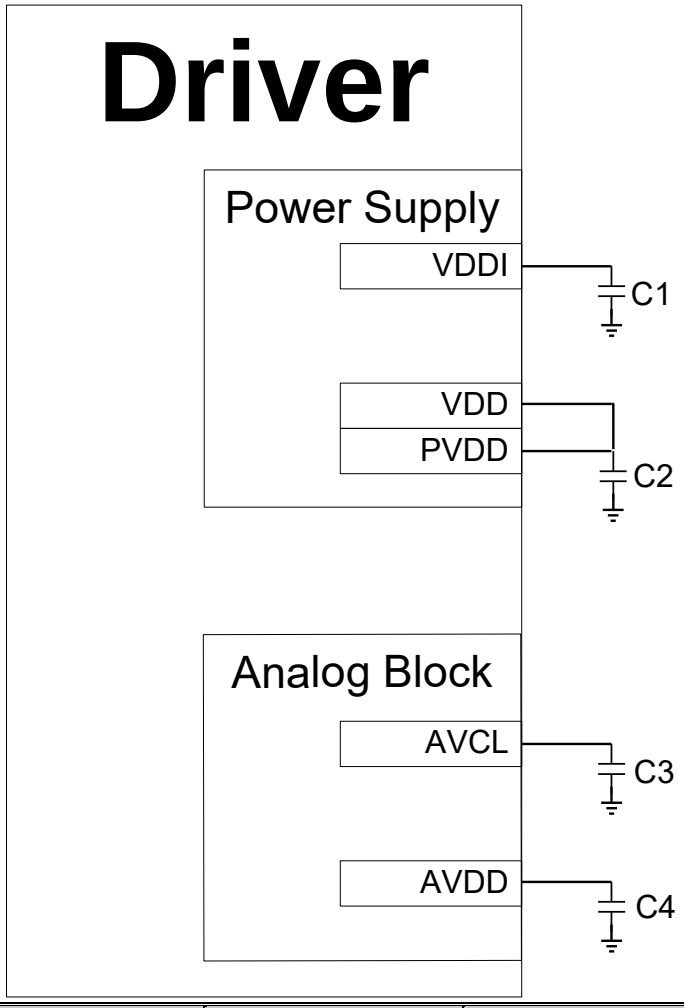
9.3.4 System Bus Timing for RGB Interface



Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLK Pulse Duty	Tclk	40	50	60	%	
HSYNC Width	Thw	2	-	-	DCLK	
HSYNC Period	Th	55	60	65	us	
VSYNC Setup Time	Tvst	12	-	-	ns	
VSYNC Hold Time	Tvhd	12	-	-	ns	
HSYNC Setup Time	Thst	12	-	-	ns	
HSYNC Hold Time	Thhd	12	-	-	ns	
Data Setup Time	Tdsu	12	-	-	ns	
Data Hold Time	Tdhd	12	-	-	ns	
DE Setup Time	Tdest	12	-	-	ns	
DE Hold Time	Tdehd	12	-	-	ns	

10. APPLICATION CIRCUIT

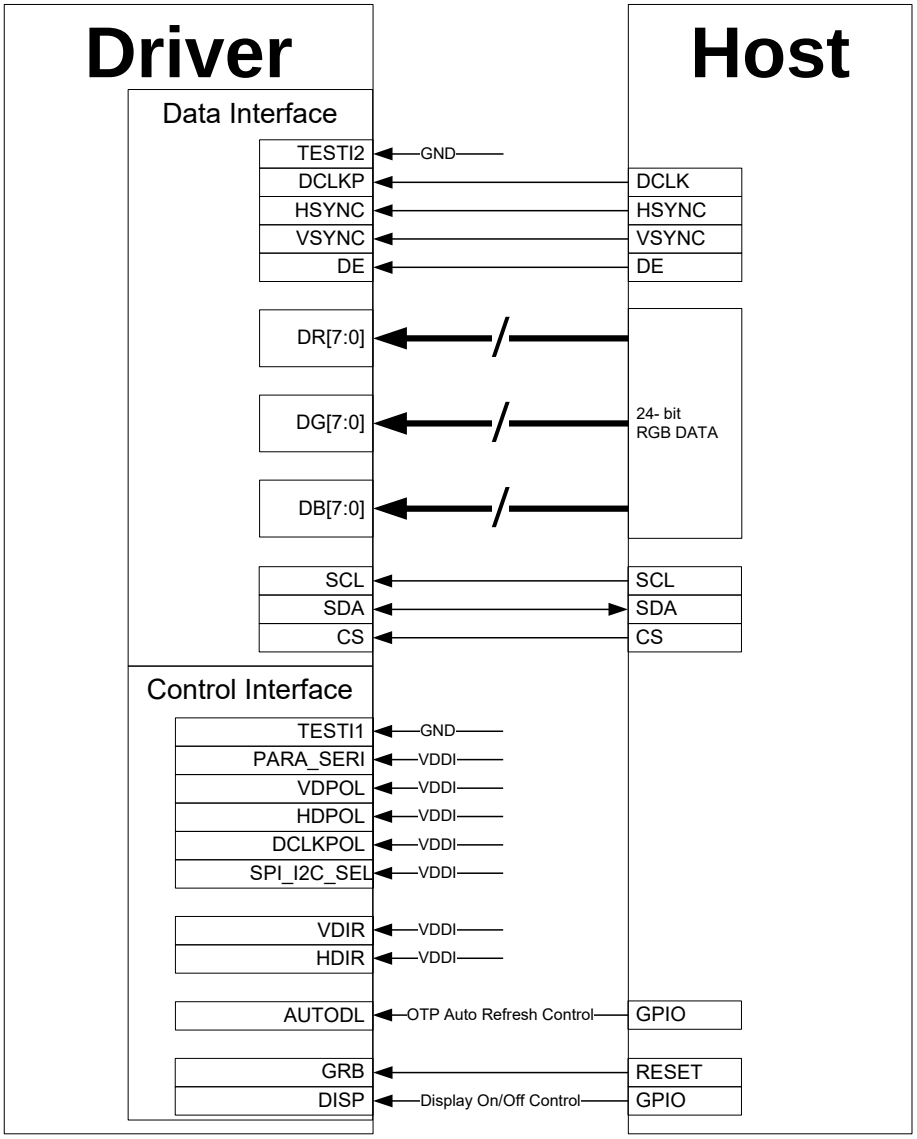
10.1 External Component of Power Circuit



Symbol	Capacitance (uf)	Voltage Proof (V)	Remarks	Note
C1	1	6	X7R	Default NC
C2	1	6	X7R	Default NC
C3	1	10	X7R	Default NC
C4	1	10	X7R	Default NC

Note: Default NC, The components would be needed depend on the system power, panel loading and display quality

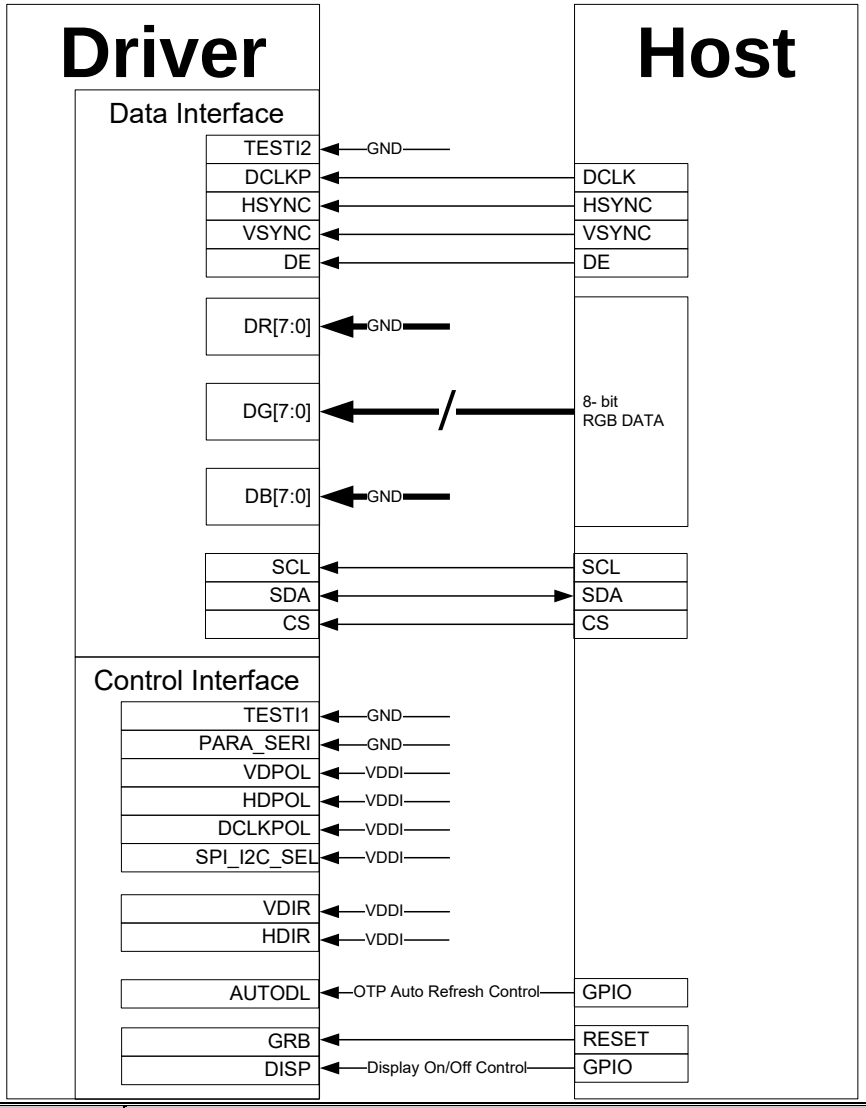
10.2 Parallel 24-bit RGB with 3-wire SPI



Pin Connection	Description
TESTI[2:1]	Reserved for testing only, please leave those pins connect to “L”
PARA_SERI= “H”	Parallel 24-bit RGB interface
VDPOL= “H”	VSYNC negative polarity
HDPOL= “H”	HSYNC negative polarity
DCLKPOL= “H”	DCLK negative polarity
SPI_I²C_SEL= “H”	3-Wire SPI
VDIR= “H”	Vertical scan direction= L1->L2->..... ->L(last line)
HDIR= “H”	Horizontal scan direction= Y1->Y2->.....->Y(last data)

Note: For detailed pin description please refer to section 6.1 PIN DESCRIPTION.

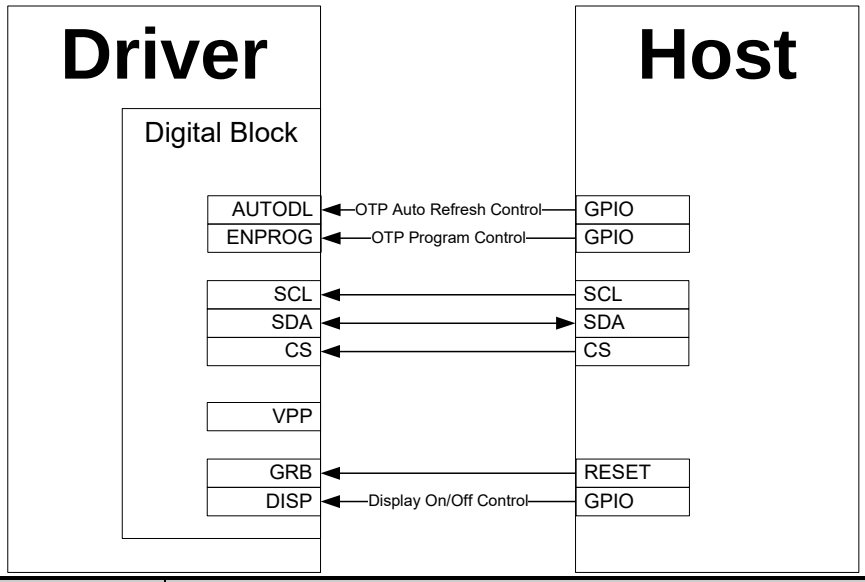
10.3 Serial 8-bit RGB with 3-wire SPI



Pin Connection	Description
TESTI[2:1]	Reserved for testing only, please leave those pins connect to “L”
PARA_SERI = “L”	Serial 8-bit RGB interface
VDPOL= “H”	VSYNC negative polarity
HDPOL= “H”	HSYNC negative polarity
DCLKPOL= “H”	DCLK negative polarity
SPI_I²C_SEL= “H”	3-Wire SPI
VDIR= “H”	Vertical scan direction= L1->L2->.....->L(last line)
HDIR= “H”	Horizontal scan direction= Y1->Y2->.....->Y(last data)

Note: For detailed pin description please refer to section 6.1 PIN DESCRIPTION.

10.4 OTP Operation

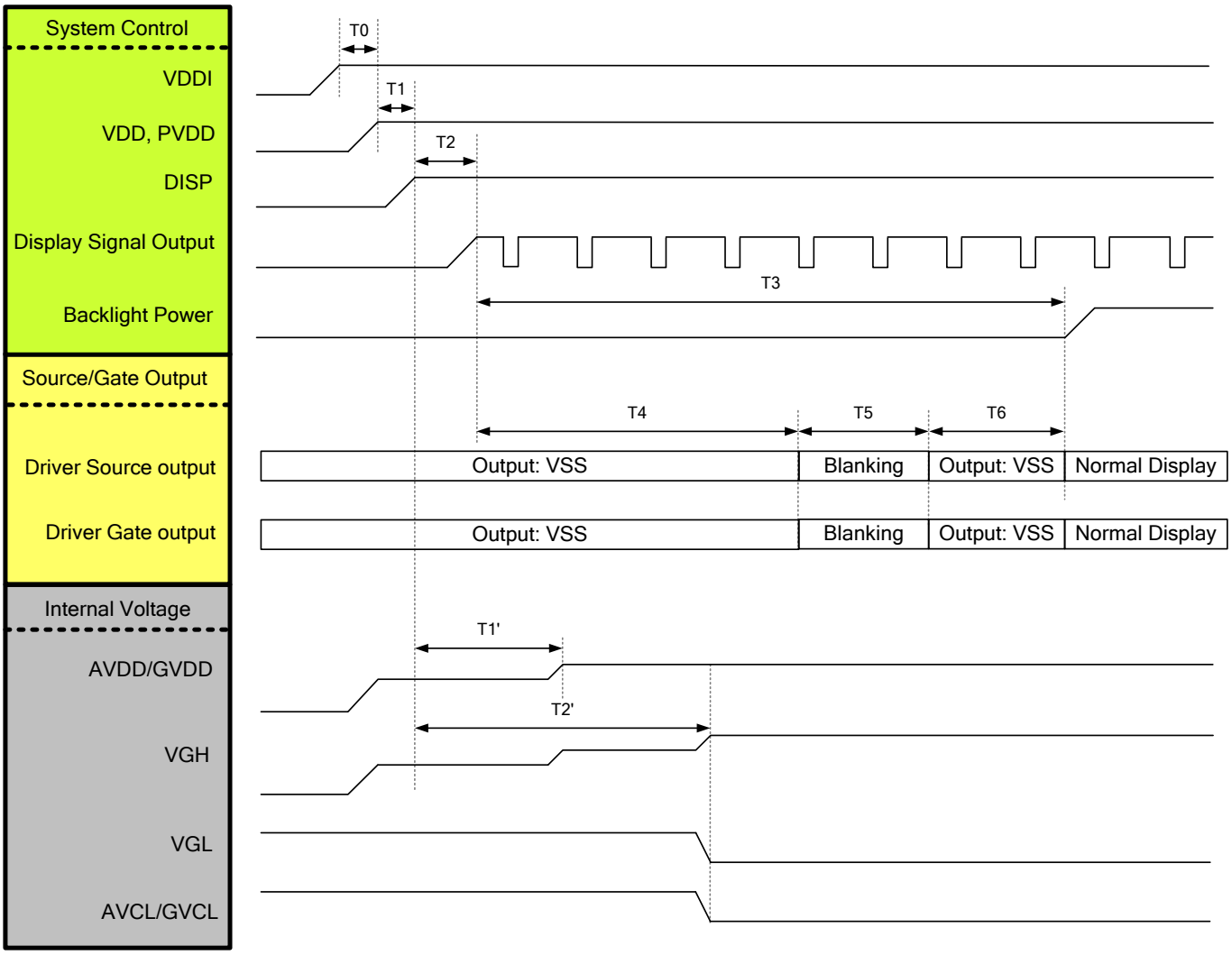


Pin Connection	Description
AUTODL	OTP auto-refresh function control
ENPROG	OTP program function control
VPP	Reserved for testing only, please leave this pin open.

Note: For detailed pin description please refer to section 6.1 PIN DESCRIPTION.

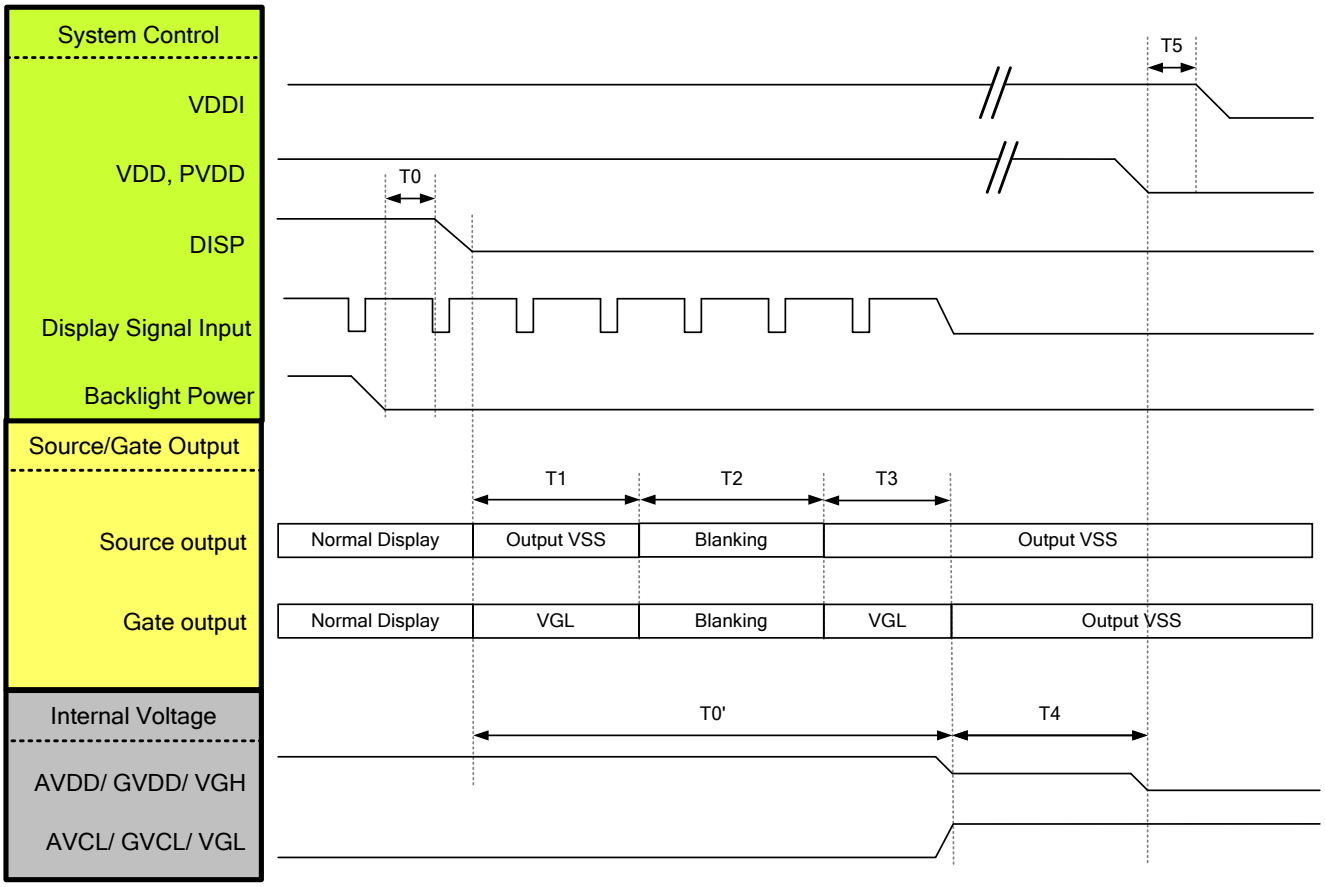
11. POWER ON/OFF SEQUENCE

11.1 Power On Sequence



Symbol	Description	Min. Time	Unit
T0	Analog power on delay time	0	ms
T1	System power stability to DISP= “High”	0	ms
T2	DISP= “High” to display signal output	10	ms
T3	Display signal output to backlight power on	250	ms
T4	Display signal output to source output	100	ms
T5	Source/ Gate blanking time	30	ms
T6	Source/ Gate automatic output VSS	80	ms
T1’	DISP= “High” to AVDD/GVDD voltage stable time	20	ms
T2’	DISP= “High” to VGH/VGL/AVCL/GVCL voltage stable time	60	ms

11.2 Power Off Sequence

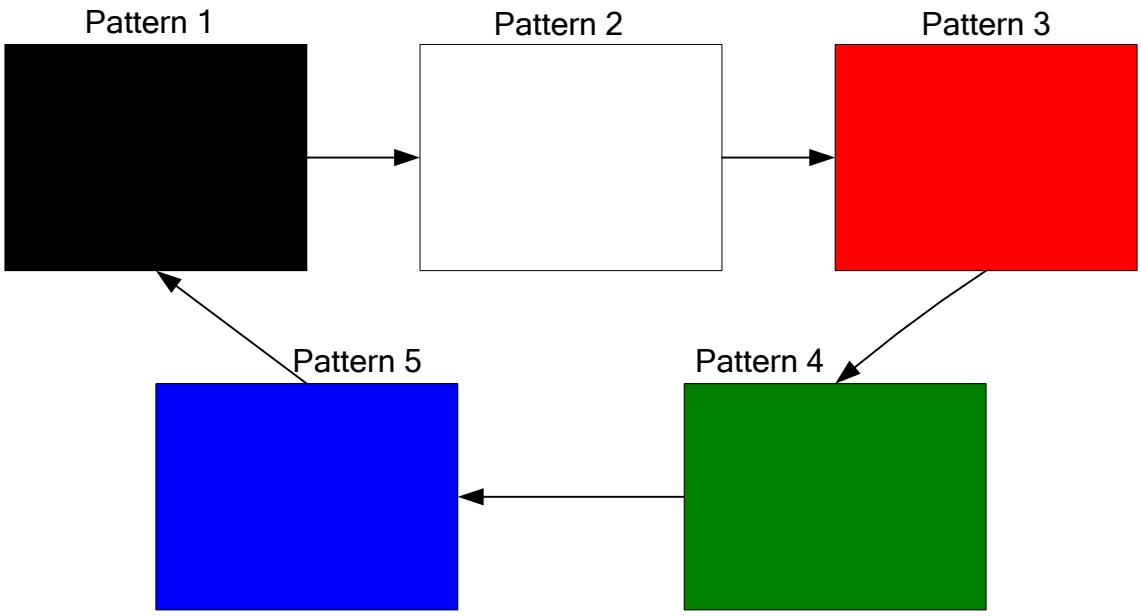


Symbol	Description	Min. Time	Unit
T0	Backlight power off to DISP off	5	ms
T1	Source voltage output VSS and Gate voltage output VGL	30	ms
T2	Source/ Gate blanking time	30	ms
T3	Source voltage output VSS and Gate voltage output VGL	20	ms
T4	AVDD/ GVDD/ VGH discharge time	5	ms
T5	Analog power off to digital power off time	0	ms
T0’	Source and Gate voltage discharge complete width	80	ms

12. BIST FUNCTION

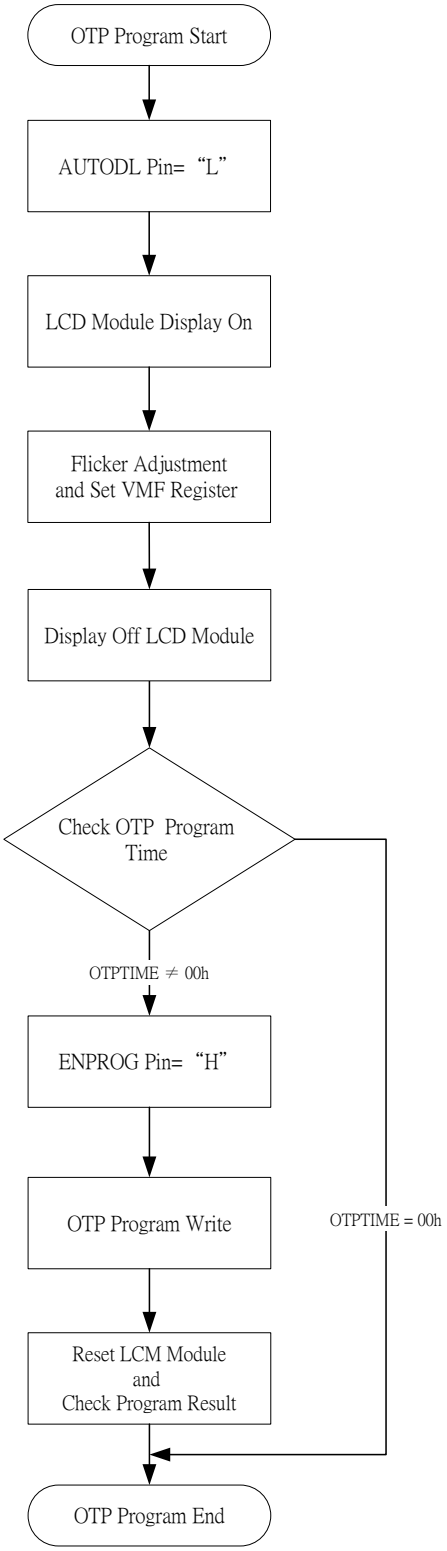
When “BIST_EN” pin sets to “H”, the BIST function is enabled. The BIST pattern will automatically display BIST pattern in the BIST mode as follows.

12.1 BIST Pattern



13. OTP PROGRAM FLOW

13.1 VCOM Offset OTP Flow



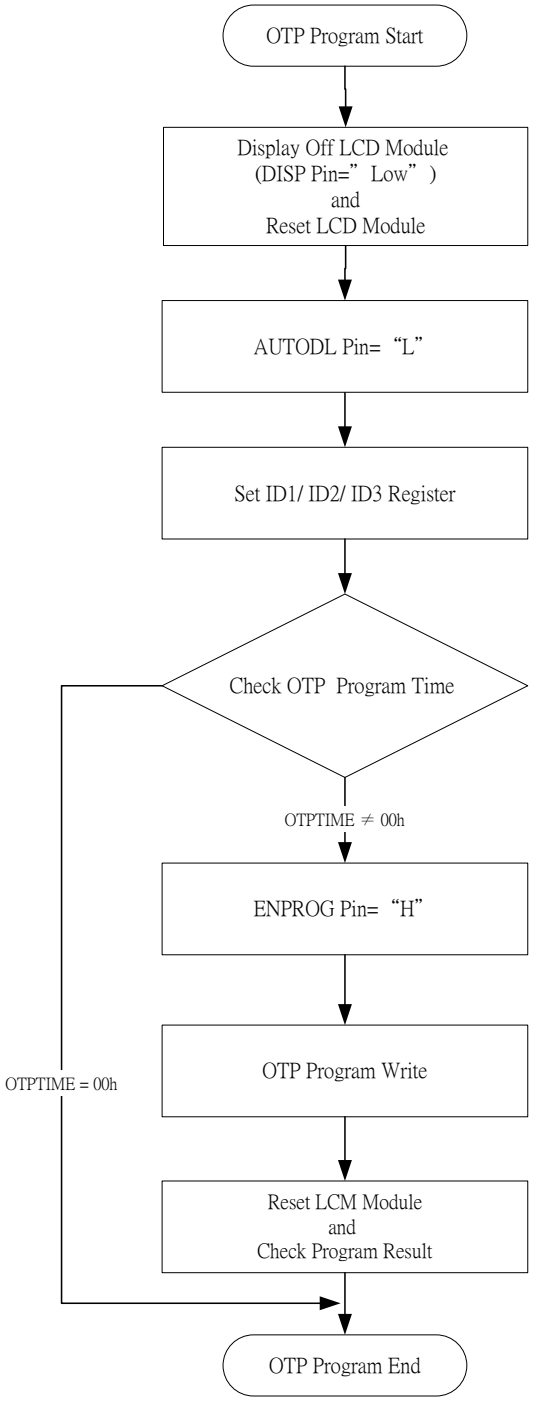
```
void Set_VMF_Register ()
{
      Write(Command,0x05);                  //Flicker adjustment and VMF[6:0] register setting
      Write(Data, VMF);
}

void Check_OTP_Program_Time()
{
      Write(Command,0x66);                  //VMF OTPTIME register address
      Read(Data, VMFOTPTIME);
}

void OTP_Program_Write()
{
      Write(Command,0x60);                  //OTP write function enable
      Write(Data,0x46);
      Write(Command,0x65);                  //OTP ACK= 0x3A
      Write(Data,0x3A);
}

void Check_Program_Result()
{
      Write(Command,0x05);                  //Read VMF[6:0] register setting
      Read(Data, VMF);
}
```

13.2 Custom Application ID Code OTP Flow



```
void Set_OTP_Register ()
{
    Write(Command,0x01);                    //The parameter should be adjusted by the customer
    Write(Data, ID);                        //ID= 0x01, ID2= 0x02, ID3= 0x03
}

void Check_OTP_Program_Time()
{
    Write(Command,0x69);                    //The parameter should be adjusted by the customer;
    Read(Data, IDOTPTIME);                  //MF OTPTIME= 0x6A, MF OTPTIME= 0x6A
}                                           //DS OTPTIME= 0x6B


void OTP_Program_Write()
{
    Write(Command,0x60);                    //OTP write function enable
    Write(Data,0x46);
    Write(Command,0x65);                    // The parameter should be adjusted by the customer;
    Write(Data,0x31);                       // ID ACK= 0x31, ID2 ACK= 0x32, ID3 ACK= 0x33
}


void Check_Program_Result ()
{
    Write(Command,0x01);                    // The parameter should be adjusted by the customer
    Read(Data, ID);                         // ID= 0x01, ID2= 0x02, ID3= 0x03
}
```

14. RECOMMENDED PANEL ROUTING RESISTANCE

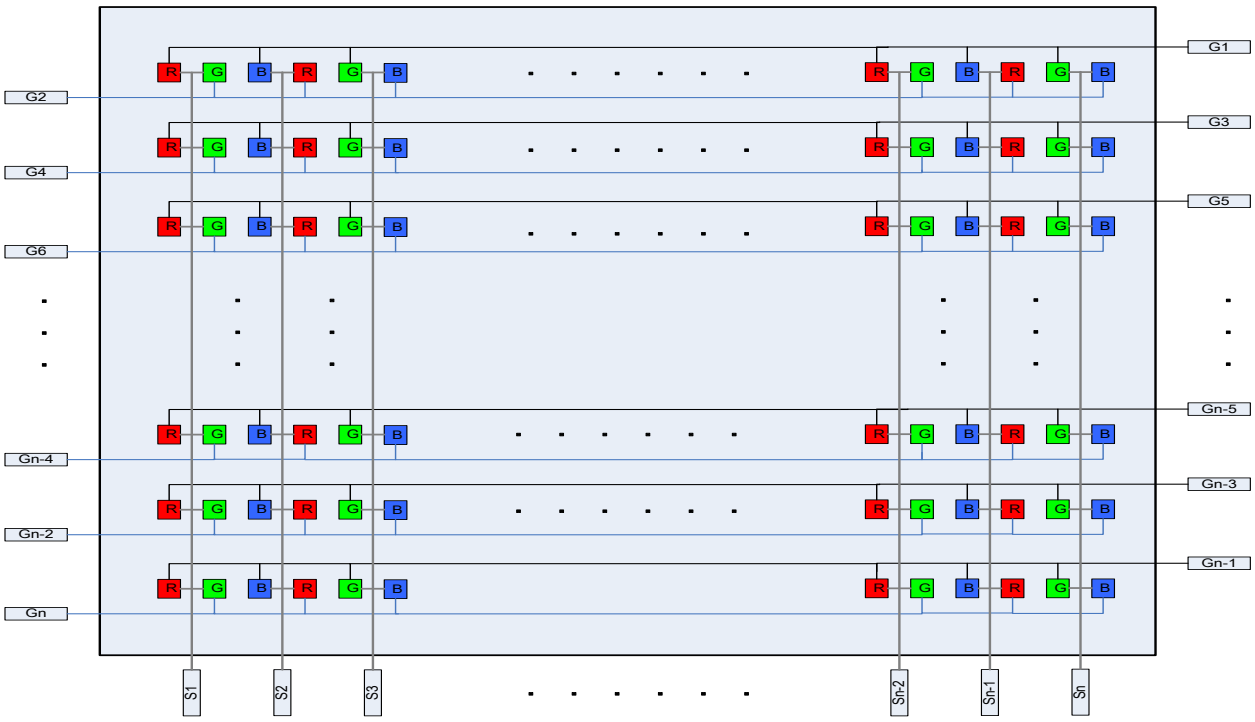
The recommended wiring resistance values are given below. The wiring resistance values affect the current capability of the power supply blocks and thus must be designed within the given range.

	Pin Name	Unit: ohm
1	VPP	<3
2	GVDD	<50
3	GVCL	<50
4	VCOM	<3
5	DGND	<3
6	VCC	<50
7	VDDI	<3
8	VDD	<3
9	VSYNC	<50
10	HSYNC	<50
11	DCLK	<50
12	VDPOL	<50
13	HDPOL	<50
14	DCLKPOL	<50
15	ENPROG	<50
16	DE	<50
17	PARA_SERI	<50
18	AUTODL	<50
19	HDIR	<50
20	VDIR	<50
21	CS	<50
22	SDA	<50
23	SCL	<50
24	DISP	<50
25	GRB	<50
26	BIST_EN	<50
27	DR7-DR0	<50
28	DG7-DG0	<50
29	DB7-DB0	<50
30	AGND	<3

	Pin Name	Unit: ohm
31	SPI_I2C_SEL	<50
32	AVCL	<50
33	AVCL1	<50
34	AVDD	<50
35	AVDD1	<50
36	VGSP	<50
37	PGND	<3
38	PVDD	<3
39	VGH	<50
40	VGL	<50

15. COLOR FILTER ARRANGEMENT

The IC supports the stripe color filter of dual-gate application. The color filter arrangement on panel is shown below.



16. REVISION HISTORY

Revision	Description	Date
Draft 0.1	1st edition	2017/11
Draft 0.2	2nd edition	2018/01
Version 0.3	3rd edition	2018/01