Sitronix

ST7528

16 Gray Scale ***Dot Matrix LCD Controller/Driver***

INTRODUCTION

The ST7528 is a driver & controller LSI for 16-level gray scale graphic dot-matrix liquid crystal display systems. It contains 2 Mode (160X100,132X128) for Segment and Common driver circuits. This chip is connected directly to a microprocessor, accepts Serial Peripheral Interface (SPI), IIC or 8-bit parallel display data and stores in an on-chip display data RAM of 160 x 129 x 4 bits. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

FEATURES

16-level (White Mode ~ Dark Mode) Gray Scale Display with PWM and FRC Methods

DDRAM data [4n : 4n+3]				Gray Scale
4n	4n + 1	4n + 2	4n+ 3	
0	0	0	0	White Mode
0	0	0	1	Gray Level 1
0	0	1	0	Gray Level 2
:	:	:	:	:
:	:	:	:	:
1	1	0	1	Gray Level 13
1	1	1	0	Gray Level 14
1	1	1	1	Dark

(Mode0: Accessible column address, n = 0, 1, 2, ……, 129, 130, 131)

(Mode1: Accessible column address, n = 0, 1, 2, ……, 157, 158, 159)

Driver Output Circuits

–Mode 0 : 132 segment outputs / 128+1 common outputs (16-level gray scale)

–Mode 1: 160 segment outputs / 100+1 common outputs (16-level gray scale)

Applicable Display Ratios

– Various partial display

– Partial window moving & data scrolling

On-chip Display Data RAM

– Capacity: 129 × 160 × 4 = 82,560 bits

–16-Gray Level display dot is illuminated by 4 bit data control

Microprocessor Interface

– 8-bit parallel bi-directional interface with 6800-series or 8080-series

– 4-line serial interface (4-line-SIF)

– 3-line serial interface (3-line-SIF)

– IIC serial interface

On-chip Low Power Analog Circuit

– On-chip oscillator circuit

– Voltage converter (x3, x4, x5 or x6)

– Voltage regulator (temperature coefficient: -0.125%/°C, or external input)

– On-chip electronic contrast control function (64 steps X 8)

– Voltage follower (LCD bias: 1/5 to 1/12)

Operating Voltage Range

– Supply voltage (VDD): 1.8 to 3.3V

(VDD2): 2.4 to 3.3V

– LCD driving voltage (VLCD = V0 - VSS): 3.5 to 15.0 V

Package Type

– Application for COG

ST7528	**6800 , 8080 , 4-Line , 3-Line interface (without IIC interface)**	
ST7528i	**IIC interface**	

Note1: we would like to recommend to use the external VOUT when the panel is large than 1.8 inch

Note2: we would like to recommend to set lower VOP than 12 voltage, when the panel size is large like 1.6 inch

ST7528 Pad Arrangement (COG)

Chip Size: 12,575 um × 1,220 um

Bump Pitch:

PAD NO 1 ~ 229, 353 ~ 385: 55 um (COM/SEG), PAD NO 230 ~ 338: 75 um (I/O) ,PAD NO 339 ~ 352: 75 um (I/O) ,

PAD 338~339: 81um.

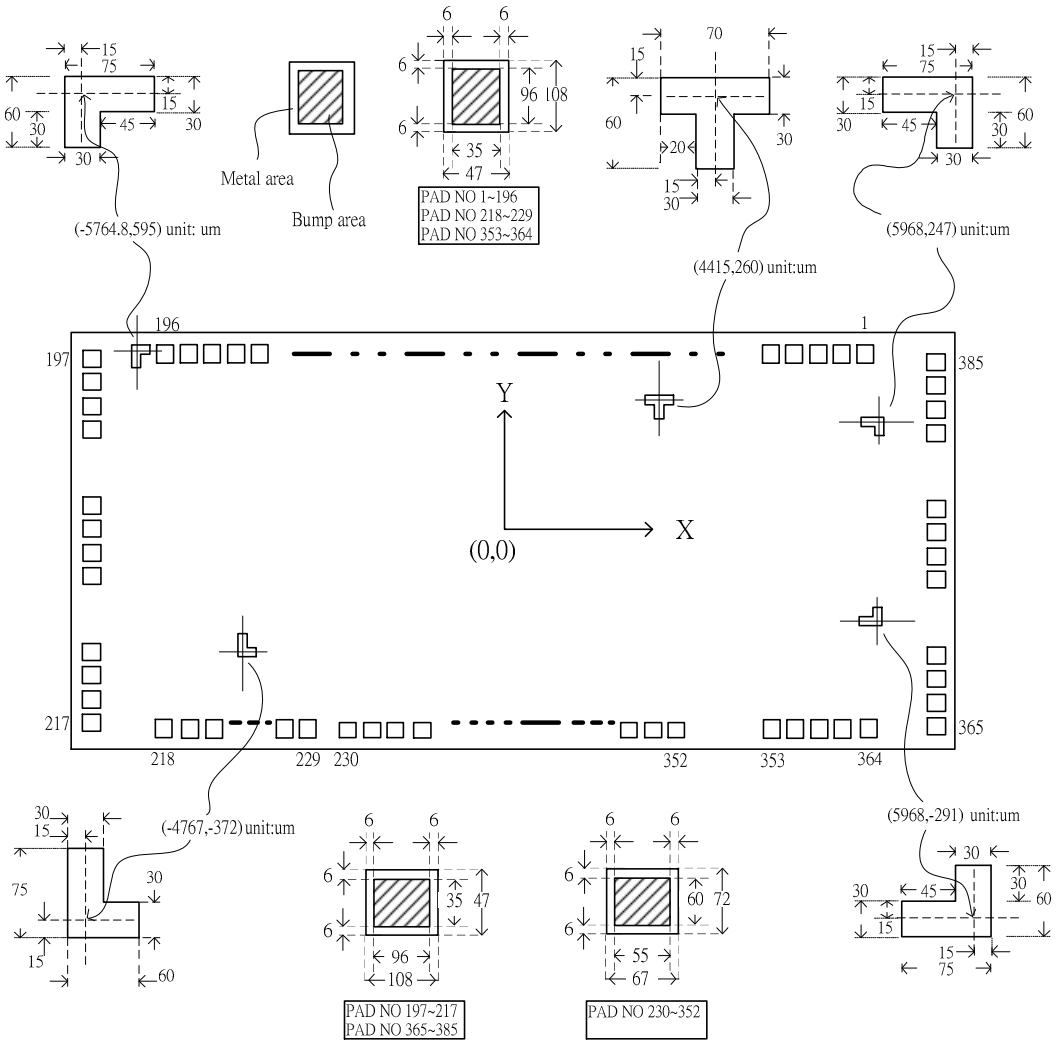
Bump Size:

PAD NO 1 ~ 196, 218 ~ 229, 353 ~ 364 : 35(x) um ×96(y) um PAD NO 197 ~ 217, 365 ~ 385 : 96(x) um ×35(y) um

PAD NO 230 ~ 352 : 55(x)um ×60(y) um

Bump Height: 17 um (Typical)

Chip Thickness: 635 um



Pad Center Coordinates

Pad No.	Name for Mode0 (132seg x 128com)	Name for Mode1 (160seg x 100com)	X(um)	Y(um)
1	COM30	COM16	5095	556
2	COM29	COM15	5040	556
3	COM28	COM14	4985	556
4	COM27	COM13	4930	556
5	COM26	COM12	4875	556
6	COM25	COM11	4820	556
7	COM24	COM10	4765	556
8	COM23	COM9	4710	556
9	COM22	COM8	4655	556
10	COM21	COM7	4600	556
11	COM20	COM6	4545	556
12	COM19	COM5	4490	556
13	COM18	COM4	4435	556
14	COM17	COM3	4380	556
15	COM16	COM2	4325	556
16	COM15	COM1	4270	556
17	COM14	COM0	4215	556
18	COM13	COMS1	4160	556
19	COM12	SEG0	4105	556
20	COM11	SEG1	4050	556
21	COM10	SEG2	3995	556
22	COM9	SEG3	3940	556
23	COM8	SEG4	3885	556
24	COM7	SEG5	3830	556
25	COM6	SEG6	3775	556
26	COM5	SEG7	3720	556
27	COM4	SEG8	3665	556
28	COM3	SEG9	3610	556
29	COM2	SEG10	3555	556
30	COM1	SEG11	3500	556
31	COM0	SEG12	3445	556
32	COMS1	SEG13	3390	556
33	SEG0	SEG14	3335	556

Pad No.	Name for Mode0 (132seg x 128com)	Name for Mode1 (160seg x 100com)	X(um)	Y(um)
34	SEG1	SEG15	3280	556
35	SEG2	SEG16	3225	556
36	SEG3	SEG17	3170	556
37	SEG4	SEG18	3115	556
38	SEG5	SEG19	3060	556
39	SEG6	SEG20	3005	556
40	SEG7	SEG21	2950	556
41	SEG8	SEG22	2895	556
42	SEG9	SEG23	2840	556
43	SEG10	SEG24	2785	556
44	SEG11	SEG25	2730	556
45	SEG12	SEG26	2675	556
46	SEG13	SEG27	2620	556
47	SEG14	SEG28	2565	556
48	SEG15	SEG29	2510	556
49	SEG16	SEG30	2455	556
50	SEG17	SEG31	2400	556
51	SEG18	SEG32	2345	556
52	SEG19	SEG33	2290	556
53	SEG20	SEG34	2235	556
54	SEG21	SEG35	2180	556
55	SEG22	SEG36	2125	556
56	SEG23	SEG37	2070	556
57	SEG24	SEG38	2015	556
58	SEG25	SEG39	1960	556
59	SEG26	SEG40	1905	556
60	SEG27	SEG41	1850	556
61	SEG28	SEG42	1795	556
62	SEG29	SEG43	1740	556
63	SEG30	SEG44	1685	556
64	SEG31	SEG45	1630	556
65	SEG32	SEG46	1575	556
66	SEG33	SEG47	1520	556
67	SEG34	SEG48	1465	556
68	SEG35	SEG49	1410	556

Pad No.	Name for Mode0 (132seg x 128com)	Name for Mode1 (160seg x 100com)	X(um)	Y(um)
69	SEG36	SEG50	1355	556
70	SEG37	SEG51	1300	556
71	SEG38	SEG52	1245	556
72	SEG39	SEG53	1190	556
73	SEG40	SEG54	1135	556
74	SEG41	SEG55	1080	556
75	SEG42	SEG56	1025	556
76	SEG43	SEG57	970	556
77	SEG44	SEG58	915	556
78	SEG45	SEG59	860	556
79	SEG46	SEG60	805	556
80	SEG47	SEG61	750	556
81	SEG48	SEG62	695	556
82	SEG49	SEG63	640	556
83	SEG50	SEG64	585	556
84	SEG51	SEG65	530	556
85	SEG52	SEG66	475	556
86	SEG53	SEG67	420	556
87	SEG54	SEG68	365	556
88	SEG55	SEG69	310	556
89	SEG56	SEG70	255	556
90	SEG57	SEG71	200	556
91	SEG58	SEG72	145	556
92	SEG59	SEG73	90	556
93	SEG60	SEG74	35	556
94	SEG61	SEG75	-19	556
95	SEG62	SEG76	-74	556
96	SEG63	SEG77	-129	556
97	SEG64	SEG78	-184	556
98	SEG65	SEG79	-239	556
99	SEG66	SEG80	-294	556
100	SEG67	SEG81	-349	556
101	SEG68	SEG82	-404	556
102	SEG69	SEG83	-459	556
103	SEG70	SEG84	-514	556

Pad No.	Name for Mode0 (132seg x 128com)	Name for Mode1 (160seg x 100com)	X(um)	Y(um)
104	SEG71	SEG85	-569	556
105	SEG72	SEG86	-624	556
106	SEG73	SEG87	-679	556
107	SEG74	SEG88	-734	556
108	SEG75	SEG89	-789	556
109	SEG76	SEG90	-844	556
110	SEG77	SEG91	-899	556
111	SEG78	SEG92	-954	556
112	SEG79	SEG93	-1009	556
113	SEG80	SEG94	-1064	556
114	SEG81	SEG95	-1119	556
115	SEG82	SEG96	-1174	556
116	SEG83	SEG97	-1229	556
117	SEG84	SEG98	-1284	556
118	SEG85	SEG99	-1339	556
119	SEG86	SEG100	-1394	556
120	SEG87	SEG101	-1449	556
121	SEG88	SEG102	-1504	556
122	SEG89	SEG103	-1559	556
123	SEG90	SEG104	-1614	556
124	SEG91	SEG105	-1669	556
125	SEG92	SEG106	-1724	556
126	SEG93	SEG107	-1779	556
127	SEG94	SEG108	-1834	556
128	SEG95	SEG109	-1889	556
129	SEG96	SEG110	-1944	556
130	SEG97	SEG111	-1999	556
131	SEG98	SEG112	-2054	556
132	SEG99	SEG113	-2109	556
133	SEG100	SEG114	-2164	556
134	SEG101	SEG115	-2219	556
135	SEG102	SEG116	-2274	556
136	SEG103	SEG117	-2329	556
137	SEG104	SEG118	-2384	556
138	SEG105	SEG119	-2439	556

Pad No.	Name for Mode0 (132seg x 128com)	Name for Mode1 (160seg x 100com)	X(um)	Y(um)
139	SEG106	SEG120	-2494	556
140	SEG107	SEG121	-2549	556
141	SEG108	SEG122	-2604	556
142	SEG109	SEG123	-2659	556
143	SEG110	SEG124	-2714	556
144	SEG111	SEG125	-2769	556
145	SEG112	SEG126	-2824	556
146	SEG113	SEG127	-2879	556
147	SEG114	SEG128	-2934	556
148	SEG115	SEG129	-2989	556
149	SEG116	SEG130	-3044	556
150	SEG117	SEG131	-3099	556
151	SEG118	SEG132	-3154	556
152	SEG119	SEG133	-3209	556
153	SEG120	SEG134	-3264	556
154	SEG121	SEG135	-3319	556
155	SEG122	SEG136	-3374	556
156	SEG123	SEG137	-3429	556
157	SEG124	SEG138	-3484	556
158	SEG125	SEG139	-3539	556
159	SEG126	SEG140	-3594	556
160	SEG127	SEG141	-3649	556
161	SEG128	SEG142	-3704	556
162	SEG129	SEG143	-3759	556
163	SEG130	SEG144	-3814	556
164	SEG131	SEG145	-3869	556
165	COM64	SEG146	-3924	556
166	COM65	SEG147	-3979	556
167	COM66	SEG148	-4034	556
168	COM67	SEG149	-4089	556
169	COM68	SEG150	-4144	556
170	COM69	SEG151	-4199	556
171	COM70	SEG152	-4254	556
172	COM71	SEG153	-4309	556
173	COM72	SEG154	-4364	556

Pad No.	Name for Mode0 (132seg x 128com)	Name for Mode1 (160seg x 100com)	X(um)	Y(um)
174	COM73	SEG155	-4419	556
175	COM74	SEG156	-4474	556
176	COM75	SEG157	-4529	556
177	COM76	SEG158	-4584	556
178	COM77	SEG159	-4639	556
179	COM78	COM50	-4694	556
180	COM79	COM51	-4749	556
181	COM80	COM52	-4804	556
182	COM81	COM53	-4859	556
183	COM82	COM54	-4914	556
184	COM83	COM55	-4969	556
185	COM84	COM56	-5024	556
186	COM85	COM57	-5079	556
187	COM86	COM58	-5134	556
188	COM87	COM59	-5189	556
189	COM88	COM60	-5244	556
190	COM89	COM61	-5299	556
191	COM90	COM62	-5354	556
192	COM91	COM63	-5409	556
193	COM92	COM64	-5464	556
194	COM93	COM65	-5519	556
195	COM94	COM66	-5574	556
196	COM95	COM67	-5629	556
197	COM96	COM68	-6233	550
198	COM97	COM69	-6233	495
199	COM98	COM70	-6233	440
200	COM99	COM71	-6233	385
201	COM100	COM72	-6233	330
202	COM101	COM73	-6233	275
203	COM102	COM74	-6233	220
204	COM103	COM75	-6233	165
205	COM104	COM76	-6233	110
206	COM105	COM77	-6233	55
207	COM106	COM78	-6233	0
208	COM107	COM79	-6233	-55

Pad No.	Name for Mode0 (132seg x 128com)	Name for Mode1 (160seg x 100com)	X(um)	Y(um)
209	COM108	COM80	-6233	-110
210	COM109	COM81	-6233	-165
211	COM110	COM82	-6233	-220
212	COM111	COM83	-6233	-275
213	COM112	COM84	-6233	-330
214	COM113	COM85	-6233	-385
215	COM114	COM86	-6233	-440
216	COM115	COM87	-6233	-495
217	COM116	COM88	-6233	-550
218	COM117	COM89	-5417	-556
219	COM118	COM90	-5362	-556
220	COM119	COM91	-5307	-556
221	COM120	COM92	-5252	-556
222	COM121	COM93	-5197	-556
223	COM122	COM94	-5142	-556
224	COM123	COM95	-5087	-556
225	COM124	COM96	-5032	-556
226	COM125	COM97	-4977	-556
227	COM126	COM98	-4922	-556
228	COM127	COM99	-4867	-556
229	COMS2	COMS2	-4812	-556
230	T9	T9	-4728	-574
231	VDD	VDD	-4653	-574
232	PS0	PS0	-4578	-574
233	PS1	PS1	-4503	-574
234	PS2	PS2	-4428	-574
235	VSS	VSS	-4353	-574
236	CSB	CSB	-4278	-574
237	CSB	CSB	-4203	-574
238	RST	RST	-4128	-574
239	RST	RST	-4053	-574
240	A0	A0	-3978	-574
241	A0	A0	-3903	-574
242	RW_WR	RW_WR	-3828	-574
243	RW_WR	RW_WR	-3753	-574

Pad No.	Name for Mode0 (132seg x 128com)	Name for Mode1 (160seg x 100com)	X(um)	Y(um)
244	E_RD	E_RD	-3678	-574
245	E_RD	E_RD	-3603	-574
246	D0	D0	-3528	-574
247	D0	D0	-3453	-574
248	D1	D1	-3378	-574
249	D1	D1	-3303	-574
250	D2	D2	-3228	-574
251	D2	D2	-3153	-574
252	D3	D3	-3078	-574
253	D3	D3	-3003	-574
254	D4	D4	-2928	-574
255	D4	D4	-2853	-574
256	D5	D5	-2778	-574
257	D5	D5	-2703	-574
258	D6	D6	-2628	-574
259	D6	D6	-2553	-574
260	D7	D7	-2478	-574
261	D7	D7	-2403	-574
262	VDD	VDD	-2328	-574
263	VDD	VDD	-2253	-574
264	VDD	VDD	-2178	-574
265	VDD	VDD	-2103	-574
266	VDD	VDD	-2028	-574
267	VDD	VDD	-1953	-574
268	VDD2	VDD2	-1878	-574
269	VDD2	VDD2	-1803	-574
270	VDD2	VDD2	-1728	-574
271	VDD2	VDD2	-1653	-574
272	VDD2	VDD2	-1578	-574
273	VDD2	VDD2	-1503	-574
274	VDD2	VDD2	-1428	-574
275	VDD2	VDD2	-1353	-574
276	VDD2	VDD2	-1278	-574
277	VDD2	VDD2	-1203	-574
278	VDD2	VDD2	-1128	-574

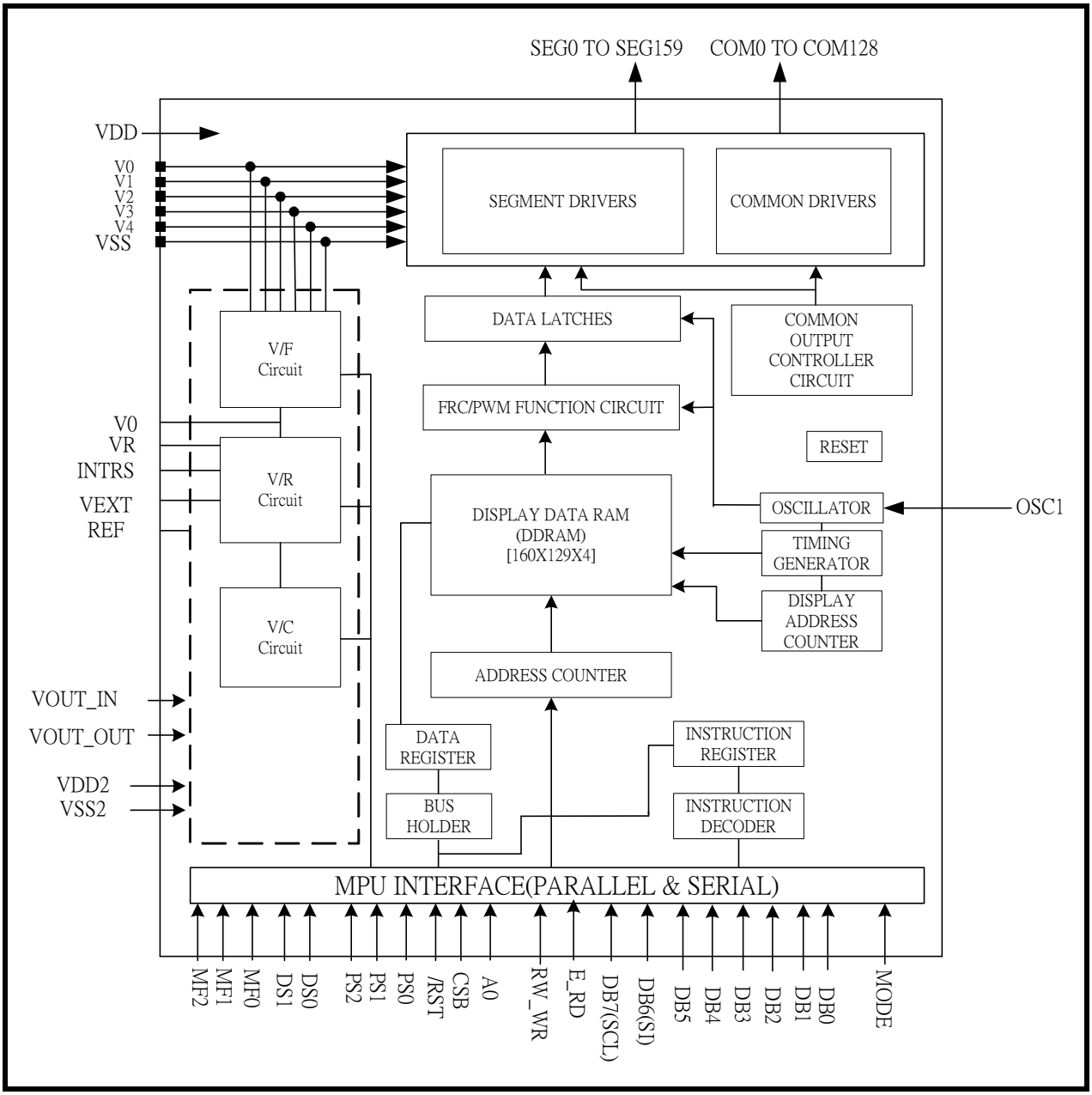
Pad No.	Name for Mode0 (132seg x 128com)	Name for Mode1 (160seg x 100com)	X(um)	Y(um)
279	VDD2	VDD2	-1053	-574
280	VDD2	VDD2	-978	-574
281	VDD2	VDD2	-903	-574
282	VDD2	VDD2	-828	-574
283	VDD2	VDD2	-753	-574
284	VSS2	VSS2	-678	-574
285	VSS2	VSS2	-603	-574
286	VSS2	VSS2	-528	-574
287	VSS2	VSS2	-453	-574
288	VSS2	VSS2	-378	-574
289	VSS2	VSS2	-303	-574
290	VSS2	VSS2	-228	-574
291	VSS2	VSS2	-153	-574
292	VSS2	VSS2	-78	-574
293	VSS2	VSS2	-3	-574
294	VSS2	VSS2	71	-574
295	VSS2	VSS2	146	-574
296	VSS2	VSS2	221	-574
297	VSS2	VSS2	296	-574
298	VSS2	VSS2	371	-574
299	VSS2	VSS2	446	-574
300	VSS	VSS	521	-574
301	VSS	VSS	596	-574
302	VSS	VSS	671	-574
303	VSS	VSS	746	-574
304	VSS	VSS	821	-574
305	VSS	VSS	896	-574
306	MODE	MODE	971	-574
307	TA	TA	1046	-574
308	MF2	MF2	1121	-574
309	MF1	MF1	1196	-574
310	MF0	MF0	1271	-574
311	DS0	DS0	1346	-574
312	DS1	DS1	1421	-574
313	VDD	VDD	1496	-574

Pad No.	Name for Mode0 (132seg x 128com)	Name for Mode1 (160seg x 100com)	X(um)	Y(um)
314	VOUT_OUT	VOUT_OUT	1571	-574
315	VOUT_OUT	VOUT_OUT	1646	-574
316	VOUT_OUT	VOUT_OUT	1721	-574
317	VOUT_OUT	VOUT_OUT	1796	-574
318	VOUT_OUT	VOUT_OUT	1871	-574
319	VOUT_OUT	VOUT_OUT	1946	-574
320	VOUT_IN	VOUT_IN	2021	-574
321	VOUT_IN	VOUT_IN	2096	-574
322	VOUT_IN	VOUT_IN	2171	-574
323	VOUT_IN	VOUT_IN	2246	-574
324	VOUT_IN	VOUT_IN	2321	-574
325	VOUT_IN	VOUT_IN	2396	-574
326	T[8]	T[8]	2471	-574
327	T[7]	T[7]	2546	-574
328	T[6]	T[6]	2621	-574
329	T[5]	T[5]	2696	-574
330	T[4]	T[4]	2771	-574
331	T[3]	T[3]	2846	-574
332	T[2]	T[2]	2921	-574
333	T[1]	T[1]	2996	-574
334	T[0]	T[0]	3071	-574
335	VDD	VDD	3146	-574
336	REF	REF	3221	-574
337	VSS	VSS	3296	-574
338	VEXT	VEXT	3371	-574
339	VDD	VDD	3452	-574
340	INTRS	INTRS	3527	-574
341	VSS	VSS	3602	-574
342	OSC1	OSC1	3677	-574
343	OSC1	OSC1	3752	-574
344	VDD	VDD	3827	-574
345	VR	VR	3902	-574
346	VR	VR	3977	-574
347	V4	V4	4052	-574
348	V3	V3	4127	-574

Pad No.	Name for Mode0 (132seg x 128com)	Name for Mode1 (160seg x 100com)	X(um)	Y(um)
349	V2	V2	4202	-574
350	V1	V1	4277	-574
351	V0	V0	4352	-574
352	V0	V0	4427	-574
353	COM63	COM49	5339	-556
354	COM62	COM48	5394	-556
355	COM61	COM47	5449	-556
356	COM60	COM46	5504	-556
357	COM59	COM45	5559	-556
358	COM58	COM44	5614	-556
359	COM57	COM43	5669	-556
360	COM56	COM42	5724	-556
361	COM55	COM41	5779	-556
362	COM54	COM40	5834	-556
363	COM53	COM39	5889	-556
364	COM52	COM38	5944	-556
365	COM51	COM37	6233	-550
366	COM50	COM36	6233	-495
367	COM49	COM35	6233	-440
368	COM48	COM34	6233	-385
369	COM47	COM33	6233	-330
370	COM46	COM32	6233	-275
371	COM45	COM31	6233	-220
372	COM44	COM30	6233	-165
373	COM43	COM29	6233	-110
374	COM42	COM28	6233	-55
375	COM41	COM27	6233	0
376	COM40	COM26	6233	55
377	COM39	COM25	6233	110
378	COM38	COM24	6233	165
379	COM37	COM23	6233	220
380	COM36	COM22	6233	275
381	COM35	COM21	6233	330
382	COM34	COM20	6233	385
383	COM33	COM19	6233	440
384	COM32	COM18	6233	495
385	COM31	COM17	6233	550

The tolerance is around +/- 1um. The number under floating point is truncated.

BLOCK DIAGRAM



PIN DESCRIPTION

POWER SUPPLY

Power Supply Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>VDD</td><td>Supply</td><td>Power supply</td></tr>
<tr><td>VSS</td><td>Supply</td><td>Ground</td></tr>
<tr><td>VSS2</td><td>Supply</td><td>Ground</td></tr>
<tr><td>VDD2</td><td>Supply</td><td>Power supply</td></tr>
<tr><td>VOUT_OUT</td><td>Supply</td><td>If the internal Vout voltage generator is used, the VOUT_IN & VOUT_OUT must be connected together. If an external supply is used, this pin must be left open.</td></tr>
<tr><td>VOUT_IN</td><td>Supply</td><td>An external Vout supply voltage can be supplied using the VOUT_IN pad. In this case, VOUT_OUT has to be left open, and the internal voltage generator has to be programmed to zero. (SET register VC=0)</td></tr>
<tr><td>V0
V1
V2
V3
V4</td><td>I/O</td><td>LCD driver supply voltages
The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application. V1,V2,V3,V4 need the capacitor between with VSS Voltages should have the following relationship;
V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS
When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias.
<table>
<tr><td>LCD bias</td><td>V1</td><td>V2</td><td>V3</td><td>V4</td></tr>
<tr><td>1/N bias</td><td>(N-1) / N x V0</td><td>(N-2) / N x V0</td><td>(2/N) x V0</td><td>(1/N) x V0</td></tr>
</table>
NOTE: N = 5 to 12</td></tr>
</table>

LCD DRIVER SUPPLY

LCD Driver Supply Pin Description

Name	I/O	Description
VR	I	V0 voltage adjustment pin It is valid only when on-chip resistors are not used (INTRS = "L") When using internal resistors (INTRS = "H"), open this pin
REF	I	Selects the external VREF voltage via the VEXT pin – REF = “H”: using the internal VREF – REF = “L”: using the external VREF
VEXT	I	Externally input reference voltage (VREF) for the internal voltage regulator It is valid only when REF is "L" When using internal voltage regulator, this pin must be open
OSC1	I	External OSC input pin, when using internal clock oscillator, connect OSC1 to VDD.

SYSTEM CONTROL

System Control Pin Description

Name	I/O	Description
INTRS	I	Internal resistor select pin This pin selects the resistors for adjusting V0 voltage level – INTRS = "H": use the internal resistors. – INTRS = "L": use the external resistors VR pin and external resistive divider control V0 voltage
T[0] ~ T[9]	O	Test pins Don' t use these pins. Please Open these pins.
TA	I	Test pin TA must connect to VDD.
Reserve	X	This pin must be OPEN
MODE	I	MODE = 0 : 129 com X 132 SEG MODE = 1 : 101 com X 160 SEG
MF[2:0]	I	Manufacturer ID code for reference, suggestion setting [MF2.MF1.MF0 = 0.0.0]
DS[1:0]	I	Display size ID code for reference, suggestion setting [DS1.DS0 = 1.0 or DS1.DS0 = 0.0]

MICROPROCESSOR INTERFACE

Microprocessor Interface Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RST</td><td>I</td><td>Reset input pin
When RESETB is “L”, initialization is executed.</td></tr>
<tr><td>PS[2:0]</td><td>I</td><td>Parallel / Serial data input select input
<table>
<tr><td>PS2</td><td>PS1</td><td>PS0</td><td>Interface mode</td><td>Data / Command</td><td>Data</td><td>Read/Write</td><td>Serial clock</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>Parallel 80</td><td>A0</td><td>DB0 to DB7</td><td>RD / WR</td><td>-</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>Parallel 68</td><td>A0</td><td>DB0 to DB7</td><td>E / RW</td><td>-</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>3Line Serial</td><td>-</td><td>SID (DB7)</td><td>Write only</td><td>SCLK (DB6)</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>4Line Serial</td><td>A0</td><td>SID (DB7)</td><td>Write only</td><td>SCLK (DB6)</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>IIC Serial</td><td>-</td><td>SDA</td><td>Read/Write</td><td>SCL</td></tr>
</table>
*NOTE: In 4-Line, 3-Line and IIC serial mode, it is impossible to read data from the on-chip RAM.
In 3-Line or 4-Line interface:
DB0 to DB5, E_RD and RW_WR must be fixed to “H” or “L”.
In IIC and 3-Line interface:
A0 must be fixed to “H” or “L”
Microprocessor interface select input pin
– PS[2:0]=001: 8080-series parallel MPU interface
– PS[2:0]=011: 68000-series parallel MPU interface
– PS[2:0]=000: 3-Line-SPI MPU interface
– PS[2:0]=010: 4-Line-SPI MPU interface
– PS[2:0]=100: IIC-SPI MPU interface</td></tr>
<tr><td>CSB</td><td>I</td><td>Chip select input pins
Data/instruction I/O is enabled only when CSB is "L". When chip select is non-active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>A0</td><td>I</td><td>Register select input pin
– A0 = "H": DB0 to DB7 are display data
– A0 = "L": DB0 to DB7 are control data</td></tr>
<tr><td>RW_WR</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><td>PS1</td><td>MPU type</td><td>RW_WR</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>RW</td><td>Read / Write control input pin
RW = “H” : read
RW = “L” : write</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WR</td><td>Write enable clock input pin
The data on DB0 to DB7 are latched at the rising edge of the /WR signal.</td></tr>
</table>
</td></tr>
</table>

Microprocessor Interface Pin Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>E_RD</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><td>PS1</td><td>MPU Type</td><td>E_RD</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read / Write control input pin
When RW = “H”: E is “H”, DB0 to DB7 are in an output status.
When RW = “L”: The data on DB0 to DB7 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is “L”, DB0 to DB7 are in an output status.</td></tr>
</table></td></tr>
<tr><td rowspan="3">DB0
to
DB7</td><td rowspan="3">I/O</td><td>8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus.
When chip select is not active (CSB=H), DB0 to DB7 may be high impedance.</td></tr>
<tr><td>When the 3-Line/4-Line serial interface selected (PS[2:0] = "000" or “010”);
– DB0 to DB5: high impedance
– DB6: serial input clock (SCLK)
– DB7: serial input data (SID)
When chip select is not active, D0 to D7 is high impedance.</td></tr>
<tr><td>When the IIC serial interface selected (PS[2:0] = "100");
D7: serial clock input (SCL)
D6 , D5 , D4: serial input data (SDA_IN)
D3, D2: (SDA_OUT) serial data acknowledge for the IIC interface. By connecting SDA_OUT to SDA_IN externally, the SDA line becomes fully IIC interface compatible. Having the acknowledge output separated from the serial data line is advantageous in chip on glass (COG) applications. In COG application where the track resistance from the SDA_OUT pad to the system SDA line can be significant, a potential divider is generated by the bus pull-up resistor and the ITO track resistance. It is possible during the acknowledge cycle the ST7528 will not be able to create a valid logic 0 level. By splitting the SDA_IN input from the SDA_OUT output the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDA_OUT pad to the system SDA line to guarantee a valid low level.
<u>D6, D5, ….D2 must be connected together (SDA)</u>
D1, D0: Is slave address (SA) bit1, 0, must connect to Vdd or Vss.
When chip select is not active, D0 to D7 is high impedance.</td></tr>
</table>

LCD DRIVER OUTPUTS

LCD Driver Output Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>SEG0
to
SEG159</td><td>O</td><td>LCD segment driver outputs
The display data and the M signal control the output voltage of segment driver.
<table>
<tr><td rowspan="2">Display data</td><td rowspan="2">M (Internal)</td><td colspan="2">Segment driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>VSS</td></tr>
<tr><td colspan="2">Power save mode</td><td>VSS</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COM0
to
COM127</td><td>O</td><td>LCD common driver outputs
The internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><td>Scan data</td><td>M (Internal)</td><td>Common driver output voltage</td></tr>
<tr><td>H</td><td>H</td><td>VSS</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
<tr><td colspan="2">Power save mode</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COMS
(COMS1)</td><td>O</td><td>Common output for the icons
The output signals of two pins are same. When not used, these pins should be left open.</td></tr>
</table>

ST7528 I/O PIN ITO Resister Limitation

PIN Name	ITO Resister
PS2,PS1,PS0,REF,OCS1,INTRS,Mode, TA	**No Limitation**
T0…9 , VR(No used) , VEXT(No used)	**Floating**
Vdd, Vdd2, Vss, Vss2, VOUT_IN , VOUT_OUT,	**<100Ω**
VR(used) , VEXT(used)	**<500Ω**
CSB , E , R/W , A0 , D0 …D7	**<1KΩ**
V1 , V2 , V3 , V4	**<500Ω**
RST	**<10KΩ**

In IIC interface: SDA , SCL ITO resister recommend to less than 100 ohm

FUNCTIONAL DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

There is CSB pin for chip selection. The ST7528 can interface with an MPU when CSB is "L". When these pins are set to any other combination, A0, E_RD, and RW_WR inputs are disabled and DB0 to DB7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel / Serial Interface

ST7528 has five types of interface with an MPU, which are three serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown in Table 1.

Table 1 Parallel / Serial Interface Mode

Type	PS2	PS1	PS0	CSB	Interface mode
Parallel	L	H	H	CSB	6800-series MPU mode
	L	L			8080-series MPU mode
Serial	L	L	L	CSB	3-Line SPI mode
	L	H	L	CSB	4-Line SPI mode
	H	L	L	CSB	IIC SPI mode

Parallel Interface (PS0 = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by PS1 as shown in Table 2. The type of data transfer is determined by signals at A0, E_RD and RW_WR as shown in Table 3.

Table 2 Microprocessor Selection for Parallel Interface

PS1	CSB	A0	E_RD	RW_WR	DB0 to DB7	MPU bus
H	CSB	A0	E	RW	DB0 to DB7	6800-series
L	CSB	A0	/RD	/WR	DB0 to DB7	8080-series

Table 3 Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	E_RD (E)	RW_WR (RW)	E_RD (/RD)	RW_WR (/WR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

NOTE: When E_RD pin is always pulled high for 6800-series interface, it can be used CSB for enable signal. In this case, interface data is latched at the rising edge of CSB and the type of data transfer is determined by signals at A0, RW_WR as in case of 6800-series mode.

Serial Interface

3-Line / 4-Line (PS[2:0] = "000" or “010”)

When the ST7528 is active (CSB=”L”), serial data (DB7) and serial clock (DB6) inputs are enabled. And not active, the internal 8-bit shift register and the 3-bit counter are reset. The display data/command indication may be controlled either via software or the Register Select (A0) Pin, based on the setting of PS1. When the A0 pin is used (PS1 = “H”), data is display data when A0 is high, and command data when A0 is low. When A0 is not used (PS1 =“L”), the LCD Driver will receive command from MCU by default. If messages on the data pin are data rather than command, MCU should send Data Direction command (11101000) to control the data direction and then one more command to define the number of data bytes will be write. After these two continuous commands are sent, the following messages will be data rather than command. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. And the DDRAM column address pointer will be increased by one automatically. The next bytes after the display data string is handled as command data.

In 3-Line mode, default message from MCU is command, the 2 bytes command of **Set Data Direction & Display Data Length** must be set before display data send from MCU, after the display data is sent over, the next message is turned to be command.

Serial mode	PS0	PS1	PS2	CSB	A0
3-Line SPI mode	L	L	L	CSB	No used
4-Line SPI mode	L	H	L	CSB	Used
IIC SPI mode	L	L	H	CSB	No Used

If A0 is not used it must be fixed either “H” or “L”

4-Line SPI Mode (PS0 = "L", PS1 = "H" , PS2 = "L")

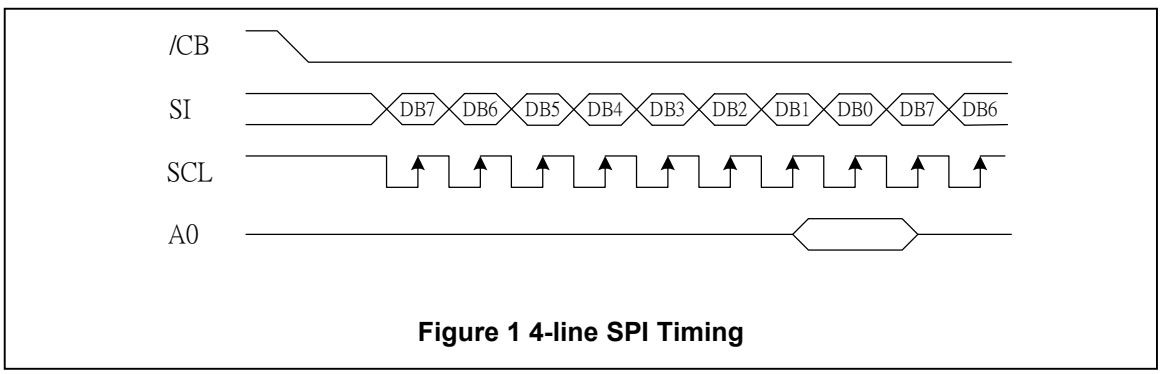
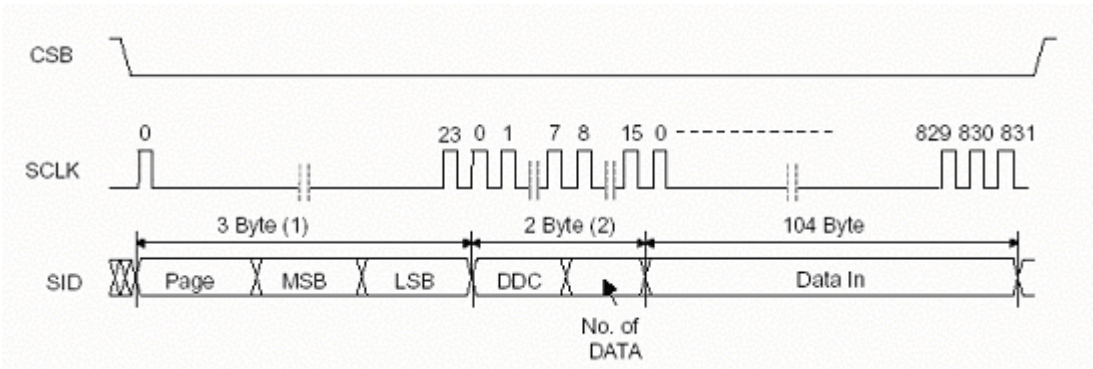


Figure 1 4-line SPI Timing

3-Line SPI Mode (PS0 = "L", PS1 = "L",PS2= "L")

To write data to the DDRAM, send Data Direction Command in 3-Line SPI mode. Data is latched at the rising edge of SCLK. And the DDRAM column address pointer will be increased by one automatically.



(1) Set Page and Column Address.

Set Page Address : 1 0 1 1 P3 P2 P1 P0

Set Column Address MSB : 0 0 0 1 0 Y7 Y6 Y5

Set Column Address LSB : 0 0 0 0 Y4 Y3 Y2 Y1

(2) Set DDC (Data Direction Command) and No. of Data Bytes.

Set Data Direction Command (For SPI mode Only):

1 1 1 0 1 0 0 0

Set No. of Data Bytes : D7 D6 D5 D4 D3 D2 D1 D0

(3) This figure is example for 104 Data bytes to be transferred.

Figure 2 3-pin SPI Timing (RS is not used)

This command is used in 3-Line SPI mode only. It will be two continuous commands, the first byte controls the data direction and informs the LCD driver the second byte will be number of data bytes will be write. After these two commands sending out, the following messages will be data. If data is stopped in transmitting, it is not valid data.

New data will be transferred serially with most significant bit first.

NOTE: In spite of transmission of data, if CSB is disabling, state terminates abnormally. Next state is initialized.

IIC Interface (PS0 = "L", PS1 = "L", PS2= "H")

The IIC interface receives and executes the commands sent via the IIC Interface. It also receives RAM data and sends it to the RAM.

The IIC Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Figure 3.

START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Figure 4.

SYSTEM CONFIGURATION

The system configuration is illustrated in Figure 5.

· Transmitter: the device, which sends the data to the bus.

· Receiver: the device, which receives the data from the bus.

· Master: the device, which initiates a transfer, generates clock signals and terminates a transfer.

· Slave: the device addressed by a master.

· Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.

· Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.

· Synchronization: procedure to synchronize the clock signals of two or more devices.

ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the IIC Interface is illustrated in Figure 5.

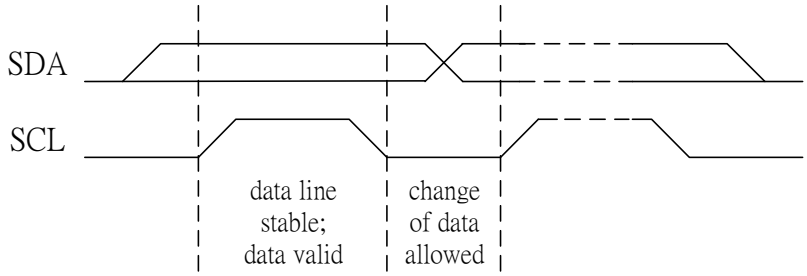


Figure 3 Bit transfer

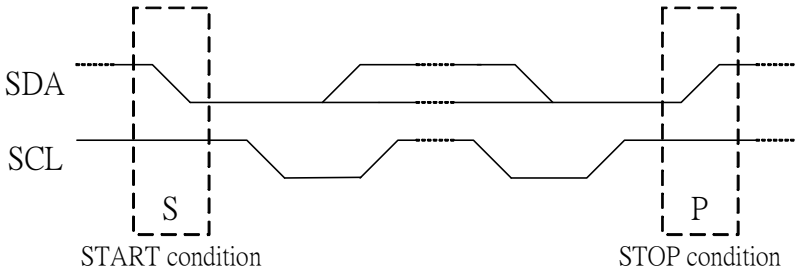


Figure 4 Definition of START and STOP conditions

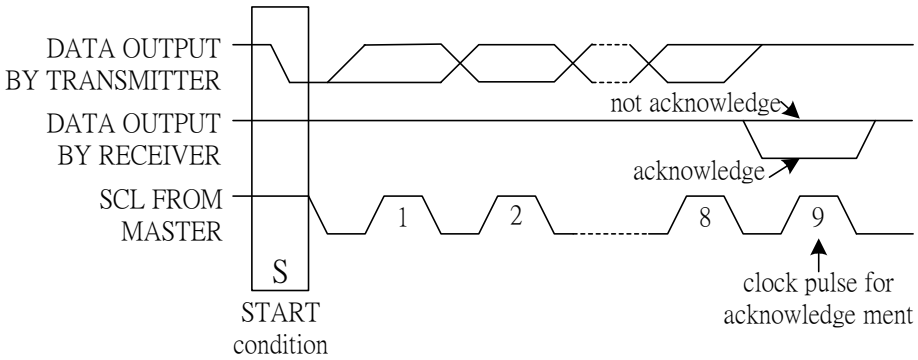


Figure 5 Acknowledgement on the 2-line Interface

IIC Interface protocol

The ST7528 supports command, data write addressed slaves on the bus.

Before any data is transmitted on the IIC Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111100, 0111101, 0111110 and 0111111) are reserved for the ST7528. The least significant bit of the slave address is set by connecting the input SA0 and SA1 to either logic 0 (VSS) or logic 1 (VDD).

The IIC Interface protocol is illustrated in Figure 6.

Note: ST7528 IIC interface can not use with other slaver IIC device

The sequence is initiated with a START condition (S) from the IIC Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the IIC Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.

A command word consists of a control byte, which defines Co and A0, plus a data byte.

The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the A0 bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the A0 bit setting; either a series of display data bytes or command data bytes may follow. If the A0 bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended ST7528 device. If the A0 bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the IIC INTERFACE-bus master issues a STOP condition (P).If the R/W bit is set to logic 1 the chip will output data immediately after the slave address if the A0 bit, which was sent during the last write access, is set to logic 0. If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

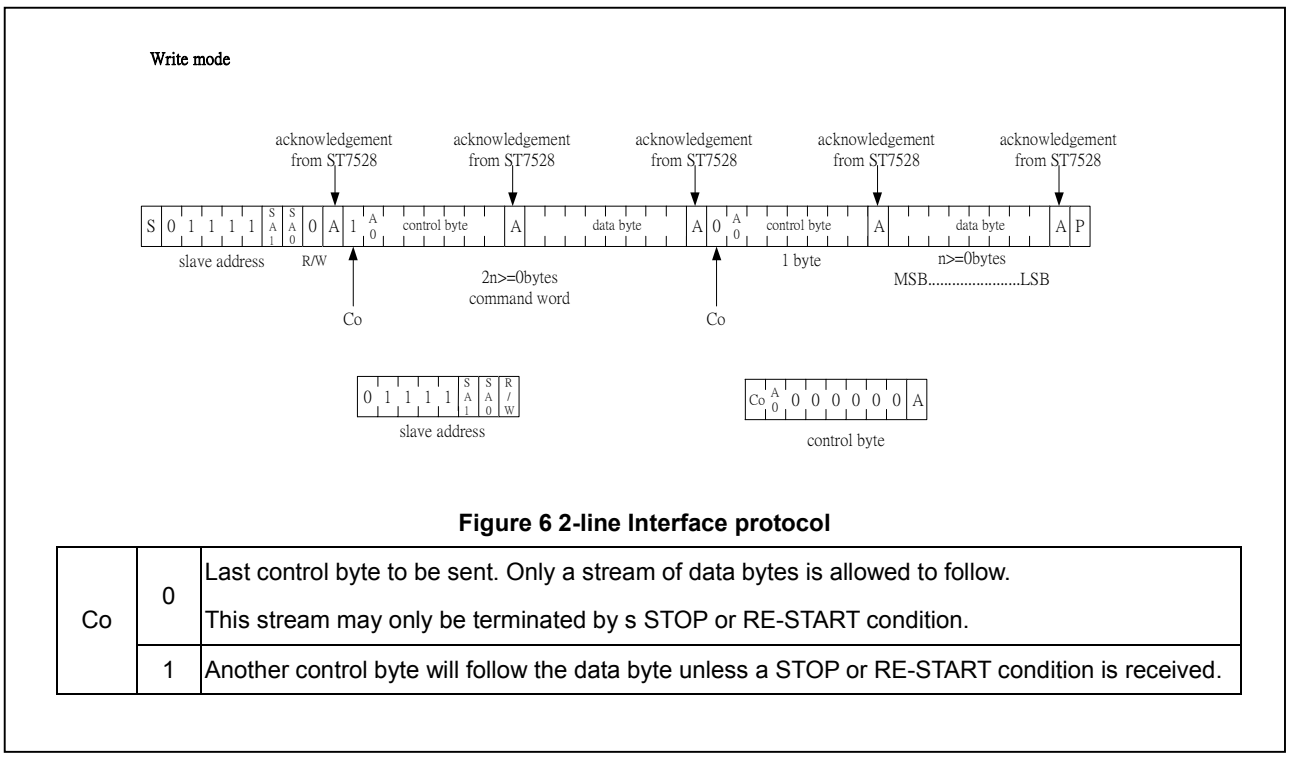


Figure 6 2-line Interface protocol

Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by s STOP or RE-START condition.
	1	Another control byte will follow the data byte unless a STOP or RE-START condition is received.

Busy Flag

The Busy Flag indicates whether the ST7528 is operating or not. When DB7 is "H" in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

Data Transfer

The ST7528 uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in Figure 7. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in Figure 8. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

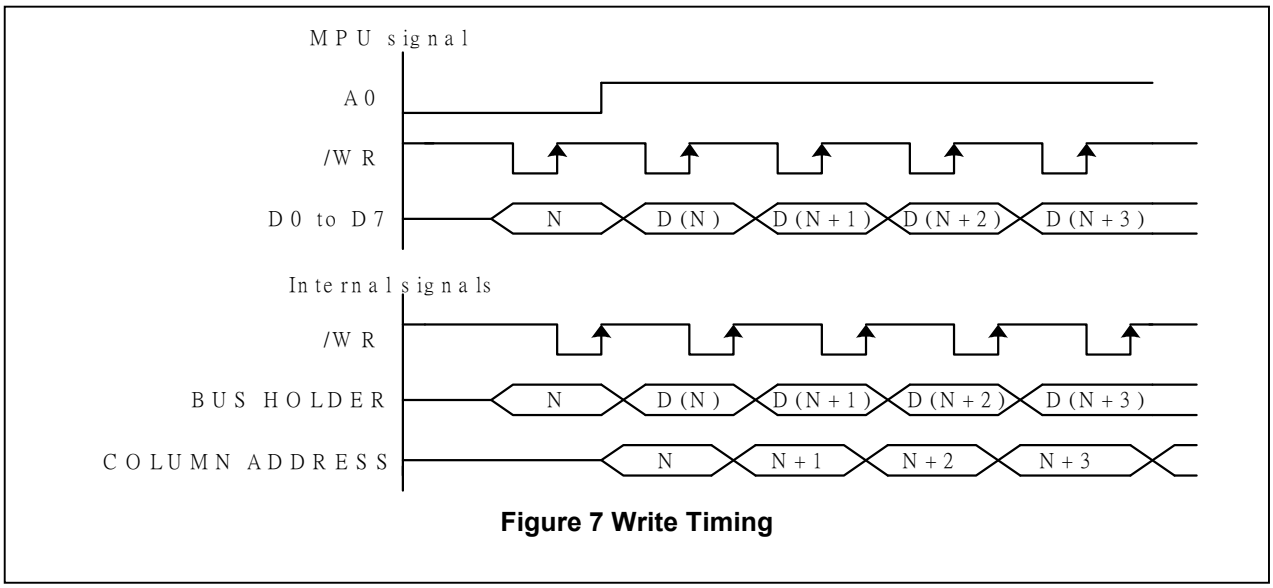


Figure 7 Write Timing

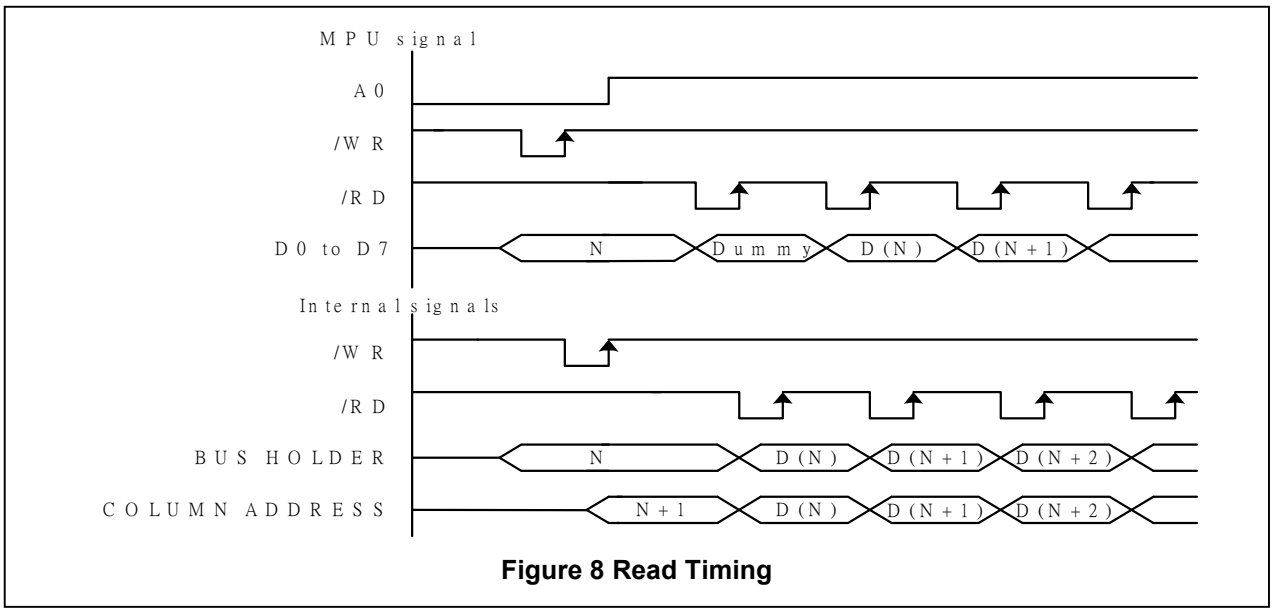


Figure 8 Read Timing

DISPLAY DATA RAM (DDRAM)

When Mode 0 is selected

The Display Data RAM stores pixel data for the LCD. It is 129-row (17 pages by 8 bits) by 132-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 129 rows are divided into 16 pages of 8 lines and the 17th page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

When Mode 1 is selected

The Display Data RAM stores pixel data for the LCD. It is 101-row (13 pages by 8 bits) by 160-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 101 rows are divided into 12 pages of 8 lines and the 13th page with 4 lines; the Page Address 16 (17th page) is for Icon page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

Page Address Circuit

In mode 0

It incorporates 4-bit Page Address register changed by only the “Set Page” instruction. Page Address 16 is a special RAM area for the icons and display data DB0 is only valid. The page address is set from 0 to 15, and Page 16 is for Icon page.

In mode 1

It incorporates 4-bit Page Address register changed by only the “Set Page” instruction. Page Address 16 is a special RAM area for the icons and display data DB0 is only valid. The page address is set from 0 to 12, and Page 16 is for Icon page.

Line Address Circuit

In mode 0

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting Line Address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM. It incorporates 7-bit Line Address register changed by only the initial display line instruction and 7-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the line address for transferring the 128-bit RAM data to the display data latch circuit. When icon is enabled by setting icon control register, display data of icons are not scrolled because the MPU can not access Line Address of icons.

In mode 1

The 7-bit Line Address register is set from 0 ~ 99, If the register is set from 100 ~ 127, It will be no operation. The register value will be kept in last value.

Column Address Circuit

In Mode 0, 1

Column Address Circuit has a 10-bit preset counter that provides Column Address to the Display Data RAM. When set Column Address MSB / LSB instruction is issued, 8-bit [Y9:Y2] are set and lowest 2 bit, Y[1:0] is set to “00”. Since this address is increased by 1 each a read or write data instruction, microprocessor can access the display data continuously. However, the counter is not increased and locked if a non-existing address above 9FH. It is unlocked if a column address is set again by set Column Address MSB / LSB instruction. And the column address counter is independent of page address register.

ADC select instruction makes it possible to invert the relationship between the Column Address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing ADC select instruction. Refer to the following Figure 9 and Figure 10.

(Note: in mode read or write in fourth, the column address will turn to next column address)

MODE 0

SEG output	SEG 0	SEG 1	SEG 2	SEG 3	…	SEG 128	SEG 129	SEG 130	SEG 131
Column address [Y9:Y2]	00H	01H	02H	03H	…	80H	81H	82H	83H
Internal column address [Y9:Y0]	00 01 02 03	04 05 06 07	08 09 0A 0B	0C 0D 0E 0F	…	200 201 202 203	204 205 206 207	208 209 20A 20B	20C 20D 20E 20F
Display data (ADC=0)	1 1 1 1	1 1 1 0	1 1 0 1	1 1 0 0	…	0 0 1 1	0 0 1 0	0 0 0 1	0 0 0 0
LCD panel display					…				
Display data (ADC=1)	0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	…	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1
LCD panel display					…				

Figure 9. The Relationship between the Column Address and the Segment Outputs

MODE 1

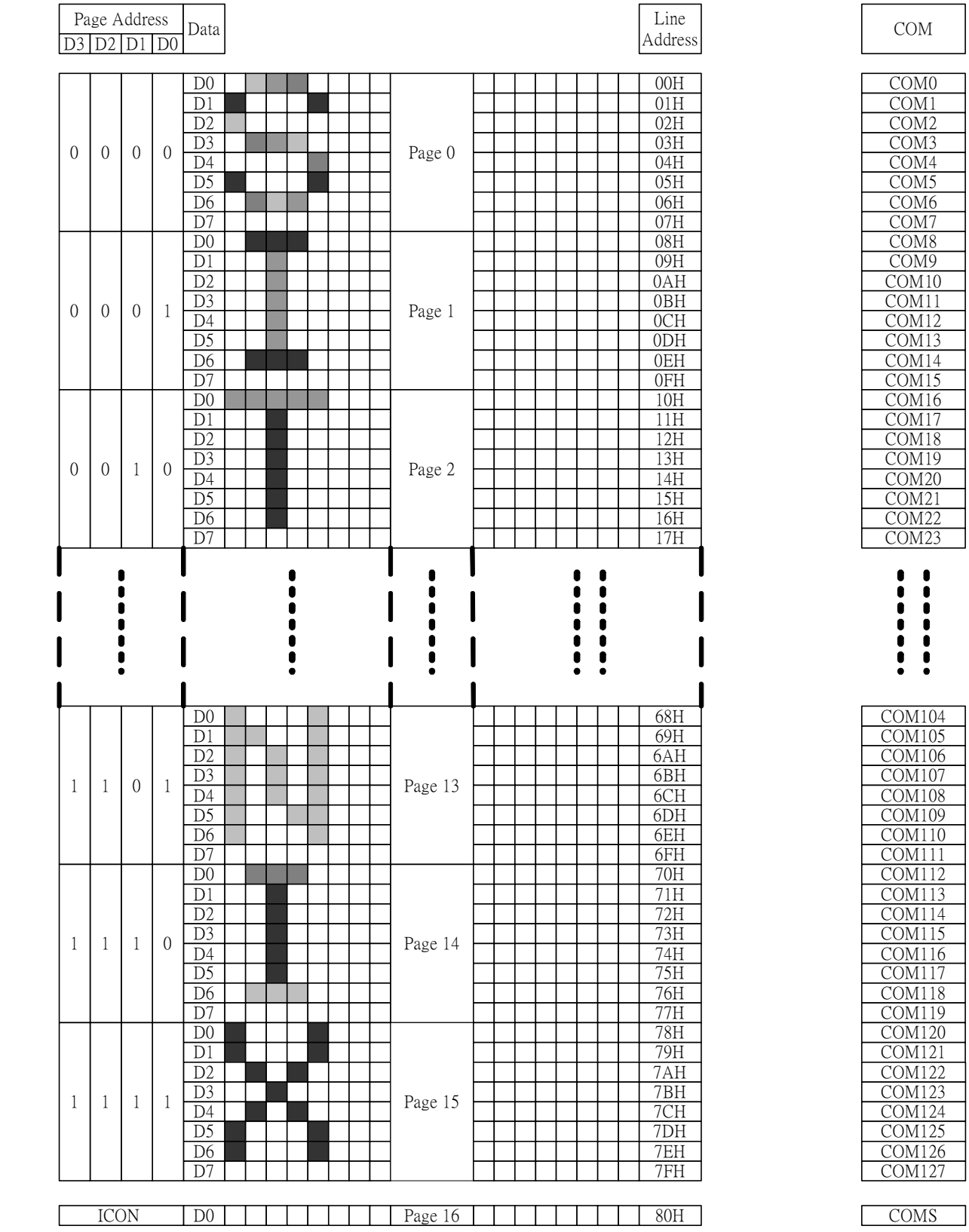
SEG output	SEG 0				SEG 1				SEG 2				SEG 3				…	SEG 156				SEG 157				SEG 158				SEG 159			
Column address [Y9:Y2]	00H				01H				02H				03H				…	9CH				9DH				9EH				9FH			
Internal column address [Y9:Y0]	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	…	270	271	272	273	274	275	276	277	278	279	27A	27B	27C	27D	27E	27F
Display data (ADC=0)	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0	…	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
LCD panel display																	…																
Display data (ADC=1)	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	…	1	1	0	0	1	1	0	1	1	1	1	0	1	1	1	1
LCD panel display																	…																

Figure 10. The Relationship between the Column Address and the Segment Outputs

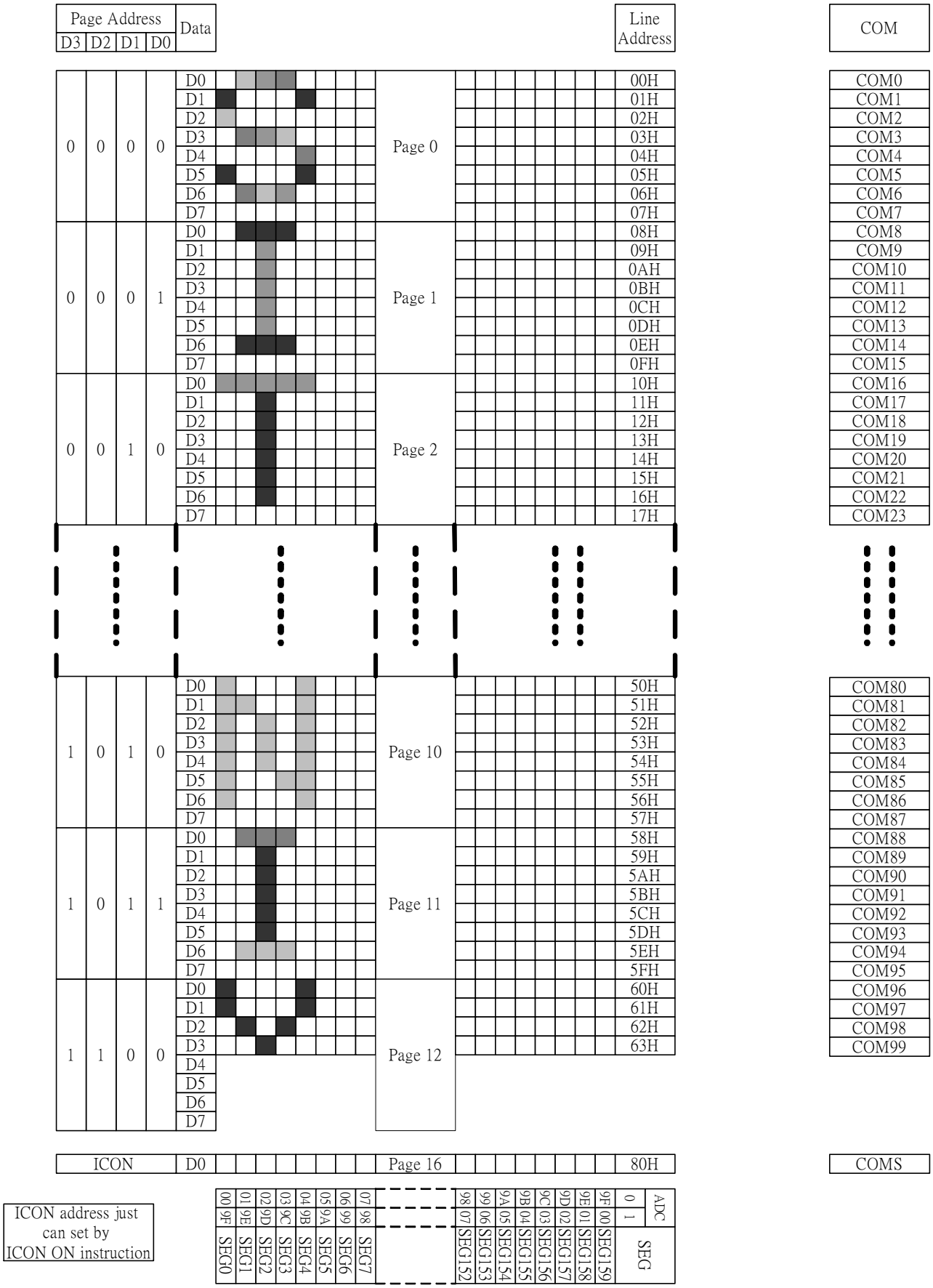
Segment Control Circuit

This circuit controls the display data by the display ON / OFF, reverse display ON / OFF and entire display ON / OFF instructions without changing the data in the display data RAM.

ST7528 Mode-0 Display RAM Mapping diagram



ST7528 Mode-1 Display RAM Mapping diagram



LCD DISPLAY CIRCUITS

FRC (Frame Rate Control) and PWM (Pulse Width Modulation) Function Circuit

The ST7528 incorporates an FRC function and a PWM function circuit to display a 16-level gray scale. The FRC function and PWM utilize liquid crystal characteristics whose transmittance is changed by an effective value of applied voltage. The ST7528 provides palette-registers to assign the desired gray level. These registers are set by the instructions and the RESETB.

ST7528-- 4FRC & 3FRC / 45PWM, 60PWM

– **Gray Scale Table of 4 FRC (Frame Rate Control)**

4 FRC setting	**(DB7 to DB0)**
1st FR (FR1)	Set 1st Frame Pulse Width Modulation Instruction
1st FR (FR1)	Set 1st Frame Pulse Width Modulation Data
2nd FR (FR2)	Set 2nd Frame Pulse Width Modulation Instruction
2nd FR (FR2)	Set 2nd Frame Pulse Width Modulation Data
3rd FR (FR3)	Set 3rd Frame Pulse Width Modulation Instruction
3rd FR (FR3)	Set 3rd Frame Pulse Width Modulation Data
4th FR (FR4)	Set 4th Frame Pulse Width Modulation Instruction
4th FR (FR4)	Set 4th Frame Pulse Width Modulation Data

– **Gray Scale Table of 3 FRC (Frame Rate Control)**

3 FRC setting	**(DB7 to DB0)**
1st FR (FR1)	Set 1st Frame Pulse Width Modulation Instruction
1st FR (FR1)	Set 1st Frame Pulse Width Modulation Data
2nd FR (FR2)	Set 2nd Frame Pulse Width Modulation Instruction
2nd FR (FR2)	Set 2nd Frame Pulse Width Modulation Data
3rd FR (FR3)	Set 3rd Frame Pulse Width Modulation Instruction
3rd FR (FR3)	Set 3rd Frame Pulse Width Modulation Data
4th FR (FR4)	No used
4th FR (FR4)	No used

-Gray Scale Table of 45 PWM (Pulse Width Modulation)

Dec	Hex	6-bits	PWM (on width)	Note
0	00	000000	0(0/45)	Brighter
1	01	000001	1/45	
2	02	000010	2/45	
3	03	000011	3/45	
4	04	000100	4/45	
…	…	…	…	
…	…	…	…	
…	…	…	…	
…	…	…	…	
42	2A	101010	42/45	
43	2B	101011	43/45	
44	2C	101100	44/45	
45	2D	101101	1(45/45)	Darker
…	…	…	…	This area is selected to OFF level (0/45 level)
…	…	…	…	
61	3D	111101	0/45	
62	3E	111110	0/45	
63	3F	111111	0/45	

-Gray Scale Table of 60 PWM (Pulse Width Modulation)

Dec	Hex	6-bits	PWM (on width)	**Note**
0	00	000000	0(0/60)	Brighter
1	01	000001	1/60	
2	02	000010	2/60	
3	03	000011	3/60	
4	04	000100	4/60	
…	…	…	…	
…	…	…	…	
…	…	…	…	
…	…	…	…	
…	…	…	…	
…	…	…	…	
56	39	111001	56/60	
57	3A	111010	57/60	
58	3B	111011	58/60	
59	3C	111100	59/60	
60	39	111001	1 (60/60)	Darker
61	3D	111101	0/60	This area is selected to OFF level (0/60 level)
62	3E	111110	0/60	
63	3F	111111	0/60	

Oscillator

This is on-chip Oscillator without external resistor. When the internal oscillator is used, this pin must connect to VDD; when the external oscillator is used, this pin could be input pin. This oscillator signal is used in the voltage converter and display timing generation circuit.

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL (internal), generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the128-bit display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M) which enables the LCD driver to make an AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Figure 11.

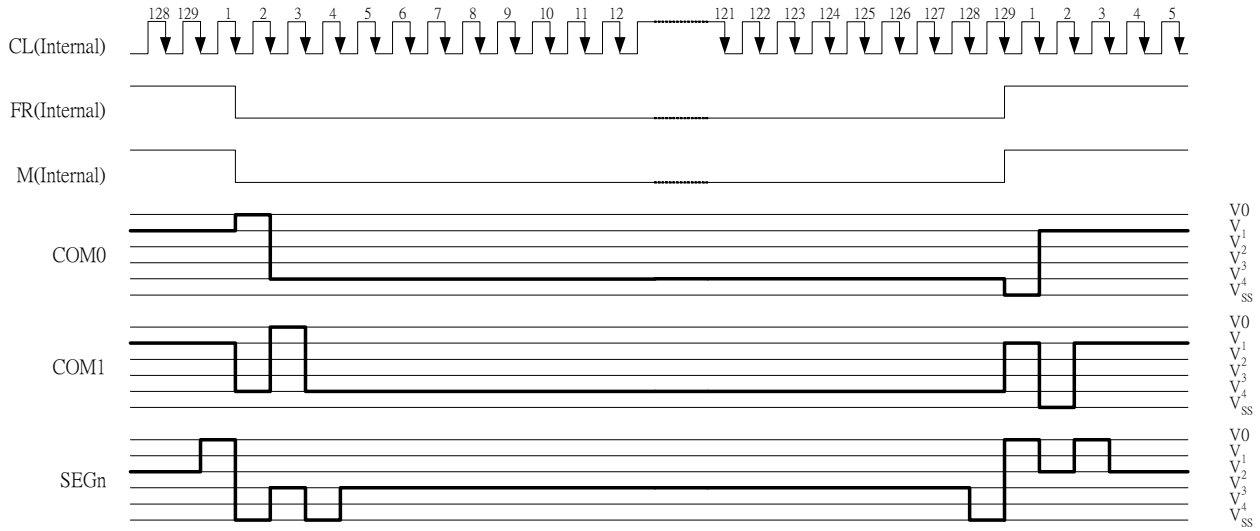


Figure 11 2-frame AC Driving Waveform (Duty Ratio: 1/129 in mode-0)

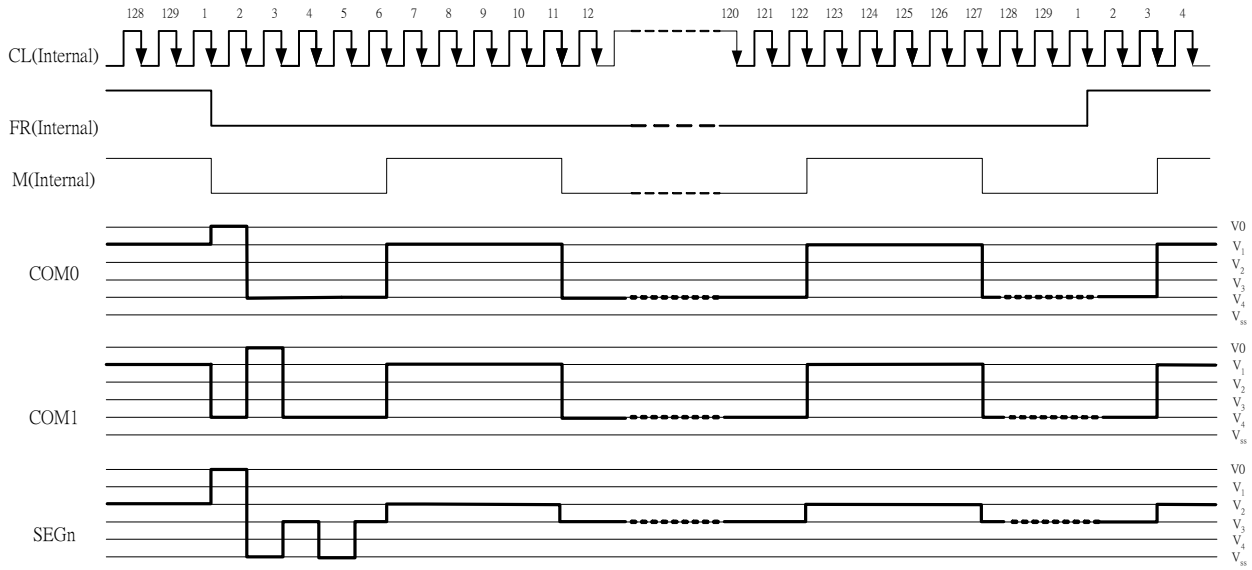
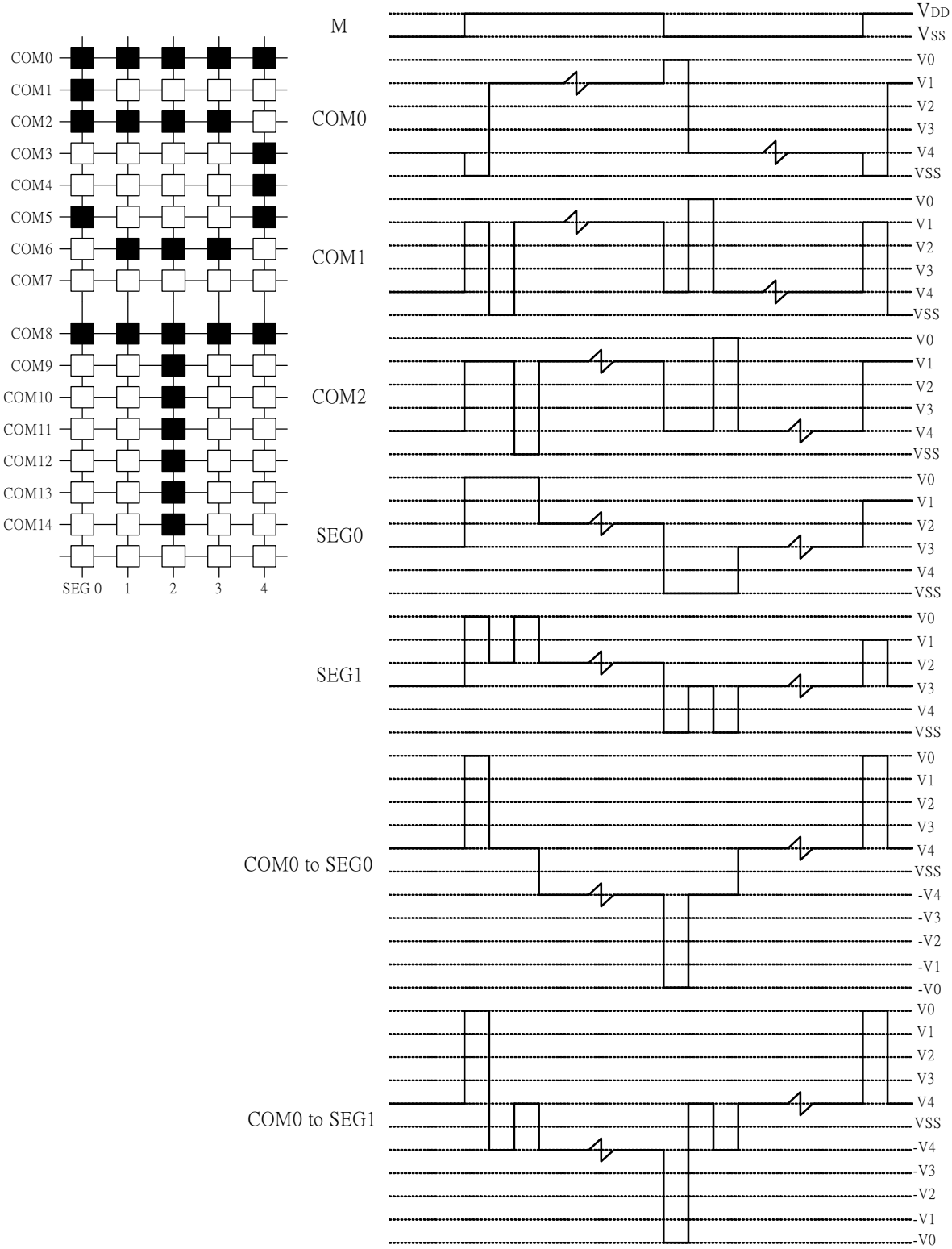


Figure 12 N-Line Inversion Driving Waveform (N=5, Duty Ratio=1/129 in mode-0)

LCD DRIVER CIRCUIT

This driver circuit is configured by 129-channel common drivers and 160-channel segment drivers. This LCD panel driver voltage depends on the combination of display data and M signal.



Partial Display on LCD

The ST7528 realizes the Partial Display function on LCD with low-ratio driving for saving power consumption and showing the various display ratio. To show the various display ratio on LCD, LCD driving ratio and bias are programmable via the instruction. And, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages.

In mode 0 the partial display ratio could be set from 16 ~ 128.

In mode 1 could be set from 16 ~ 100.

If the partial display region is out of the Max. Display range, it would be no operation.

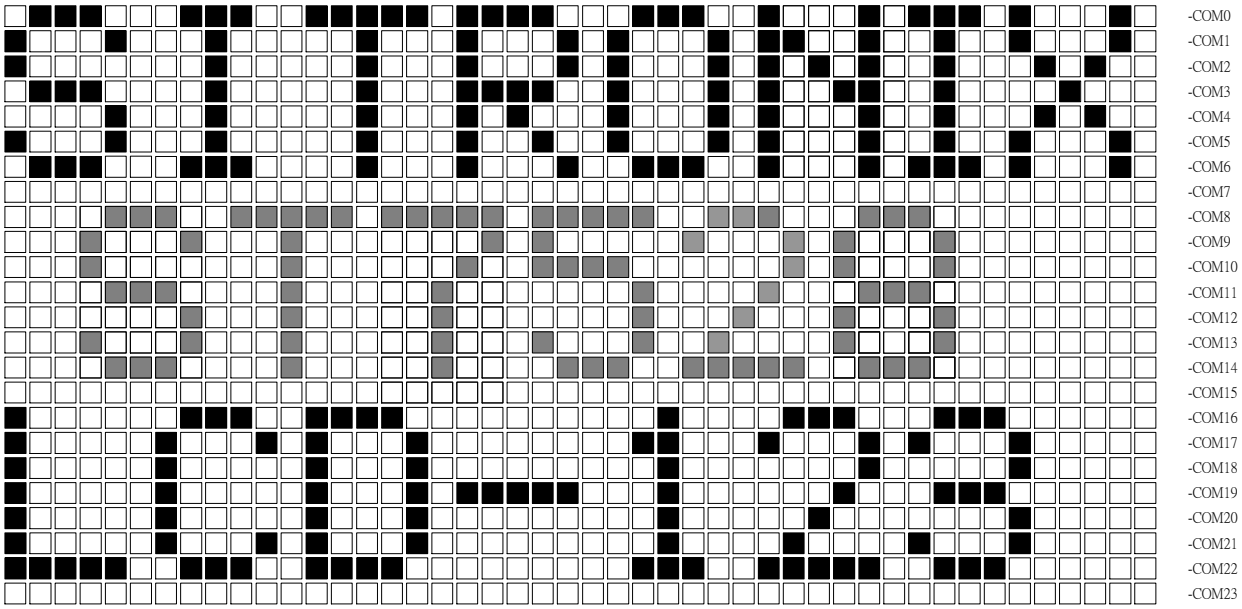


Figure 13 Reference Example for Partial Display

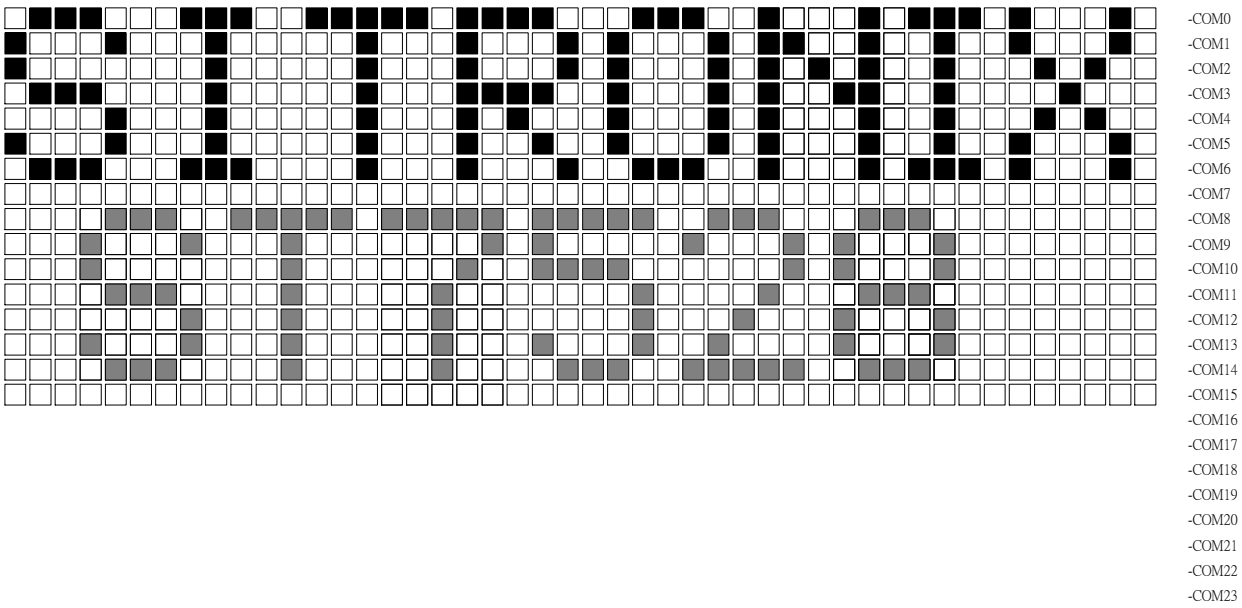


Figure 14 Partial Display (Partial Display ratio=16,initial COM0=0)

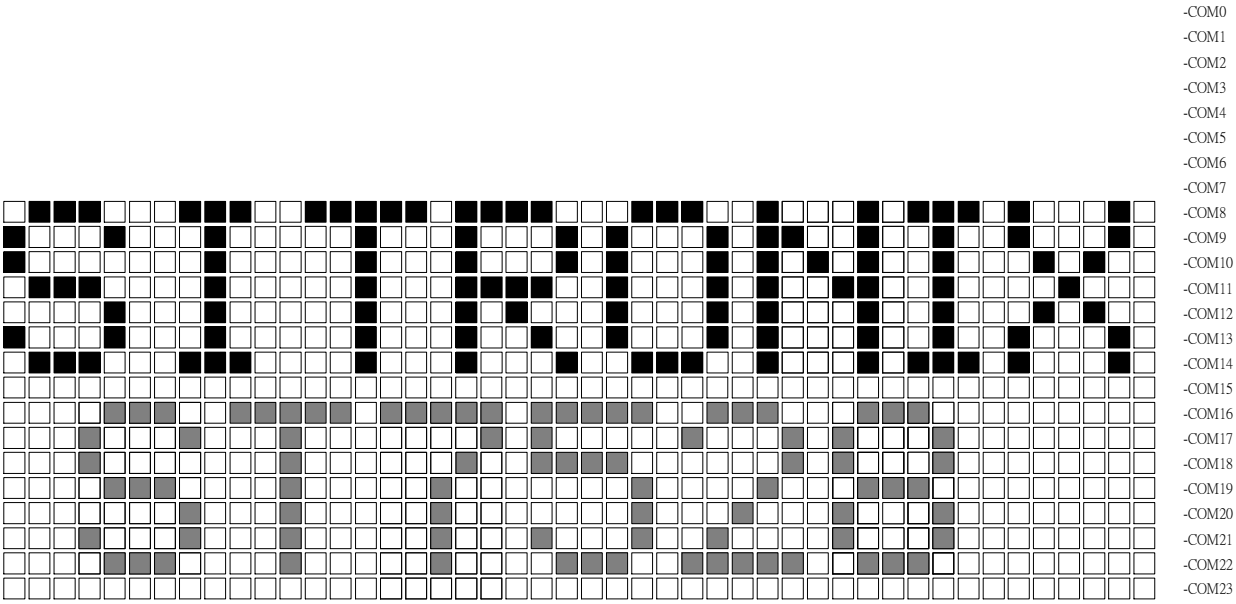


Figure 15 Moving Display (Partial Display ratio=16,Initial COM0=8)

POWER SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction. For details, refers to "Instruction Description". Table 4 shows the referenced combinations in using Power Supply circuits.

Table 4 Recommended Power Supply Combinations

User setup	Power control (VC VR VF)	V/C circuits	V/R circuits	V/F circuits	VOUT_IN	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	ON	ON	ON	Internal	Without capacitor	With capacitor
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	OFF	ON	ON	External input	Without capacitor	With capacitor
Only the voltage follower circuits are used	0 0 1	OFF	OFF	ON	OPEN	External input	With capacitor
Only the external power supply circuits are used	0 0 0	OFF	OFF	OFF	OPEN	External input	External input

Voltage Converter Circuits

These circuits boost up the electric potential between VDD2 and Vss to 3, 4, 5 or 6 times toward positive side and boosted voltage is outputted from VOUT pin. It is possible to select the lower boosting level in any boosting circuit by “Set DC-DC Step-up” instruction. When the higher level is selected by instruction, VOUT voltage is not valid.

Note: we would like to recommend to use the external VOUT when the panel is large than 1.8 inch

Voltage Regulator Circuits

The function of the internal Voltage Regulator circuits is to determine liquid crystal operating voltage, V0, by adjusting resistors, Ra and Rb, within the range of |V0| < |VOUT|. Because VOUT is the operating voltage of operational-amplifier circuits shown in Figure 16, it is necessary to be applied internally or externally.

For the Eq. 1, we determine V0 by Ra, Rb and VEV. The Ra and Rb are connected internally or externally by INTRS pin. And VEV called the voltage of electronic volume is determined by Eq. 2, where the parameter α is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 63. VREF voltage at Ta= 25°C is shown in Table 5.

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times VEV\ [V] \quad \text{------ (Eq. 1)}$$

$$VEV = \left(1 - \frac{(63 - \alpha)}{210}\right) \times VREF\ [V] \quad \text{------ (Eq. 2)}$$

Table 5 VREF Voltage at Ta = 25°C

REF	Temp. coefficient	VREF [V]
1	-0.125% / °C	2.1
0	External input	VEXT

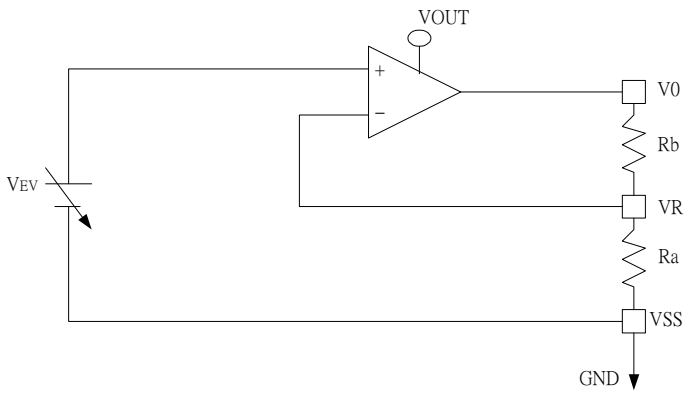


Figure 16 Internal Voltage Regulator Circuit

In Case of Using Internal Resistors, Ra and Rb (INTRS = "H")

When INTRS pin is **"H"**, resistor Ra is connected internally between VR pin and VSS, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

Table 6 Internal Rb / Ra Ratio depending on 3-bit Data (R2 R1 R0)

	3-bit data settings (R2 R1 R0)							
	0 0 0	**0 0 1**	**0 1 0**	**0 1 1**	**1 0 0**	**1 0 1**	**1 1 0**	**1 1 1**
1 + (Rb / Ra)	2.3	3.0	3.7	4.4	5.1	5.8	6.5	7.2

Figure 17 shows V0 voltage measured by adjusting internal regulator register ratio (Rb / Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25 °C.

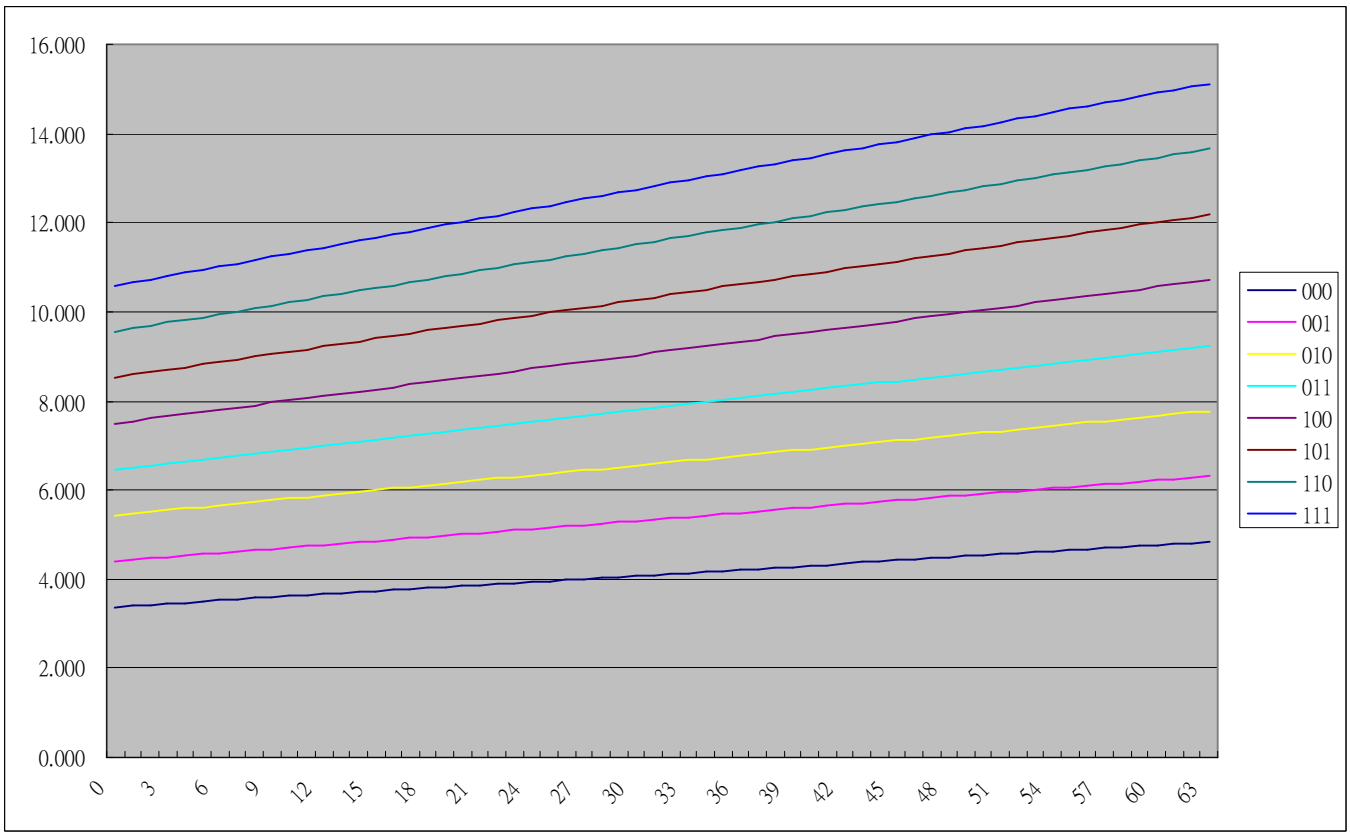


Figure 17 Electronic volume register (0 to 63)

In Case of Using External Resistors, Ra and Rb (INTRS = "L")

When INTRS pin is "L", it is necessary to connect external regulator resistor Ra between VR and VSS, and Rb between V0 and VR.

Example: For the following requirements

1. LCD driver voltage, V0 = 10V

2. 6-bit reference voltage register = (1, 0, 0, 0, 0, 0)

3. Maximum current flowing Ra, Rb = 1 uA

From Eq. 1

$$10 = \left(1 + \frac{Rb}{Ra}\right) \times VEV\ [V] \text{ ------ (Eq. 3)}$$

From Eq. 1

$$VEV = \left(1 - \frac{(63 - 32)}{210}\right) \times 2.1 = 1.79\ [V] \text{ ------ (Eq. 4)}$$

From requirement 3.

$$\frac{10}{Ra + Rb} = 1\ [uA] \text{ ------ (Eq. 5)}$$

From equations Eq. 3, 4 and 5

Ra = 1.79 [MΩ]

Rb = 8.21 [MΩ]

Table 7 Shows the Range of V0 depending on the above Requirements.

Table 7 The Range of V0

	Electronic volume level				
	0	**.....**	**32**	**.....**	**63**
V0	8.21	.....	10.00	.....	11.73

Voltage Follower Circuits

VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3 and V4), and those output impedance are converted by the Voltage Follower for increasing drive capability. Table 8 shows the relationship between V1 to V4 level and each duty ratio.

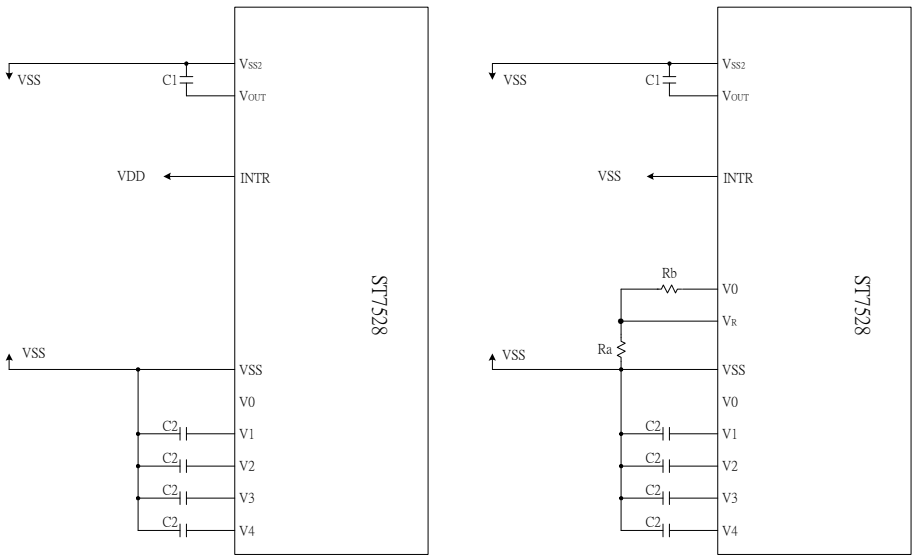
Table 8 The Relationship between V1 to V4 Level and Each Duty Ratio

LCD bias	**V1**	**V2**	**V3**	**V4**	**Remarks**
1/N	(N-1)/N x V0	(N-2)/N x V0	2/N x V0	1/N x V0	N = 5 to 12

Bias Power Save circuit:

When we set the Instruction of Bias Power Save, the bias also could be working, and the IC current consumption will be lower about 100uA to 200uA (according to the panel loading)

Follower voltage reference circuit (Internal Booster & Regulator)

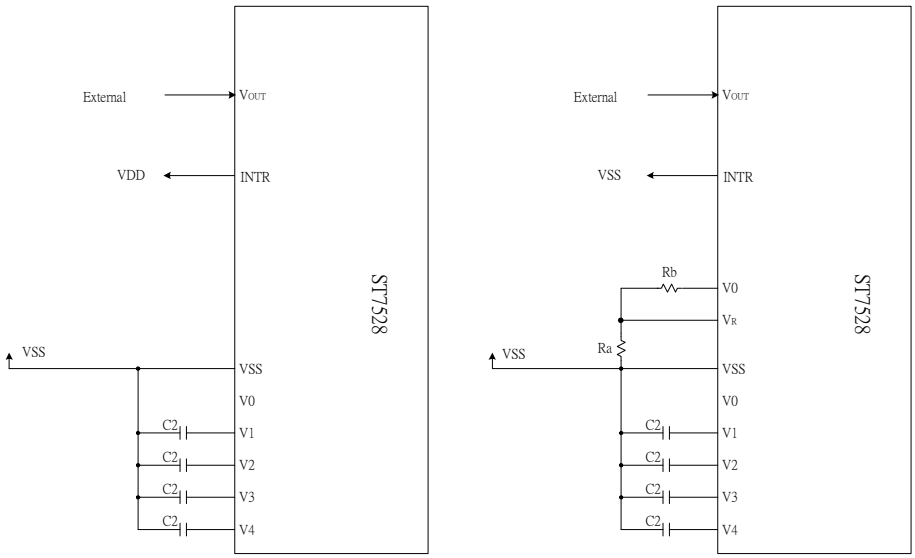


Left is using internal Resister

Right is using External Resister

C1= 1u F ~ 4.7u F, C2 = 0.1u F ~ 1u F (suggestion value: C1=1uF, C2=0.1uF)

Follower voltage reference circuit (External Vout & Internal Regulator)



Left is using internal Resister

Right is using External Resister

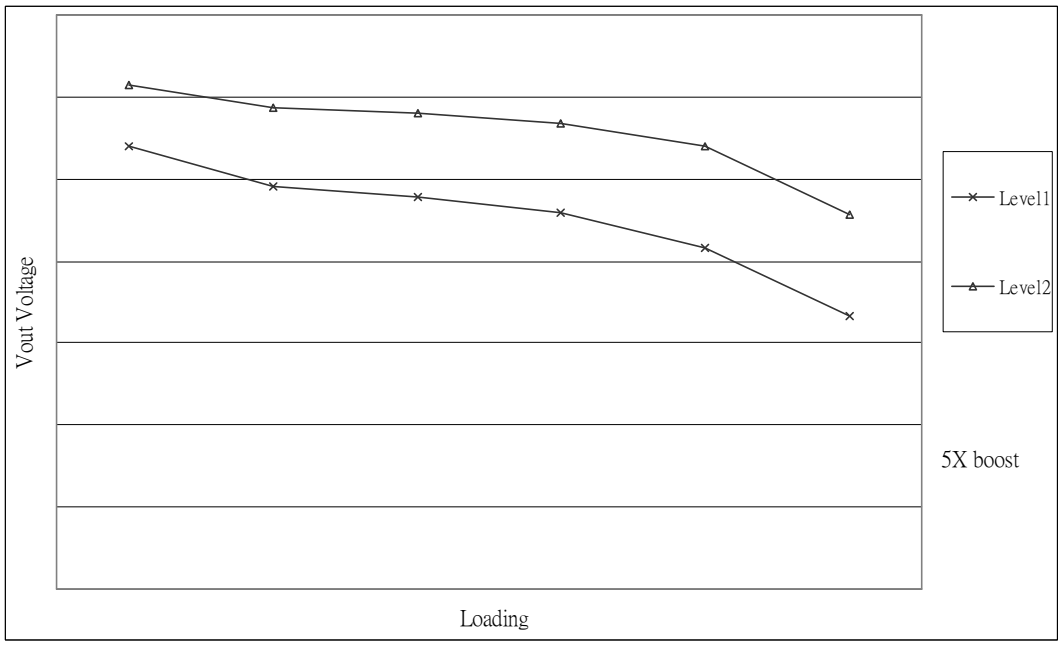
C1= 1u F ~ 4.7u F, C2 = 0.1u F ~ 1u F (suggestion value: C1=1uF , C2=0.1uF)

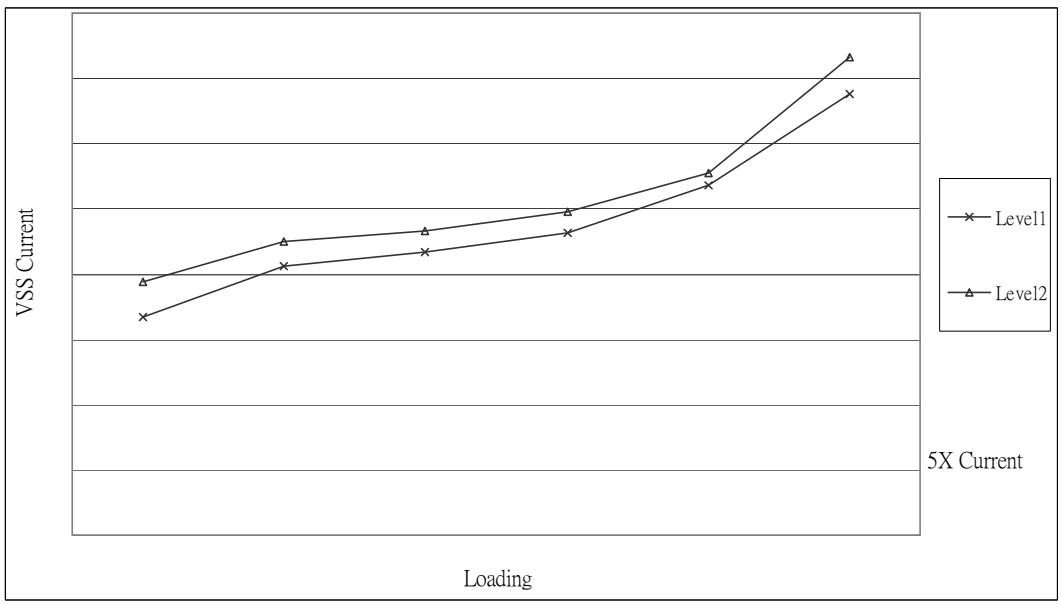
Booster Efficiency

By Booster Stages (3X, 4X, 5X, 6X) and Booster Efficiency (Level1~2) commands, we could easily set the best Booster performance with suitable current consumption. If the Booster Efficiency is set to higher level (level2 is higher than level1), The Boost Efficiency is better than lower level, and it just need few more power consumption current. It could be applied to each multiple voltage Condition.

When the LCD Panel loading is heavier, then the Performance of Booster will be not in a good working condition. We could set the BE level to be higher. We do not need to change to higher Booster Stage, and just need few more current.

The Booster Efficiency Command could be used together with Booster Stage Command to choose one best Boost output condition. We could see the Boost Stage Command as a large scale operation, and see the Booster Efficiency Command as a small scale operation. These commands are very convenient for using.





RESET CIRCUIT

Setting RESETB to “L” or Reset instruction can initialize internal function.
When RESETB becomes “L”, following procedure is occurred.
Page address: 0
Column address: 0
Read-modify-write: OFF
Display ON / OFF: OFF
Initial display line: 0 (first)
Initial COM0 register: 0 (COM0)
Partial display ratio: 1/128
Reverse display ON / OFF: OFF (normal)
N-line inversion register: 0 (disable)
Entire Display ON/OFF: OFF
ICON Control register ON/OFF: OFF (ICON disable)
Power control register (VC, VR, VF) = (0, 0, 0)
DC-DC converter circuit = (0, 0)
Booster Efficiency BE = (1)
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
Contrast Level: 32
LCD bias ratio: 1/12
COM Scan Direction: 0
ADC Select: 0
Oscillator: OFF
Power Save Mode: Release
Display Data Length register: 0 (for SPI mode)
All Gray Level Set : OFF
In Level0, 2, 4, 6, 8, 10, 12, 14 , the Gray Level palette register (GA5, GA4, GA3, GA2, GA1, GA0) = (0,0,0,0,0)
All Gray Level Set : OFF
In Level1, 3, 5, 7, 9, 11, 13, 15, the Gray Level palette register (GA5, GA4, GA3, GA2, GA1, GA0) = (1,1,1,1,1)
FRC, PWM mode: 4FRC, 45PWM

When RESET instruction is issued, following procedure is occurred.
Page address: 0
Column address: 0
Read-modify-write: OFF
Initial display line: 0 (First)
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
Contrast Level: 32
Display Data Length register: 0 (for SPI mode)
All Gray Level Set : OFF
In Level0, 2, 4, 6, 8, 10, 12, 14 , the Gray Level palette register (GA5, GA4, GA3, GA2, GA1, GA0) = (0,0,0,0,0)
All Gray Level Set : OFF
In Level1, 3, 5, 7, 9, 11, 13, 15, the Gray Level palette register (GA5, GA4, GA3, GA2, GA1, GA0) = (1,1,1,1,1)
FRC, PWM mode: 4FRC, 45PWM
While RESETB is “L” or reset instruction is executed, no instruction except read status can be accepted. Reset status appears at DB4. After DB4 becomes ”L”, any instruction can be accepted. RESETB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESETB is essential before used.

Instruction	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
EXT=0 or 1											
Mode Set	0	0	0	0	1	1	1	0	0	0	2-byte instruction to set Mode and FR(Frame frequency control) BE(Booster efficiency control)
	0	0	FR3	FR2	FR1	FR0	0	BE	x'	EXT	
EXT=0											
Read display data	1	1	Read data								Read data into DDRAM
Write display data	1	0	Write data								Write data into DDRAM
Read status	0	1	BUSY	ON	RES	MF2	MF1	MF0	DS1	DS0	Read the internal status
ICON control register ON/OFF	0	0	1	0	1	0	0	0	1	ICON	ICON=0: ICON disable(default) ICON=1: ICON enable & set the page address to 16
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	Y9	Y8	Y7	Y6	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y5	Y4	Y3	Y2	Set column address LSB
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	release modify-read mode
Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=0: Display OFF D=1: Display ON
Set initial display line register	0	0	0	1	0	0	0	0	x'	x'	2-byte instruction to specify the initial display line to realize vertical scrolling
	0	0	x'	S6	S5	S4	S3	S2	S1	S0	
Set initial COM0 register	0	0	0	1	0	0	0	1	x'	x'	2-byte instruction to specify the initial COM0 to realize window scrolling
	0	0	x'	C6	C5	C4	C3	C2	C1	C0	
Select partial display line	0	0	0	1	0	0	1	0	x'	x'	2-byte instruction to set partial display ratio
	0	0	D7	D6	D5	D4	D3	D2	D1	D0	
Set N-line inversion	0	0	0	1	0	0	1	1	x'	x'	2-byte instruction to set N-line inversion register
	0	0	x'	x'	x'	N4	N3	N2	N1	N0	
Release N-line inversion	0	0	1	1	1	0	0	1	0	0	Release N-line inversion mode
Reverse display ON/OFF	0	0	1	0	1	0	0	1	1	REV	REV=0: normal display REV=1: reverse display
Entire display ON/OFF	0	0	1	0	1	0	0	1	0	EON	EON=0: normal display EON=1: entire display ON

Instruction	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Ext=0											
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Select DC-DC step-up	0	0	0	1	1	0	0	1	DC1	DC0	Select the step-up of internal voltage converter
Select regulator register	0	0	0	0	1	0	0	R2	R1	R0	Select the internal resistance ratio of the regulator resistor
Select electronic volumn register	0	0	1	0	0	0	0	0	0	1	2-byte instruction to specify the reference voltage
	0	0	x'	x'	EV5	EV4	EV3	EV2	EV1	EV0	
Select LCD bias	0	0	0	1	0	1	0	B2	B1	B0	Select LCD bias
Set Bias Power Save Mode	0	0	1	1	1	1	0	0	1	1	Bias Power save Save the Bias current consumption
	0	0	0	0	0	0	0	0	0	0	
Release Bias Power Save Mode	0	0	1	1	1	1	0	0	1	1	Bias Power save release set the Bias power to normal
	0	0	0	0	0	0	0	1	0	0	
SHL select	0	0	1	1	0	0	SHL	x'	x'	x'	COM bi-directional selection SHL=0: normal direction SHL=1: reverse direction
ADC select	0	0	1	0	1	0	0	0	0	ADC	SEG bi-direction selection ADC=0: normal direction ADC=1: reverse direction
Oscillator on start	0	0	1	0	1	0	1	0	1	1	Start the built-in oscillator
Set power save mode	0	0	1	0	1	0	1	0	0	P	P=0: normal mode P=1: sleep mode
Release power save mode	0	0	1	1	1	0	0	0	0	1	release power save mode
Reset	0	0	1	1	1	0	0	0	1	0	initial the internal function
Set data direction & display data length(DDL)	x'	x'	1	1	1	0	1	0	0	0	2-byte instruction to specify the number of data bytes. (SPI mode)
	x'	x'	D7	D6	D5	D4	D3	D2	D1	D0	
Select FRC and PWM mode	0	0	1	0	0	1	0	FRC	PWM1	PWM0	FRC(1:3FRC, 0:4FRC) PWM1 PWM0 0 0 45PWM 0 1 45 PWM 1 0 60PWM 1 1 ---
NOP	0	0	1	1	1	0	0	0	1	1	*No operation*
Test Instruction	0	0	1	1	1	1	x'	x'	x'	x'	*Don't use this instruction*

ST7528

Instruction	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
EXT=1											
Set white mode and 1st frame,	0	0	1	0	0	0	0	0	0	0	Set white mode and 1st frame
set pulse width	0	0	X'	X'	GA05	GA04	GA03	GA02	GA01	GA00	
Set white mode and 2nd frame,	0	0	1	0	0	0	0	0	0	1	Set white mode and 2nd frame
set pulse width	0	0	X'	X'	GA05	GA04	GA03	GA02	GA01	GA00	
Set white mode and 3rd frame,	0	0	1	0	0	0	0	0	1	0	Set white mode and 3rd frame
set pulse width	0	0	X'	X'	GA05	GA04	GA03	GA02	GA01	GA00	
Set white mode and 4th frame,	0	0	1	0	0	0	0	0	1	1	Set white mode and 4th frame
set pulse width	0	0	X'	X'	GA05	GA04	GA03	GA02	GA01	GA00	
Set gray level 1 mode	0	0	84H~87H (4 bytes)								Set gray level1
Set gray level 2 mode	0	0	88H~8BH (4 bytes)								Set gray level2
Set gray level 3 mode	0	0	8CH~8FH (4bytes)								Set gray level3
Set gray level 4 mode	0	0	90H~93H (4bytes)								Set gray level4
Set gray level 5 mode	0	0	94H~97H (4bytes)								Set gray level5
Set gray level 6 mode	0	0	98H~9BH (4 bytes)								Set gray level6
Set gray level 7 mode	0	0	9CH~9FH (4 bytes)								Set gray level7
Set gray level 8 mode	0	0	A0H~A3H (4 bytes)								Set gray level8
Set gray level 9 mode	0	0	A4H~A7H (4 bytes)								Set gray level9
Set gray level 10 mode	0	0	A8H~ABH (4 bytes)								Set gray level10
Set gray level 11mode	0	0	ACH~AFH (4 bytes)								Set gray level11
Set gray level 12 mode	0	0	B0H~B3H (4 bytes)								Set gray level12
Set gray level 13 mode	0	0	B4H~B7H (4 bytes)								Set gray level13
Set gray level 14 mode	0	0	B8H~BBH (4 bytes)								Set gray level14
Set Dark mode and 1st frame,	0	0	1	0	1	1	1	1	0	0	Set Dark mode and 1st frame, set pulse width
set pulse width	0	0	X'	X'	GAF5	GAF4	GAF3	GAF2	GAF1	GAF0	
Set Dark mode and 2nd frame,	0	0	1	0	1	1	1	1	0	1	Set Dark mode and 2nd frame, set pulse width
set pulse width	0	0	X'	X'	GAF5	GAF4	GAF3	GAF2	GAF1	GAF0	
Set Dark mode and 3rd frame,	0	0	1	0	1	1	1	1	1	0	Set Dark mode and 3rd frame, set pulse width
set pulse width	0	0	X'	X'	GAF5	GAF4	GAF3	GAF2	GAF1	GAF0	
Set Dark mode and 4th frame,	0	0	1	0	1	1	1	1	1	1	Set Dark mode and 4th frame, set pulse width
set pulse width	0	0	X'	X'	GAF5	GAF4	GAF3	GAF2	GAF1	GAF0	

Set Mode Register

2-byte instruction to set Mode (EXT) and FR (Frame frequency control), BE (Booster efficiency control).

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	0	0

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	FR3	FR2	FR1	FR0	0	BE	x'	EXT

Frame frequency

This command is used to set the frame frequency. This table is suitable for no partial display

FR_3	FR_2	FR_1	FR_0	FR frequency
0	0	0	0	77 Hz ±5%
0	0	0	1	51 Hz ±20%
0	0	1	0	55 Hz ±20%
0	0	1	1	58 Hz ±20%
0	1	0	0	63 Hz ±20%
0	1	0	1	67 Hz ±20%
0	1	1	0	68 Hz ±20%
0	1	1	1	70 Hz ±20%
1	0	0	0	73 Hz ±20%
1	0	0	1	75 Hz ±20%
1	0	1	0	80 Hz ±20%
1	0	1	1	85 Hz ±20%
1	1	0	0	91 Hz ±20%
1	1	0	1	102 Hz ±20%
1	1	1	0	113 Hz ±20%
1	1	1	1	123 Hz ±20%

Booster Efficiency

The ST7528 incorporates software configurable Booster Efficiency Command. It could be used with Voltage multiplier to get the suitable Vout and Power consumption. Default setting is Level 2

Flag	Description	
BE	0	Booster Efficiency Level 1
	1	Booster Efficiency Level 2

Mode Set

Flag	Description	
EXT	Default	EXT=0
	EXT=0	The Instruction of EXT=0 Mode is available
	EXT=1	The Instruction of EXT=1 Mode is available

Read Display Data

8-bit data from Display Data RAM specified by the column address and page address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display Data cannot be read through the serial interface.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read data							

Write Display Data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Write data							

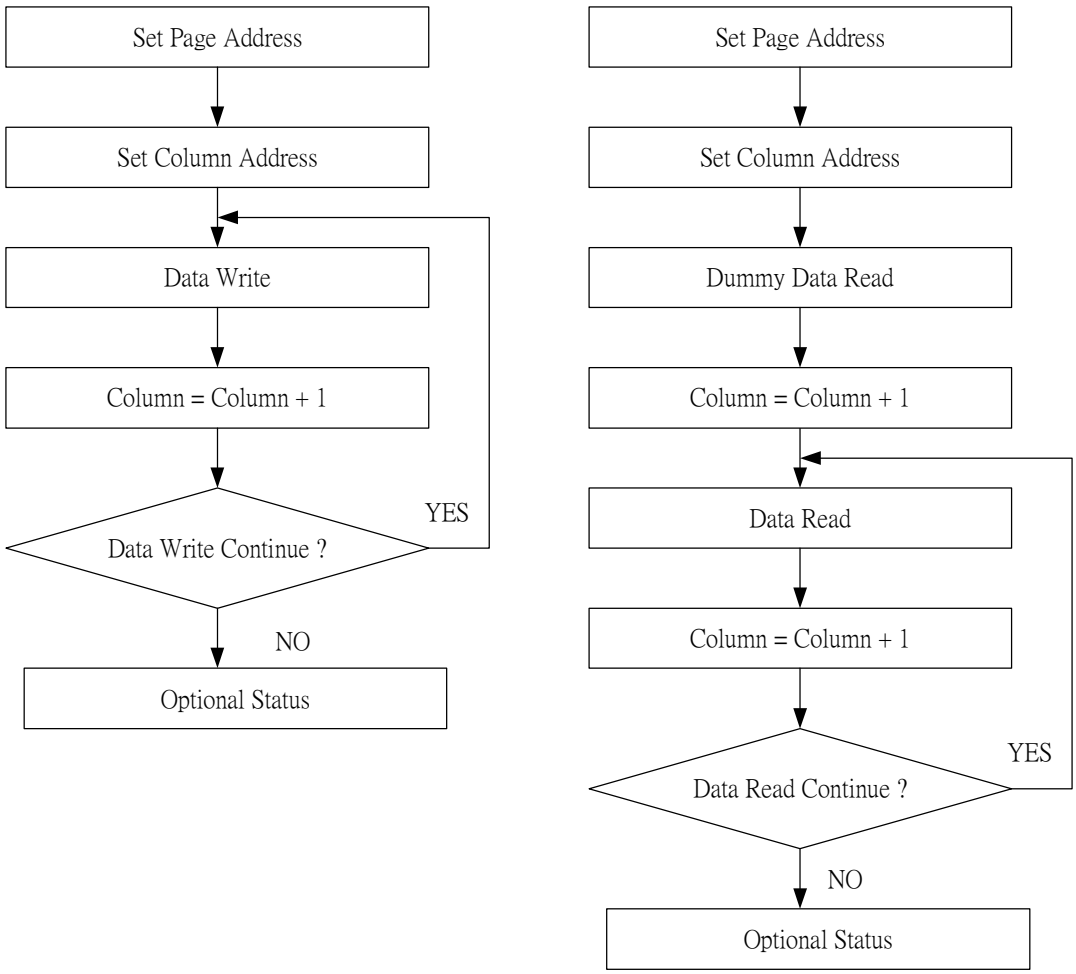


Figure 18 Sequence for Writing Display Data (Left) and Sequence for Reading Display Data (Right)

Read Status

Indicates the internal status of the ST7528

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	ON	RES	MF2	MF1	MF0	DS1	DS0

Flag	Description
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low. 0: chip is active, 1: chip is being busy
ON	Indicates display ON / OFF status 0: display OFF, 1: display ON
RESET	Indicates the initialization is in progress by RESET signal. 0: chip is active, 1: chip is being reset
MF	Manufacturer ID; suggest value: MF2 MF1 MF0 = [0 0 0] The value of MF2, MF1 and MF0 will follow the hardware selection.
DS	Display size ID; suggest value: DS1 DS0 = [1 0] The value of DS1 and DS2 will follow the hardware selection.

ICON Control Register ON/OFF

This instruction makes ICON enable or disable. By default, ICON display is disabled (ICON= 0). When ICON control register is set to “1”, ICON display is enabled and page address is set to “16”. Then user can write data for icons. It is impossible to set the page address to “16” by Set Page Address instruction. Therefore, when writing data for icons, ICON control register ON instruction would be used to set the page address to “16”. When ICON control register is set to “0”, ICON display is disabled.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	ICON

ICON=0: ICON disable (default)

ICON=1: ICON enable & set the page address to 16

Set Page Address

Sets the Page Address of display data RAM from the microprocessor into the page address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write or read display data. Changing the Page Address doesn't affect the display status. Set Page Address instruction can not be used to set the page address to “16”. Use ICON control register ON/OFF instruction to set the page address to “16”.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
1	1	1	0	14
1	1	1	1	15

Set Column Address

Sets the Column Address of display RAM from the microprocessor into the column address register. Along with the Column Address, the Column Address defines the address of the display RAM to write or read display data.

When the microprocessor reads or writes display data to or from display RAM, Column Addresses are automatically increased.

Set Column Address MSB

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	Y9	Y8	Y7	Y6

Set Column Address LSB

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y5	Y4	Y3	Y2

Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Column address [Y9:Y2]
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	0	126
0	1	1	1	1	1	1	1	127
:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	1	0	158
1	0	0	1	1	1	1	1	159

Set Modify-Read

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Modify-Read instruction.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

Reset Modify-Read

This instruction cancels the Modify-Read mode, and makes the column address return to its initial value just before the set Modify-Read instruction is started.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0

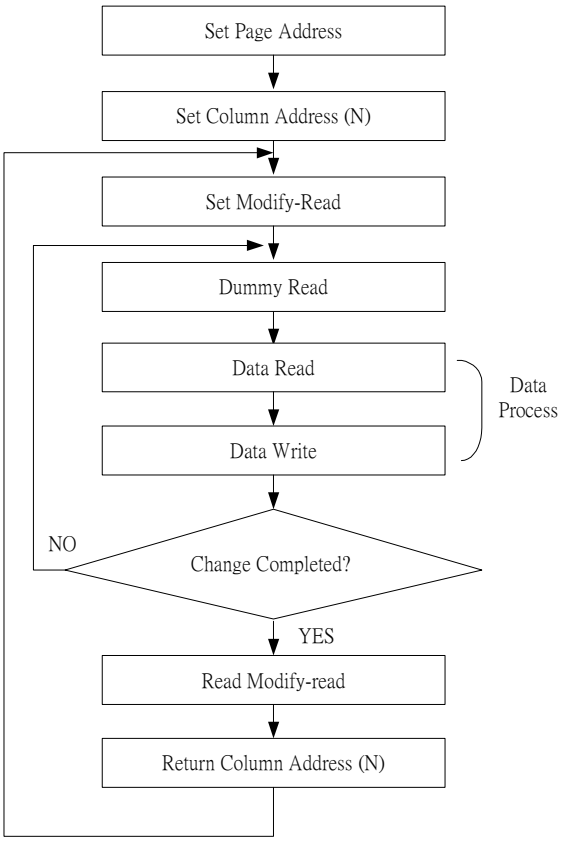


Figure 19 Sequence for Cursor Display

Display ON / OFF

Turns the display ON or OFF.

This command has priority over Entire Display On/Off and Reverse Display On/Off. Commands are accepted while the display is off, but the visual state of the display does not change.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1: display ON

DON = 0: display OFF

Set Initial Display Line Register

Sets the line address of display RAM to determine the initial display line using 2-byte instruction. The RAM display data is displayed at the top of row (COM0) of LCD panel.

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	0	x	x

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	S6	S5	S4	S3	S2	S1	S0

S6	S5	S4	S3	S2	S1	S0	**Line address**
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:
1	1	1	1	1	0	0	124
1	1	1	1	1	0	1	125
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

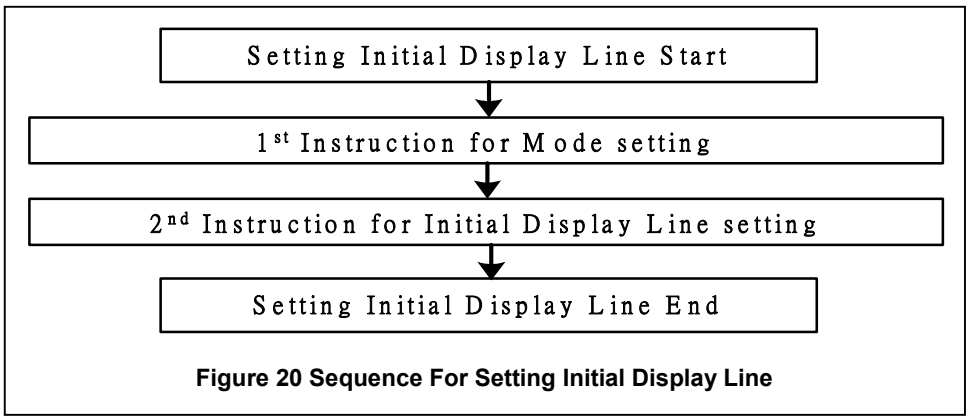


Figure 20 Sequence For Setting Initial Display Line

Set Initial COM0 Register

Sets the initial row (COM) of the LCD panel using the 2-byte instruction. By using this instruction, it is possible to realize the window moving without the change of display data.

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	1	x	x

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	C6	C5	C4	C3	C2	C1	C0

C6	C5	C4	C3	C2	C1	C0	**Initial COM0**
0	0	0	0	0	0	0	COM0
0	0	0	0	0	0	1	COM1
0	0	0	0	0	1	0	COM2
0	0	0	0	0	1	1	COM3
:	:	:	:	:	:	:	:
1	1	1	1	1	0	0	COM124
1	1	1	1	1	0	1	COM125
1	1	1	1	1	1	0	COM126
1	1	1	1	1	1	1	COM127

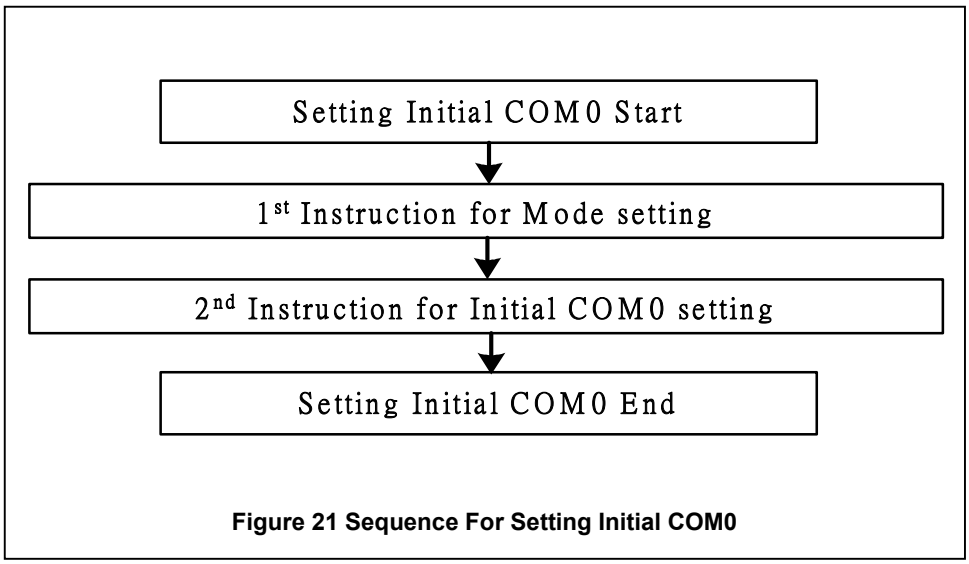


Figure 21 Sequence For Setting Initial COM0

Select partial display line

Sets the ratio within range of 16 to 128 (ICON disabled) or 17 to 129 (ICON enabled) to realize partial display by using the 2-byte instruction.

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	0	x	x

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	D7	D6	D5	D4	D3	D2	D1	D0

D7	D6	D5	D4	D3	D2	D1	D0	Selected partial Display line mode 0	Selected partial Display line mode 1
0	0	0	0	0	0	0	0	No operation	No operation
:	:	:	:	:	:	:	:		
0	0	0	0	1	1	1	1		
0	0	0	1	0	0	0	0	1/16	1/16
0	0	0	1	0	0	0	1	1/17	1/17
:	:	:	:	:	:	:	:	:	:
0	1	1	0	0	1	0	0	1/100	1/100
:	:	:	:	:	:	:	:	:	1/100
0	1	1	1	1	1	1	1	1/127	1/100
1	0	0	0	0	0	0	0	1/128	1/100
1	0	0	0	0	0	0	1	No Operation	No Operation
:	:	:	:	:	:	:	:		
1	1	1	1	1	1	1	1		

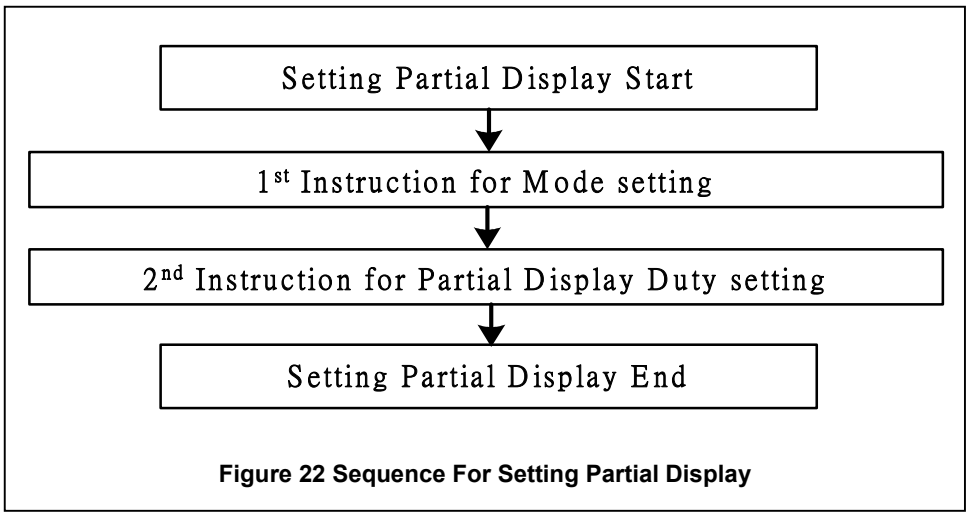


Figure 22 Sequence For Setting Partial Display

Set N-line Inversion Register

Sets the inverted line number within range of 3 to 33 to improve the display quality by controlling the phase of the internal LCD AC signal (M) by using the 2-byte instruction.

The DC-bias problem could be occurred if K is even number. So, we recommend customers to set K to be odd number. K : D/N

D : The number of display ratio (D is selectable by customers)

N : N for N-line inversion (N is selectable by customers).

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	1	x	x

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	x	x	N4	N3	N2	N1	N0

N4	N3	N2	N1	N0	Selected n-line inversion
0	0	0	0	0	0-line inversion (frame inversion)
0	0	0	0	1	3-line inversion
0	0	0	1	0	4-line inversion
0	0	0	1	1	5-line inversion
:	:	:	:	:	:
1	1	1	0	1	31-line inversion
1	1	1	1	0	32-line inversion
1	1	1	1	1	33-line inversion

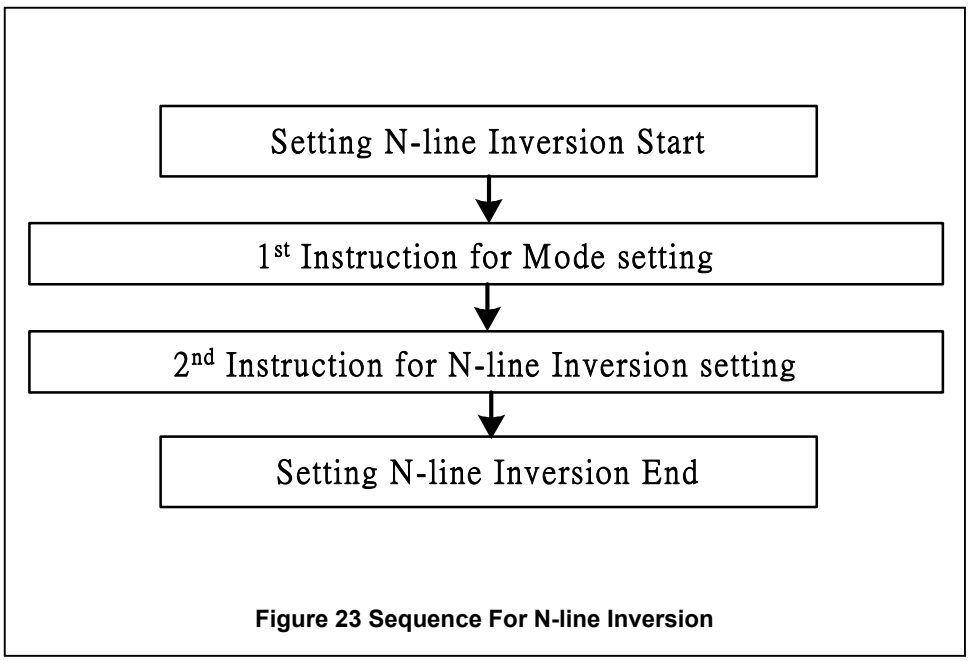


Figure 23 Sequence For N-line Inversion

Release N-line Inversion

Returns to the frame inversion condition from the n-line inversion condition.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	1	0	0

Reverse Display ON / OFF

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	White	Gray level 1	…..	Gray level 14	– Dark
0 (normal)	White (“0000”)	Gray 1 (“0001”)	…..	Gray 14 (“1110”)	Dark (“1111”)
1 (reverse)	Dark (“1111”)	Gray 14 (“1110”)	…..	Gray 1 (“0001”)	White (“0000”)

Entire Display ON / OFF

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the Reverse Display ON / OFF instruction.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

Entire	White	Gray level 1	…..	Gray level 14	– Dark
0 (normal)	White (“0000”)	Gray 1 (“0001”)	…..	Gray 14 (“1110”)	Dark (“1111”)
1 (Entire)	Dark (“1111”)	Dark (“1111”)	Dark (“1111”)	Dark (“1111”)	Dark (“1111”)

Power Control

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Status of internal power supply circuits
0			Internal voltage converter circuit is OFF
1			Internal voltage converter circuit is ON
	0		Internal voltage regulator circuit is OFF
	1		Internal voltage regulator circuit is ON
		0	Internal voltage follower circuit is OFF
		1	Internal voltage follower circuit is ON

Set Bias Power Save Mode

Consist of 2-byte Instructions

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	0	1	1

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0

This command is for saving the IC current consumption by Bias Power Saving

After this Instruction is set, Bias function is also working

Release Bias Power Save Mode

Consist of 2-byte Instructions

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	0	1	1

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	0	0

This command is for release Bias Power Save

Select DC-DC Step-up

Selects one of 4 DC-DC step-up to reduce the power consumption by this instruction. It is very useful to realize the partial display function.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	0	1	DC1	DC0

DC1	DC0	Selected DC-DC converter circuit
0	0	3 times boosting circuit
0	1	4 times boosting circuit
1	0	5 times boosting circuit
1	1	6 times boosting circuit

Select Regulator Resistor

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit. Refer to the Table 6.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	1+ (Rb / Ra)
0	0	0	2.3
0	0	1	3.0
0	1	0	3.7
0	1	1	4.4
1	0	0	5.1
1	0	1	5.8
1	1	0	6.5
1	1	1	7.2

Set Electronic Volume Register

Consist of 2-byte Instructions

The 1st instruction set Reference Voltage mode, the 2nd one updates the contents of reference voltage register.

After second instruction, Reference Voltage mode is released.

The 1st Instruction: Set Reference Voltage Select Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The 2nd Instruction: Set Reference Voltage Register

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	x	EV5	EV4	EV3	EV2	EV1	EV0

EV5	EV4	EV3	EV2	EV1	EV0	Reference voltage parameter (a)
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

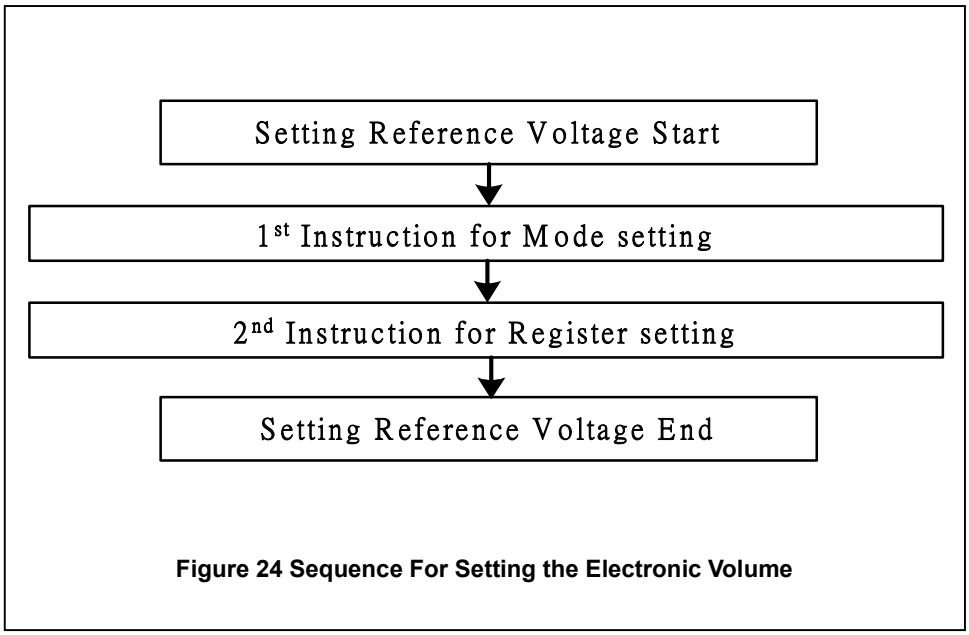


Figure 24 Sequence For Setting the Electronic Volume

Select LCD Bias

Selects LCD bias ratio of the voltage required for driving the LCD.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	0	B2	B1	B0

B2	B1	B0	LCD bias
0	0	0	1/5
0	0	1	1/6
0	1	0	1/7
0	1	1	1/8
1	0	0	1/9
1	0	1	1/10
1	1	0	1/11
1	1	1	1/12

SHL Select

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	x	x	x

In Mode 0

SHL = 0: normal direction (COM0 → COM127)

SHL = 1: reverse direction (COM127 → COM0)

In Mode 1

SHL = 0: normal direction (COM0 → COM99)

SHL = 1: reverse direction (COM99 → COM0)

ADC Select

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins could be reversed by software. This makes IC layout flexible in LCD module assembly.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

In Mode 0

ADC = 0: normal direction (SEG0 → SEG127)

ADC = 1: reverse direction (SEG127 → SEG0)

In Mode 1

ADC = 0: normal direction (SEG0 → SEG159)

ADC = 1: reverse direction (SEG159 → SEG)

Oscillator ON Start

This instruction enables the built-in oscillator circuit.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1

Power Save

The ST7528 enters the Power Save status to reduce the power consumption to the static power consumption value and returns to the normal operation status by the following instructions.

Set Power Save Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	P

P = 0: normal mode

P = 1: sleep mode

Release Power Save Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	1

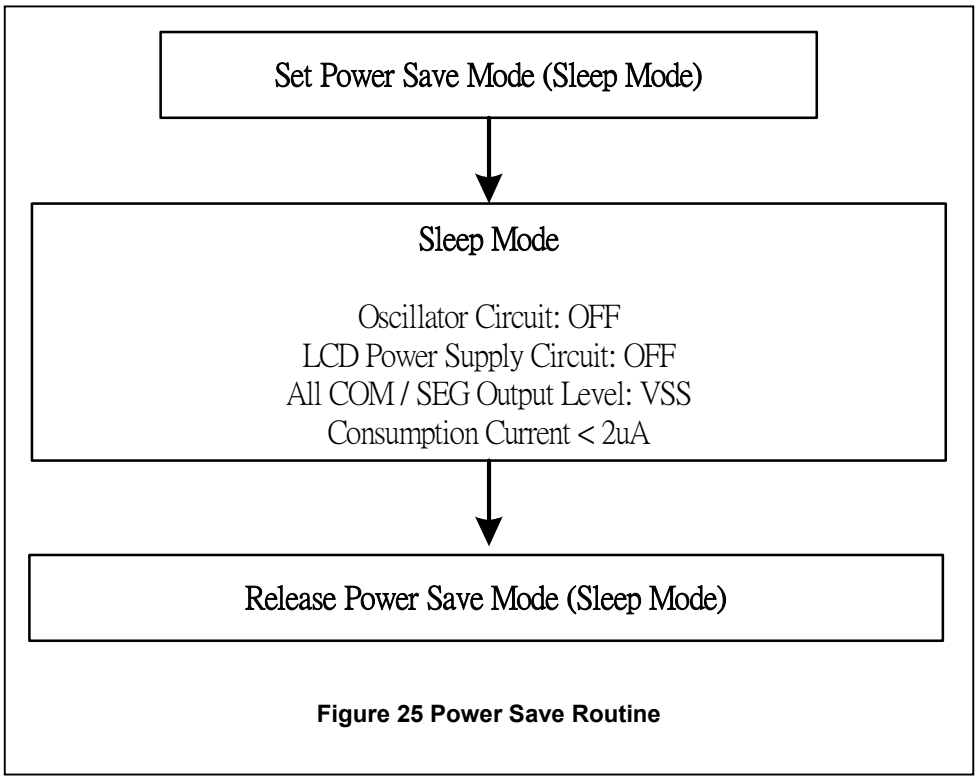


Figure 25 Power Save Routine

Reset

This instruction Resets initial display line, column address, page address, and common output status select to their initial status, but dose not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the RESETB pin.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

Set Data Direction & Display Data Length (3-Line SPI Mode)

Consists of 2 bytes instruction.

This command is used in 3-Line SPI mode only (PS0 = ”L” and PS1 = ”L”). It will be two continuous commands, the first byte control the data direction(write mode only) and inform the LCD driver the second byte will be number of data bytes will be write. When A0 is not used, the Display Data Length instruction is used to indicate that a specified number of display data bytes are to be transmitted. The next byte after the display data string is handled as command data.

The 1st Instruction: Set Data Direction (Only Write Mode)

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
x	x	1	1	1	0	1	0	0	0

The 2nd Instruction: Set Display Data Length (DDL) Register

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
x	x	D7	D6	D5	D4	D3	D2	D1	D0

D7	D6	D5	D4	D3	D2	D1	D0	Display Data Length
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	1	254
1	1	1	1	1	1	1	0	255
1	1	1	1	1	1	1	1	256

NOP

No operation

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

Test Instruction

This instruction is for testing IC. Please do not use it.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	x	x	x	x

Set FRC & PWM mode

Selects 3/4 FRC and 45 / 60 PWM

FRC	PWM1	PWM0	Status of PWM & FRC
0			4FRC
1			3FRC
	0	0	45PWM
	0	1	45PWM
	1	0	60PWM
	1	1	---

NOTE: the value of register could not set [PWM1:PWM0]=[1:1]

Set Gray Scale Mode & Register

Consists of 2 bytes instruction. The first byte sets grayscale mode and the second byte updates the contents of gray scale register without issuing any other instruction.

– Set Gray Scale Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	GRAY3	GRAY2	GRAY1	GRAY0	FRAMX1	FRAMX0

GRAY3	GRAY2	GRAY1	GRAY0	FRAMX1	FRAMX0	Description
0	0	0	0	0	0	In case of setting whit mode and 1st frame
0	0	0	0	0	1	In case of setting whit mode and 2nd frame
0	0	0	0	1	0	In case of setting whit mode and 3rd frame
0	0	0	0	1	1	In case of setting whit mode and 4th frame
0	0	0	1	0	0	In case of setting GRAY LEVEL 1 mode and 1st frame
0	0	0	1	0	1	In case of setting GRAY LEVEL 1 mode and 2 rd frame
0	0	0	1	1	0	In case of setting GRAY LEVEL 1 mode and 3rd frame
:	:	:	:	:	:	:
1	1	1	0	0	1	In case of setting GRAY LEVEL 14 mode and 2nd frame
1	1	1	0	1	0	In case of setting GRAY LEVEL 14 mode and 3rd frame
1	1	1	0	1	1	In case of setting GRAY LEVEL 14 mode and 4th frame
1	1	1	1	0	0	In case of setting dark mode and 1st frame
1	1	1	1	0	1	In case of setting dark mode and 2nd frame
1	1	1	1	1	0	In case of setting dark mode and 3rd frame
1	1	1	1	1	1	In case of setting dark mode and 4th frame

--Set Gray Scale Register

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	X	X	GAX5	GAX4	GAX3	GAX2	GAX1	GAX0

GAX5	GAX4	GAX3	GAX2	GAX1	GAX0	**Pulse width (45 PWM)**	**Pulse width (60 PWM)**
0	0	0	0	0	0	0/45	0/60
0	0	0	0	0	1	1/45	1/60
0	0	0	0	1	0	2/45	2/60
0	0	0	0	1	1	3/45	3/60
0	0	0	1	0	0	4/45	4/60
:	:	:	:	:	:	:	:
1	0	1	0	1	1	43/45	43/60
1	0	1	1	0	0	44/45	44/60
1	0	1	1	0	1	45/45	45/60
1	0	1	1	1	0	0/45	46/60
1	0	1	1	1	1	0/45	47/60
:	:	:	:	:	:	:	:
1	1	1	0	1	1	0/45	59/60
1	1	1	1	0	0	0/45	60/60
1	1	1	1	0	1	0/45	0/60
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0/45	0/60

COMMAND DESCRIPTION

Referential Instruction Setup Flow: Initializing with the built-in Power Supply Circuits

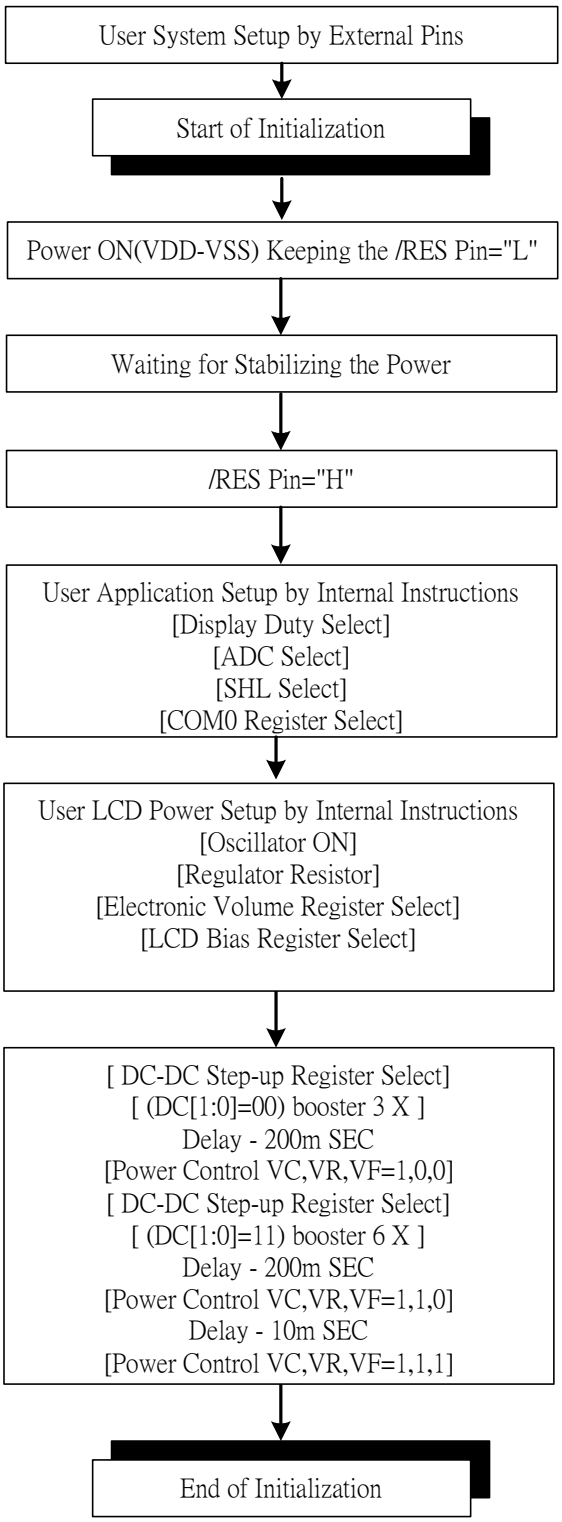


Figure 26 Initializing with the Built-in Power Supply Circuits

Referential Instruction Setup Flow: Initializing without the built-in Power Supply Circuits

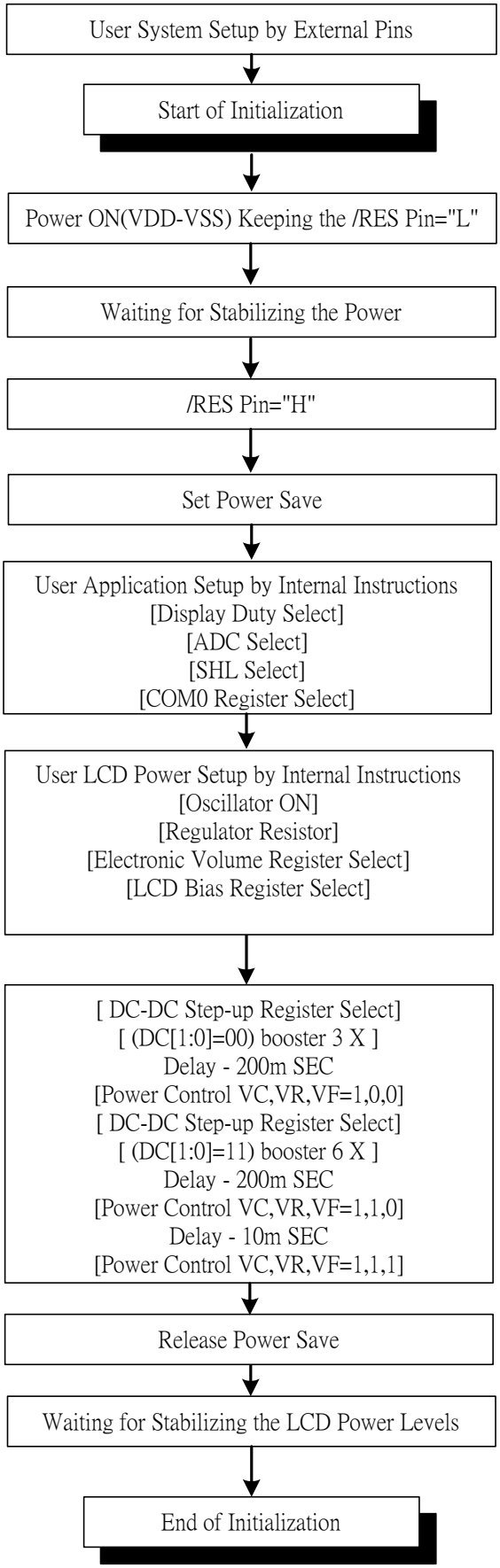


Figure 27 Initializing without Built-in Power Supply Circuits

Referential Instruction Setup Flow: Data Displaying

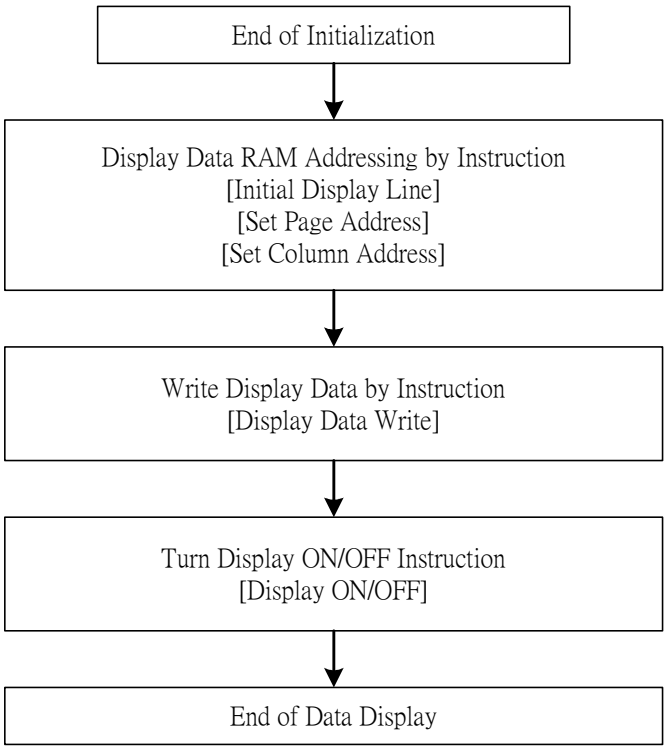


Figure 28 Data Displaying

Referential Instruction Setup Flow: Power OFF

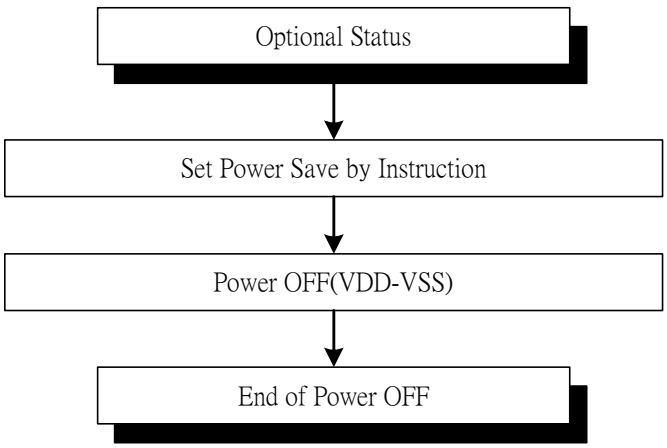
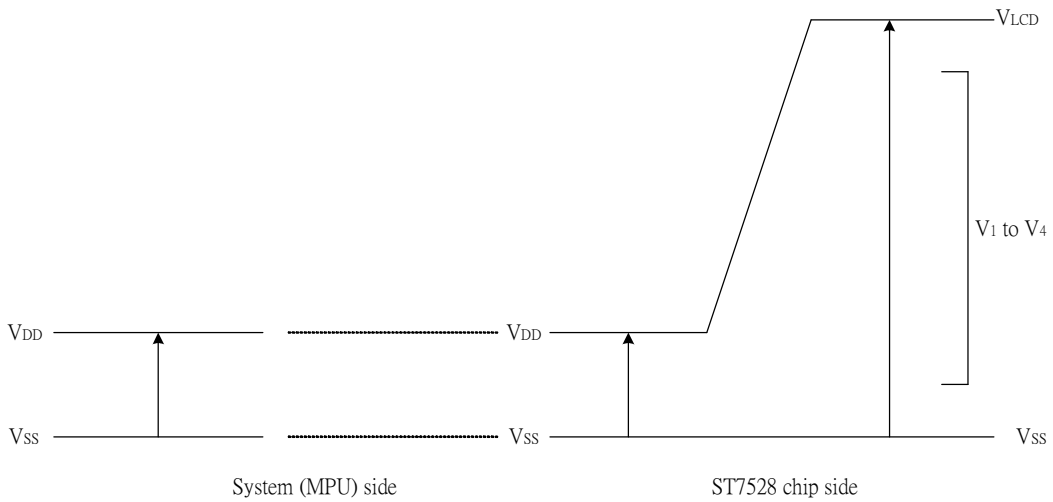


Figure 29 Power OFF

LIMITING VALUES

In accordance with the Absolute Maximum Rating System; see notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Power Supply Voltage	VDD	–0.5 ~ +3.6	V
Power Supply Voltage	VDD2	–0.5 ~ +3.6	V
External Reference Voltage	VEXT	2.0 ~ 3.3	V
Power supply voltage	V0	3.5~15	V
Power supply voltage	VOUT_IN	–0.5 ~ +20	V
Power supply voltage	V1, V2, V3, V4	0.3 to VOUT_IN	V
Input voltage	VIN	–0.5 to VDD+0.5	V
Output voltage	VO	–0.5 to VDD+0.5	V
Operating temperature	TOPR	–30 to +85	°C
Storage temperature	TSTR	–65 to +150	°C



Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
3. Insure that the voltage levels of V1, V2, V3, and V4 are always such that

   VOUT_IN ≧ V0 ≧ V1 ≧ V2 ≧ V3 ≧ V4 ≧ Vss

DC CHARACTERISTICS

V_{DD} = 1.8 V to 3.3V; V_{SS} = 0 V; V_{LCD} = 3.0 to 13.0V; T_{amb} = -30℃ to +85℃; unless otherwise specified.

Item	Symbol	Condition	Rating			Units	Applicable Pin
			Min.	Typ.	Max.		
Operating Voltage (1)	VDD		1.8	—	3.3	V	Vss*1
Operating Voltage (2)	VDD2	(Relative to VSS)	2.4	—	3.3	V	VSS2
High-level Input Voltage	VIHC		0.7 x VDD	—	VDD	V	*2
Low-level Input Voltage	VILC		VSS	—	0.3 x VDD	V	*2
High-level Output Voltage	VOHC	IOH=1mA	0.7 x VDD	—	VDD	V	*3
Low-level Output Voltage	VOLC	IOL=-1mA	VSS	—	0.3 x VDD	V	*3
Input leakage current	ILI	VIN = VDD or VSS	–1.0	—	1.0	μA	*4
Output leakage current	ILO	VIN = VDD or VSS	–3.0	—	3.0	μA	*5
Liquid Crystal Driver ON Resistance	RON	Ta = 25°C (Relative To VSS) VOUT_IN = 15.0 V	—	2.0	3.5	KΩ	SEGn COMn *6
		Ta = 25°C (Relative To VSS) VOUT_IN = 8.0 V	—	3.2	5.4		
Default Oscillator Frequency — Internal Oscillator	fOSC	Mode0 128 line Ta = 25°C 60 PWM	570.57	600.6	630.63	kHz	*7
Default Oscillator Frequency — External Input	fCL		570.57	600.6	630.63	kHz	OSC
Max OSC under FR=1,1,1,1	fOSC		767.52	959.4	1151.28	kHz	
Mode 10 Default Frame frequency	fFRAME		73.15	77	80.85	Hz	

Item		Symbol	Condition	Rating			Units	Applicable Pin
				Min.	Typ.	Max.		
Internal Power	Input voltage	VDD	(Relative To VSS)	1.8	—	3.3	V	
	Supply Step-up output voltage Circuit	VOUT_OUT	(Relative To VSS)	—	—	18	V	VOUT_OUT
	Voltage regulator Circuit Operating Voltage	VOUT_IN	(Relative To VSS)	—	—	18	V	VOUT_IN

Bare Dice Consumption Current : During Display, with the Internal Power Supply, Current consumed by total ICs when an external power supply(VDD,VDD2) is used .

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern SNOW	ISS	VDD = 3.3 V, V0 – VSS = 10.7 V 5X booster 1/11 bias	—	550	650	μA	*8
Power Down	ISS	Ta = 25°C	—	0.01	2	μA	*9

Notes to the DC characteristics

1. The maximum possible V_{OUT} voltage that may be generated is dependent on voltage, temperature and (display) load.
2. Internal clock
3. Power-down mode. During power down all static currents are switched off.
4. If external V_{LCD}, the display load current is not transmitted to I_{DD}.
5. V_{OUT} external voltage applied to VOUT_IN pin; VOUT_IN disconnected from VOUT_OUT

References for items market with *

*1 While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.

*2 The A0, D0 to D5, D6 (SI), D7 (SCL), /RD (E), /WR ,/(R/W), CSB, IMS, OSC, P/S, /DOF, RESB ,and MODE terminals.

*3 The D0 to D7, and OSC terminals.

*4 The A0,/RD (E), /WR ,/(R/W), CSB, IMS, OSC, P/S, /DOF, RESB ,and MODE terminals.

*5 Applies when the D0 to D5, D6 (SI), D7 (SCL) terminals are in a high impedance state.

*6 These are the resistance values for when a 0.1 V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V1, V2, V3, and V4). These are specified for the operating voltage range.

RON = 0.1 V /ΔI (Where ΔI is the current that flows when 0.1 V is applied while the power supply is ON.)

*7 The relationship between the oscillator frequency and the frame rate frequency.

*8,9 It indicates the current consumed on bare dice when the internal oscillator circuit and display are turned on.

TIMING CHARACTERISTICS

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

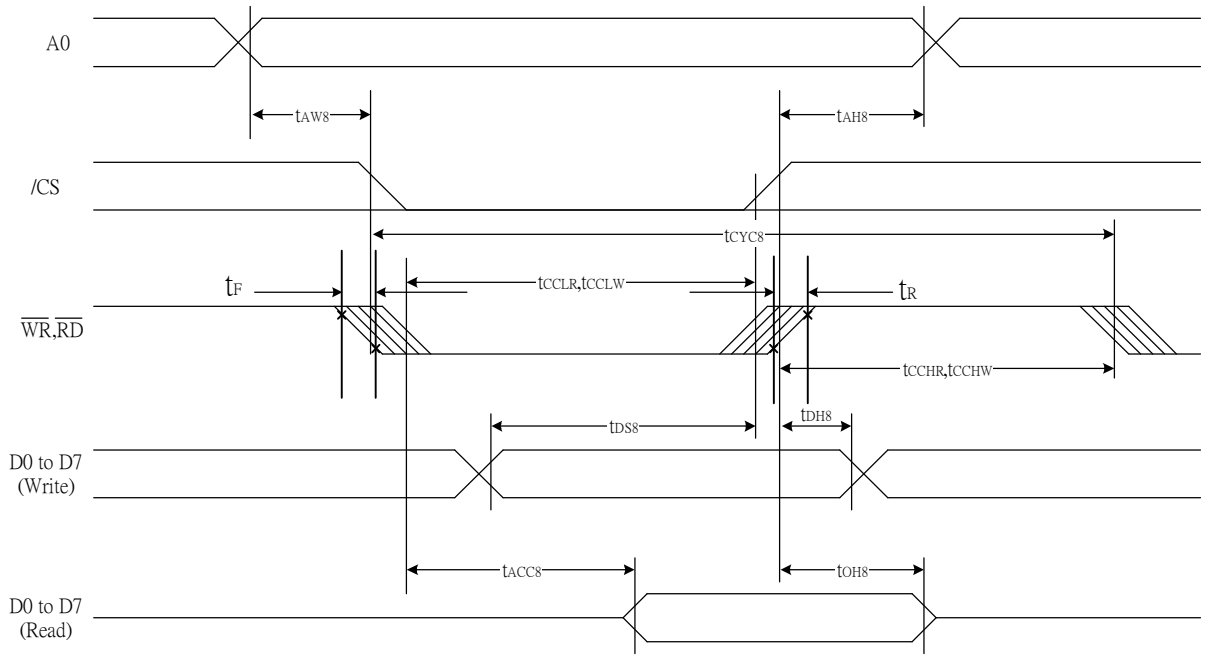


Figure 26.

(VDD = 3.3V , Ta = -30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		240	—	
Enable L pulse width (WRITE)	WR	tCCLW		80	—	
Enable H pulse width (WRITE)		tCCHW		80	—	
Enable L pulse width (READ)	RD	tCCLR		140	—	
Enable H pulse width (READ)		tCCHR		80		
WRITE Data setup time	D0 to D7	tDS8		40	—	
WRITE Data hold time		tDH8		10	—	
READ access time		tACC8	CL = 100 pF	—	70	
READ Output disable time		tOH8	CL = 100 pF	5	50	
tF				—	10	
tR				—	10	

(VDD = 2.7 V , Ta = -30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		400	—	
Enable L pulse width (WRITE)	WR	tCCLW		220	—	
Enable H pulse width (WRITE)		tCCHW		180	—	
Enable L pulse width (READ)	RD	tCCLR		220	—	
Enable H pulse width (READ)		tCCHR		180	—	
WRITE Data setup time	D0 to D7	tDS8		40	—	
WRITE Data hold time		tDH8		15	—	
READ access time		tACC8	CL = 100 pF	—	140	
READ Output disable time		tOH8	CL = 100 pF	10	100	
tF				—	10	
tR				—	10	

(VDD = 1.8V , Ta = -30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		640	—	
Enable L pulse width (WRITE)	WR	tCCLW		360	—	
Enable H pulse width (WRITE)		tCCHW		280	—	
Enable L pulse width (READ)	RD	tCCLR		360	—	
Enable H pulse width (READ)		tCCHR		280		
WRITE Data setup time	D0 to D7	tDS8		80	—	
WRITE Data hold time		tDH8		30	—	
READ access time		tACC8	CL = 100 pF	—	240	
READ Output disable time		tOH8	CL = 100 pF	10	200	
tF				—	10	
tR				—	10	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) $\leqq$ (tCYC8 – tCCLW – tCCHW) for (tr + tf) $\leqq$ (tCYC8 – tCCLR – tCCHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tCCLW and tCCLR are specified as the overlap between CSB being “L” and WR and RD being at the “L” level.

System Bus Read/Write Characteristics 1 (For the 6800 Series MPU)

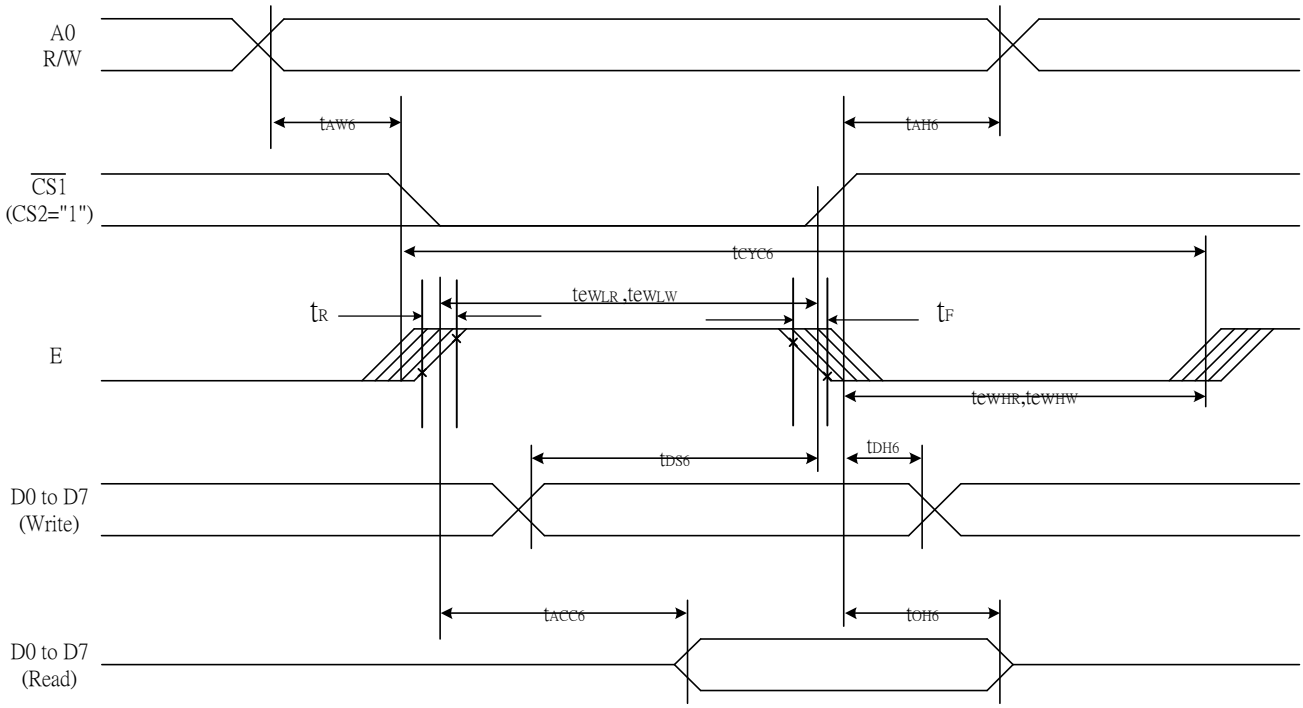


Figure 30

(V_{DD} = 3.3 V,Ta = -30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		240	—	
Enable L pulse width (WRITE)	E_WR	tEWLW		80	—	
Enable H pulse width (WRITE)		tEWHW		80	—	
Enable L pulse width (READ)	E_RD	tEWLR		80	—	
Enable H pulse width (READ)		tEWHR		140		
WRITE Data setup time	D0 to D7	tDS6		40	—	
WRITE Data hold time		tDH6		10	—	
READ access time		tACC6	CL = 100 pF	—	70	
READ Output disable time		tOH6	CL = 100 pF	5	50	
tF				—	10	
tR				—	10	

(VDD = 2.7V,Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		400	—	
Enable L pulse width (WRITE)	WR	tEWLW		220	—	
Enable H pulse width (WRITE)		tEWHW		180	—	
Enable L pulse width (READ)	RD	tEWLR		220	—	
Enable H pulse width (READ)		tEWHR		180	—	
WRITE Data setup time	D0 to D7	tDS6		40	—	
WRITE Data hold time		tDH6		15	—	
READ access time		tACC6	CL = 100 pF	—	140	
READ Output disable time		tOH6	CL = 100 pF	10	100	
tF				—	10	
tR				—	10	

(VDD =1.8V,Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		640	—	
Enable L pulse width (WRITE)	WR	tEWLW		360	—	
Enable H pulse width (WRITE)		tEWHW		280	—	
Enable L pulse width (READ)	RD	tEWLR		360	—	
Enable H pulse width (READ)		tEWHR		280	—	
WRITE Data setup time	D0 to D7	tDS6		80	—	
WRITE Data hold time		tDH6		30	—	
READ access time		tACC6	CL = 100 pF	—	240	
READ Output disable time		tOH6	CL = 100 pF	10	200	
tF				—	10	
tR				—	10	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≦ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≦ (tCYC6 – tEWLR – tEWHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tEWLW and tEWLR are specified as the overlap between CSB being “L” and E.

SERIAL INTERFACE (4-Line Interface)

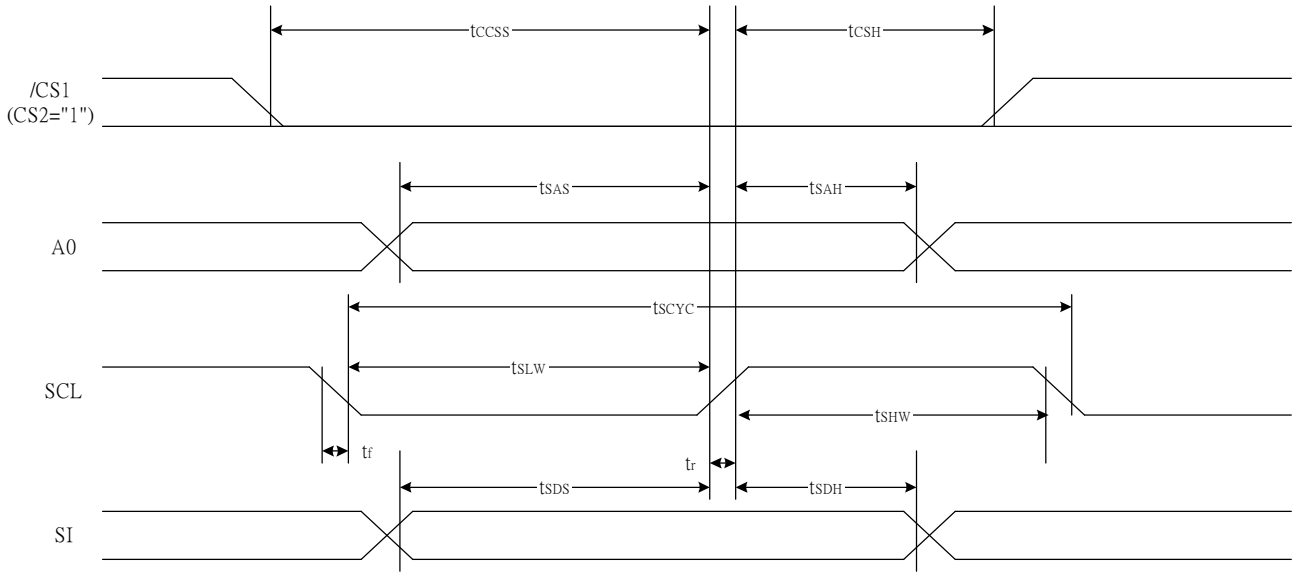


Figure 31

(V_{DD}=3.3V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		50	—	ns
SCL “H” pulse width		tSHW		25	—	
SCL “L” pulse width		tSLW		25	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		10	—	
Data setup time	SI	tSDS		20	—	
Data hold time		tSDH		10	—	
CS-SCL time	CSB	tCSS		20	—	
CS-SCL time		tCSH		40	—	

(V_{DD}=2.7V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		100	—	ns
SCL “H” pulse width		tSHW		50	—	
SCL “L” pulse width		tSLW		50	—	
Address setup time	A0	tSAS		30	—	
Address hold time		tSAH		20	—	
Data setup time	SI	tSDS		30	—	
Data hold time		tSDH		20	—	
CS-SCL time	CSB	tCSS		30	—	
CS-SCL time		tCSH		60	—	

(V_{DD}=1.8V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		200	—	ns
SCL “H” pulse width		tSHW		80	—	
SCL “L” pulse width		tSLW		80	—	
Address setup time	A0	tSAS		60	—	
Address hold time		tSAH		30	—	
Data setup time	SI	tSDS		60	—	
Data hold time		tSDH		30	—	
CS-SCL time	CSB	tCSS		40	—	
CS-SCL time		tCSH		100	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

SERIAL INTERFACE(3-Line Interface)

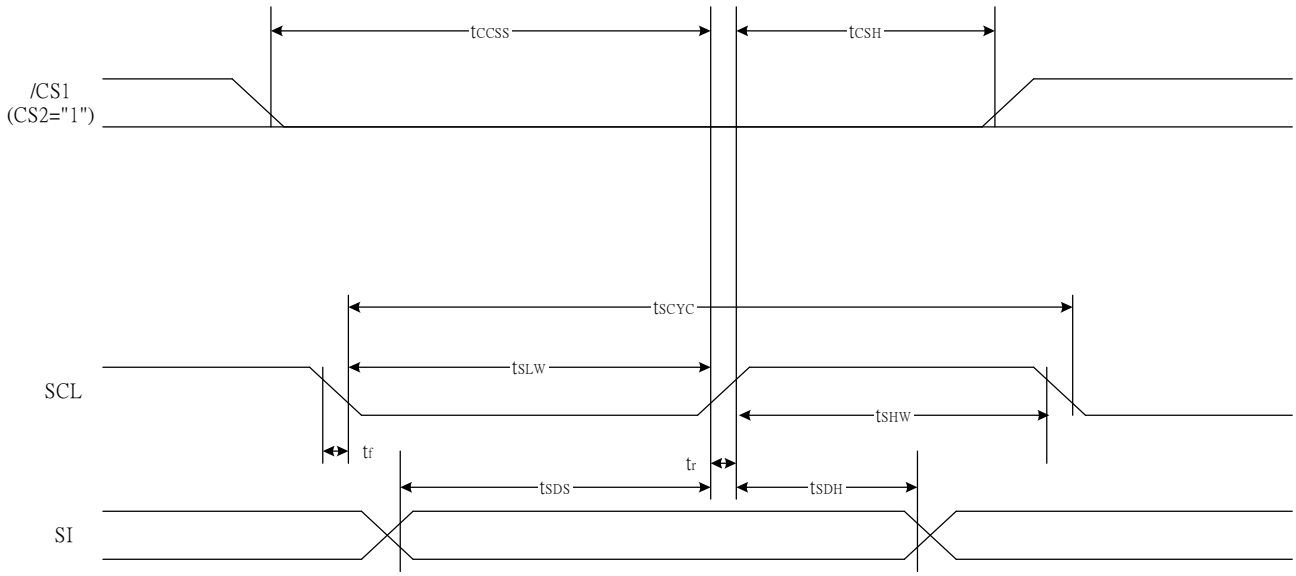


Figure 32

(V_{DD}=3.3V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		50	—	ns
SCL “H” pulse width		tSHW		25	—	
SCL “L” pulse width		tSLW		25	—	
Data setup time	SI	tSDS		20	—	
Data hold time		tSDH		10	—	
CS-SCL time	CSB	tCSS		20	—	
CS-SCL time		tCSH		40	—	

(V_{DD}=2.7V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		100	—	ns
SCL “H” pulse width		tSHW		50	—	
SCL “L” pulse width		tSLW		50	—	
Data setup time	SI	tSDS		30	—	
Data hold time		tSDH		20	—	
CS-SCL time	CSB	tCSS		30	—	
CS-SCL time		tCSH		60	—	

(V_{DD}=1.8V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		200	—	ns
SCL “H” pulse width		tSHW		80	—	
SCL “L” pulse width		tSLW		80	—	
Data setup time	SI	tSDS		60	—	
Data hold time		tSDH		30	—	
CS-SCL time	CSB	tCSS		40	—	
CS-SCL time		tCSH		100	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

SERIAL INTERFACE(IIC Interface)

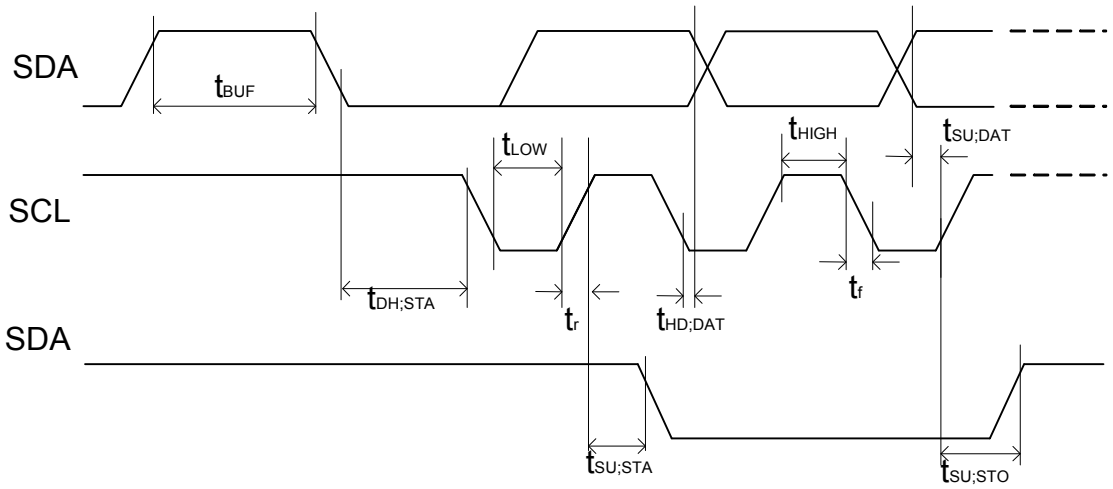


Figure 33

(V_{DD}=3.3V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
SCL clock frequency	SCL	FSCLK		-	400	kHZ
SCL clock low period	SCL	TLOW		1.3	-	us
SCL clock high period	SCL	THIGH		0.6	-	us
Data set-up time	SI	TSU;Data		100	-	ns
Data hold time	SI	THD;Data		0	0.9	us
SCL,SDA rise time	SCL	TR		20+0.1Cb	300	ns
SCL,SDA fall time	SCL	TF		20+0.1Cb	300	ns
Capacitive load represented by each bus line		Cb		-	400	pF
Setup time for a repeated START condition	SI	TSU;SUA		0.6	-	us
Start condition hold time	SI	THD;STA		0.6	-	us
Setup time for STOP ondition		TSU;STO		0.6	-	us
Tolerable spike width on bus		TSW		-	50	ns
BUS free time between a STOP and StART condition	SCL	TBUF		1.3		us

RESET TIMING

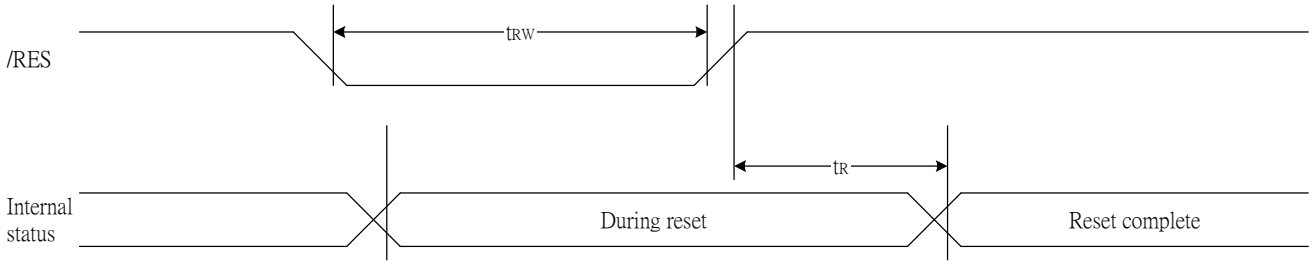


Figure 34

(VDD = 3.3V , Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	1	us
Reset “L” pulse width	RESB	tRW		1	—	—	us

(VDD = 2.7V , Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	1.5	us
Reset “L” pulse width	RESB	tRW		1.5	—	—	us

(VDD = 1.8V , Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	2.0	us
Reset “L” pulse width	RESB	tRW		2.0	—	—	us

POWER PAD CONNECT

The pinning of the ST7528 is optimized for single plane wiring e.g. for chip-on-glass display modules. Display size: 160 X 100 pixels or 132 X 128 pixels.

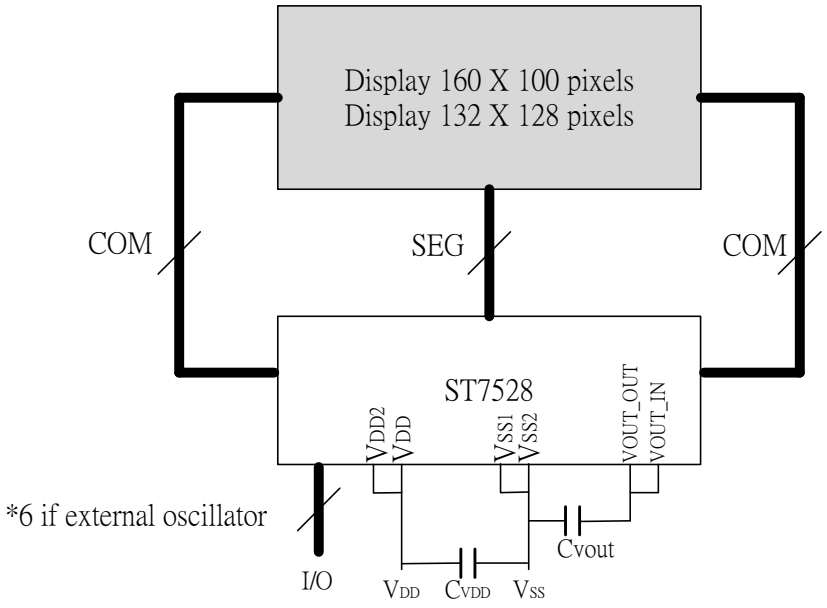


Figure 35 Application diagram: internal charge pump is used and s single V_{DD}

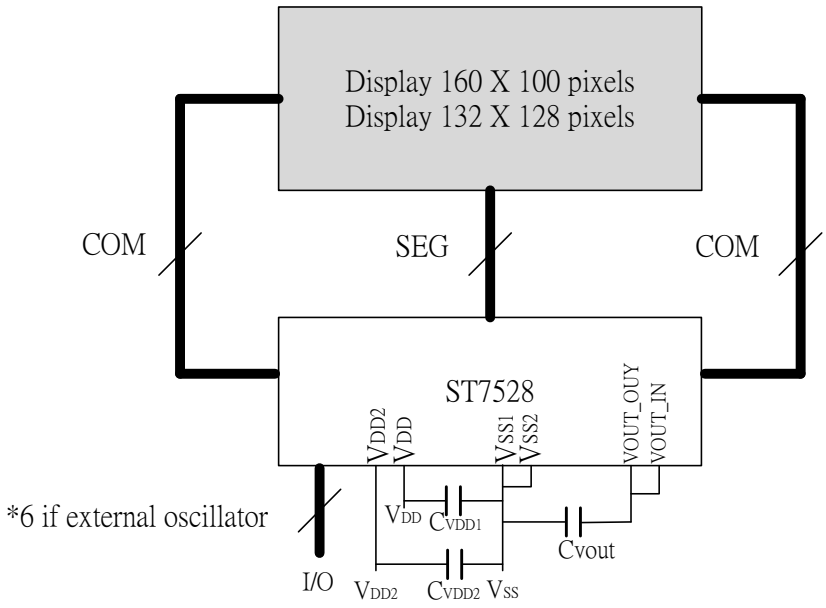


Figure 36 Application diagram: Internal charge pump is used and two separate VDD(V_{DD2})

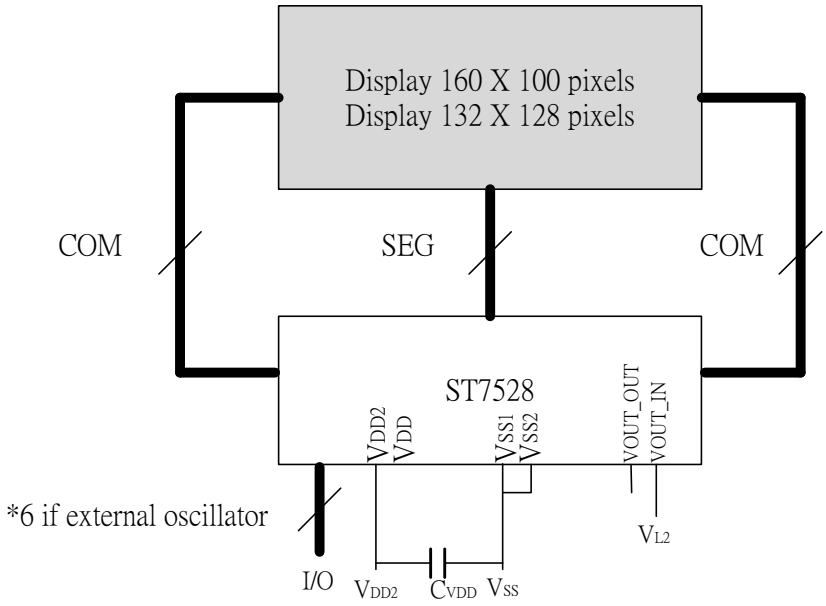


Figure 37 application diagram : External high voltage generation is used

The required minimum value for the external capacitors in an application with the ST7528 are:

C_{VLCD} = min. 100nF $C_{VDD,2}$= min. 1.0 μF

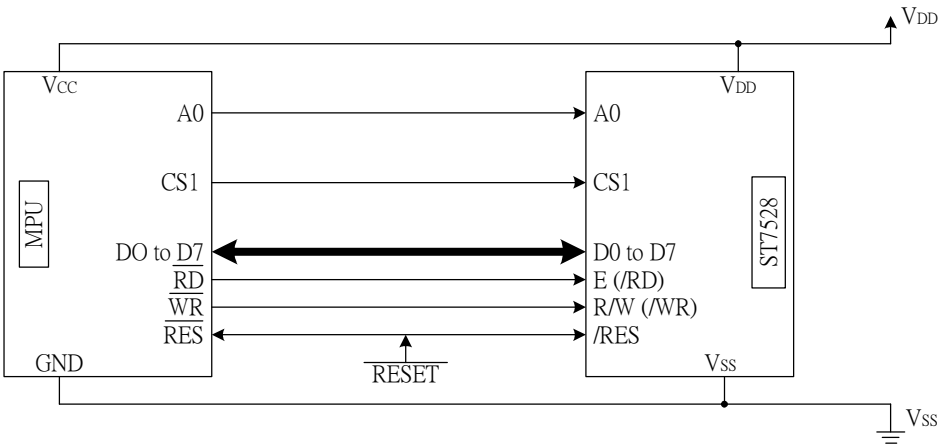
Higher capacitor values are recommended for ripple reduction.

THE MPU INTERFACE (REFERENCE EXAMPLES)

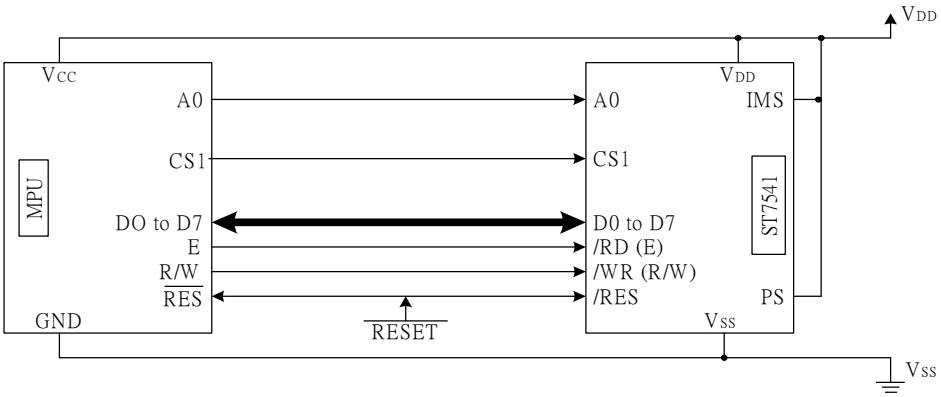
The ST7528 Series can be connected to either60X86 Series MPUs or to 6800Series MPUs. Moreover, using the serial interface it is possible to operate the ST7528 series chips with fewer signal lines.

The display area can be enlarged by using multiple ST7528 Series chips. When this is done, the chip select signal can be used to select the individual ICs to access.

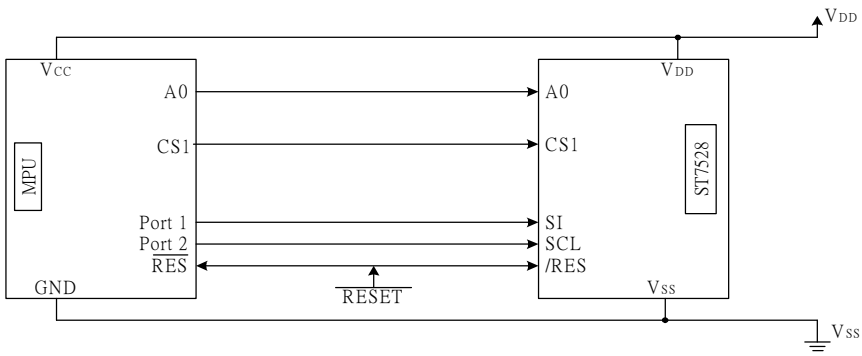
(1) 8080 Series MPUs



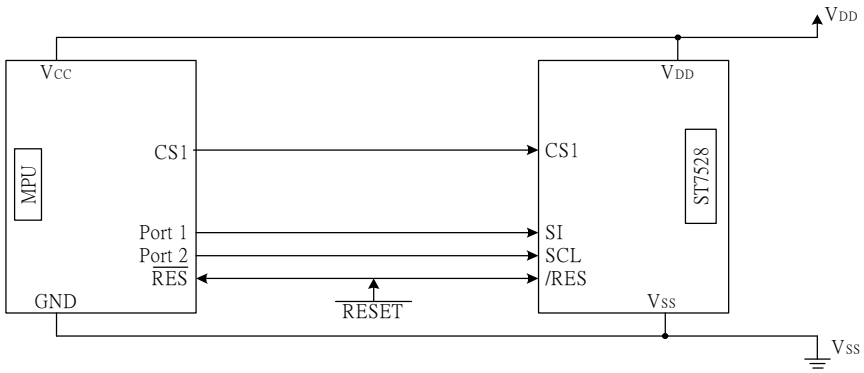
(2) 6800 Series MPUs



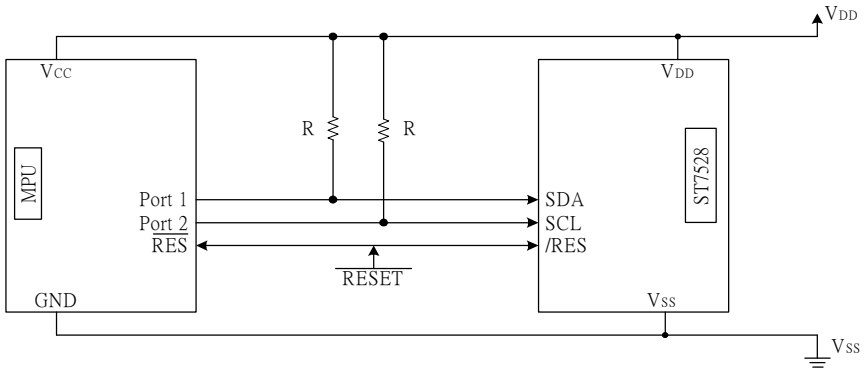
(3) Using the Serial Interface (4-line interface)



(4) Using the Serial Interface (3-line interface)

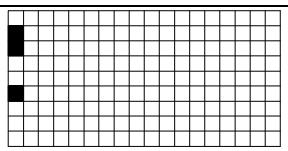


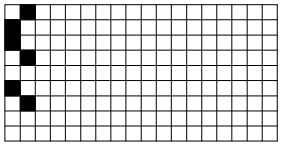
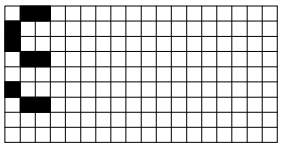
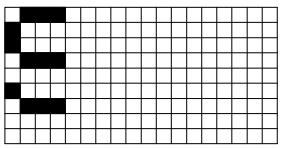
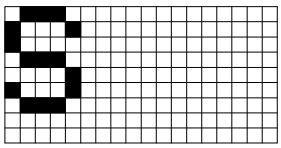
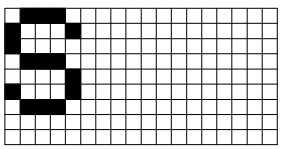
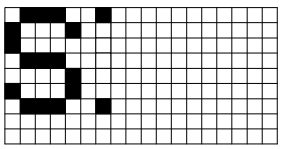
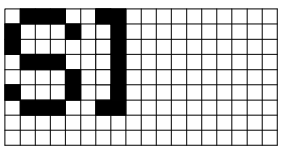
(5) Using the Serial Interface (IIC interface)

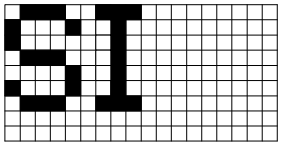


APPLICATION Program Example

16-Gray programming example for ST7528

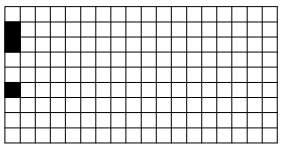
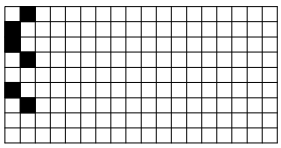
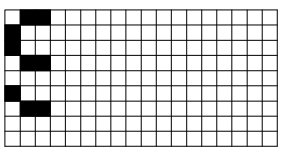
SETP	SERIAL BUS BYTE	DISPLAY	OPERATION
0	Start		CSB IS going low.
1	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 0 1 x' 0		Mode Set. FR[3:0] = 0000 BE = 1 EXT= 0 (Normal INST. Mode)
2	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 1 0 1 0 1 1		OSC ON
3.a	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 1 0 0 1 DC1 DC0		Set DC-DC Step up Set Vout
3.b	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 0 R2 R1 R0		Set Ra/Rb Set R[2:0]
3.c	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 0 0 0 0 1 0 x' x' Ev5 Ev4 Ev3 Ev2 Ev1 Ev0		Set EV Set Ev[5:0]
3.d	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 0 1 0 B2 B1 B0		Set Bias Set B[2:0]
4.a	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 0 1 x' 1		Mode Set. EXT= 1 (Extension INST. Mode)
4.b	SET pulse width of Gray scale		Gray-Scale Setting
4.c	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 0 1 x' 0		Mode Set. EXT= 0 (Normal INST. Mode)
5.a	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 1 0 1 1 1 1		SET Power Control Booster ON Regulator ON Follower ON
5.b	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 1 0 1 1 1 1		Display control. Display on
6	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1 1 0		Data Write. Y,X are initialized to 0 by default, so they aren't set here…

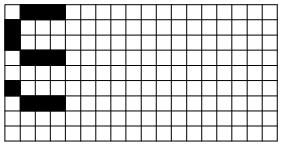
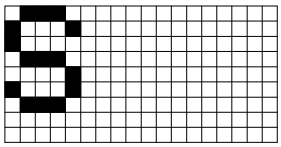
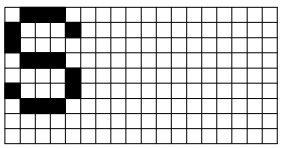
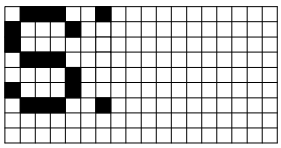
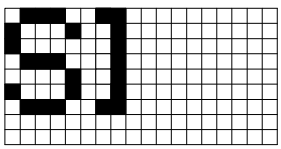
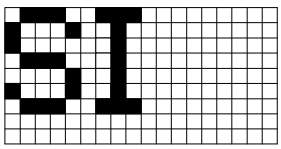
7	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1		Data Write.
8	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1		Data Write.
9	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1		Data Write.
10	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 1 1 0 0 1 0 1 0 0 1 1 0 0 1 0 1 0 0 1 1 0 0 1 0 1 0 0 1 1 0 0 1 0		Data Write.
11	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0		Data Write.
12	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 0 0 0 1 1 0 1 0 0 0 0 0 1 1 0 1 0 0 0 0 0 1 1 0 1 0 0 0 0 0 1		Data Write.
13	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1		Data Write.

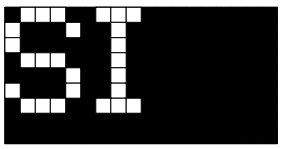
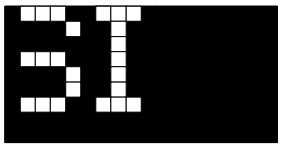
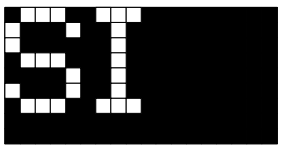
14	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 0 0 0 1 1 0 1 0 0 0 0 0 1 1 0 1 0 0 0 0 0 1 1 0 1 0 0 0 0 0 1		Data Write.
15	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 1 0 0 1 1 1		Display Control. Set Reverse display mode REV=1
16	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0		Set column address of RAM. Set address to “00000000”. Y[9:2]=00000000 (Y[1:0] default is 00)
17	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0		Data Write.

programming example for ST7528(Use IIC Interface)

SETP	SERIAL BUS BYTE	DISPLAY	OPERATION
1	IIC INTERFACE Start		
2	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0		Slave address for write
3	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 0 0 0		Control byte with cleared Co bit and A0 set to logic 0
4	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 1 1 0 0 0 0 0 0 0 0 1 x’ 0		Mode Set. FR[3:0] = 0000 BE= 1 EXT= 0 (Normal INST. Mode)
5	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 1 0 1 1		OSC ON
6.a	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 1 0 0 1 DC1 DC0		Set DC-DC Step up Set Vout
6.b	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 1 0 R2 R1 R0		Set Ra/Rb Set R[2:0]
6.c	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0		Set EV

	1 0 0 0 0 0 0 1 x' x' Ev5 Ev4 Ev3 Ev2 Ev1 Ev0		Set Ev[5:0]
6.d	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 1 0 B2 B1 B0		Set Bias Set B[2:0]
7.a	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 1 1 0 0 0 0 0 0 0 0 1 x' 1		Mode Set. EXT= 1 (Extension INST. Mode)
7.b	SET pulse width of Gray scale		Gray-Scale Setting
7.c	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 1 1 0 0 0 0 0 0 0 0 1 x' 0		Mode Set. EXT= 0 (Normal INST. Mode)
8.a	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 0 1 1 1 1		SET Power Control Booster ON Regulator ON Follower ON
8.b	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 1 1 1 1		Display control. Display on
9	IIC INTERFACE Start		restart
10	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0		Slave address for write
11	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 0 0 0 0		Control byte with clear Co bit and A0 set to logic 1
12	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 0 0 1 1 0 0 0 1 0 0 1 1 0 0 0 1 0 0 1 1 0 0 0 1 0 0 1 1 0		Data Write. Y,X are initialized to 0 by default, so they aren't set here…
13	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 1 0 0 1 0 1 0 0 1 0 0 1 0 1 0 0 1 0 0 1 0 1 0 0 1 0 0 1		Data Write.
14	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 1 0 0 1 0 1 0 0 1 0 0 1 0 1 0 0 1 0 0 1 0 1 0 0 1 0 0 1		Data Write.

15	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 1 0 0 1 0 1 0 0 1 0 0 1 0 1 0 0 1 0 0 1 0 1 0 0 1 0 0 1		Data Write.
16	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 1 0 0 1 0 0 0 1 1 0 0 1 0 0 0 1 1 0 0 1 0 0 0 1 1 0 0 1 0		Data Write.
17	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		Data Write.
18	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 0 0 0 1 0 1 0 0 0 0 0 1 0 1 0 0 0 0 0 1 0 1 0 0 0 0 0 1		Data Write.
19	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1		Data Write.
20	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 0 0 0 1 0 1 0 0 0 0 0 1 0 1 0 0 0 0 0 1 0 1 0 0 0 0 0 1		Data Write.
21	IIC INTERFACE start		restart
22	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0		Slave address for write
23	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0		Control byte with set Co bit and A0 set to logic 0

24	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 1 1 1		Display Control. Set Reverse display mode REV=1
25	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0		Control byte with set Co bit and A0 set to logic 0
26	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0		Set column address of RAM. Set address to “00000000”. Y[9:2]=00000000 (Y[1:0] default is 00)
27	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 1 0 0 0 0 0 0		Control byte with set Co bit and A0 set to logic 1
28	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		Data Write.
29	IIC INTERFACE start		restart
30	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0		Slave address for write
31	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0		Control byte with set Co bit and A0 set to logic 0
32	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0		Set X address of RAM. Set address to “0000000”.
33	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0		Control byte with cleared Co bit and A0 set to logic 0

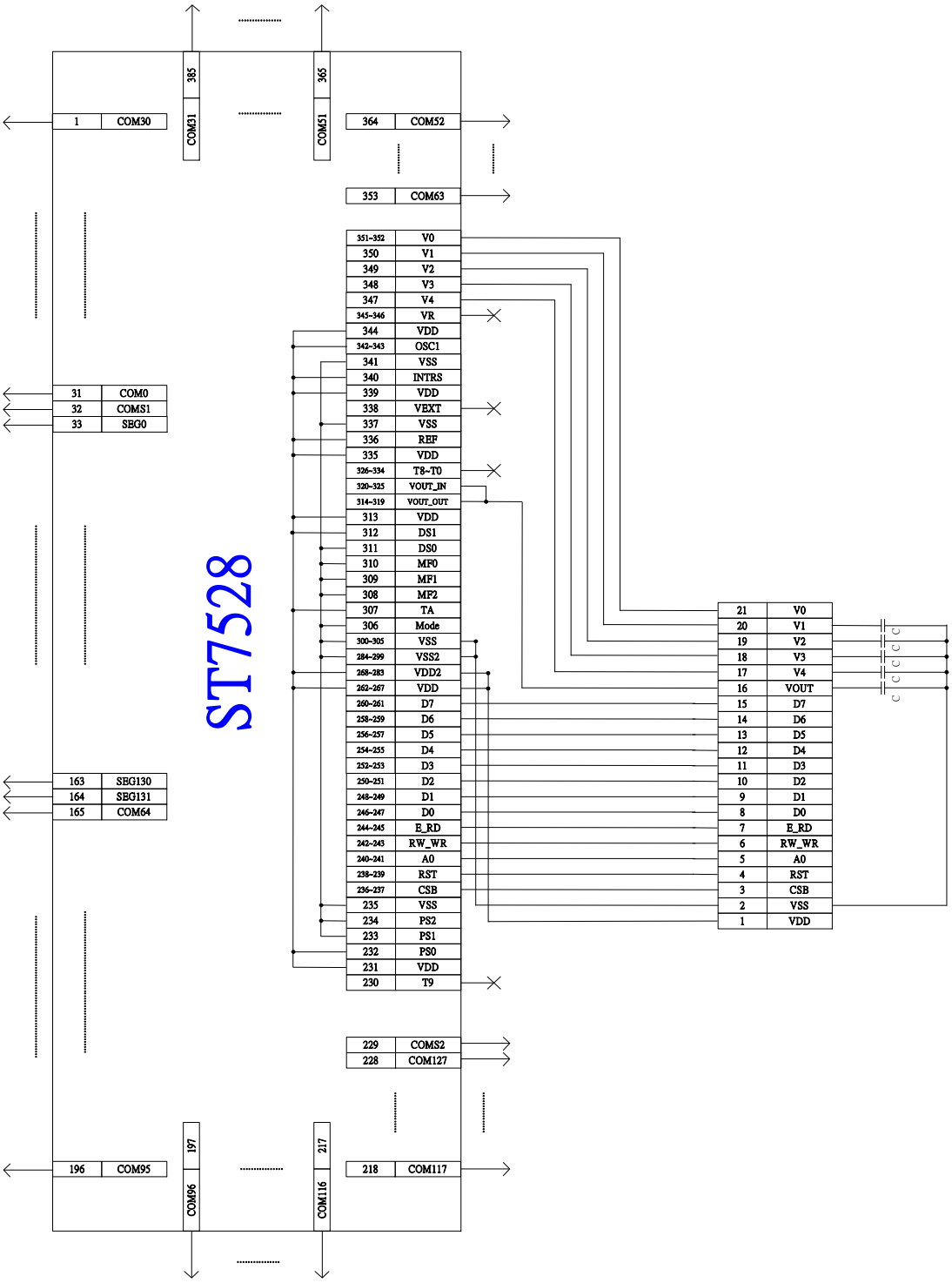
ST7528 APPICATION NOTE

ST7528

Internal analog circuit
Mode 0, Resolution : 129(128COM+ICON)*132(SEG)
Interface:8080 series
OSC1:External for input
(the same pin shoud be connected together,
for example,pin246(D0) connect to pin247(D0)
exclude power pin)

PS0:VDD
PS1:VSS
PS2:VSS
Mode:VSS
TA:VDD
REF:VDD
INTRS:VDD

VR:OPEN
VEXT:OPEN
T0~T9:OPEN
MF[2:0]:VDD OR VSS=(0,0,0)
DS[1:0]:VDD OR VSS=(1,0)
(MF[2:0]&DS[1:0] is ID of this IC,
these pins cannot be left open)
C=1uF

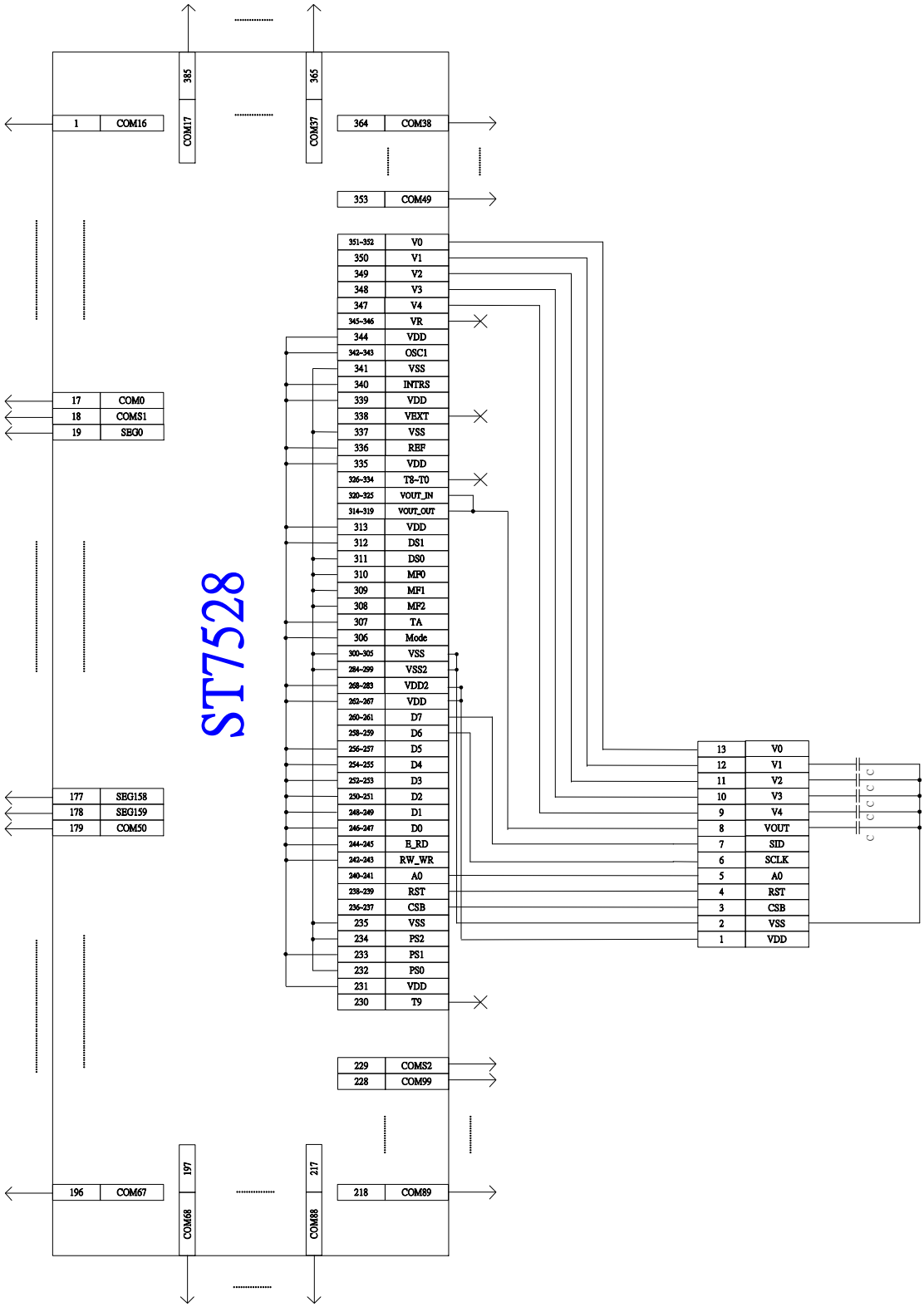


ST7528

Internal analog circuit
Mode1: Resolution : 101(100COM+ICON)*160(SEG)
Interface : 4 SPI
OSC1:External for input
(the same pin shoud be connected together,
for example,pin246(D0) connect to pin247(D0)
exclude power pin)

PS0:VSS
PS1:VDD
PS2:VSS
Mode:VDD
TA:VDD
REF:VDD
INTRS:VDD

VR:OPEN
VEXT:OPEN
T0~T9:OPEN
MF[2:0]:VDD OR VSS=(0,0,0)
DS[1:0]:VDD OR VSS=(1,0)
(MF[2:0]&DS[1:0] is ID of this IC,
these pins cannot be left open)
C=1uF

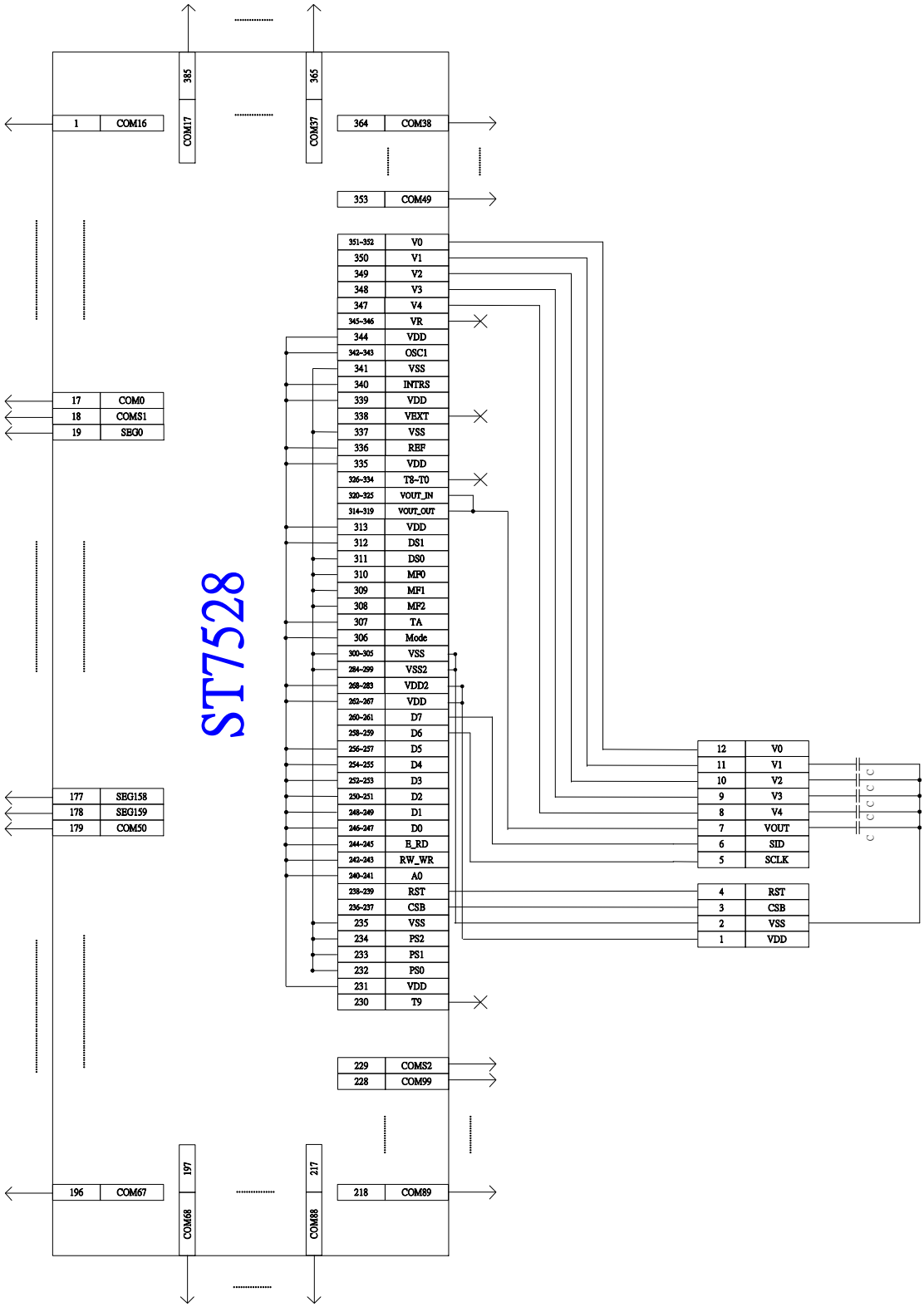


ST7528

Internal analog circuit
Mode1: Resolution : 101(100COM+ICON)*160(SEG)
Interface : 3 SPI
OSC1:External for input
(the same pin shoud be connected together,
for example,pin246(D0) connect to pin247(D0)
exclude power pin)

PS0:VSS
PS1:VSS
PS2:VSS
Mode:VDD
TA:VDD
REF:VDD
INTRS:VDD

VR:OPEN
VEXT:OPEN
T0~T9:OPEN
MF[2:0]:VDD OR VSS=(0,0,0)
DS[1:0]:VDD OR VSS=(1,0)
(MF[2:0]&DS[1:0] is ID of this IC,
these pins cannot be left open)
C=1uF

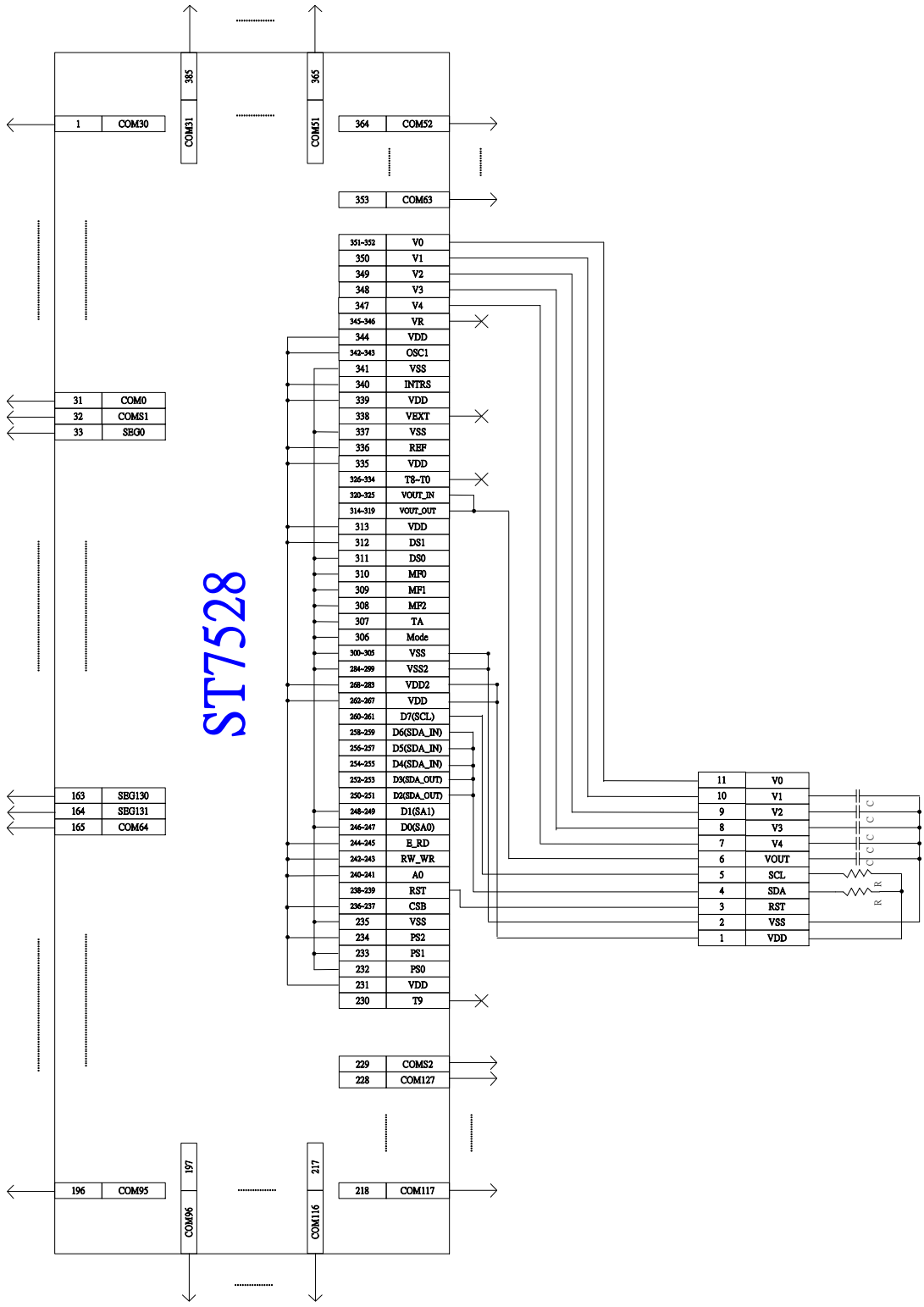


ST7528

Internal analog circuit
Mode0, Resolution : 129(128COM+ICON)*132(SEG)
Interface : I2C
OSC1:External for input
(the same pin shoud be connected together,
for example,pin246(D0) connect to pin247(D0)
exclude power pin)
SA[1:0]:VDD OR VSS=(0,0)
(SA[1:0] are Slave address of I2C)

PS0:VSS
PS1:VSS
PS2:VDD
Mode:VSS
TA:VDD
REF:VDD
INTRS:VDD

VR:OPEN
VEXT:OPEN
T0~T9:OPEN
MF[2:0]:VDD OR VSS=(0,0,0)
DS[1:0]:VDD OR VSS=(1,0)
(MF[2:0]&DS[1:0] is ID of this IC,
these pins cannot be left open)
C=1uF ; R=10K歐姆

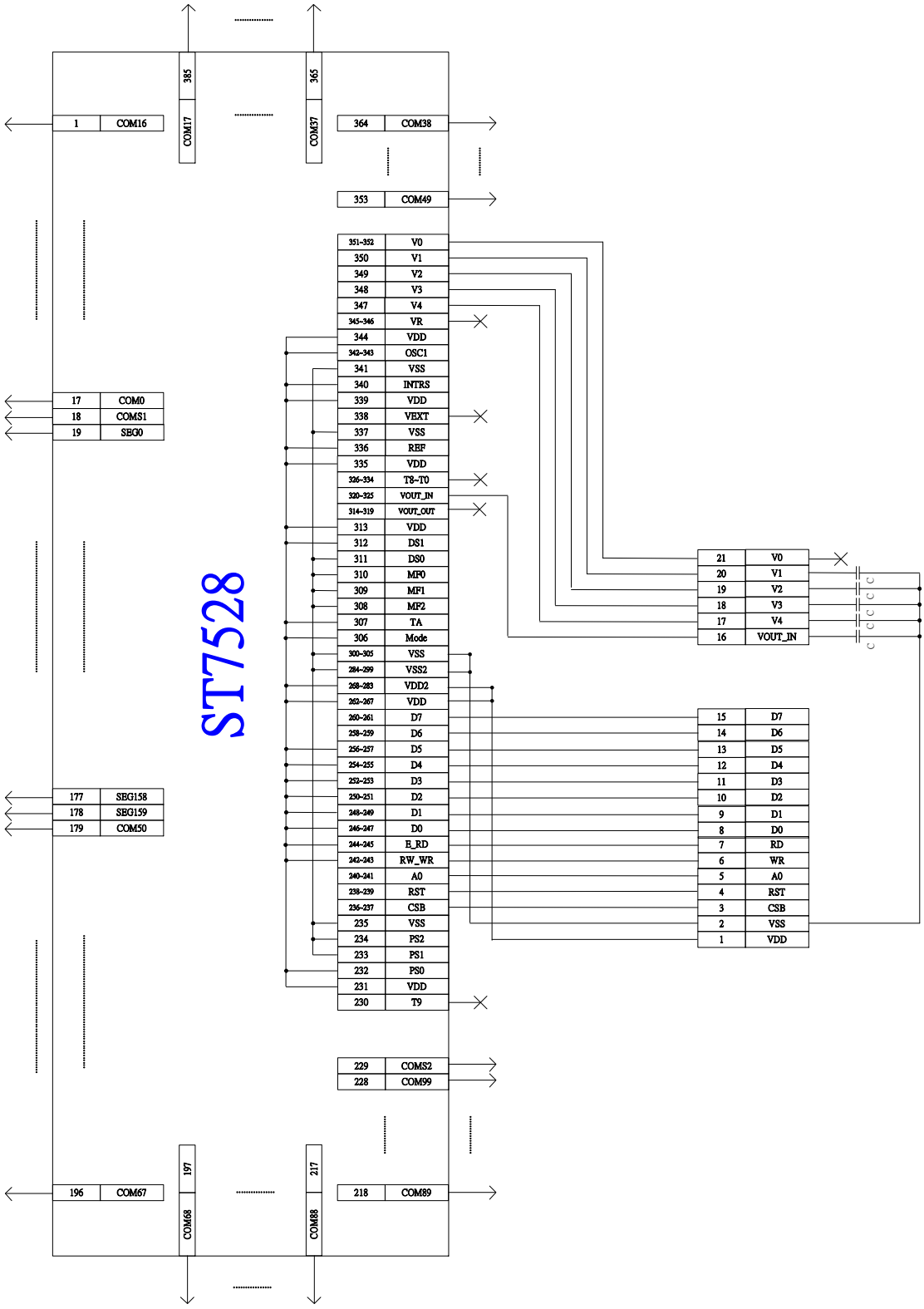


ST7528

Internal analog circuit
Mode1: Resolution : 101(100COM+ICON)*160(SEG)
Interface : 8080 interface
OSC1:External for input
External VOUT from VOUT_IN
(the same pin shoud be connected together,
for example,pin246(D0) connect to pin247(D0)
exclude power pin)

PS0:VDD
PS1:VSS
PS2:VSS
Mode:VDD
TA:VDD
REF:VDD
INTRS:VDD

VR:OPEN
VEXT:OPEN
T0~T9:OPEN
MF[2:0]:VDD OR VSS=(0,0,0)
DS[1:0]:VDD OR VSS=(1,0)
(MF[2:0]&DS[1:0] is ID of this IC,
these pins cannot be left open)
C=1uF



Reversion History

1.5V	2004/6/29	80,68,IIC Timing character definition
1.6V	2004/7/21	Modify Application Note VDD, VSS routing
1.7V	2004/10/12	Add Timing parameter , tF and tR
1.8V	2004/11/26	● Modify Vout Max limitation from 15V to 18V ● Add VEXT using range (2.0V~3.3V)
1.9V	2005/01/18	● Modify Frame rate frequency typical and Max/Min value. ● Modify 3FRC/4FRC setting description (page 33). ● Add description about the Panel Size large than 1.6”, the VOP can not set over 12 voltage. ● Add description about IIC interface can not use with other IIC slaver device. ● Modify page 29, 30 key error. ● Change “partial display duty ratio” to “select partial display line”. ● Add description on instruction of Frame Frequency to suitable for no partial display. ● Add release bias power save instruction.
2.0V	2005/10/05	● Remove page-3 “PAD NO 352 ~ 353: 913 um PAD NO 229 ~ 230: 84 um“. ● Change VDD1 to VDD.
2.1V	2005/10/20	Modify E_RD , RW_WR , Pin description, and add VR,VEXT ITO resister limitation.
2.2V	2005/12/22	Modify PAD Coordinates.
2.3V	2005/12/27	● Add DS1.DS0 recommended setting. ● Modify ADC description mistake.