Sitronix

ST7531

65K Color Dot Matrix LCD Controller/Driver

1. INTRODUCTION

The ST7531 is a driver & controller LSI for 65K color graphic dot-matrix liquid crystal display systems. It generates 256 Segment and 160 Common driver circuits. This chip is connected directly to a microprocessor, accepts Serial Peripheral Interface (SPI), 8-bit/16-bit parallel or IIC display data and stores in an on-chip display data RAM. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

Driver Output Circuits

–256 segment outputs / 160 common outputs

–Maximum resolution is 170(SPRD) x 160.

Applicable Duty Ratios

– Various partial display

– Partial window moving & data scrolling

Microprocessor Interface

– 8/16-bit parallel bi-directional interface with 6800-series or 8080-series

–4-line serial interface (write only)

–9 bit 3-line serial interface (write only)

On-chip Display Data RAM

– Capacity : 160 x 256 x 5bit = 204800bits (Max)

On-chip Low Power Analog Circuit

– On-chip oscillator circuit

– Voltage converter (x2, x3, x4, x5, x6, x7, x8)

– Voltage regulator

– Voltage follower

(LCD bias: 1/5, 1/7, 1/9, 1/10, 1/11, 1/12, 1/13, 1/14)

Operating Voltage Range

– Supply voltage

(VDD, VDD1, VDD2, VDD3, VDD4, VDD5): 2.4 to 3.3V

– LCD driving voltage (VLCD = V0 - VSS): 3.76 to 18.0 V

Temperature Gradient Coefficient

– -0.130%/℃ +/-10%

LCD driving voltage (EEPROM)

– To store contrast adjustment value for better display

Package Type

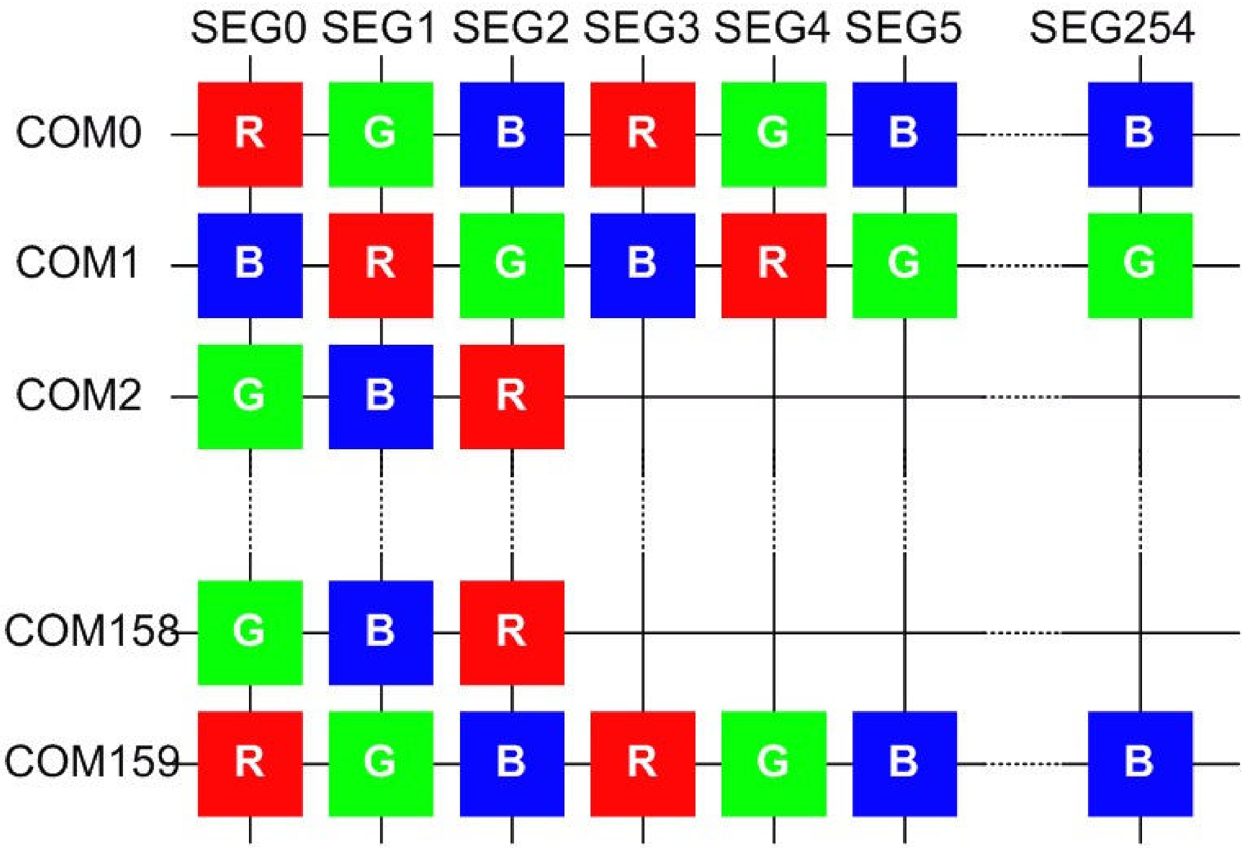
– Application for COG

ST7531	6800, 8080, 4-Line, 3-Line interface	ST

3. SPRD- B Mode Color Filter ([M1,M0] = [1,0])

The ST7531 applies SPRD- B mode color filter, which is shown in the figures below.

Note: When you use SPRD B mode, you must use this color filter placement. You can not change COM and SEG ITO layout direction.



4. Pad Arrangement

Chip Size :

16.550mm x 1.525mm

Pad pitch :

Com, Seg pad pitch: 43µm

IO pad pitch: 110µm

Test pin pad pitch: 75µm

Pad size :

Com, Seg pad size:

Pad No1~362 : 25µm (X) x 96µm (Y)

Pad No363~390 : 96µm (X) x 25µm (Y)

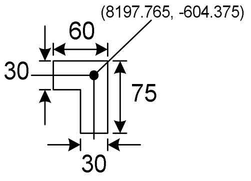
Pad No544~571 : 96µm (X) x 25µm (Y)

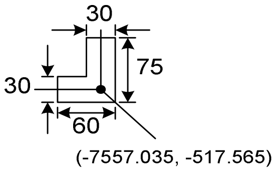
IO pad pad size: 90µm (X) x 40µm (Y)

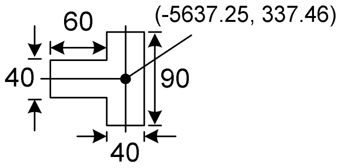
Test pin pad size: 55µm (X) x 40µm (Y)

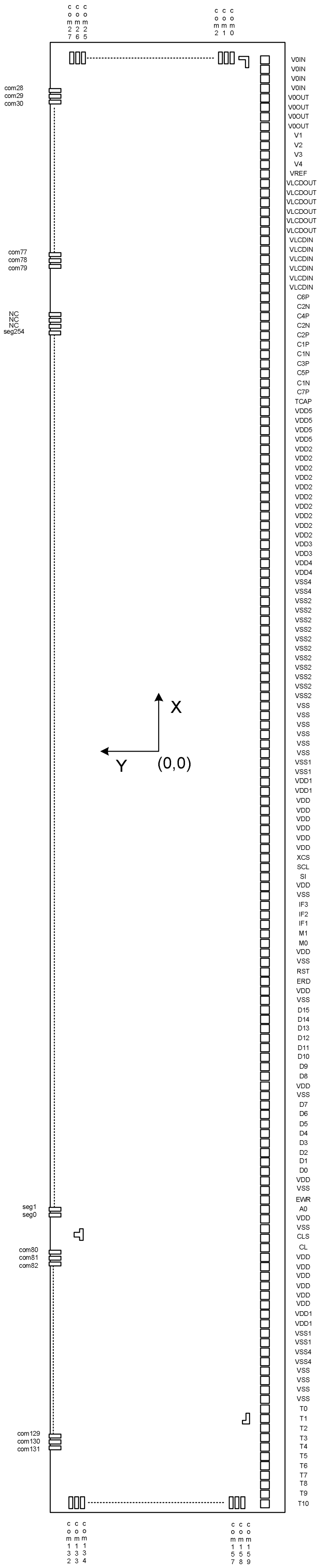
Bump Height: 17µm

Chip Thickness: 635µm









5. Pad Center Coordinates

PAD No.	PIN Name	X	Y
1	COM[28]	7917	683
2	COM[29]	7874	683
3	COM[30]	7831	683
4	COM[31]	7788	683
5	COM[32]	7745	683
6	COM[33]	7702	683
7	COM[34]	7659	683
8	COM[35]	7616	683
9	COM[36]	7573	683
10	COM[37]	7531	683
11	COM[38]	7487	683
12	COM[39]	7444	683
13	COM[40]	7401	683
14	COM[41]	7358	683
15	COM[42]	7315	683
16	COM[43]	7272	683
17	COM[44]	7229	683
18	COM[45]	7186	683
19	COM[46]	7143	683
20	COM[47]	7100	683
21	COM[48]	7057	683
22	COM[49]	7014	683
23	COM[50]	6971	683
24	COM[51]	6928	683
25	COM[52]	6885	683
26	COM[53]	6842	683
27	COM[54]	6799	683
28	COM[55]	6756	683
29	COM[56]	6713	683
30	COM[57]	6670	683
31	COM[58]	6627	683
32	COM[59]	6584	683
33	COM[60]	6541	683
34	COM[61]	6498	683
35	COM[62]	6455	683
36	COM[63]	6412	683
37	COM[64]	6369	683
38	COM[65]	6326	683
39	COM[66]	6283	683
40	COM[67]	6240	683
41	COM[68]	6197	683
42	COM[69]	6154	683
43	COM[70]	6111	683
44	COM[71]	6068	683
45	COM[72]	6025	683
46	COM[73]	5982	683
47	COM[74]	5939	683
48	COM[75]	5896	683
49	COM[76]	5853	683
50	COM[77]	5810	683
51	COM[78]	5767	683
52	COM[79]	5724	683
53	(NC)	5526	683
54	(NC)	5482	683
55	SEG[255]	5440	683
56	SEG[254]	5396	683
57	SEG[253]	5354	683
58	SEG[252]	5310	683
59	SEG[251]	5268	683
60	SEG[250]	5224	683
61	SEG[249]	5182	683
62	SEG[248]	5138	683
63	SEG[247]	5096	683
64	SEG[246]	5052	683
65	SEG[245]	5010	683
66	SEG[244]	4966	683
67	SEG[243]	4924	683
68	SEG[242]	4880	683
69	SEG[241]	4838	683
70	SEG[240]	4794	683
71	SEG[239]	4752	683
72	SEG[238]	4708	683
73	SEG[237]	4666	683
74	SEG[236]	4622	683
75	SEG[235]	4580	683
76	SEG[234]	4536	683

PAD No.	PIN Name	X	Y
77	SEG[233]	4494	683
78	SEG[232]	4450	683
79	SEG[231]	4408	683
80	SEG[230]	4364	683
81	SEG[229]	4322	683
82	SEG[228]	4278	683
83	SEG[227]	4236	683
84	SEG[226]	4192	683
85	SEG[225]	4150	683
86	SEG[224]	4106	683
87	SEG[223]	4064	683
88	SEG[222]	4020	683
89	SEG[221]	3978	683
90	SEG[220]	3934	683
91	SEG[219]	3892	683
92	SEG[218]	3848	683
93	SEG[217]	3806	683
94	SEG[216]	3762	683
95	SEG[215]	3720	683
96	SEG[214]	3676	683
97	SEG[213]	3634	683
98	SEG[212]	3590	683
99	SEG[211]	3548	683
100	SEG[210]	3504	683
101	SEG[209]	3462	683
102	SEG[208]	3418	683
103	SEG[207]	3376	683
104	SEG[206]	3332	683
105	SEG[205]	3290	683
106	SEG[204]	3246	683
107	SEG[203]	3204	683
108	SEG[202]	3160	683
109	SEG[201]	3118	683
110	SEG[200]	3074	683
111	SEG[199]	3032	683
112	SEG[198]	2988	683
113	SEG[197]	2946	683
114	SEG[196]	2902	683
115	SEG[195]	2860	683
116	SEG[194]	2816	683
117	SEG[193]	2774	683
118	SEG[192]	2730	683
119	SEG[191]	2688	683
120	SEG[190]	2644	683
121	SEG[189]	2602	683
122	SEG[188]	2558	683
123	SEG[187]	2516	683
124	SEG[186]	2472	683
125	SEG[185]	2430	683
126	SEG[184]	2386	683
127	SEG[183]	2344	683
128	SEG[182]	2300	683
129	SEG[181]	2258	683
130	SEG[180]	2214	683
131	SEG[179]	2172	683
132	SEG[178]	2128	683
133	SEG[177]	2086	683
134	SEG[176]	2042	683
135	SEG[175]	2000	683
136	SEG[174]	1956	683
137	SEG[173]	1914	683
138	SEG[172]	1870	683
139	SEG[171]	1828	683
140	SEG[170]	1784	683
141	SEG[169]	1742	683
142	SEG[168]	1698	683
143	SEG[167]	1656	683
144	SEG[166]	1612	683
145	SEG[165]	1570	683
146	SEG[164]	1526	683
147	SEG[163]	1484	683
148	SEG[162]	1440	683
149	SEG[161]	1398	683
150	SEG[160]	1354	683
151	SEG[159]	1312	683
152	SEG[158]	1268	683
153	SEG[157]	1226	683
154	SEG[156]	1182	683

PAD No.	PIN Name	X	Y
155	SEG[155]	1140	683
156	SEG[154]	1096	683
157	SEG[153]	1054	683
158	SEG[152]	1010	683
159	SEG[151]	968	683
160	SEG[150]	924	683
161	SEG[149]	882	683
162	SEG[148]	838	683
163	SEG[147]	796	683
164	SEG[146]	752	683
165	SEG[145]	710	683
166	SEG[144]	666	683
167	SEG[143]	624	683
168	SEG[142]	580	683
169	SEG[141]	538	683
170	SEG[140]	494	683
171	SEG[139]	452	683
172	SEG[138]	408	683
173	SEG[137]	366	683
174	SEG[136]	322	683
175	SEG[135]	280	683
176	SEG[134]	236	683
177	SEG[133]	194	683
178	SEG[132]	150	683
179	SEG[131]	108	683
180	SEG[130]	64	683
181	SEG[129]	22	683
182	SEG[128]	-22	683
183	SEG[127]	-64	683
184	SEG[126]	-108	683
185	SEG[125]	-150	683
186	SEG[124]	-194	683
187	SEG[123]	-236	683
188	SEG[122]	-280	683
189	SEG[121]	-322	683
190	SEG[120]	-366	683
191	SEG[119]	-408	683
192	SEG[118]	-452	683
193	SEG[117]	-494	683
194	SEG[116]	-538	683
195	SEG[115]	-580	683
196	SEG[114]	-624	683
197	SEG[113]	-666	683
198	SEG[112]	-710	683
199	SEG[111]	-752	683
200	SEG[110]	-796	683
201	SEG[109]	-838	683
202	SEG[108]	-882	683
203	SEG[107]	-924	683
204	SEG[106]	-968	683
205	SEG[105]	-1010	683
206	SEG[104]	-1054	683
207	SEG[103]	-1096	683
208	SEG[102]	-1140	683
209	SEG[101]	-1182	683
210	SEG[100]	-1226	683
211	SEG[99]	-1268	683
212	SEG[98]	-1312	683
213	SEG[97]	-1354	683
214	SEG[96]	-1398	683
215	SEG[95]	-1440	683
216	SEG[94]	-1484	683
217	SEG[93]	-1526	683
218	SEG[92]	-1570	683
219	SEG[91]	-1612	683
220	SEG[90]	-1656	683
221	SEG[89]	-1698	683
222	SEG[88]	-1742	683
223	SEG[87]	-1784	683
224	SEG[86]	-1828	683
225	SEG[85]	-1870	683
226	SEG[84]	-1914	683
227	SEG[83]	-1956	683
228	SEG[82]	-2000	683
229	SEG[81]	-2042	683
230	SEG[80]	-2086	683
231	SEG[79]	-2128	683
232	SEG[78]	-2172	683

PAD No.	PIN Name	X	Y
233	SEG[77]	-2214	683
234	SEG[76]	-2258	683
235	SEG[75]	-2300	683
236	SEG[74]	-2344	683
237	SEG[73]	-2386	683
238	SEG[72]	-2430	683
239	SEG[71]	-2472	683
240	SEG[70]	-2516	683
241	SEG[69]	-2558	683
242	SEG[68]	-2602	683
243	SEG[67]	-2644	683
244	SEG[66]	-2688	683
245	SEG[65]	-2730	683
246	SEG[64]	-2774	683
247	SEG[63]	-2816	683
248	SEG[62]	-2860	683
249	SEG[61]	-2902	683
250	SEG[60]	-2946	683
251	SEG[59]	-2988	683
252	SEG[58]	-3032	683
253	SEG[57]	-3074	683
254	SEG[56]	-3118	683
255	SEG[55]	-3160	683
256	SEG[54]	-3204	683
257	SEG[53]	-3246	683
258	SEG[52]	-3290	683
259	SEG[51]	-3332	683
260	SEG[50]	-3376	683
261	SEG[49]	-3418	683
262	SEG[48]	-3462	683
263	SEG[47]	-3504	683
264	SEG[46]	-3548	683
265	SEG[45]	-3590	683
266	SEG[44]	-3634	683
267	SEG[43]	-3676	683
268	SEG[42]	-3720	683
269	SEG[41]	-3762	683
270	SEG[40]	-3806	683
271	SEG[39]	-3848	683

PAD No.	PIN Name	X	Y
272	SEG[38]	-3892	683
273	SEG[37]	-3934	683
274	SEG[36]	-3978	683
275	SEG[35]	-4020	683
276	SEG[34]	-4064	683
277	SEG[33]	-4106	683
278	SEG[32]	-4150	683
279	SEG[31]	-4192	683
280	SEG[30]	-4236	683
281	SEG[29]	-4278	683
282	SEG[28]	-4322	683
283	SEG[27]	-4364	683
284	SEG[26]	-4408	683
285	SEG[25]	-4450	683
286	SEG[24]	-4494	683
287	SEG[23]	-4536	683
288	SEG[22]	-4580	683
289	SEG[21]	-4622	683
290	SEG[20]	-4666	683
291	SEG[19]	-4708	683
292	SEG[18]	-4752	683
293	SEG[17]	-4794	683
294	SEG[16]	-4838	683
295	SEG[15]	-4880	683
296	SEG[14]	-4924	683
297	SEG[13]	-4966	683
298	SEG[12]	-5010	683
299	SEG[11]	-5052	683
300	SEG[10]	-5096	683
301	SEG[9]	-5138	683
302	SEG[8]	-5182	683
303	SEG[7]	-5224	683
304	SEG[6]	-5268	683
305	SEG[5]	-5310	683
306	SEG[4]	-5354	683
307	SEG[3]	-5396	683
308	SEG[2]	-5440	683
309	SEG[1]	-5482	683
310	SEG[0]	-5526	683

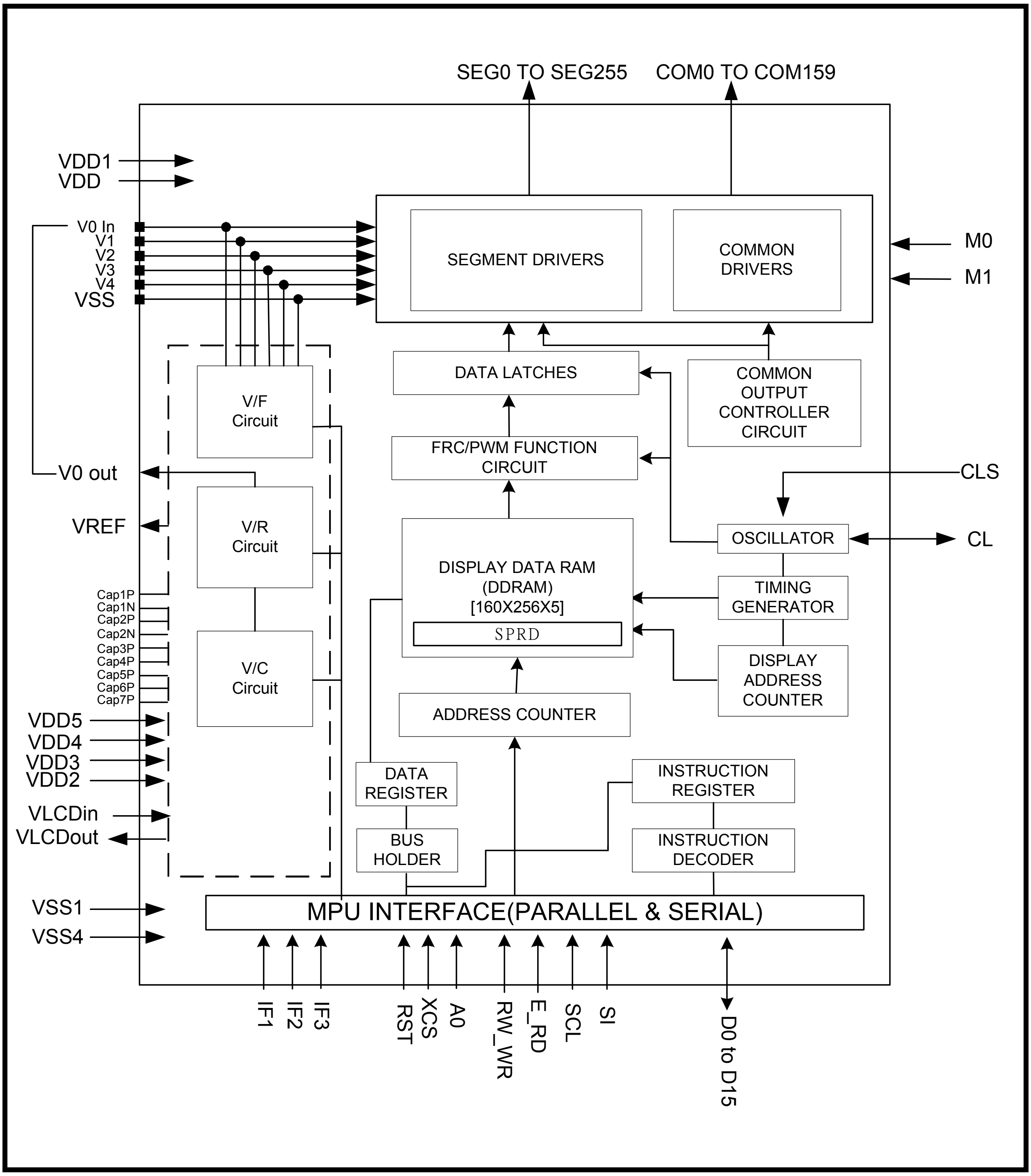
PAD No.	PIN Name	X	Y
311	COM[80]	-5724	683
312	COM[81]	-5767	683
313	COM[82]	-5810	683
314	COM[83]	-5853	683
315	COM[84]	-5896	683
316	COM[85]	-5939	683
317	COM[86]	-5982	683
318	COM[87]	-6025	683
319	COM[88]	-6068	683
320	COM[89]	-6111	683
321	COM[90]	-6154	683
322	COM[91]	-6197	683
323	COM[92]	-6240	683
324	COM[93]	-6283	683
325	COM[94]	-6326	683
326	COM[95]	-6369	683
327	COM[96]	-6412	683
328	COM[97]	-6455	683
329	COM[98]	-6498	683
330	COM[99]	-6541	683
331	COM[100]	-6584	683
332	COM[101]	-6627	683
333	COM[102]	-6670	683
334	COM[103]	-6713	683
335	COM[104]	-6756	683
336	COM[105]	-6799	683
337	COM[106]	-6842	683
338	COM[107]	-6885	683
339	COM[108]	-6928	683
340	COM[109]	-6971	683
341	COM[110]	-7014	683
342	COM[111]	-7057	683
343	COM[112]	-7100	683
344	COM[113]	-7143	683
345	COM[114]	-7186	683
346	COM[115]	-7229	683
347	COM[116]	-7272	683
348	COM[117]	-7315	683
349	COM[118]	-7358	683
350	COM[119]	-7401	683
351	COM[120]	-7444	683
352	COM[121]	-7487	683
353	COM[122]	-7531	683
354	COM[123]	-7573	683
355	COM[124]	-7616	683
356	COM[125]	-7659	683
357	COM[126]	-7702	683
358	COM[127]	-7745	683
359	COM[128]	-7788	683
360	COM[129]	-7831	683
361	COM[130]	-7874	683
362	COM[131]	-7917	683
363	COM[132]	-8196	661
364	COM[133]	-8196	618
365	COM[134]	-8196	575
366	COM[135]	-8196	532
367	COM[136]	-8196	489
368	COM[137]	-8196	446
369	COM[138]	-8196	403
370	COM[139]	-8196	360
371	COM[140]	-8196	317
372	COM[141]	-8196	274
373	COM[142]	-8196	231
374	COM[143]	-8196	188
375	COM[144]	-8196	145
376	COM[145]	-8196	102
377	COM[146]	-8196	59
378	COM[147]	-8196	16
379	COM[148]	-8196	-27
380	COM[149]	-8196	-70
381	COM[150]	-8196	-113
382	COM[151]	-8196	-156
383	COM[152]	-8196	-199
384	COM[153]	-8196	-242
385	COM[154]	-8196	-285
386	COM[155]	-8196	-328
387	COM[156]	-8196	-371
388	COM[157]	-8196	-414

PAD No.	PIN Name	X	Y
389	COM[158]	-8196	-457
390	COM[159]	-8196	-500
391	T[10]	-8197	-712
392	T[9]	-8122	-712
393	T[8]	-8047	-712
394	T[7]	-7972	-712
395	T[6]	-7897	-712
396	T[5]	-7822	-712
397	T[4]	-7747	-712
398	T[3]	-7672	-712
399	T[2]	-7597	-712
400	T[1]	-7522	-712
401	T[0]	-7447	-712
402	VSS	-7355	-712
403	VSS	-7245	-712
404	VSS	-7135	-712
405	VSS	-7025	-712
406	VSS4	-6915	-712
407	VSS4	-6805	-712
408	VSS1	-6695	-712
409	VSS1	-6585	-712
410	VDD1	-6475	-712
411	VDD1	-6365	-712
412	VDD	-6255	-712
413	VDD	-6145	-712
414	VDD	-6035	-712
415	VDD	-5925	-712
416	VDD	-5815	-712
417	VDD	-5705	-712
418	CL	-5595	-712
419	CLS	-5485	-712
420	VSS	-5375	-712
421	VDD	-5265	-712
422	A0	-5155	-712
423	RW_WR	-5045	-712
424	VSS	-4935	-712
425	VDD	-4825	-712
426	D0	-4715	-712
427	D1	-4605	-712
428	D2	-4495	-712
429	D3	-4385	-712
430	D4	-4275	-712
431	D5	-4165	-712
432	D6	-4055	-712
433	D7	-3945	-712
434	VSS	-3835	-712
435	VDD	-3725	-712
436	D8	-3615	-712
437	D9	-3505	-712
438	D10	-3395	-712
439	D11	-3285	-712
440	D12	-3175	-712
441	D13	-3065	-712
442	D14	-2955	-712
443	D15	-2845	-712
444	VSS	-2735	-712
445	VDD	-2625	-712
446	E_RD	-2515	-712
447	RST	-2405	-712
448	VSS	-2295	-712
449	VDD	-2185	-712
450	M0	-2075	-712
451	M1	-1965	-712
452	IF1	-1855	-712
453	IF2	-1745	-712
454	IF3	-1635	-712
455	VSS	-1525	-712
456	VDD	-1415	-712
457	SI	-1305	-712
458	SCL	-1195	-712
459	XCS	-1085	-712
460	VDD	-975	-712
461	VDD	-865	-712
462	VDD	-755	-712
463	VDD	-645	-712
464	VDD	-535	-712
465	VDD	-425	-712
466	VDD1	-315	-712

PAD No.	PIN Name	X	Y
467	VDD1	-205	-712
468	VSS1	-95	-712
469	VSS1	15	-712
470	VSS	125	-712
471	VSS	235	-712
472	VSS	345	-712
473	VSS	455	-712
474	VSS	565	-712
475	VSS	675	-712
476	VSS2	785	-712
477	VSS2	895	-712
478	VSS2	1005	-712
479	VSS2	1115	-712
480	VSS2	1225	-712
481	VSS2	1335	-712
482	VSS2	1445	-712
483	VSS2	1555	-712
484	VSS2	1665	-712
485	VSS2	1775	-712
486	VSS2	1885	-712
487	VSS4	1995	-712
488	VSS4	2105	-712
489	VDD4	2215	-712
490	VDD4	2325	-712
491	VDD3	2435	-712
492	VDD3	2545	-712
493	VDD2	2655	-712
494	VDD2	2765	-712
495	VDD2	2875	-712
496	VDD2	2985	-712
497	VDD2	3095	-712
498	VDD2	3205	-712
499	VDD2	3315	-712
500	VDD2	3425	-712
501	VDD2	3535	-712
502	VDD2	3645	-712
503	VDD5	3755	-712
504	VDD5	3865	-712
505	VDD5	3975	-712
506	VDD5	4085	-712
507	TCAP	4195	-712
508	C7P	4305	-712
509	C1N	4415	-712
510	C5P	4525	-712
511	C3P	4635	-712
512	C1N	4745	-712
513	C1P	4855	-712
514	C2P	4965	-712
515	C2N	5075	-712
516	C4P	5185	-712
517	C2N	5295	-712
518	C6P	5405	-712
519	VLCDIN	5515	-712
520	VLCDIN	5625	-712
521	VLCDIN	5735	-712
522	VLCDIN	5845	-712
523	VLCDIN	5955	-712
524	VLCDIN	6065	-712
525	VLCDOUT	6175	-712
526	VLCDOUT	6285	-712
527	VLCDOUT	6395	-712
528	VLCDOUT	6505	-712
529	VLCDOUT	6615	-712
530	VLCDOUT	6725	-712
531	VREF	6835	-712
532	V4	6945	-712
533	V3	7055	-712
534	V2	7165	-712
535	V1	7275	-712
536	V0OUT	7385	-712
537	V0OUT	7495	-712
538	V0OUT	7605	-712
539	V0OUT	7715	-712
540	V0IN	7825	-712
541	V0IN	7935	-712
542	V0IN	8045	-712
543	V0IN	8155	-712
544	COM[0]	8196	-500

PAD No.	PIN Name	X	Y
545	COM[1]	8196	-457
546	COM[2]	8196	-414
547	COM[3]	8196	-371
548	COM[4]	8196	-328
549	COM[5]	8196	-285
550	COM[6]	8196	-242
551	COM[7]	8196	-199
552	COM[8]	8196	-156
553	COM[9]	8196	-113
554	COM[10]	8196	-70
555	COM[11]	8196	-27
556	COM[12]	8196	16
557	COM[13]	8196	59
558	COM[14]	8196	102
559	COM[15]	8196	145
560	COM[16]	8196	188
561	COM[17]	8196	231
562	COM[18]	8196	274
563	COM[19]	8196	317
564	COM[20]	8196	360
565	COM[21]	8196	403
566	COM[22]	8196	446
567	COM[23]	8196	489
568	COM[24]	8196	532
569	COM[25]	8196	575
570	COM[26]	8196	618
571	COM[27]	8196	661

f. BLOCK DIAGRAM



7. PIN DESCRIPTION

7.1 POWER SUPPLY

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>VDD</td><td>Supply</td><td>Power supply for logic circuit</td></tr>
<tr><td>VDD1</td><td>Supply</td><td>Power supply for OSC circuit</td></tr>
<tr><td>VDD2</td><td>Supply</td><td>Power supply for Booster Circuit</td></tr>
<tr><td>VDD3
VDD4
VDD5</td><td>Supply</td><td>Power supply for LCD</td></tr>
<tr><td>VSS
VSS1
VSS4</td><td>Supply</td><td>Ground. Ground system should be connected together.</td></tr>
<tr><td>V_{LCDOUT}</td><td>Supply</td><td>If the internal voltage generator is used, the V_{LCDIN} & V_{LCDOUT} must be connected together.
If an external supply is used, this pin must be left open.</td></tr>
<tr><td>V_{LCDIN}</td><td>Supply</td><td>An external LCD supply voltage can be supplied using the V_{LCDIN} pad. In this case, V_{LCDOUT} has to be left open, and the internal voltage generator has to be programmed to zero. (SET register VB=0)</td></tr>
<tr><td>V0In
V0out
V1
V2
V3
V4</td><td>Supply</td><td>LCD driver supply voltages
V0In & V0out should be connected together in FPC area.
Voltages should have the following relationship:
$V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq VSS$
When the internal power circuit is active, these voltages are generated as the following table according to the state of LCD bias.
<table>
<tr><th>LCD bias</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr>
<tr><th>1/N bias</th><td>(N-1) / N x V0</td><td>(N-2) / N x V0</td><td>(2/N) x V0</td><td>(1/N) x V0</td></tr>
</table>
NOTE: N = 5 to 14</td></tr>
</table>

7.2 LCD DRIVER SUPPLY

Name	I/O	Description
VREF	O	Reference voltage output for monitor only. Leave it open.
CLS	I	When using internal clock oscillator, connect CLS to VDD. When using external clock oscillator, connect CLS to VSS.
CL	I/O	When using internal clock oscillator, it is the output of oscillator. When using external clock oscillator, it is the input of oscillator.

7.3 SYSTEM CONTROL

Name	I/O	Description
TCAP	O	Test pin. Leave it open.
T[0]~T[10]	---	Test pin. Leave it open.

7.4 MICROPROCESSOR INTERFACE

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>M0, M1</td><td>I</td><td>M0 must be fixed to Vss.
M1 must fixed to VDD.
This pin is reserved for internal setting.</td></tr>
<tr><td>RST</td><td>I</td><td>Reset input pin
When RST is “L”, initialization is executed.</td></tr>
<tr><td>XCS</td><td>I</td><td>Chip select input pins
Data/instruction I/O is enabled only when XCS is "L". When chip select is non-active, DB0 to DB15 may be high impedance.</td></tr>
<tr><td>IF[3:1]</td><td>I</td><td>Parallel / Serial data input select input
<table>
<tr><th>IF1</th><th>IF2</th><th>IF3</th><th>MPU interface type</th></tr>
<tr><td>H</td><td>H</td><td>H</td><td>80 series 16-bit parallel</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>80 series 8-bit parallel</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>68 series 16-bit parallel</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>68 series 8-bit parallel</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>9-bit serial (3 line)</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>8-bit serial (4 line)</td></tr>
</table></td></tr>
<tr><td>A0</td><td>I</td><td>Register select input pin
– A0 = "H": DB0 to DB15 or SI are display data
– A0 = "L": DB0 to DB15 or SI are control data</td></tr>
<tr><td>RW_WR</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>MPU type</th><th>RW_WR</th><th>Description</th></tr>
<tr><td>6800-series</td><td>RW</td><td>Read / Write control input pin
RW = “H” : read
RW = “L” : write</td></tr>
<tr><td>8080-series</td><td>/WR</td><td>Write enable clock input pin
The data on DB0 to DB15 are latched at the rising edge of the /WR signal.</td></tr>
</table></td></tr>
<tr><td>E_RD</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>MPU Type</th><th>E_RD</th><th>Description</th></tr>
<tr><td>6800-series</td><td>E</td><td>Read / Write control input pin
– RW = “H”: When E is “H”, DB0 to DB15 are in an output status.
– RW = “L”: The data on DB0 to DB15 are latched at the falling edge of the E signal.</td></tr>
<tr><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is “L”, DB0 to DB15 are in an output status.</td></tr>
</table></td></tr>
<tr><td>D15 to D0</td><td>I/O</td><td>They connect to the standard 8-bit or 16-bit MPU bus via the 8/16 –bit bi-directional bus.
When the following interface is selected and the XCS pin is high, the following pins become high impedance, which should be fixed to V_{DD} or V_{SS}.
1. 8-bit parallel: D15-D8 are in the state of high impedance
2. Serial interface: D15-D0 are in the state of high impedance</td></tr>
<tr><td>SI</td><td>I</td><td>This pin is used to input serial data when the serial interface is selected. (3 line and 4 line)</td></tr>
<tr><td>SCL</td><td>I</td><td>This pin is used to input serial clock when the serial interface is selected.
The data is latched at the rising edge. (3 line and 4 line)</td></tr>
</table>

NOTE:

Microprocessor interface pins should not be floating in any operation mode.

7.5 LCD DRIVER OUTPUTS

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>SEG0
to
SEG255</td><td>O</td><td>LCD segment driver outputs
The display data and the M signal control the output voltage of segment driver.
<table>
<tr><th rowspan="2">Display data</th><th rowspan="2">M (Internal)</th><th colspan="2">Segment driver output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>VSS</td></tr>
<tr><td colspan="2">Power save mode</td><td>VSS</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COM0
to
COM159</td><td>O</td><td>LCD common driver outputs
The internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><th>Scan data</th><th>M (Internal)</th><th>Common driver output voltage</th></tr>
<tr><td>H</td><td>H</td><td>VSS</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
<tr><td colspan="2">Power save mode</td><td>VSS</td></tr>
</table></td></tr>
</table>

8. FUNCTIONAL DESCRIPTION

8.1 MICROPROCESSOR INTERFACE

Chip Select Input

The XCS pin is for chip selection. The ST7531 can function with an MPU when XCS is "L". In case of serial interface, the internal shift register and the counter are reset.

8.1.1 Selecting Parallel / Serial Interface

ST7531 has six types of interface with an MPU, which are four parallel and three serial interfaces. This parallel or serial interface is determined by IF pin as shown in table 8.1.1.

Table 8.1.1 Parallel / Serial Interface Mode

IF1	IF2	IF3	Interface type	XCS	A0	/RD(E)	/WR(R/W)	D15 to D8	D7 to D0	SI	SCL	ACK
H	H	H	80 serial 16-bit parallel	XCS	A0	/RD	/WR	D15 to D8	D7 to D0	--	--	--
H	H	L	80 serial 8-bit parallel	XCS	A0	/RD	/WR	--	D7 to D0	--	--	--
H	L	L	68 serial 16-bit parallel	XCS	A0	E	R/W	D15 to D8	D7 to D0	--	--	--
L	H	H	68 serial 8-bit parallel	XCS	A0	E	R/W	--	D7 to D0	--	--	--
L	L	H	9-bit SPI mode (3 line)	XCS	--	--	--	--		SI	SCL	--
L	L	L	8-bit SPI mode (4 line)	XCS	A0	--	--	--		SI	SCL	--

Note: "--" means "disabled" in pins A0, E_RD, and RW_WR, and "high impedance" in pins DB0 to DB15.

8.1.2 8- or 16-bit Parallel Interface

The ST7531 identifies the type of the data bus signals according to the combination of A0, /RD (E) and /WR (W/R) as shown in table 8.1.2.

Table 8.1.2 Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	R/W	E	/RD	/WR	
H	H	H	L	H	Display data read out
H	L	H	H	L	Display data write
L	H	H	L	H	Register status read
L	L	H	H	L	Writes to internal register (instruction)

Relation between Data Bus and Gradation Data

ST7531 offers the dithered 65K, dithered 262K, and dithered 16M color display.

When using 65K, 262K, and 16M color, you can specify color for each of R, G, B using the palette function.

(1) 65K color display

1. 8-bit mode

D7	D6	D5	D4	D3	D2	D1	D0	
R	R	R	R	R	G	G	G	1st write
G	G	G	B	B	B	B	B	2nd write

A single pixel of data is read after the second write operation as shown, and it is written in the display RAM.

2. 16-bit mode

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	R	R	R	R	G	G	G	G	G	G	B	B	B	B	B

Data is acquired through the operation of writing signal, and then written to the display RAM.

(2) 262K color display

1. 8-bit mode

D7	D6	D5	D4	D3	D2	D1	D0	
R	R	R	R	R	R	X	X	1st write
G	G	G	G	G	G	X	X	2nd write
B	B	B	B	B	B	X	X	3rd write

A single pixel of data is read after the third write operation as shown, and it is written in the display RAM.

2. 16 bit mode

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
R	R	R	R	R	R	X	X	G	G	G	G	G	G	X	X	1st write
B	B	B	B	B	B	X	X	X	X	X	X	X	X	X	X	2nd write

A single pixel of data is read after the second write operation as shown, and it is written in the display RAM.

“XXXX” are dummy bits, which are ignored for display.

(3) 16M color display

1. 8-bit mode

D7	D6	D5	D4	D3	D2	D1	D0	
R	R	R	R	R	R	R	R	1st write
G	G	G	G	G	G	G	G	2nd write
B	B	B	B	B	B	B	B	3rd write

A single pixel of data is read after the third write operation as shown, and it is written in the display RAM.

2. 16 bit mode

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
R	R	R	R	R	R	R	R	G	G	G	G	G	G	G	G	1st write
B	B	B	B	B	B	B	B	X	X	X	X	X	X	X	X	2nd write

A single pixel of data is read after the second write operation as shown, and it is written in the display RAM.

8.1.3 8-bit (4 line) and 9-bit (3 line) Serial Interface

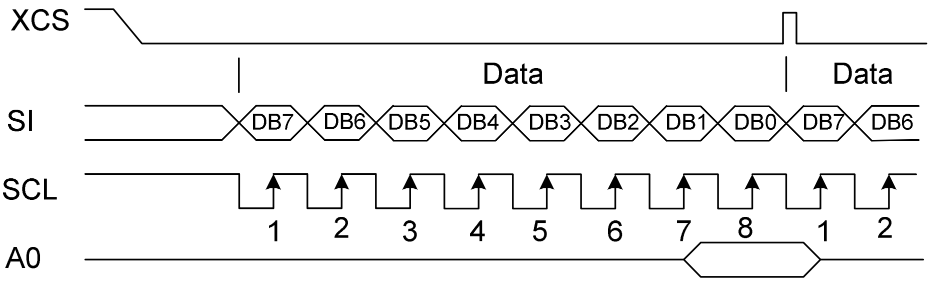
The 8-bit serial interface uses four pins XCS, SI, SCL, and A0 to enter commands and data. Meanwhile, the 9-bit serial interface uses three pins XCS, SI and SCL for the same purpose.

Data read is not available in the serial interface. The entered data must be 8 bits. Refer to the following chart for entering commands, parameters or gray-scale data.

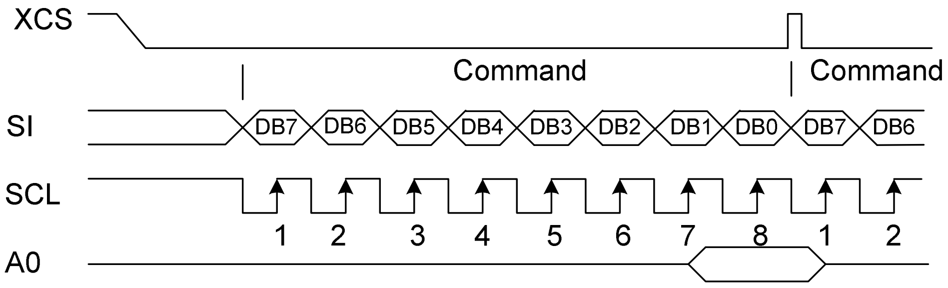
The relation between gray-scale data and data bus in the serial input is the same as that in the 8-bit parallel interface mode at every gradation.

(1) 8-bit serial interface (4 line)

When entering data (parameters): A0= HIGH at the rising edge of the 8th SCL.

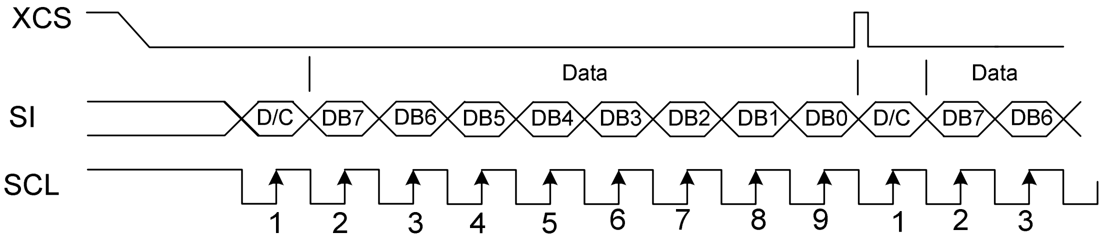


When entering command: A0= LOW at the rising edge of the 8th SCL

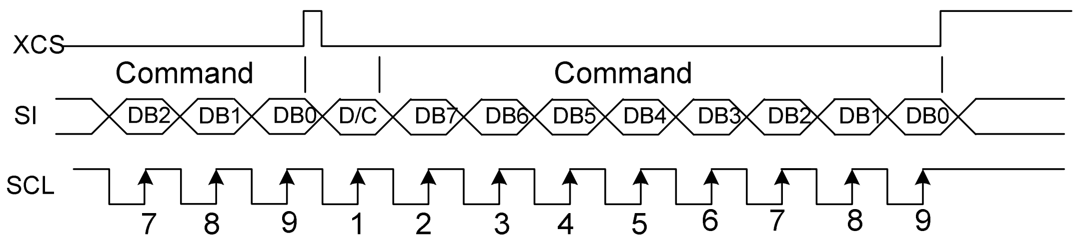


(2) 9-bit serial interface (3 line)

When entering data (parameters): SI= HIGH at the rising edge of the 1st SCL.



When entering command: SI= LOW at the rising edge of the 1st SCL.



- If XCS is set to HIGH while the 8 bits from D7 to D0 are entered, the data concerned is invalid. Before entering succeeding sets of data, you must correctly input the data concerned again.
- In order to avoid data transfer error due to incoming noise, it is recommended to set XCS at HIGH on byte basis to initialize the serial-to-parallel conversion counter and the register.
- When executing the command RAMWR, set XCS to HIGH after writing the last address (after starting the 9th pulse in case of 9-bit serial input or after starting the 8th pulse in case of 8-bit serial input).

8.2 ACCESS TO DDRAM AND INTERNAL REGISTERS

Since ST7531 access from MPU by pipeline processing via the bus holder attached to the internal that requires only the cycle time but no waiting time, it can achieves high-speed data transfer.

For example, when MPU writes data to the DDRAM, the data is once held by the bus holder and then written to the DDRAM before the succeeding write cycle start. When MPU reads data from the DDRAM, the first read cycle is dummy and the data read in the dummy cycle is held by the bus holder, and then it read from the bus holder to the system bus in the succeeding read cycle. Fig. 8.2.1 illustrates these relations.

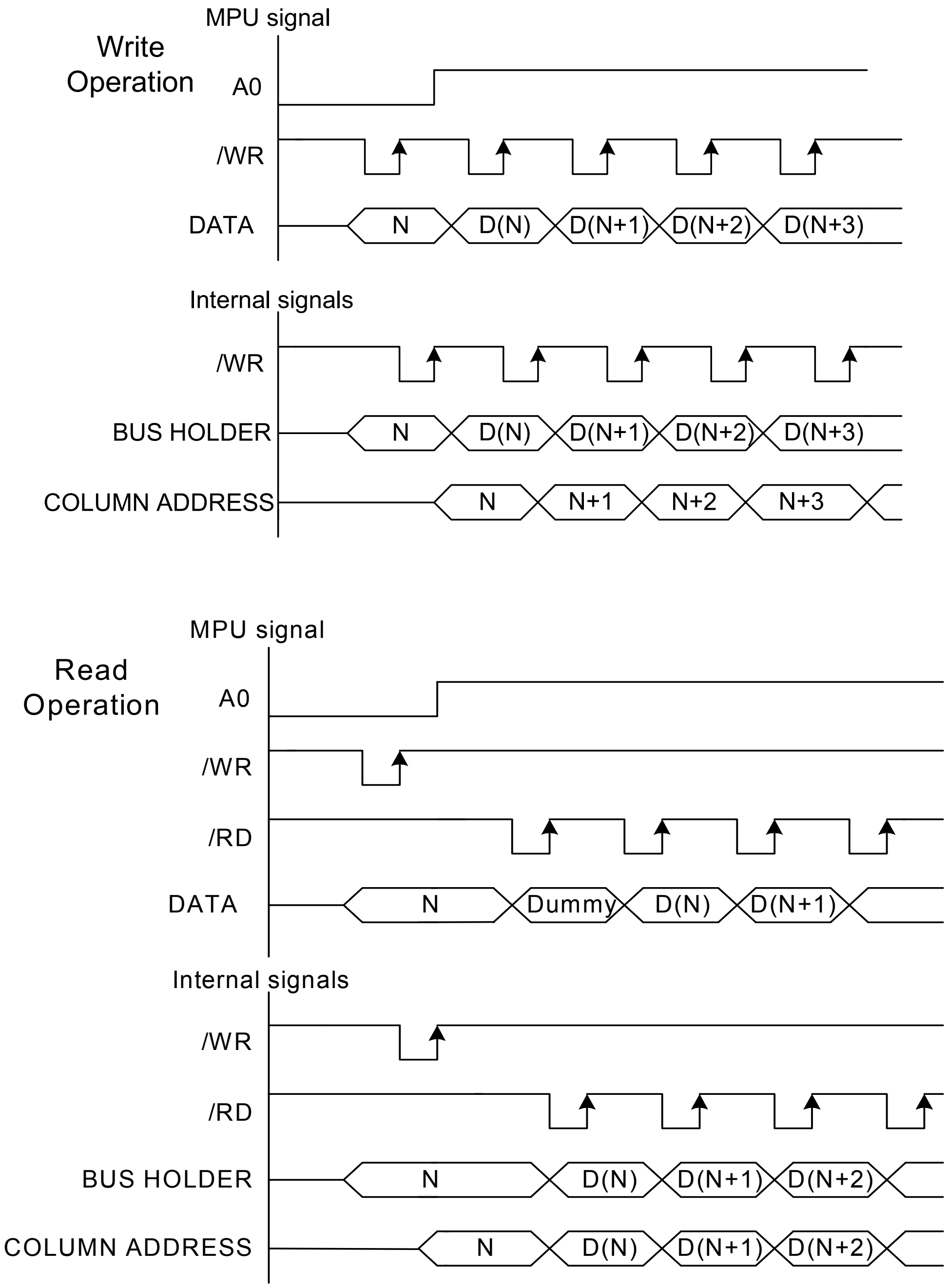


Fig 8.2.1

8.3 DISPLAY DATA RAM (DDRAM)

8.3.1 DDRAM

It is 160 X 256 X 5 bits capacity RAM prepared for storing dot data. You can access a desired bit by specifying the LINE address and column address. Since the display data from MCU D7 to D0 and D15 to D8 correspond to one or two pixels, data transfer related restrictions are reduced, and the display would be flexible.

The RAM on ST7531 is separated to a block per 4 lines to allow the display system to process data on the block basis.

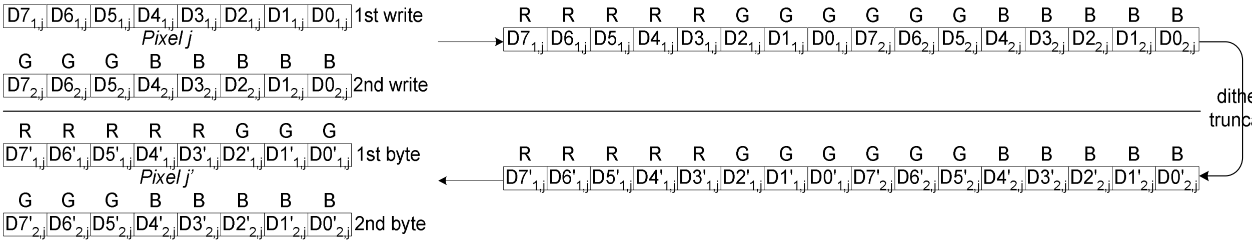
The reading and writing RAM operations of MPU are performed via the I/O buffer circuit. Reading of the RAM for the liquid crystal drive is controlled from another separate circuit.

Refer to the following memory map for the RAM configuration.

Memory Map (using the 32 gray-scale dithered 65Kcolor, 8-bit mode)

RGB alignment (Command of data control CLR = 0)												
			Column									
LCD read direction	CI = 0		0		1	2		3		168		169
	Color		R	G	B	R	G	B		R	G	B
	Data Line		$D7'_{1,0}$ $D6'_{1,0}$ $D5'_{1,0}$ $D4'_{1,0}$ $D3'_{1,0}$	$D2'_{1,(0+1)/2}$ $D1'_{1,(0+1)/2}$ $D0'_{1,(0+1)/2}$ $D7'_{2,(0+1)/2}$ $D6'_{2,(0+1)/2}$	$D4'_{2,1}$ $D3'_{2,1}$ $D2'_{2,1}$ $D1'_{2,1}$ $D0'_{2,1}$	$D7'_{1,2}$ $D6'_{1,2}$ $D5'_{1,2}$ $D4'_{1,2}$ $D3'_{1,2}$	$D2'_{1,(2+3)/2}$ $D1'_{1,(2+3)/2}$ $D0'_{1,(2+3)/2}$ $D7'_{2,(2+3)/2}$ $D6'_{2,(2+3)/2}$	$D4'_{2,3}$ $D3'_{2,3}$ $D2'_{2,3}$ $D1'_{2,3}$ $D0'_{2,3}$		$D7'_{1,168}$ $D6'_{1,168}$ $D5'_{1,168}$ $D4'_{1,168}$ $D3'_{1,168}$	$D2'_{1,(168+169)/2}$ $D1'_{1,(168+169)/2}$ $D0'_{1,(168+169)/2}$ $D7'_{2,(168+169)/2}$ $D6'_{2,(168+169)/2}$	$D4'_{2,169}$ $D3'_{2,169}$ $D2'_{2,169}$ $D1'_{2,169}$ $D0'_{2,169}$
	CI = 1		169		168	167		166		1		0
	Color		B	G	R	B	G	R		B	G	R
	Data Line		$D4'_{2,169}$ $D3'_{2,169}$ $D2'_{2,169}$ $D1'_{2,169}$ $D0'_{2,169}$	$D2'_{1,(168+169)/2}$ $D1'_{1,(168+169)/2}$ $D0'_{1,(168+169)/2}$ $D7'_{2,(168+169)/2}$ $D6'_{2,(168+169)/2}$	$D7'_{1,168}$ $D6'_{1,168}$ $D5'_{1,168}$ $D4'_{1,168}$ $D3'_{1,168}$	$D2'_{1,167}$ $D1'_{1,167}$ $D0'_{1,167}$ $D7'_{2,167}$ $D6'_{2,167}$	$D4'_{2,(166+167)/2}$ $D3'_{2,(166+167)/2}$ $D2'_{2,(166+167)/2}$ $D1'_{2,(166+167)/2}$ $D0'_{2,(166+167)/2}$	$D7'_{1,166}$ $D6'_{1,166}$ $D5'_{1,166}$ $D4'_{1,166}$ $D3'_{1,166}$		$D4'_{2,1}$ $D3'_{2,1}$ $D2'_{2,1}$ $D1'_{2,1}$ $D0'_{2,1}$	$D2'_{1,(0+1)/2}$ $D1'_{1,(0+1)/2}$ $D0'_{1,(0+1)/2}$ $D7'_{2,(0+1)/2}$ $D6'_{2,(0+1)/2}$	$D7'_{1,0}$ $D6'_{1,0}$ $D5'_{1,0}$ $D4'_{1,0}$ $D3'_{1,0}$
Block	LI = 0	LI = 1										
0	0	159										
	1	158										
	2	157										
	3	156										
1	4	155										
	5	154										
	6	153										
	7	152										
2	8	151										
	9	150										
38	152	7										
	153	6										
	154	5										
	155	4										
39	156	3										
	157	2										
	158	1										
	159	0										
SEGout			0	1	2	3	4	5		252	253	254

You can change position of R and B with DATACTRL command.

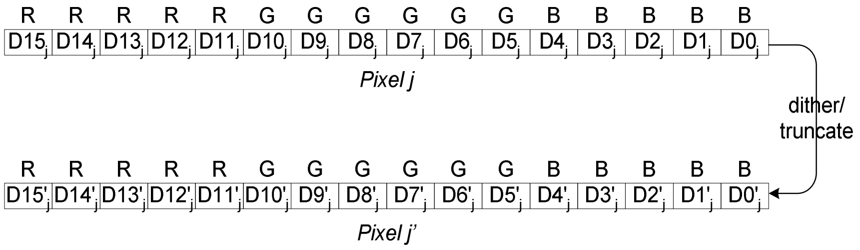


$Dk_{i,j}$ is the k^th^ data bit of the i^th^ write for pixel j, $Dk'_{i,j}$ is the k^th^ data bit of the i^th^ write for pixel j after dithering or truncating, and $Dk'_{i,(j+(j+1))/2}$ is the average value of the k^th^ data bit of the i^th^ write for pixel j and pixel j+1after dithering or truncating.

Memory Map (using the 32 gray-scale, dithered 65K color, 16-bit mode)

RGB alignment (Command of data control CLR = 0)												
			Column									
LCD	CI = 0		0		1	2		3		168		169
read	Color		R	G	B	R	G	B		R	G	B
direction	Data Line		$D15'_0$ $D14'_0$ $D13'_0$ $D12'_0$ $D11'_0$	$D10'_{(0+1)/2}$ $D9'_{(0+1)/2}$ $D8'_{(0+1)/2}$ $D7'_{(0+1)/2}$ $D6'_{(0+1)/2}$	$D4'_1$ $D3'_1$ $D2'_1$ $D1'_1$ $D0'_1$	$D15'_2$ $D14'_2$ $D13'_2$ $D12'_2$ $D11'_2$	$D10'_{(2+3)/2}$ $D9'_{(2+3)/2}$ $D8'_{(2+3)/2}$ $D7'_{(2+3)/2}$ $D6'_{(2+3)/2}$	$D4'_3$ $D3'_3$ $D2'_3$ $D1'_3$ $D0'_3$		$D15'_{168}$ $D14'_{168}$ $D13'_{168}$ $D12'_{168}$ $D11'_{168}$	$D10'_{(168+169)/2}$ $D9'_{(168+169)/2}$ $D8'_{(168+169)/2}$ $D7'_{(168+169)/2}$ $D6'_{(168+169)/2}$	$D4'_{169}$ $D3'_{169}$ $D2'_{169}$ $D1'_{169}$ $D0'_{169}$
	CI = 1		169		168	167		166		1		0
	Color		B	G	R	B	G			B	G	R
	Data Line		$D4'_{169}$ $D3'_{169}$ $D2'_{169}$ $D1'_{169}$ $D0'_{169}$	$D10'_{(168+169)/2}$ $D9'_{(168+169)/2}$ $D8'_{(168+169)/2}$ $D7'_{(168+169)/2}$ $D6'_{(168+169)/2}$	$D15'_{168}$ $D14'_{168}$ $D13'_{168}$ $D12'_{168}$ $D11'_{168}$	$D4'_{167}$ $D3'_{167}$ $D2'_{167}$ $D1'_{167}$ $D0'_{167}$	$D10'_{(166+167)/2}$ $D9'_{(166+167)/2}$ $D8'_{(166+167)/2}$ $D7'_{(166+167)/2}$ $D6'_{(166+167)/2}$	$D15'_{166}$ $D14'_{166}$ $D13'_{166}$ $D12'_{166}$ $D11'_{166}$		$D4'_1$ $D3'_1$ $D2'_1$ $D1'_1$ $D0'_1$	$D10'_{(0+1)/2}$ $D9'_{(0+1)/2}$ $D8'_{(0+1)/2}$ $D7'_{(0+1)/2}$ $D6'_{(0+1)/2}$	$D15'_0$ $D14'_0$ $D13'_0$ $D12'_0$ $D11'_0$
Block	LI = 0	LI = 1										
0	0	159										
	1	158										
	2	157										
	3	156										
1	4	155										
	5	154										
	6	153										
	7	152										
2	8	151										
	9	150										
38	152	7										
	153	6										
	154	5										
	155	4										
39	156	3										
	157	2										
	158	1										
	159	0										
SEGout			0	1	2	3	4	5		252	253	254

You can change position of R and B with DATACTRL command.

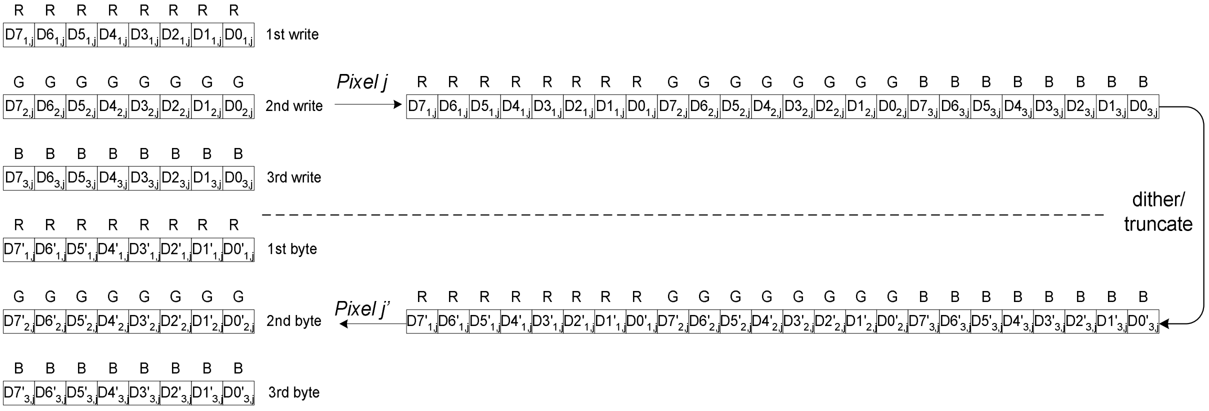


$Dk_{,j}$ is the k^{th} data bit of pixel j, $Dk'_{,j}$ is the k^{th} data bit of pixel j after dithering or truncating, and $Dk'_{,(j+(j+1))/2}$ is the average value of the k^{th} data bit of pixel j and pixel j+1 after dithering or truncating.

Memory Map (using the 32 gray-scale, dithered 262K/16Mcolor, 8-bit mode)

RGB alignment (Command of data control CLR = 0)												
			Column									
LCD read direction	CI = 0		0		1	2		3		168		169
	Color		R	G	B	R	G	B		R	G	B
	Data Line		$D7'_{1,0}$ $D6'_{1,0}$ $D5'_{1,0}$ $D4'_{1,0}$ $D3'_{1,0}$	$D7'_{2,(0+1)/2}$ $D6'_{2,(0+1)/2}$ $D5'_{2,(0+1)/2}$ $D4'_{2,(0+1)/2}$ $D3'_{2,(0+1)/2}$	$D7'_{3,1}$ $D6'_{3,1}$ $D5'_{3,1}$ $D4'_{3,1}$ $D3'_{3,1}$	$D7'_{1,2}$ $D6'_{1,2}$ $D5'_{1,2}$ $D4'_{1,2}$ $D3'_{1,2}$	$D7'_{2,(2+3)/2}$ $D6'_{2,(2+3)/2}$ $D5'_{2,(2+3)/2}$ $D4'_{2,(2+3)/2}$ $D3'_{2,(2+3)/2}$	$D7'_{3,3}$ $D6'_{3,3}$ $D5'_{3,3}$ $D4'_{3,3}$ $D3'_{3,3}$		$D7'_{1,168}$ $D6'_{1,168}$ $D5'_{1,168}$ $D4'_{1,168}$ $D3'_{1,168}$	$D7'_{2,(168+169)/2}$ $D6'_{2,(168+169)/2}$ $D5'_{2,(168+169)/2}$ $D4'_{2,(168+169)/2}$ $D3'_{2,(168+169)/2}$	$D7'_{3,169}$ $D6'_{3,169}$ $D5'_{3,169}$ $D4'_{3,169}$ $D3'_{3,169}$
	CI = 1		169		168	167		166		1		0
	Color		B	G	R	B	G			B	G	R
	Data Line		$D7'_{3,169}$ $D6'_{3,169}$ $D5'_{3,169}$ $D4'_{3,169}$ $D3'_{3,169}$	$D7'_{2,(168+169)/2}$ $D6'_{2,(168+169)/2}$ $D5'_{2,(168+169)/2}$ $D4'_{2,(168+169)/2}$ $D3'_{2,(168+169)/2}$	$D7'_{1,168}$ $D6'_{1,168}$ $D5'_{1,168}$ $D4'_{1,168}$ $D3'_{1,168}$	$D7'_{3,167}$ $D6'_{3,167}$ $D5'_{3,167}$ $D4'_{3,167}$ $D3'_{3,167}$	$D7'_{2,(166+167)/2}$ $D6'_{2,(166+167)/2}$ $D5'_{2,(166+167)/2}$ $D4'_{2,(166+167)/2}$ $D3'_{2,(166+167)/2}$	$D7'_{1,166}$ $D6'_{1,166}$ $D5'_{1,166}$ $D4'_{1,166}$ $D3'_{1,166}$		$D7'_{3,1}$ $D6'_{3,1}$ $D5'_{3,1}$ $D4'_{3,1}$ $D3'_{3,1}$	$D7'_{2,(0+1)/2}$ $D6'_{2,(0+1)/2}$ $D5'_{2,(0+1)/2}$ $D4'_{2,(0+1)/2}$ $D3'_{2,(0+1)/2}$	$D7'_{1,0}$ $D6'_{1,0}$ $D5'_{1,0}$ $D4'_{1,0}$ $D3'_{1,0}$
Block	LI = 0	LI = 1										
0	0	159										
	1	158										
	2	157										
	3	156										
1	4	155										
	5	154										
	6	153										
	7	152										
2	8	151										
	9	150										
38	152	7										
	153	6										
	154	5										
	155	4										
39	156	3										
	157	2										
	158	1										
	159	0										
SEGout			0	1	2	3	4	5		252	253	254

You can change position of R and B with DATACTRL command.

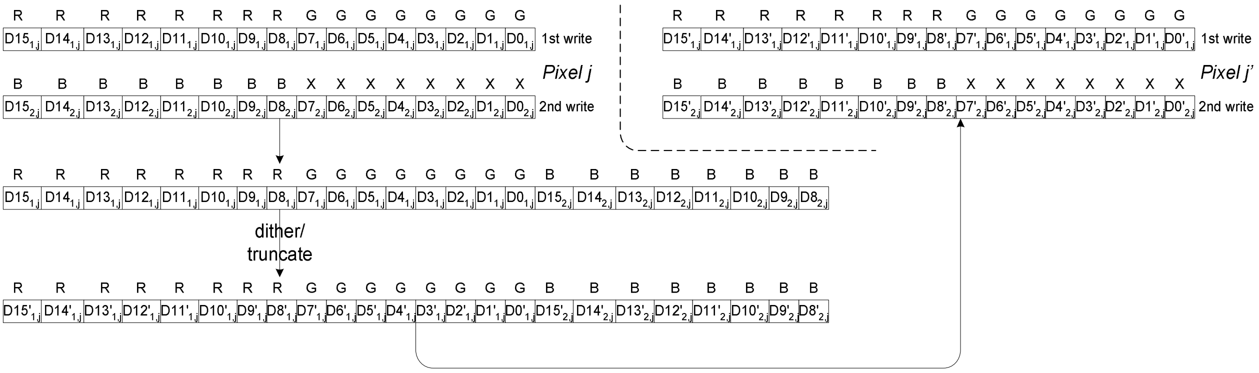


$Dk_{i,j}$ is the k^{th} data bit of the i^{th} write for pixel j, $Dk'_{i,j}$ is the k^{th} data bit of the i^{th} write for pixel j after dithering or truncating, and $Dk'_{i,(j+(j+1))/2}$ is the average value of the k^{th} data bit of the i^{th} write for pixel j and pixel j+1after dithering or truncating.

Memory Map (using the 32 gray-scale, dithered 262K/16M color, 16-bit mode)

RGB alignment (Command of data control CLR = 0)											
			Column								
LCD read direction	CI = 0		0		1	2		3	168		169
	Color		R	G	B	R	G	B	R	G	B
	Data Line		$D15'_{1,0}$ $D14'_{1,0}$ $D13'_{1,0}$ $D12'_{1,0}$ $D11'_{1,0}$	$D7'_{1,(0+1)/2}$ $D6'_{1,(0+1)/2}$ $D5'_{1,(0+1)/2}$ $D4'_{1,(0+1)/2}$ $D3'_{1,(0+1)/2}$	$D15'_{2,1}$ $D14'_{2,1}$ $D13'_{2,1}$ $D12'_{2,1}$ $D11'_{2,1}$	$D15'_{1,2}$ $D14'_{1,2}$ $D13'_{1,2}$ $D12'_{1,2}$ $D11'_{1,2}$	$D7'_{1,(2+3)/2}$ $D6'_{1,(2+3)/2}$ $D5'_{1,(2+3)/2}$ $D4'_{1,(2+3)/2}$ $D3'_{1,(2+3)/2}$	$D15'_{2,3}$ $D14'_{2,3}$ $D13'_{2,3}$ $D12'_{2,3}$ $D11'_{2,3}$	$D15'_{1,168}$ $D14'_{1,168}$ $D13'_{1,168}$ $D12'_{1,168}$ $D11'_{1,168}$	$D7'_{1,(168+169)/2}$ $D6'_{1,(168+169)/2}$ $D5'_{1,(168+169)/2}$ $D4'_{1,(168+169)/2}$ $D3'_{1,(168+169)/2}$	$D15'_{2,169}$ $D14'_{2,169}$ $D13'_{2,169}$ $D12'_{2,169}$ $D11'_{2,169}$
	CI = 1		169		168	167		166	1		0
	Color		B	G	R	B	G	R	B	G	R
	Data Line		$D15'_{2,169}$ $D14'_{2,169}$ $D13'_{2,169}$ $D12'_{2,169}$ $D11'_{2,169}$	$D7'_{1,(168+169)/2}$ $D6'_{1,(168+169)/2}$ $D5'_{1,(168+169)/2}$ $D4'_{1,(168+169)/2}$ $D3'_{1,(168+169)/2}$	$D15'_{1,168}$ $D14'_{1,168}$ $D13'_{1,168}$ $D12'_{1,168}$ $D11'_{1,168}$	$D15'_{2,167}$ $D14'_{2,167}$ $D13'_{2,167}$ $D12'_{2,167}$ $D11'_{2,167}$	$D7'_{1,(166+167)/2}$ $D6'_{1,(166+167)/2}$ $D5'_{1,(166+167)/2}$ $D4'_{1,(166+167)/2}$ $D3'_{1,(166+167)/2}$	$D15'_{1,166}$ $D14'_{1,166}$ $D13'_{1,166}$ $D12'_{1,166}$ $D11'_{1,166}$	$D15'_{2,1}$ $D14'_{2,1}$ $D13'_{2,1}$ $D12'_{2,1}$ $D11'_{2,1}$	$D7'_{1,(0+1)/2}$ $D6'_{1,(0+1)/2}$ $D5'_{1,(0+1)/2}$ $D4'_{1,(0+1)/2}$ $D3'_{1,(0+1)/2}$	$D15'_{1,0}$ $D14'_{1,0}$ $D13'_{1,0}$ $D12'_{1,0}$ $D11'_{1,0}$
Block	LI = 0	LI = 1									
0	0	159									
	1	158									
	2	157									
	3	156									
1	4	155									
	5	154									
	6	153									
	7	152									
2	8	151									
	9	150									
38	152	7									
	153	6									
	154	5									
	155	4									
39	156	3									
	157	2									
	158	1									
	159	0									
SEGout			0	1	2	3	4	5	252	253	254

You can change position of R and B with DATACTRL command.



$Dk_{i,j}$ is the k^{th} data bit of the i^{th} write for pixel j, $Dk'_{i,j}$ is the k^{th} data bit of the i^{th} write for pixel j after dithering or truncating, and $Dk'_{i,(j+(j+1))/2}$ is the average value of the k^{th} data bit of the i^{th} write for pixel j and pixel j+1after dithering or truncating.

8.3.2 Line Address Control Circuit

This circuit is to control the address in the line direction when MPU accesses the DDRAM or read the DDRAM to display image on the LCD.

You can specify a range of the line address with line address set command. When the line-direction scan is specified with DATACTRL command and the address are increased from the start up to the end line, the column address is increased by 1 and the line address returns to the start line.

The DDRAM supports up to 160 lines, and thus the total line becomes 160.

In the READ operation, as the end line is reached, the column address is automatically increased by 1 and the line address returns to the start line.

Users may inverse the correspondence between the DDRAM address and common output via the address normal/inverse parameter of DATACTRL command.

8.3.3 Column Address Control Circuit

This circuit is to control the address in the column direction when MPU accesses the DDRAM. You can specify a range of the column address with column address set command. When the column-direction scan is specified with DATACTRL command and the address are increased from the start up to the end line, the line address is increased by 1 and the column address returns to the start column.

In the READ operation, the column address is also automatically increased by 1 and returns to the start line as the end column is reached.

Just like the line address control circuit, users may inverse the correspondence between the DDRAM column address and segment output via the column address normal/inverse parameter of DATACTRL command. This arrangement makes the chip layout on the LCD module flexible.

8.3.4 I/O Buffer Circuit

It is the bi-directional buffer when MPU reads or writes the DDRAM. Since the READ or WRITE operation of MPU to DDRAM is performed independently from data output to the display data latch circuit, asynchronous access to the DDRAM while the LCD is turned on does not cause troubles such as flicking of the display images.

8.3.5 Block Address Circuit

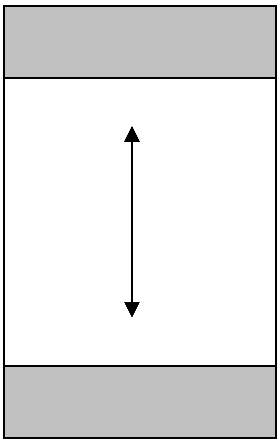
The circuit associates lines on DDRAM with COM output. ST7531 processes signals for the liquid crystal display on 4-line basis. Thus, when specifying a specific area in the area of scroll display or partial display, you must designate it in block.

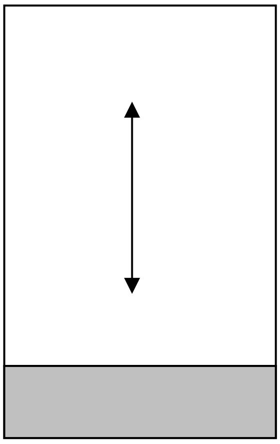
8.3.6 Display Data Latch Circuit

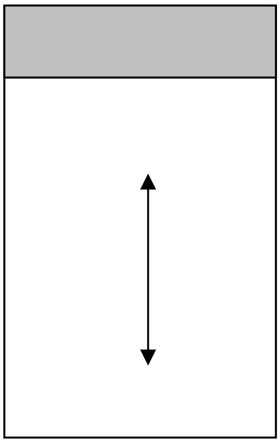
This circuit is used to temporarily hold display data to be output from the DDRAM to the SEG decoder circuit. Since display normal/inverse and display on/off commands are used to control data in the latch circuit alone, they do not modify data in the DDRAM.

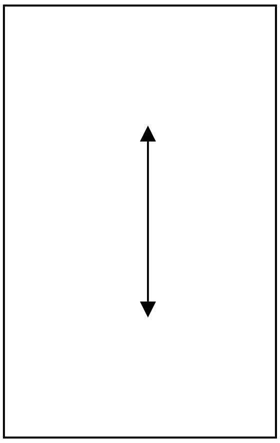
8.4 Area Scroll Display

The user may scroll the display screen partially in any one of the following four scroll patterns via AREA SCROLL SET and SCROLL START SET commands.


Center mode


Top mode


Bottom mode

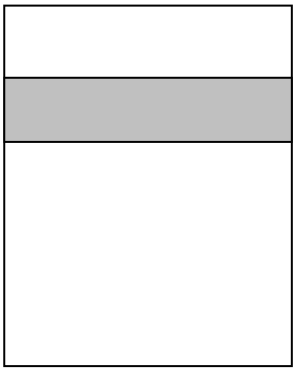

Whole mode

▨ Fixed area

↕ Scrolled area

8.5 Partial Display

The user may turn on the partial display (division by line) of the screen via PARTIAL IN command. This mode consumes less current than the whole screen display and is suitable for the equipment in the standby state.



▨ : Display area (partial display area)

□ : Non-display area

If the partial display region is out of the maximum display range, it will be no operation.

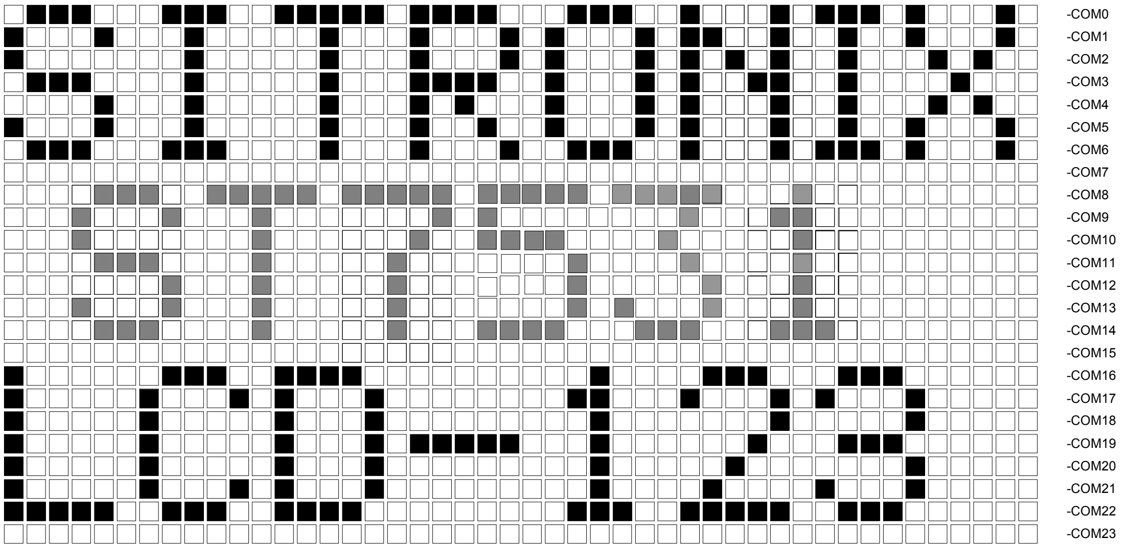


Figure 8.5.1.Reference Example for Partial Display

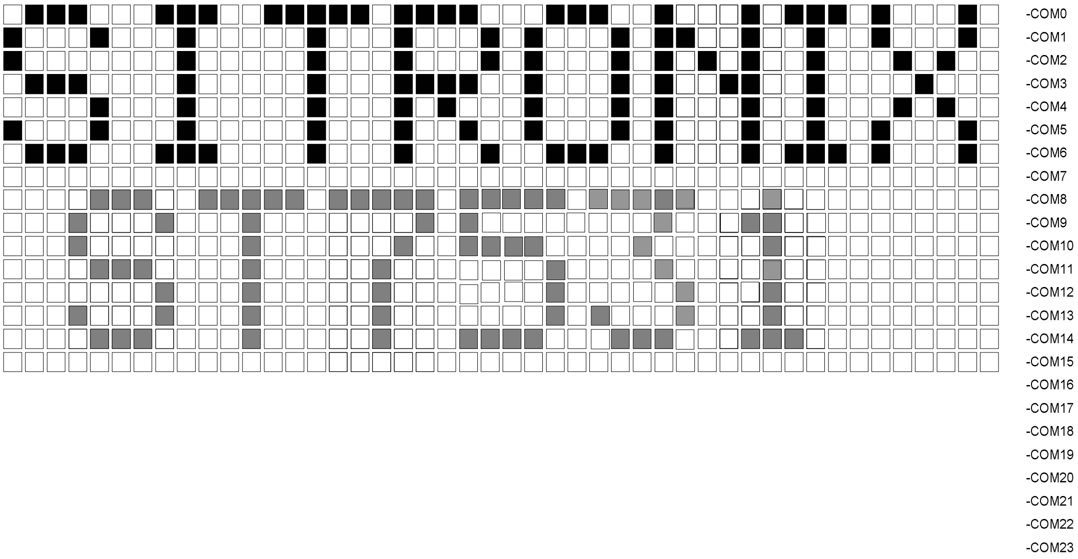


Figure 8.5.2.Partial Display

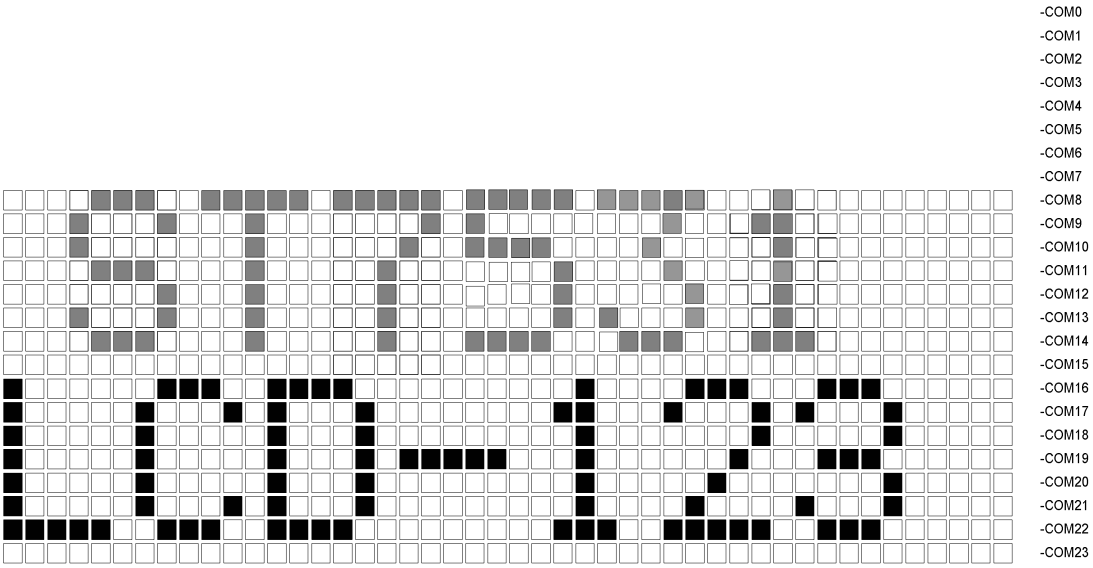


Figure 8.5.3.Moving Display

8.6 Gray-Scale Display

ST7531 incorporates a 2 FRC & 31 PWM function circuit to display a 32 gray-scale display.

8.7 Oscillation Circuit

This is an on-chip oscillator without external resistor. When the internal oscillator is used, this pin must connect to VDD; when the external oscillator is used, this pin could be an input pin. This oscillator signal is used in the voltage converter and display timing generation circuit.

8.8 Display Timing Generator Circuit

This circuit generates some signals for displaying on LCD. The display clock, CL (internal), generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 160-bit display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the MPU. The display clock generates an LCD AC signal (M) which enables the LCD driver to make an AC drive waveform. It also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Figure 8.8.1.

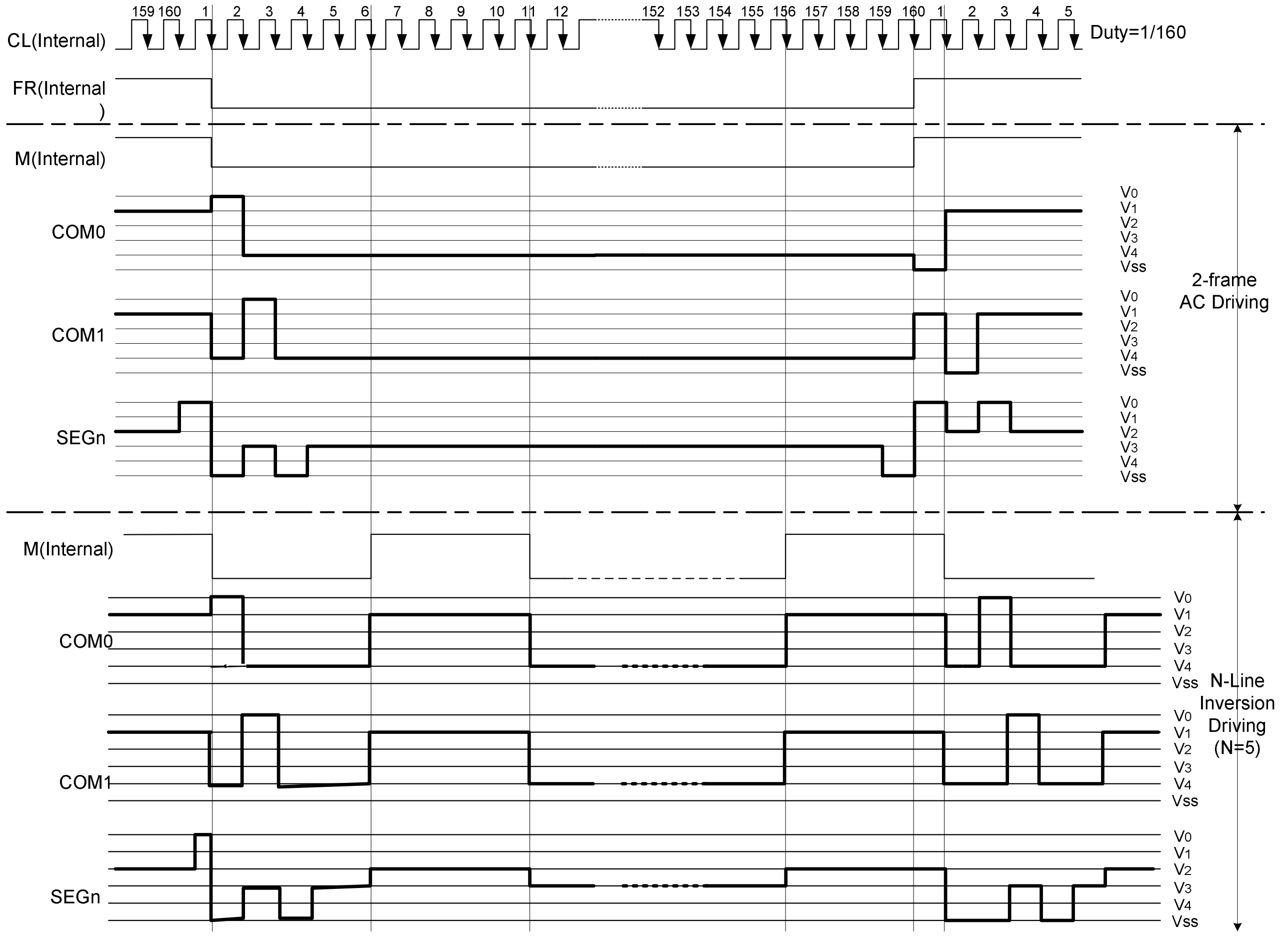
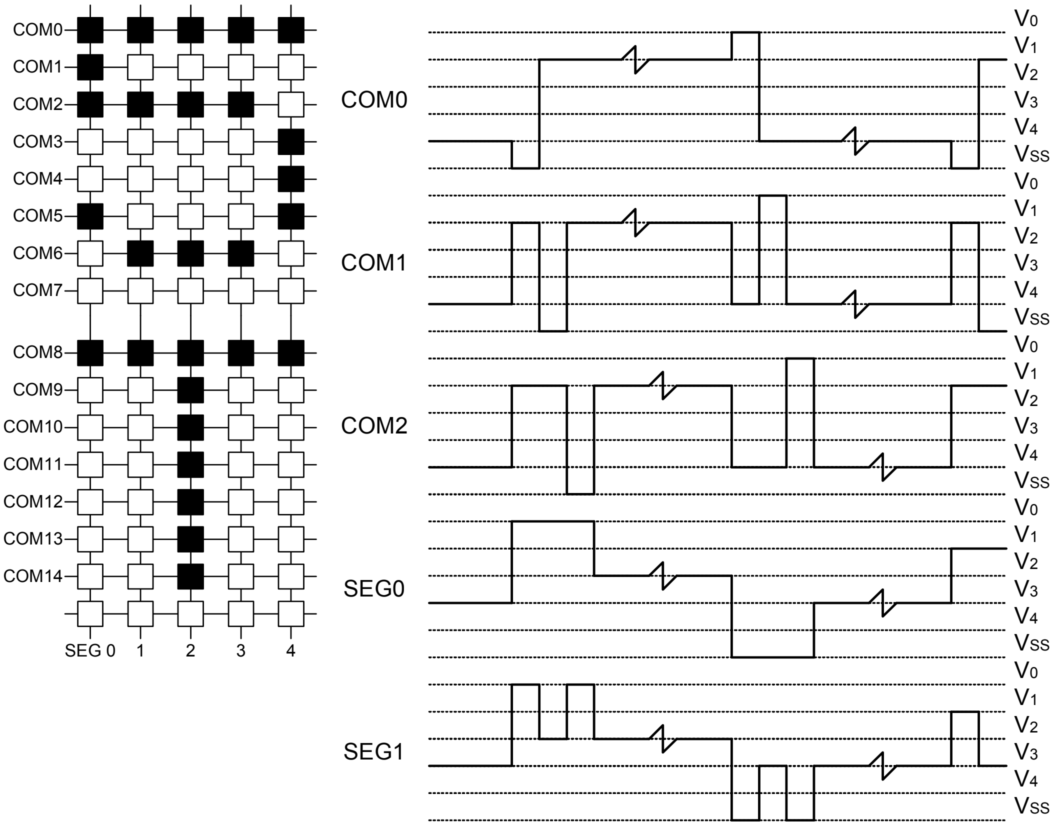


Figure 8.8.1 2-frame AC Driving Waveform (Duty Ratio: 1/160)

8.9 Liquid Crystal drive Circuit

This driver circuit is configured by 160-channel common drivers and 256-channel segment drivers. This LCD panel driver voltage depends on the combination of display data and M signal.



8.10 Liquid Crystal Driver Power Circuit

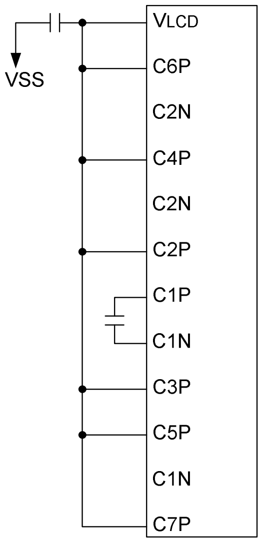
The power supply circuit generates the voltage levels required to drive liquid crystal driver with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction. For details, refers to "Instruction Description". Table 8.10.1 shows the referenced combinations in using Power Supply circuits.

Table 8.10.1 Recommended Power Supply Combinations

User setup	Power control (VB VR VF)	V/B circuits	V/R circuits	V/F circuits	VLCD	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	ON	ON	ON	Open	Open	Open
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	OFF	ON	ON	External input	Open	Open
Only the voltage follower circuits are used	0 0 1	OFF	OFF	ON	Open	External input	Open
Only the external power supply circuits are used	0 0 0	OFF	OFF	OFF	Open	External input	External input

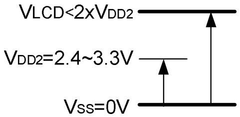
8.10.1 Voltage Converter Circuits

The Step-up Voltage Circuits

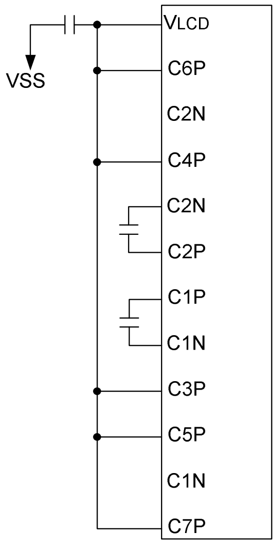


Do Not over Voltage limitation

2x step-up voltage circuit

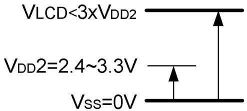


2x step-up voltage relationships

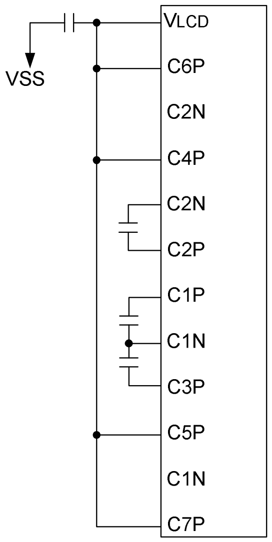


Do Not over Voltage limitation

3x step-up voltage circuit

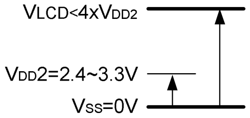


3x step-up voltage relationships

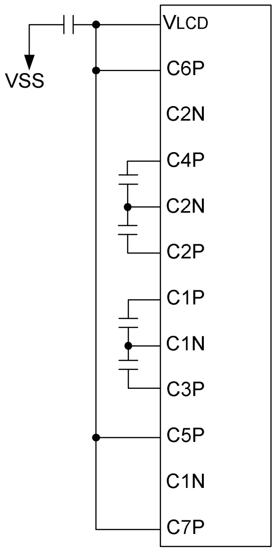


Do Not over Voltage limitation

4x step-up voltage circuit

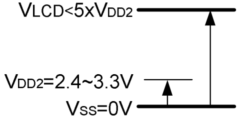


4x step-up voltage relationships

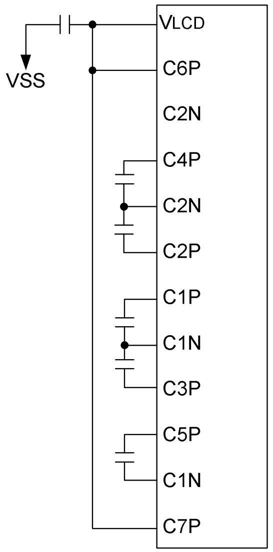


Do Not over Voltage limitation

5x step-up voltage circuit

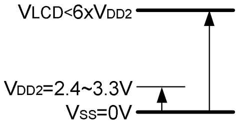


5x step-up voltage relationships

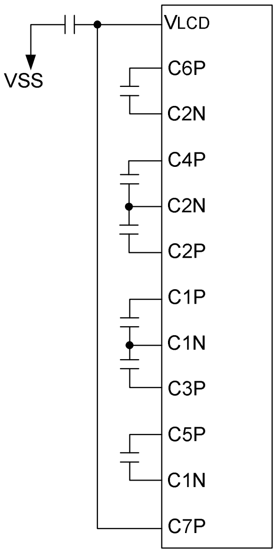


Do Not over Voltage limitation

6x step-up voltage circuit

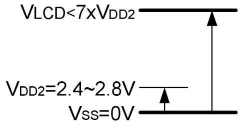


6x step-up voltage relationships

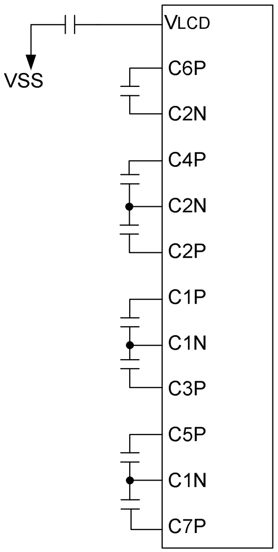


Do Not over Voltage limitation

7x step-up voltage circuit

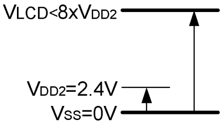


7x step-up voltage relationships



Do Not over Voltage limitation

8x step-up voltage circuit



8x step-up voltage relationships

Note: The regulating capacitance on V0 ~ V4 should be between 1.0 to 2.2 μF.

8.10.2 Voltage Regulator Circuits

SET VOP (SETVOP)

The set VOP function is to program the optimum LCD supply voltage V_0.

SETVOP

Reset state of VPR[8:0] is 257_{DEC} = 13.88V.

The V_0 value is programmed via the VPR[8:0] register.

V_0 = a + (VPR[8:6]VPR[5:0]) x b

Ex: VPR[5:0]=000001, VPR[8:6]=100

→ VPR[8:0]=100000001

→ 3.6+257x0.04=13.88

where a is a fixed constant value 3.6, b is a fixed constant value 0.04, VPR[8:0] is the programmed V_0 value with programming range from 5 to 410 ($19A_{HEX}$), and VPR[5:0] is the set contrast value which can be set via the interface and is in two's complement format.(See command VOLUP & VOLDOWN)

The VPR[8:0] value must be in the V_0 programming range as given in Fig.8.10.2. Evaluating equation (1), values outside the programming range indicated in Fig.8.10.2 may result.

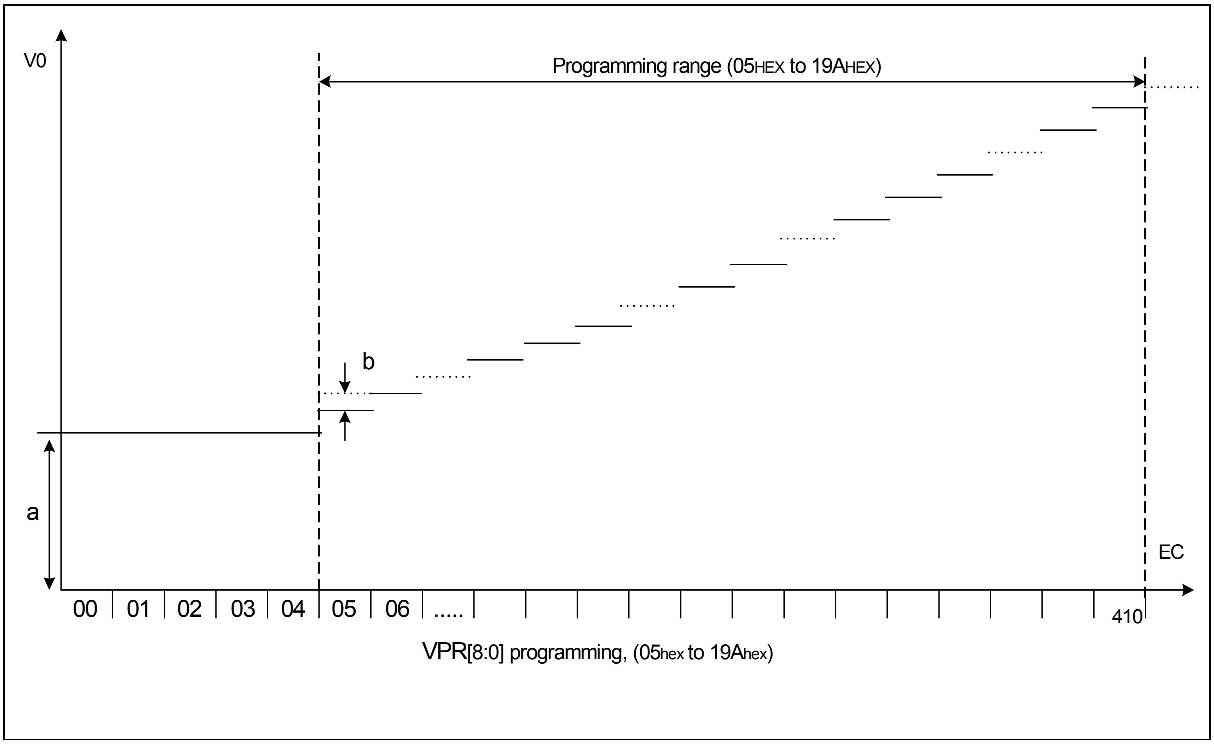


Fig. 8.10.2 V0 programming range

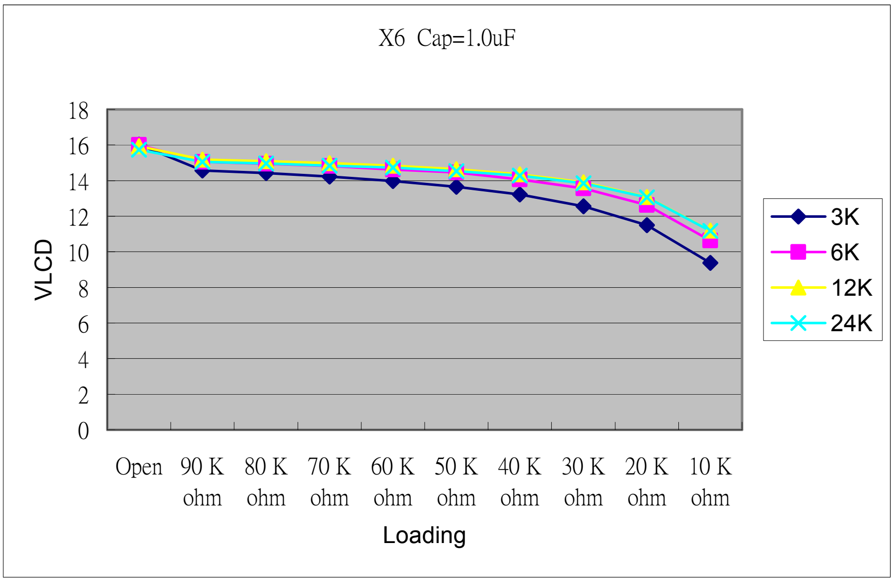
Although the programming range for the internally generated V_0 allows values above the maximum allowed V_0, the customer has to ensure setting the VPR register and selecting the temperature compensation under all condition and including all tolerances that the maximum allowed V_0 (20V) will never be exceeded.

Booster Efficiency

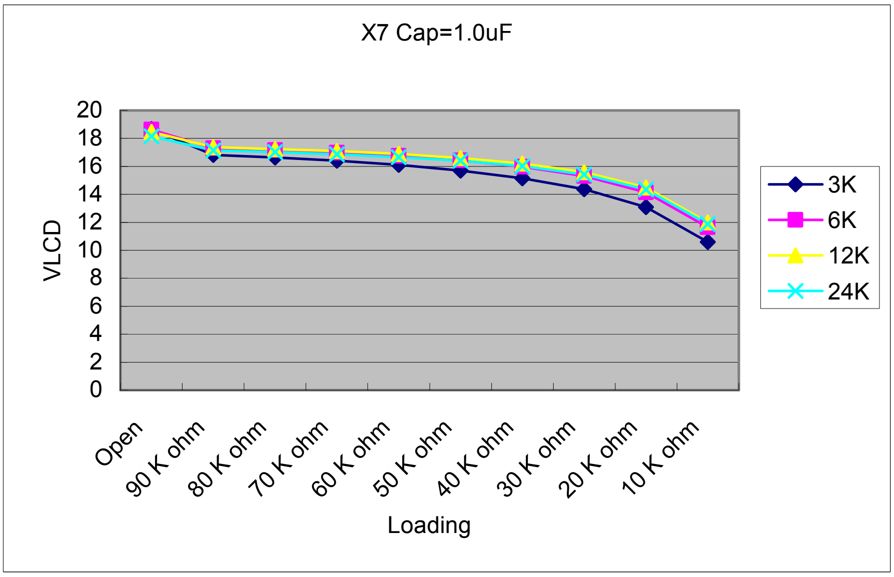
By BOOSTER STAGES (2X, 3X, 4X, 5X, 6X, 7X, 8X) and BOOSTER EFFICIENCY (Level1~4) commands, we could easily set the best booster performance with suitable current consumption. If the booster efficiency is set to higher level (level4 is higher than level1), the boost efficiency is better than lower level, and it only needs a little bit more power consumption current. It could be applied to each multiple voltage condition.

When the loading of LCD panel is heavier, the performance of booster will not be in a good working condition. The user may set the BE level to be higher and only a little bit more current needed. Never consider to change to higher booster stage at beginning stage unless it is necessary.

The BOOSTER EFFICIENCY command could be used together with BOOSTER STAGE command to choose one best boost output condition. The user could regard the BOOSTER STAGE command as a large scale operation, and the BOOSTER EFFICIENCY command as a small scale operation. These commands are very convenient for using.



Condition : VDD = 2.7V, Cap = 1.0uF, Booster = 6x, measured on chip



Condition : VDD = 2.7V, Cap = 1.0uF, Booster = 7x, measured on chip

RESET CIRCUIT

When Power is Turned On

Input power (VDD1~VDD5)

↓

Be sure to apply POWER-ON RESET (RST = LOW)

↓

<Display Setting>	**<<State after resetting>>**
Display control (DISCTRL)	
Setting clock dividing ratio:	2 dividing
Duty setting:	1/4
Setting reverse rotation number of line:	11H reverse rotations
Common scan direction (COMSCN)	
Setting scan direction:	COM0 -> COM79, COM80-> COM159
Temperature Gradient Setting (TMPGRD)	

↓

Oscillation ON (OSCON)	Oscillation OFF

↓

Sleep-out (SLIPOUT)	Sleep-in

↓

<Power Supply Setting>	**<<State after resetting>>**
Electronic volume control (VOLCTRL)	
Setting volume value:	0
Setting built-in resistance value:	0 (3.95)
Power control (PWRCTR)	
Setting operation of power supply circuit:	All OFF

↓

<Display Setting 2>	**<<State after resetting>>**
Normal rotation of display (DISNOR)/Inversion of display (DISINV):	Normal rotation of display
Partial-in (PTLIN)/Partial-out (PTLOUT)	Partial-out
Setting fix area:	0
Area scroll set (ASSET)	
Setting area scroll region:	0
Setting area scroll type:	Full-screen scroll
Scroll start set (SCSTART)	
Setting scroll start address:	0

↓

<Display Setting 3>	**<<State after resetting>>**
Data control (DATCTRL)	
Setting normal rotation/inversion of line address:	Normal rotation

Setting normal rotation/inversion of column address: Normal rotation

Setting direction of address scanner: Column direction

Setting RGB arrangement: RGB

Setting gradation: 65k-color

↓

<RAM Setting> **<<State after resetting>>**

Line address set (LASET)

Setting start line address: 0

Setting end line address: 0

Column address set (CASET)

Setting start column address: 0

Setting end column address: 0

↓

<RAM Write> **<<State after resetting>>**

Memory write command (RAMWR)

Writing displayed data: Repeat as many as the number needed and exit by entering other command.

↓

<Waiting (approximately 100ms)>

Wait until the power supply voltage has stabilized.

Enter the command of power supply control first, and then wait at least 100ms before entering the display ON command when the built-in power supply circuit operates.

If you do not wait, an unexpected display may appear on the liquid crystal panel.

↓

DISPLAY ON (DISON): DISPLAY OFF

*1: When the IC is in SLEEP IN state, the liquid crystal drive power supply, the boosting power output, and GND pin are connected together, therefore, the SLEEP OUT command must be entered to cancel the SLEEP state prior to turning on the built-in circuit.

(Note) If changes are unnecessary after resetting, command input is unnecessary.

8. COMMANDS

8.1 Command table

Ext=0 or Ext=1

Index	Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Hex	Parameter
1	Ext In	0	1	0	0	0	1	1	0	0	0	0	Ext=0 Set	30	None
2	Ext Out	0	1	0	0	0	1	1	0	0	0	1	Ext=1 Set	31	None

Ext=0

Index	Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Hex	Parameter
1	DISON	0	1	0	1	0	1	0	1	1	1	1	Display On	AF	None
2	DISOFF	0	1	0	1	0	1	0	1	1	1	0	Display Off	AE	None
3	DISNOR	0	1	0	1	0	1	0	0	1	1	0	Normal Display	A6	None
4	DISINV	0	1	0	1	0	1	0	0	1	1	1	Inverse Display	A7	None
5	COMSCN	0	1	0	1	0	1	1	1	0	1	1	COM Scan Direction	BB	1 byte
6	DISCTRL	0	1	0	1	1	0	0	1	0	1	0	Display Control	CA	3 bytes
7	SLPIN	0	1	0	1	0	0	1	0	1	0	1	Sleep In	95	None
8	SLPOUT	0	1	0	1	0	0	1	0	1	0	0	Sleep Out	94	None
9	LASET	0	1	0	0	1	1	1	0	1	0	1	Line Address Set	75	2 bytes
10	CASET	0	1	0	0	0	0	1	0	1	0	1	Column Address Set	15	2 bytes
11	DATSDR	0	1	0	1	0	1	1	1	1	0	0	Data Scan Direction	BC	3 bytes
12	RAMWR	0	1	0	0	1	0	1	1	1	0	0	Writing to Memory	5C	Data
13	PTLIN	0	1	0	1	0	1	0	1	0	0	0	Partial display in	A8	2 bytes
14	PTLOUT	0	1	0	1	0	1	0	1	0	0	1	Partial display out	A9	None
15	ASCSET	0	1	0	1	0	1	0	1	0	1	0	Area Scroll Set	AA	4 bytes
16	SCSTART	0	1	0	1	0	1	0	1	0	1	1	Scroll Start Set	AB	1 byte
17	OSCON	0	1	0	1	1	0	1	0	0	0	1	Internal OSC on	D1	None
18	OSCOFF	0	1	0	1	1	0	1	0	0	1	0	Internal OSC off	D2	None
19	PWRCTRL	0	1	0	0	0	1	0	0	0	0	0	Power Control	20	1 byte
20	VOLCTRL	0	1	0	1	0	0	0	0	0	0	1	EC control	81	2 bytes
21	VOLUP	0	1	0	1	1	0	1	0	1	1	0	EC increase 1	D6	None
22	VOLDOWN	0	1	0	1	1	0	1	0	1	1	1	EC decrease 1	D7	None
23	RESERVED	0	1	0	1	0	0	0	0	0	1	0	Not Use	82	0
24	EPSRRD1	0	1	0	0	1	1	1	1	1	0	0	READ Register1	7C	None
25	EPSRRD2	0	1	0	0	1	1	1	1	1	0	1	READ Register2	7D	None
26	NOP	0	1	0	0	0	1	0	0	1	0	1	NOP Instruction	25	None

27	STREAD	0	0	1	Read Data								Status Read		
28	EPINT	0	1	0	0	0	0	0	0	1	1	1	Initial code(1)	07	1 byte

Ext=1

Index	***Command***	***A0***	***RD***	***WR***	***D7***	***D6***	***D5***	***D4***	***D3***	***D2***	***D1***	***D0***	***Function***	***Hex***	***Parameter***
1	Gray 1 Set	0	1	0	0	0	1	0	0	0	0	0	FRAME 1 Gray PWM Set	20	16 bytes
2	Gray 2 Set	0	1	0	0	0	1	0	0	0	0	1	FRAME 2 Gray PWM Set	21	16 bytes
3	Wt. Set	0	1	0	0	0	1	0	0	0	1	0	Weight Set	22	3 bytes
4	ANASET	0	1	0	0	0	1	1	0	0	1	0	Analog Circuit Set	32	3 bytes
5	DITHOFF	0	1	0	0	0	1	1	0	1	0	0	Dithering Circuit Off	34	None
6	DITHON	0	1	0	0	0	1	1	0	1	0	1	Dithering Circuit On	35	None
7	EPCTIN	0	1	0	1	1	0	0	1	1	0	1	Control EEPROM	CD	1 byte
8	EPCOUT	0	1	0	1	1	0	0	1	1	0	0	Cancel EEPROM	CC	None
9	EPMWR	0	1	0	1	1	1	1	1	1	0	0	Write to EEPROM	FC	None
10	EPMRD	0	1	0	1	1	1	1	1	1	0	1	Read from EEPROM	FD	None

Note: The table above is for 8-bit interface. For the application of 16-bit interface, fill D15~8 with 0, and other bits are just the same with the table above.

EXT= "0" or "1"

(1) Extension instruction disable (EXT IN) - Parameter Byte: None (30H)

Use the "EXT=0" command table

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	1	0	0	0	0

(2) Extension instruction enable (EXT OUT) - Parameter Byte: None (31H)

Use the extended command table EXT="1"

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	1	0	0	0	1

EXT= "0"

(1) Display ON (DISON) - Parameter Byte: None (AFH)

It is to turn the display on. When the display is turned on, segment and common outputs are generated at the level corresponding to the display data and display timing. As long as the sleep mode is selected, the display cannot be turned on. Thus, whenever using this command, the sleep mode must be cancelled first.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	1	1	1	1

(2) Display OFF (DISOFF) - Parameter Byte: None (AEH)

It is to forcibly turn the display off. As long as the display is turned off, every segment and common outputs are forced to VSS level.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	1	1	1	0

(3) Normal display (DISNOR) - Parameter Byte: None (A6H)

It is to normally highlight the display area without modifying contents of the display data RAM.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	0	1	1	0

(4) Inverse display (DISINV) - Parameter Byte: None (A7)

It is to inversely highlight the display area without modifying contents of the display data RAM. This command does not invert non-display areas in case of using partial display.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	0	1	1	1

(5) Common scan (COMSCN) - Parameter Byte: 1 (BBH)

It is to specify the common output scan direction. This command is for the convenience of wiring on the LCD panel.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	1	1	0	1	1	—
Parameter Byte 1 (PB1)	1	1	0	*	*	*	*	*	CD2	CD1	CD0	Common Scan direction

When 1/160 is selected for the display duty, pins and common output are scanned in the order shown below.

CD2	CD1	CD0	Common scan direction					
			COM0 pin		COM79 pin	COM80 pin		COM159 pin
0	0	0	0	→	79	80	→	159
0	0	1	0	→	79	159	→	80
0	1	0	79	→	0	80	→	159
0	1	1	79	→	0	159	→	80

Original graphic :

CD[2-0] = [0,0,0] (0→79, 80→159)

CD[2-0] = [0,0,1] (0→79, 159→80)

CD[2-0] = [0,1,0] (79→0, 80→159)

CD[2-0] = [0,1,1] (79→0, 159→80)

Figure 8.1.1 Common scan direction configuration

(6) Display control (DISCTRL) - Parameter Byte: 3 (CAH)

This command and succeeding parameters are used to perform the display timing-related setups. This command must be selected before using SLPOUT. Do not change this command while the display is turned on.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	1	0	0	1	0	1	0	
Parameter Byte 1 (PB1)	1	1	0	*	*	*	0	0	CLD	0	0	CL dividing ratio, F1 and F2 drive pattern.
Parameter Byte 2 (PB2)	1	1	0	*	*	DT5	DT4	DT3	DT2	DT1	DT0	Drive duty
Parameter Byte 3 (PB3)	1	1	0	*	*	*	FI	LF3	LF2	LF1	LF0	FR inverse-set value

PB1 specifies the CL dividing ratio.

CLD: CL dividing ratio. They are used to change number of dividing stages of external or internal clock.

CLD=0: not divide, CLD=1: 2 divisions.

PB2 specifies the duty of the module on block basis. Initial: 00H

(Numbers of display lines)/4-1 = DT5 x 2^5 + DT4 x 2^4 + DT3 x 2^3 + DT2 x 2^2 + DT1 x 2^1 + DT0 x 2^0

For example, 1/128 duty → 128/4-1=31 → (DT5, DT4, DT3, DT2, DT1, DT0) = (0, 1, 1, 1, 1, 1)

PB3 specifies number of line cycles (range from 2 to 16) in a frame.

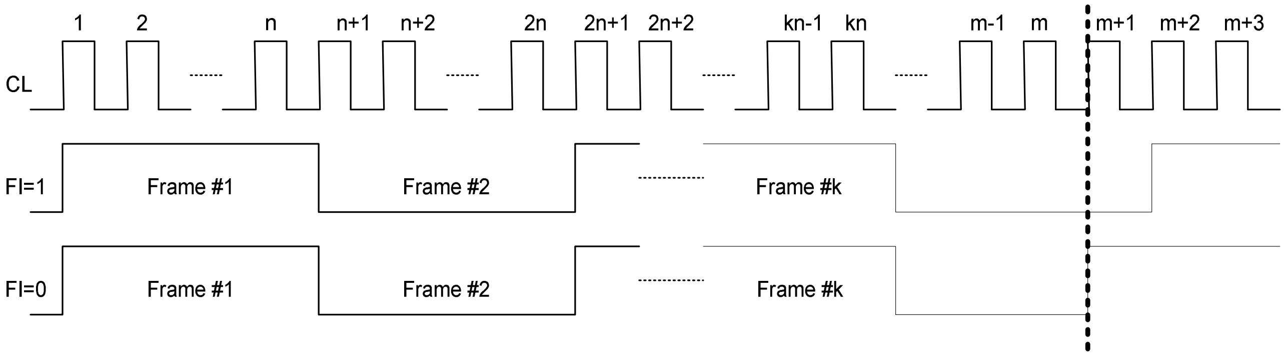
Number of line cycles-1 = LF3 x 2^3 + LF2 x 2^2 + LF1 x 2^1 + LF0 x 2^0

For example, 11 line cycles in a frame → 11-1=10 → (LF3, LF2, LF1, LF0) = (1, 0, 1, 0)

In the default, 11 line cycles in a frame is selected.

FI decides the inversion type of frame at the end of common scan cycle while the number of duty is not divisible by the number of line cycles per frame. For example, in the application of 1/m duty and n line cycles in a frame set, the difference of the choice in FI is shown as the following figure.

m = n x k + r, where m, n, k, and r are all whole numbers, and r is the remainder of m divided by n (r < n).



(7) Sleep in (SLPIN) - Parameter Byte: None (95H)

This command is to enter the SLEEP MODE.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	0	1	0	1	0	1

(8) Sleep out (SLPOUT) - Parameter Byte: None (94H)

This command is to exit the SLEEP MODE.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	0	1	0	1	0	0

(9) Line address set (LASET) - Parameter Byte: 2 (75H)

This command is to specify the line address area when MPU makes access to the display data RAM. As the addresses are increased from the start to the end line in the line-direction scan, the column address is increased by 1 and the line address return to the start line. Note that the start and end line must be a pair. Moreover, the relation "start line <end line" must be maintained.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	1	1	1	0	1	0	1	—
Parameter Byte 1 (PB1)	1	1	0	SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0	Start Line
Parameter Byte 2 (PB2)	1	1	0	EL7	EL6	EL5	EL4	EL3	EL2	EL1	EL0	End Line

Note: The range of line address is 0 ~ 159.

(10) Column address set (CASET) - Parameter Byte: 2 (15H)

This command is to specify the column address area when MPU makes access to the display data RAM. As the addresses are increased from the start to the end column in the column-direction scan, the line address is incremented by 1 and the column address is returned to the start column. Note that the start and end line must be a pair. Moreover, the relation "start column <end column" must be maintained.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	0	1	0	1	0	1	—
Parameter Byte 1 (PB1)	1	1	0	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	Start Column
Parameter Byte 2 (PB2)	1	1	0	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	End Column

Note: The range of column address is 0 ~ 169.

(11) Data scan direction (DATSDR) - Parameter Byte: 3 (BCH)

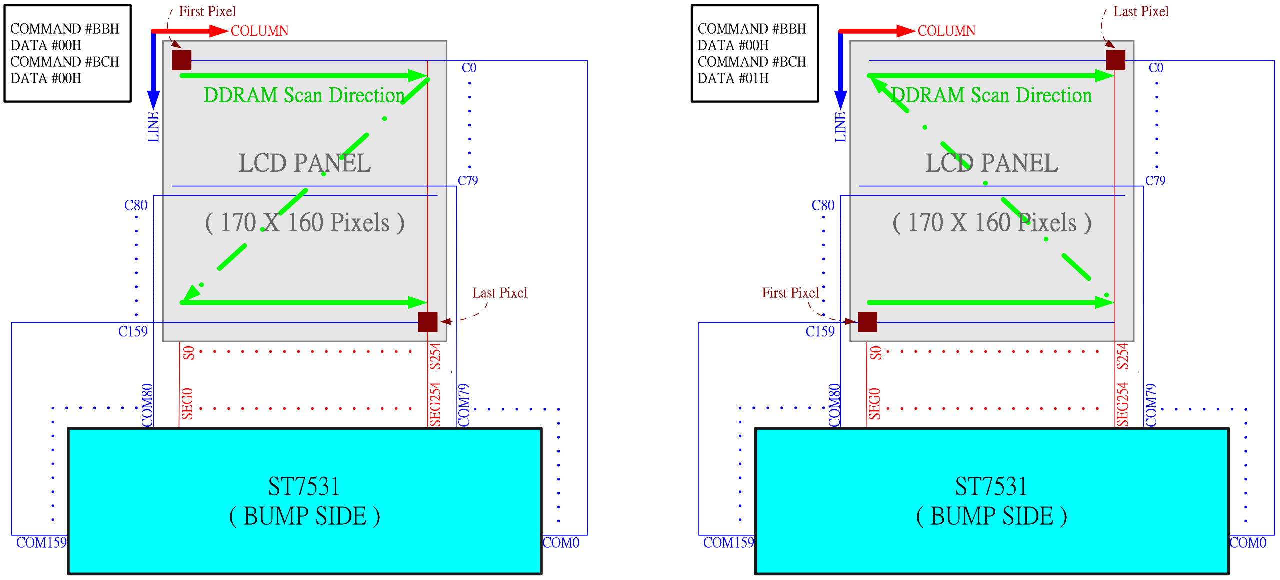
This command is to setup various parameters in the operations of display data stored on the built-in RAM by MPU.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	1	1	1	0	0	—
Parameter Byte 1 (PB1)	1	1	0	*	*	*	*	*	0	CI	LI	Normal/inverse display of address and address scan direction.
Parameter Byte 2 (PB2)	1	1	0	*	*	*	*	*	*	*	CLR	RGB arrangement
Parameter Byte 3 (PB3)	1	1	0	*	*	*	*	*	GS2	GS1	GS0	Gray-scale setup

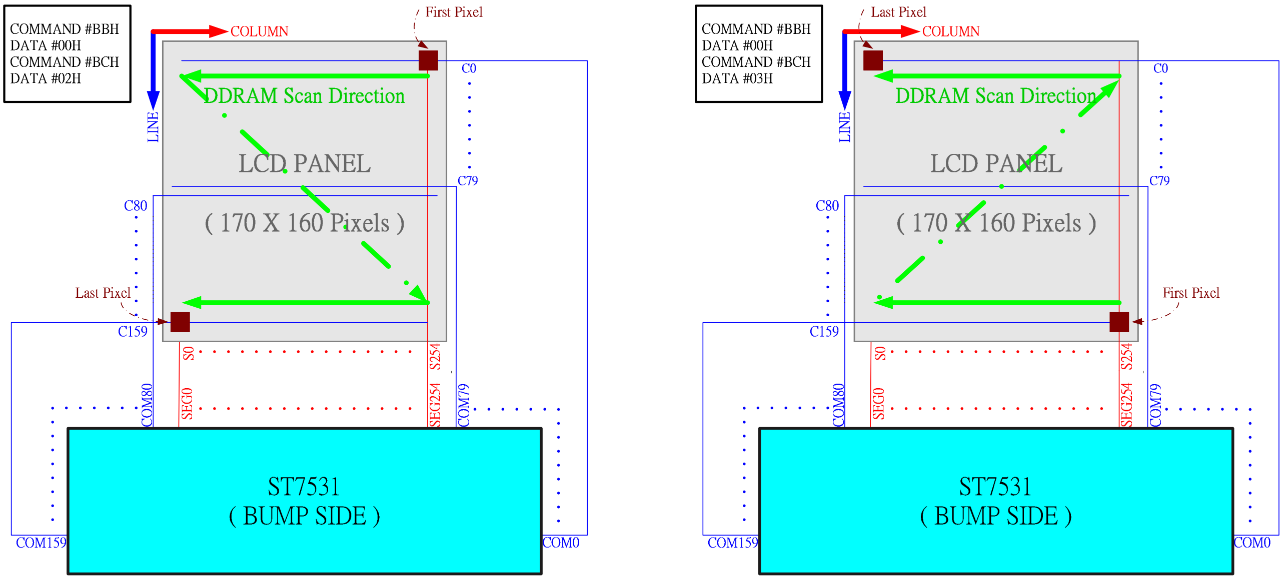
PB1 is to specify the normal/inverse display of the line and column address and the address scanning direction.

LI: Normal/inverse direction of the line address. LI =0: Normal, LI =1: Inverse

CI: Normal/reverse direction of the column address. CI =0: Normal, CI =1: Reverse



(a) COMMAND #BCH, DATA #00H **(b) COMMAND #BCH, DATA #01H**



(c) COMMAND #BCH, DATA #02H **(d) COMMAND #BCH, DATA #03H**

Figure 8.1.2 Different RAM accessing setup under COMMAND #BBH, DATA #00H
(a) COMMAND #BCH, DATA #00H
(b) COMMAND #BCH, DATA #01H
(c) COMMAND #BCH, DATA #02H
(d) COMMAND #BCH, DATA #03H

PB2 is to change RGB arrangement of the segment output according to RGB arrangement on the LCD panel. This command will set the writing position of data (R, G, B) on the display memory to be changed or not.

CLR	Line	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	…	SEG254
0	0, 3, 6, …	R	G	B	R	G	B	R	G	…	B
	1, 4, 7, …	B	R	G	B	R	G	B	R	…	G
	2, 5, 8, …	G	B	R	G	B	R	G	B	…	R
1	0, 3, 6, …	B	G	R	B	G	R	B	G	…	R
	1, 4, 7, …	G	R	B	G	R	B	G	R	…	B
	2, 5, 8, …	R	B	G	R	B	G	R	B	…	G

PB3 is to select desired display colors between the 32 gray-scale dithered 65K, 262K, or 16M.

GS2	GS1	GS0	Numbers of gray-scale
0	0	1	32 gray-scale 65K
0	1	0	32 gray-scale 262K
1	0	0	32 gray-scale 16M

(12) Memory write (RAMWR) - Parameter Byte: Numbers of data written (5CH)

This command turns on the data entry mode when MPU writes data to the display memory. This command will always sets the line and column address at the start address while executed. The following parameter byte rewrites contents of the display data RAM and increases the line or column address automatically. The write mode is automatically cancelled if any other command is entered.

1. 8-bit bus

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	1	0	1	1	1	0	0	—
Parameter Byte 1 (PB1)	1	1	0	Data to be written								Data to be written

2. 16-bit bus

	A0	RD	RW	D15	D14	…	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	*	*	…	*	*	0	1	0	1	1	1	0	0	Memory write
Parameter Byte 1 (PB1)	1	1	0	Data to be written													Write date

(13) Partial in (PTLIN) - Parameter Byte: 2 (A8H)

This command is to specify the partial display area. It will turn on partial display of the screen (dividing screen by lines) to save power. Since ST7531 processes the liquid crystal display signal on 4-line basis (block basis), the display and no-display areas are also specified on 4-bit line (block basis).

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	0	1	0	0	0	--
Parameter Byte 1 (PB1)	1	1	0	*	*	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0	Start block address
Parameter Byte 2 (PB2)	1	1	0	*	*	PTE5	PTE4	PTE3	PTE2	PTE1	PTE0	End block address

Only the address of the display block can be specified for the partial display. Do not specify an address not to be displayed when scrolled.

(14) Partial out (PTLOUT) - Parameter Byte: none (A9H)

This command is to exit the PARTIAL DISPLAY MODE.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	1	0	0	1

(15) Area scroll set (ASCSET) - Parameter Byte: 4 (AAH)

It is to scroll only the specified portion of the screen (dividing the screen by lines). This command specifies the scrolling type of area, fixed area and scrolled area.

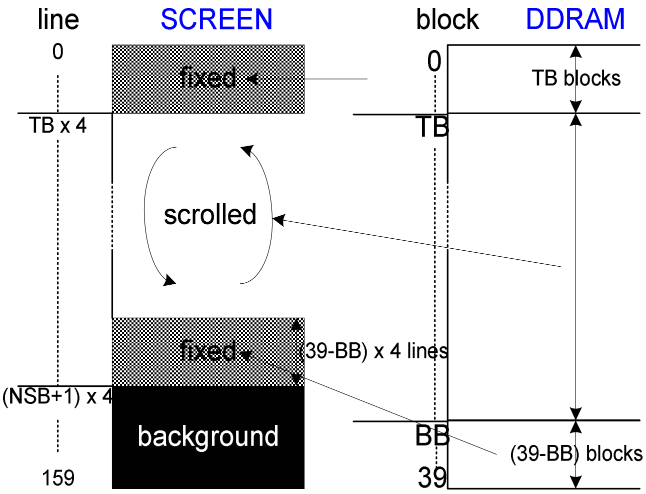
	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	0	1	0	1	0	--
Parameter Byte 1 (PB1)	1	1	0	*	*	TB5	TB4	TB3	TB2	TB1	TB0	Top block address
Parameter Byte 2 (PB2)	1	1	0	*	*	BB5	BB4	BB3	BB2	BB1	BB0	Bottom block address
Parameter Byte 3 (PB3)	1	1	0	*	*	NSB5	NSB4	NSB3	NSB2	NSB1	NSB0	Number of specified blocks
Parameter Byte 4 (PB4)	1	1	0	*	*	*	*	*	*	SCM1	SCM0	Area scroll mode

PB4: It is used to specify the scrolling mode.

SCM1	SCM0	Scrolling Mode	Settings		
			Top block address (TB)	**Bottom block address (BB)**	**Number of specified blocks (NSB)**
0	0	Center mode	Top(fixed area) height = Top address	Bottom(fixed area) height = 39-Bottom address	Bottom start address = Specified number
0	1	Top mode	0	Bottom(fixed area) height = 39-Bottom address	Bottom start address = Specified number
1	0	Bottom mode	Top(fixed area) height = Top address	39	39
1	1	Whole mode	0	39	39

Since ST7531 processes the liquid crystal display signals on the four-line basis (block basis), fixed and scrolled areas are also specified on the four-line basis (block basis).

DDRAM address of the top fixed area is set in the block address increasing direction starting with the 0th block. DDRAM address of the bottom fixed area is set in the block address decreasing direction starting with 39st block. The DDRAM address of other blocks fixed areas are assigned to the scrolled + background areas.



PB1 is to specify the top block address of the scrolled + background areas. Specify the 0th block for the top screen scroll or whole screen scroll.

PB2 specifies the bottom address of the scroll + background areas. Specify the 39th block for the bottom or whole screen scroll. The relation that top block address < bottom block address must be maintained.

PB3 specifies a specific number of blocks {Numbers of (Top fixed area +Scroll area) block-1}. In the case of the bottom scroll or whole screen scroll, the value is identical with PB2.

The user can turn on the area scroll function by executing the area scroll set command first and then specifying the display start block of the scroll area with the scroll start set command.

(16) Scroll start address set (SCSTART) - Parameter Byte: 1 (ABH)

This command is to specify which line address of DDRAM to be the start line content shown on screen. Note that you must execute this command after executing the area scroll set command. Scroll becomes available by dynamically changing the start block address.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	0	1	0	1	1	--
Parameter Byte 1 (PB1)	1	1	0	*	*	SB5	SB4	SB3	SB2	SB1	SB0	Start block address

Note : Don't repeat "Area scroll set(AAH)" instruction when "Scroll start address set" is executed.

(17) Internal oscillation on (OSCON) - Parameter Byte: none (D1H)

This command turns on the internal oscillation circuit. It is valid only when the internal oscillation circuit CLS = HIGH.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	0	0	1

(18) Internal oscillation off (OSCOFF) - Parameter Byte: none (D2H)

It turns off the internal oscillation circuit. The circuit is also turned off in the reset mode.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	0	1	0

(19) Power control set (PWRCTRL) - Parameter Byte: 1 (20H)

This command is used to turn on or off the Booster circuit, voltage regulator circuit, and reference voltage.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	1	0	0	1	0	0	0	0	0	--
Parameter Byte 1 (PB1)	1	1	0	*	*	*	0	VB	0	VF	VR	LCD drive power

VR turns on/off the reference voltage generation circuit. VR = “1”: ON, VR =” 0”: OFF

VF turns on/off the circuit voltage follower. VF = “1”: ON, VF =” 0”: OFF

VB: It turns on or off the Booster. VB = “1”: ON, VB =” 0”: OFF

(20) Electronic volume control (VOLCTRL) - Parameter Byte: 2 (81H)

The command is used to program the optimum LCD supply voltage V_0. Refer to 8.10.2.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	0	0	0	0	0	1	--
Parameter Byte 1 (PB1)	1	1	0	*	*	VPR5	VPR4	VPR3	VPR2	VPR1	VPR0	VPR[5:0]
Parameter Byte 2 (PB2)	1	1	0	*	*	*	*	*	VPR8	VPR7	VPR6	VPR[8:6]

With the VOLUP and VOLDOWN command the V_0 voltage and therewith the contrast of the LCD can be adjusted.

(21) Increment electronic control (VOLUP) - Parameter Byte: none (D6H)

This command increments electronic control offset value of voltage regulator (V0) circuit by 1. Each step is 0.04V.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	1	1	0

If you set the electronic control value to 111111, the control value is set to 000000 after this command has been executed.

(22) Decrement electronic control (VOLDOWN) - Parameter Byte: none (D7H)

This command decrements electronic control offset value of voltage regulator (V0) circuit by 1. Each step is 0.04V.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	1	1	1

If you set the electronic control value to 000000, the control value is set to 111111 after this command has been executed.

(23) Reserved (82H)

Do not use this command.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	0	0	0	0	1	0

(24) Read Register 1 (EPSRRD1) Command: 1 Parameter Byte: none (7CH)

Execute the EPSRRD1 and STREAD (Status Read) commands in succession to read the Electronic Control value.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	1	1	1	1	1	0	0

Execute the Status Read command immediately after this command and execute the NOP command after the STREAD (Status Read) command.

(25) Read Register 2 (EPSRRD2) Command: 1 Parameter Byte: none (7DH)

Execute the EPSRRD2 and STREAD (Status Read) commands in succession to read the built-in resistance ratio.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	1	1	1	1	1	0	1

Execute the Status Read command immediately after this command and execute the NOP(Reset) command after the STREAD (Status Read) command.

(26) Non-operating (NOP) - Parameter Byte: none (25H)

This command does not affect the operation but has the function of canceling the IC test mode. Thus, it is recommended to enter it periodically to prevent malfunctioning due to noise and so on.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	0	0	1	0	1

(27) Status read (STREAD) - Parameter Byte: none

The command is to read the internal condition of the IC. One status can be displayed depending on the setting status after reset or after NOP operation.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	0	1	Status data							

D7: Area scroll mode	Refer to SCM1 (ASCSET)	
D6: Area scroll mode	Refer to SCM0 (ASCSET)	
D5: RMW on/off	0 : Out	1 : In
D4: Scan direction	0 : Column	1 : Line
D3: Display ON/OFF	0 : OFF	1 : ON
D2: EEPROM access	0: OutAccess	1: InAccess
D1: Display normal/inverse	0 : Inverse	1 : Normal
D0: Partial display	0 : OFF	1 : ON

(28) Initial code (1) (EPINT) Command: 1; Parameter: 1 (07H)

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	0	0	0	1	1	1	07H
Parameter(P1)	1	1	0	0	0	0	1	1	0	0	1	19H

This command is used for EEPROM internal ACK signal generating ,suggest using this command before EEPROM read/write operation . This command improve the EEPROM internal ACK signal under unstable power system.

EXT="1"

The ST7531 applies 16-gray level and 2 FRC to achieve 32-gray scale display. Every gray level is in the strength controlled by 31-PWM (5-bit). The following 2 commands are to set the gray scale value.

(1) Set Gray 1 value (Gray 1 set) - Parameter Byte: 16 (20H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Gray1 Set	0	1	0	0	0	1	0	0	0	0	0	ODD FRAME Gray PWM Set
Parameter Byte 1 (PB1)	1	1	0	*	*	*	G0F14	G0F13	G0F12	G0F11	G0F10	Set Gray level 0 at odd frames
Parameter Byte 2 (PB2)	1	1	0	*	*	*	G1F14	G1F13	G1F12	G1F11	G1F10	Set Gray level 1 at odd frames
Parameter Byte 14 (PB14)	1	1	0	*	*	*	G13F14	G13F13	G13F12	G13F11	G13F10	Set Gray level 13 at odd frames
Parameter Byte 16 (PB16)	1	1	0	*	*	*	G15F14	G15F13	G15F12	G15F11	G15F10	Set Gray level 15 at odd frames

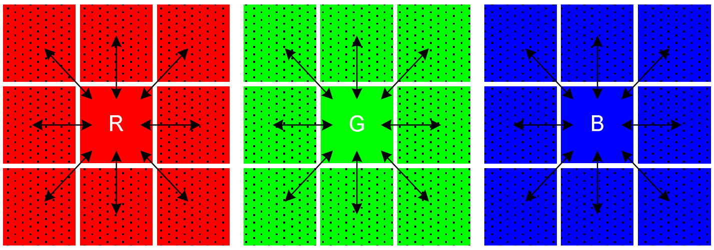
(2) Set Gray 2 value (Gray 2 set) - Parameter Byte: 16 (21H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Gray1 Set	0	1	0	0	0	1	0	0	0	0	1	EVEN FRAME Gray PWM Set
Parameter Byte 1 (PB1)	1	1	0	*	*	*	G0F24	G0F23	G0F22	G0F21	G0F20	Set Gray level 0 at even frames
Parameter Byte 2 (PB2)	1	1	0	*	*	*	G1F24	G1F23	G1F22	G1F21	G1F20	Set Gray level 1 at even frames
Parameter Byte 14 (PB14)	1	1	0	*	*	*	G13F24	G13F23	G13F22	G13F21	G13F20	Set Gray level 13 at even frames
Parameter Byte 16 (PB16)	1	1	0	*	*	*	G15F24	G15F23	G15F22	G15F21	G15F20	Set Gray level 15 at even frames

(3) Weight Set (Wt. set) - Parameter Byte: 3 (22H)

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	1	0	---
Parameter Byte 1 (PB1)	1	1	0	*	*	*	*	*	WT2	WT1	WT0	
Parameter Byte 2 (PB2)	1	1	0	*	*	*	ED4	ED3	ED2	ED1	ED0	set edge detector detect value
Parameter Byte 3 (PB3)	1	1	0	*	*	*	*	*	*	EE	WE	

PB1: Weighting Set



Compared with stripe, SPRD uses fewer channels but lost only a little part of display information. The additional "Weighting set" is to recompense color information.

In normal display, there is relativity of color between pixel and pixel. Therefore, the lost element can be used to compensate the next pixel and enhance the display quality.

The sum of all "Weight set" values should be equal to "1" :

$R(x-1,y-1) + R(x,y-1) + R(x+1,y-1) + R(x-1,y) + R(x,y) + R(x+1,y) + R(x-1,y+1) + R(x,y+1) + R(x+1,y+1) = 1$

$G(x-1,y-1) + G(x,y-1) + G(x+1,y-1) + G(x-1,y) + G(x,y) + G(x+1,y) + G(x-1,y+1) + G(x,y+1) + G(x+1,y+1) = 1$

$B(x-1,y-1) + B(x,y-1) + B(x+1,y-1) + B(x-1,y) + B(x,y) + B(x+1,y) + B(x-1,y+1) + B(x,y+1) + B(x+1,y+1) = 1$

WT2	WT1	WT0	Weighting k
0	0	0	0/8
0	0	1	1/8
0	1	0	2/8
0	1	1	3/8 (default)
1	0	0	4/8

Assume the dots on display are arranged as follows.

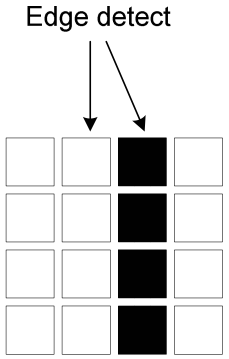
D_0	D_1	…	D_i	…	D_{n-1}	D_n

After processed, $\mathbf{D_i}$ will become $\mathbf{kD_{i-1}+(1-k)\,D_i}$. In addition, the new value will be saved as $\mathbf{D_i}$'– the new $\mathbf{D_i}$ in RAM.

PB2: set edge detector detect value

ED4	ED3	ED2	ED1	ED0	detect value
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	1	1	1	0	14
0	1	1	1	1	15
1	0	0	0	0	16 (default)
1	0	0	0	1	17
1	0	0	1	0	18
1	1	1	0	0	28
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31

When "Edge detect" is enabled, the difference value between pixel and pixel which is large enough will activate the "Weight set" function.



PB3:

EE	WE	
0	0	no weighting
0	1	weighting enable
1	*	weighting + edge detect

***: don't care**

(4) Analog circuit set (ANASET) – Parameter Byte: 3 (32H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	1	0	0	1	0	–
Parameter Byte 1 (PB1)	1	1	0	*	*	*	*	*	OSF2	OSF1	OSF0	OSC frequency Adjustment
Parameter Byte 2 (PB2)	1	1	0	*	*	*	*	*	*	BE1	BE0	Booster Efficiency Set
Parameter Byte 3 (PB3)	1	1	0	*	*	*	*	*	BS2	BS1	BS0	Bias setting

PB1: Oscillator frequency adjustment

OSF2	OSF1	OSF0	Frequency (KHz)
0	0	0	12.7 (Default)
1	0	0	13.2
0	1	0	14.3
1	1	0	15.7
0	0	1	17.3
1	0	1	19.3
0	1	1	21.9
1	1	1	25.4

Condition : 1/160 duty, fCL(Hz) = Frame frequency x (duty + 1dummy)

PB2: Booster Efficiency set

BE1	BE0	Frequency on booster capacitors (Hz)
0	0	3K
0	1	6K (Default)
1	0	12K
1	1	24K

PB3: Select LCD bias ratio of the voltage required for driving the LCD.

BS2	BS1	BS0	LCD bias
0	0	0	1/14
0	0	1	1/13
0	1	0	1/12
0	1	1	1/11
1	0	0	1/10
1	0	1	1/9
1	1	0	1/7
1	1	1	1/5

(5) Color Dither OFF (DITHOFF) - Parameter Byte: None (34H)

Turn off the dithering circuit.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	1	0	1	0	0

(6) Color Dither ON (DITHON) - Parameter Byte: None (35H)

Turn on the dithering circuit.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	1	0	1	0	1

(7) Control EEPROM (EPCTIN) - Parameter Byte: 1 (CDH)

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	0	1	1	0	1
Parameter Byte 1 (PB1)	1	1	0	0	0	EEWR	0	0	0	0	0

When EEWR = “1”, EEPROM will be Write Enable; when EEWR = “0”, EEPROM will be Read Enable.

(8) Cancel EEPROM Command (EPCOUT) - Parameter Byte: None (CCH)

This command is to cancel the EEPROM Read/Write Enable.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	0	1	1	0	0

(9) Write data to EEPROM (EPMWR) - Parameter Byte: None (FCH)

This command is to Write data to EEPROM.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	1	1	1	0	0

(10) Read data from EEPROM (EPMRD) - Parameter Byte: None (FDH)

This command is to Read data from EEPROM.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	1	1	1	0	1

8.2 Referential Instruction Setup Flow

8.2.1 EEPROM Setting Flow

The ST7531 provide the Write and Read function to write the Electronic Control value into and read them from the built-in EEPROM. Using the Write and Read functions, you can store these values appropriate to each LCD panel. This function is very convenient for user in setting from some different panel's voltage. But using this function must attention the setting procedure. Please see the following diagram.

Note: When "Writing" value to EEPROM, the voltage of $VOUT_{IN}$ must be more than 18V.

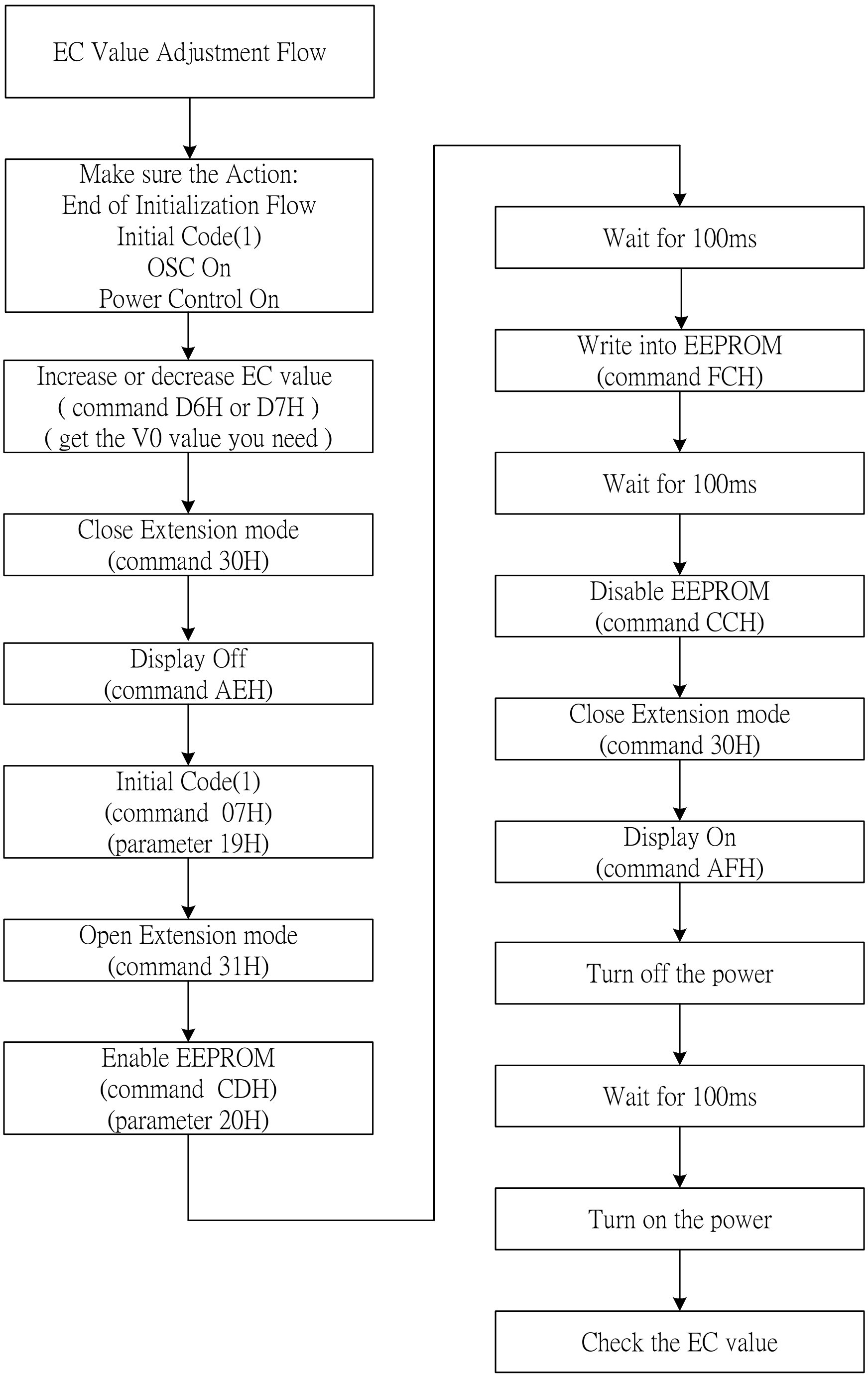


Figure 8.2.1.1 Flow of EC value adjustment and writing into EEPROM

Note: When “Reading” value from EEPROM, the voltage of $VOUT_{IN}$ must be more than 6V.

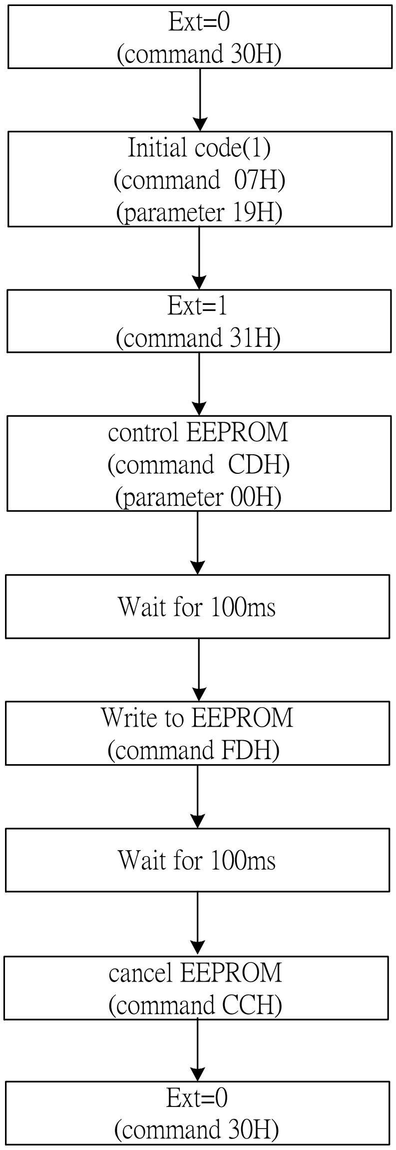


Figure 8.2.1.2 EEPROM Reading flow

Example：EEPROM Read Operation

```
void ReadEEPROM( void )
    {

        Write( COMMAND, 0x0030 );           // Ext = 0
        Write( COMMAND, 0x0007 );           // Initial code (1)
        Write( DATA, 0x0019 );
        Write( COMMAND, 0x0031 );           // Ext = 1
        Write( COMMAND, 0x00CD );           // EEPROM ON
        Write( DATA, 0x0000 );              // Entry "Read Mode"
        Delay( 100ms );                     // Waite for EEPROM Operation ( 100ms )
        Write( COMMAND, 0x00FD );           // Start EEPROM Reading Operation
        Delay( 100ms );                     // Waite for EEPROM Operation ( 100ms )
        Write( COMMAND, 0x00CC );           // Exist EEPROM Mode
        Write( COMMAND, 0x0030 );           // Ext = 0

    }
```

Example：EEPROM Write Operation

```
void WriteEEPROM( void )
    {

        Write( COMMAND, 0x0030 );           // Ext = 0
        Write( COMMAND, 0x00AE );           // Display OFF
        Write( COMMAND, 0x0007 );           // Initial code(1)
        Write( DATA, 0x0019 );
        Write( COMMAND, 0x0031 );           // Ext = 1
        Write( COMMAND, 0x00CD );           // EEPROM ON
        Write( DATA, 0x0020 );              // Entry "Write Mode"
        Delay( 100ms );                     // Waite for EEPROM Operation ( 100ms )
        Write( COMMAND, 0x00FC );           // Start EEPROM Writing Operation
        Delay( 100ms );                     // Waite for EEPROM Operation ( 100ms )
        Write( COMMAND, 0x00CC );           // Exist EEPROM Mode
        Write( COMMAND, 0x0030 );           // Ext = 0
        Write( COMMAND, 0x00AF );           // Display ON

    }
```

8.2.2 Initializing with the Built-in Power Supply Circuits

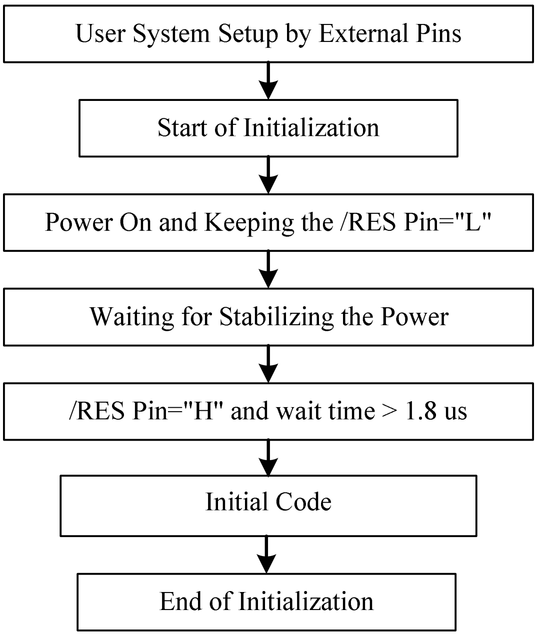
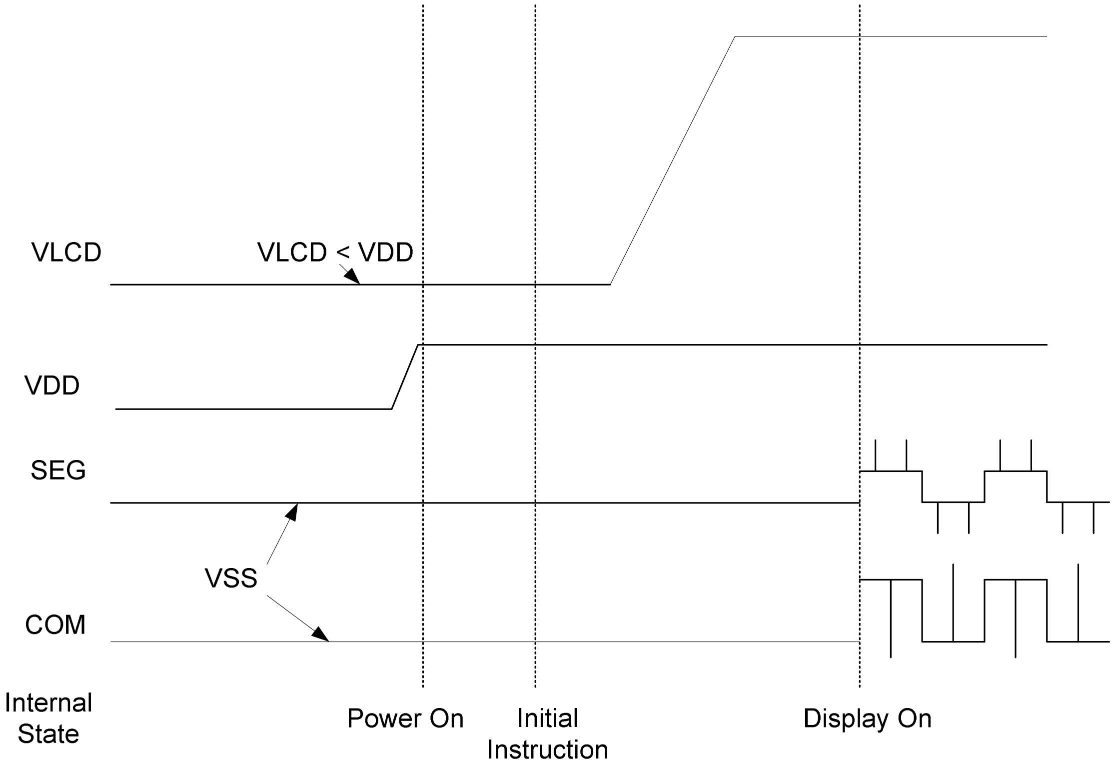


Figure 8.2.2.1 Initializing with the Built-in Power Supply Circuits

When Power-ON (VDD/VDD2 goes from low to high), please follow the sequence shown below. If not, some unpredictable result may occur.



Example：Initial code for 170X160

```
void ST7531_Init( void )
    {
        Write( COMMAND, 0x0030 );       //Ext = 0

        Write( COMMAND, 0x0094 );       //Sleep Out

        Write( COMMAND, 0x00D1 );       //OSC On
        Write( COMMAND, 0x0020 );       //Power Control Set
        Write( DATA, 0x0008 );          //Booster Must Be On First
        Delay( 1ms );
        Write( COMMAND, 0x0020 );       //Power Control Set
        Write( DATA, 0x000B );          //Booster, Regulator, Follower ON

        Write( COMMAND, 0x0081 );       //Electronic Control
        Write( DATA, 0x0004 );          //Vop=14.0V
        Write( DATA, 0x0004 );

        Write( COMMAND, 0x00CA );       //Display Control
        Write( DATA, 0x0000 );          //CL=X1
        Write( DATA, 0x0027 );          //Duty=160
        Write( DATA, 0x0000 );          //FR Inverse-Set Value

        Write( COMMAND, 0x00A6 );       // Normal Display

        Write( COMMAND, 0x00BB );       //COM Scan Direction
        Write( DATA, 0x0001 );          // 0→79 159→80

        Write( COMMAND, 0x00BC );       //Data Scan Direction
        Write( DATA, 0x0000 );          //Normal
        Write( DATA, 0x0000 );          //RGB Arrangement
        Write( DATA, 0x0001 );          //65K COLOR

        Write( COMMAND, 0x0075 );       //Line Address Set
        Write( DATA, 0x0000 );          //Start Line=0
        Write( DATA, 0x009F );          //End Line =159

        Write( COMMAND, 0x0015 );       //Column Address Set
        Write( DATA, 0x0000 );          //Start Column=0
        Write( DATA, 0x00A9 );          //End Column =169

        Write( COMMAND, 0x0031 );       //Ext = 1

        Write( COMMAND, 0x0032 );       //Analog Circuit Set
        Write( DATA, 0x0000 );          //OSC Frequency =000 (Default)
        Write( DATA, 0x0001 );          //Booster Efficiency=01(Default)
        Write( DATA, 0x0000 );          //Bias=1/14

        Write( COMMAND, 0x0034 );       //Dithering Off

        ReadEEPROM();                   //Read EEPROM Flow

        Write( COMMAND, 0x0030 );       //Ext = 0

        Write( COMMAND, 0x00AF );       //Display On

    }
```

NOTE:

Microprocessor interface pins should not be floating in any operation mode.

8.2.3 Data Displaying

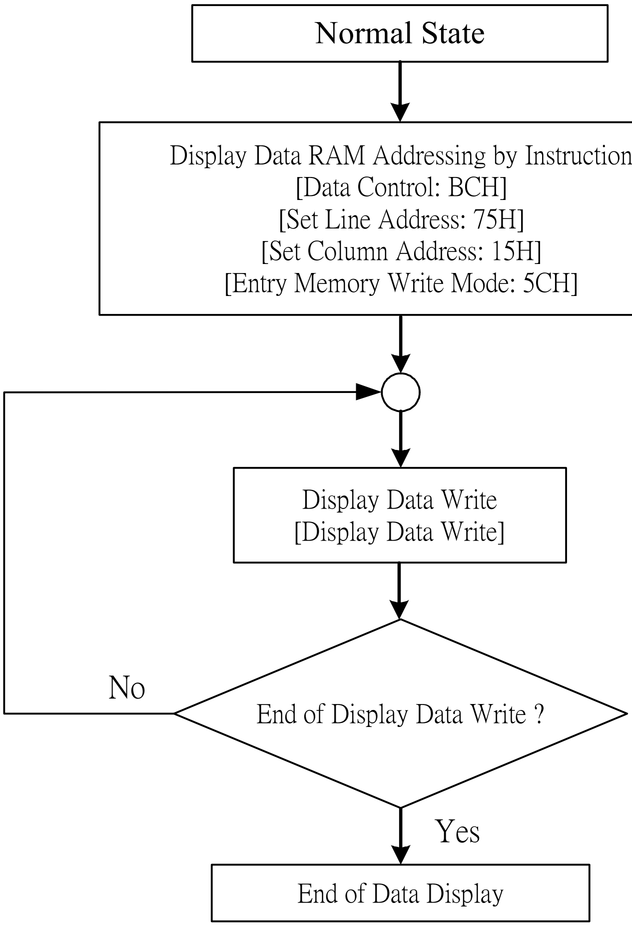


Figure 8.2.3.1 Data Displaying

Example：Display for 170X160

```
void Display( char *pattern )
        {

          unsigned char i, j;

          Write( COMMAND, 0x0030 );                    // Ext = 0
          Write( COMMAND, 0x0015 );                    // Column address set
          Write( DATA, 0x0000 );                       // From column0 to column169
          Write( DATA, 0x00A9 );
          Write( COMMAND, 0x0075 );                    // Page address set
          Write( DATA, 0x0000 );                       // From line0 to line159
          Write( DATA, 0x009F);
          Write( COMMAND, 0x005C )                     // Entry Memory Write Mode
          for( j = 0; j < 160 ; j++ )
             For( i = 0 ; i < 170 ; i++ )
                Write( DATA, pattern[ j * 160 + i ] );  // Display Data Write


        }
```

8.2.4 Partial Display In/Out

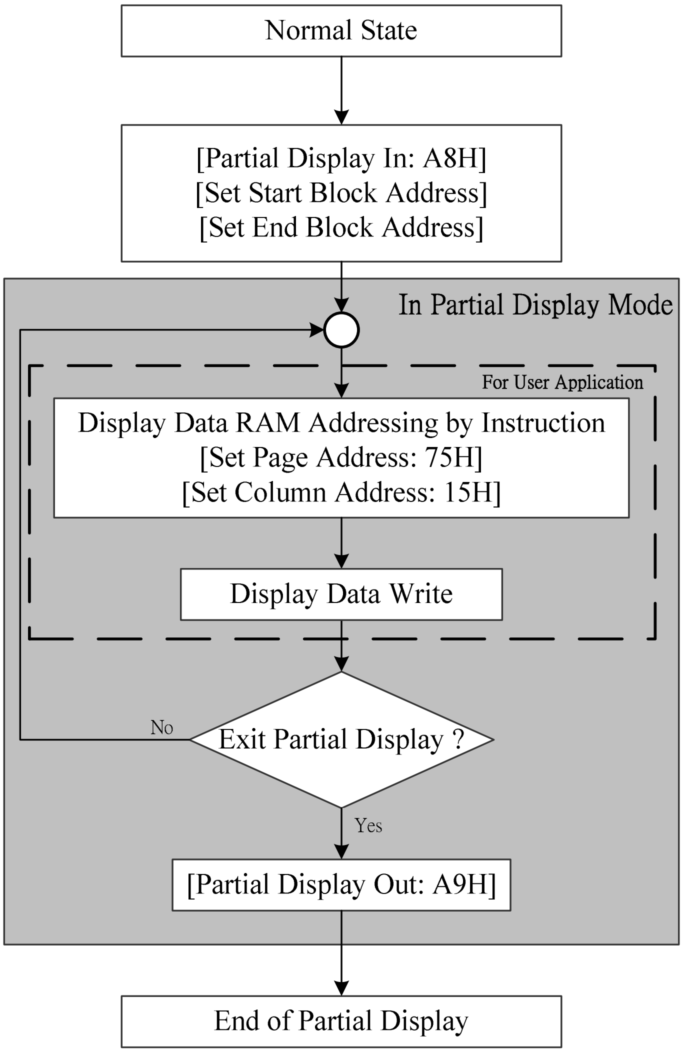


Figure 8.2.4.1 Partial Display In/Out

Example：Partial Display In/Out Operation

```
void PartailIn( unsigned char start_block, unsigned char end_block )
      {
         Write( COMMAND, 0x0030 );               // Ext = 0
         Write( COMMAND, 0x00A8);                // Partial Display In Function
         Write( DATA, start_block );             // Start Block
         Write( DATA, end_block );               // End Block

      }

void PartailOut( void )
      {
         Write( COMMAND, 0x0030 );               // Ext = 0
         Write( COMMAND, 0x00A9 );               // Partial Display Out Function

      }
```

```
extern unsigned char *display_pattern;
void main()
    {

        PartialIn( 11, 18 );                    // entry partial display mode

        Windowing( 0, 11*4, 169, 18*4 );        // set the page and column range
        PartialDisplay( display_pattern );      // Fill the data into partial display area
              .
              .
              .
        PartialOut();                           // Out of partial display mode

    }
```

8.2.5 Scroll Display

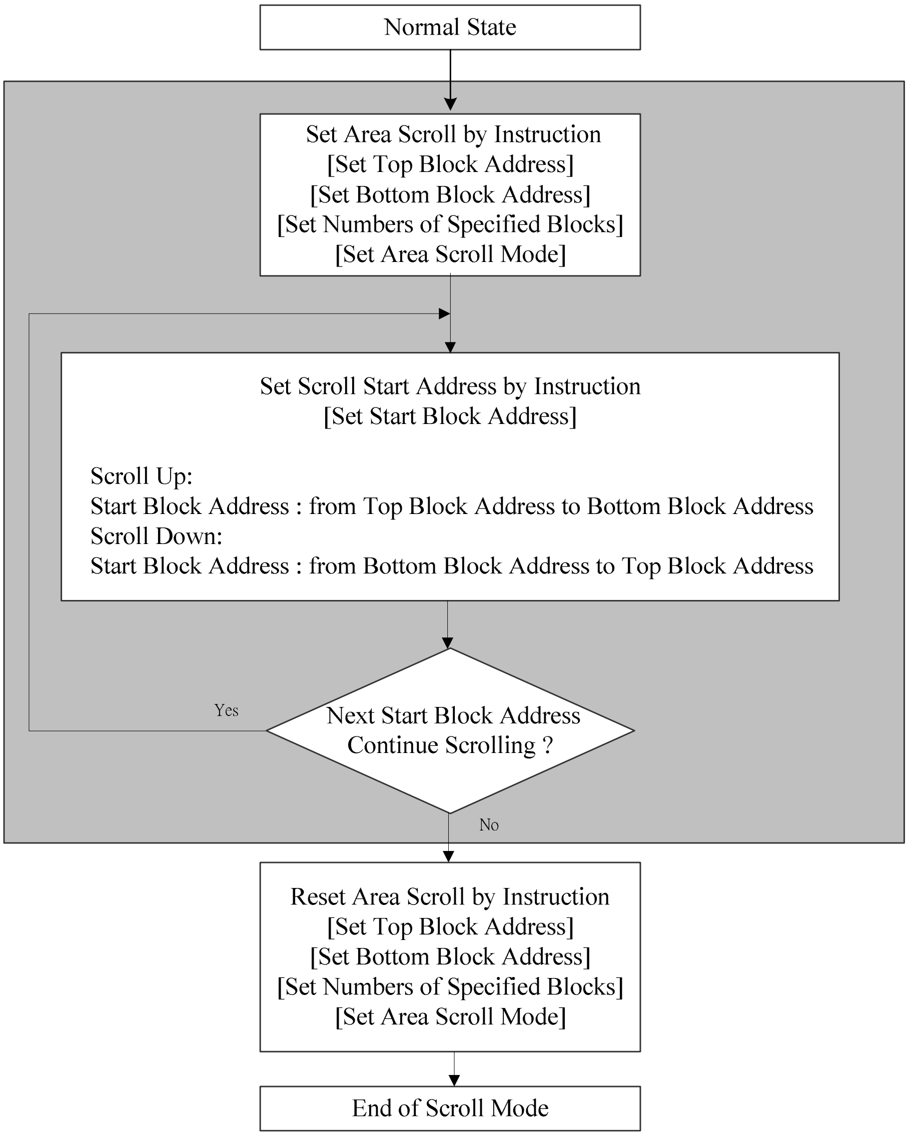


Figure 8.2.5.1 Scroll Display

Example：Screen Scroll Operation

```
void CenterScreenScroll( void )
      {

          Write( COMMAND, 0x0030 );             // Ext = 0
          Write( COMMAND, 0x00AA);              // Partial Display In Function
          Write( DATA, 0x000A );                // Top_Block=10
          Write( DATA, 0x0014 );                // Bottom_Block=20
          Write( DATA, 0x0014 );                // Number of Specified Blocks=Bottom_Block=20
          Write( DATA, 0x0000 );                // Area Scroll Type=Center Screen Scroll

          ScrollUp() or ScrollDown();           // Scroll Up or Scroll Down

      }

void TopScreenScroll( void )
      {

          Write( COMMAND, 0x0030 );             // Ext = 0
          Write( COMMAND, 0x00AA);              // Partial Display In Function
          Write( DATA, 0x0000 );                // Top_Block=0
          Write( DATA, 0x0014 );                // Bottom_Block=20
          Write( DATA, 0x0014 );                // Number of Specified Blocks=Bottom_Block=20
          Write( DATA, 0x0001 );                // Area Scroll Type=Top Screen Scroll

          ScrollUp() or ScrollDown();           // Scroll Up or Scroll Down

      }

void BottomScreenScroll( void )
      {

          Write( COMMAND, 0x0030 );             // Ext = 0
          Write( COMMAND, 0x00AA);              // Partial Display In Function
          Write( DATA, 0x000A );                // Top_Block=10
          Write( DATA, 0x0019 );                // Bottom_Block=25
          Write( DATA, 0x0019 );                // Number of Specified Blocks=Bottom_Block=25
          Write( DATA, 0x0002 );                // Area Scroll Type=Bottom Screen Scroll

          ScrollUp() or ScrollDown();           // Scroll Up or Scroll Down

      }

void WholeScreenScroll( void )
      {

          Write( COMMAND, 0x0030 );             // Ext = 0
          Write( COMMAND, 0x00AA);              // Partial Display In Function
          Write( DATA, 0x0000 );                // Top_Block=0
          Write( DATA, 0x0019 );                // Bottom_Block=25
          Write( DATA, 0x0019 );                // Number of Specified Blocks=Bottom_Block=25
          Write( DATA, 0x0003 );                // Area Scroll Type=Whole Screen Scroll

          ScrollUp() or ScrollDown();           // Scroll Up or Scroll Down

      }
```

```
void ScrollUp( void )
       {

          Write( COMMAND, 0x0030 );                // Ext = 0
          Write( COMMAND, 0x00AB);                 // Scroll Start Set
          Write( DATA, Top_Block);                 // Start Block Address=Top_Block
          Delay();                                 // Delay

          Write( COMMAND, 0x00AB);                 // Scroll Start Set
          Write( DATA, Top_Block +1 );             // Start Block Address= Top_Block+1
          Delay();                                 // Delay

          Write( COMMAND, 0x00AB);                 // Scroll Start Set
          Write( DATA, Top_Block +2 );             // Start Block Address= Top_Block +2
          Delay();                                 // Delay
          ……
          ……
          Write( COMMAND, 0x00AB);                 // Scroll Start Set
          Write( DATA, Bottom_Block );             // Start Block Address= Bottom_Block
          Delay();                                 // Delay

       }

void ScrollDown( void )
       {

          Write( COMMAND, 0x0030 );                // Ext = 0
          Write( COMMAND, 0x00AB);                 // Scroll Start Set
          Write( DATA, Bottom_Block);              // Start Block Address= Bottom_Block
          Delay();                                 // Delay

          Write( COMMAND, 0x00AB);                 // Scroll Start Set
          Write( DATA, Bottom_Block -1 );          // Start Block Address= Bottom_Block -1
          Delay();                                 // Delay

          Write( COMMAND, 0x00AB);                 // Scroll Start Set
          Write( DATA, Bottom_Block -2 );          // Start Block Address= Bottom_Block -2
          Delay();                                 // Delay
          ……
          ……
          Write( COMMAND, 0x00AB);                 // Scroll Start Set
          Write( DATA, Top _Block );               // Start Block Address= Top_Block
          Delay();                                 // Delay

       }
```

8.2.6 Display On / OFF

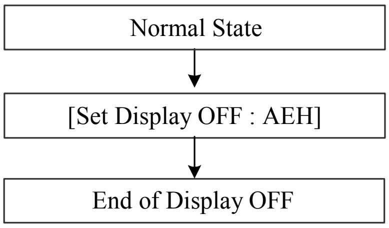


Figure 8.2.6.1 Display Off

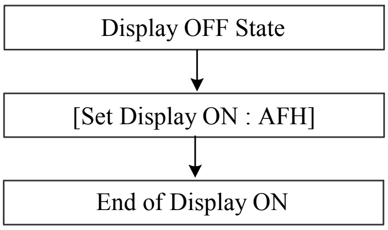


Figure 8.2.6.2 Display On

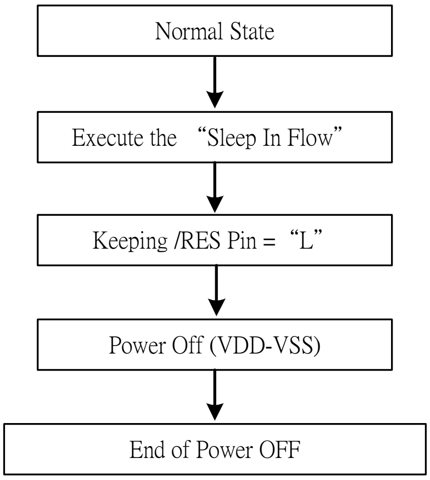
Example：Display OFF Operation

```
void DisplayOff( void )
     {
         Write( COMMAND, 0x0030 );       // Ext = 0
         Write( COMMAND, 0x00AE );       // Display Off
     }
```

Example：Display ON Operation

```
void DisplayOn( void )
     {
         Write( COMMAND, 0x0030 );       // Ext = 0
         Write( COMMAND, 0x00AF );       // Display On
     }
```

8.2.7 Power OFF



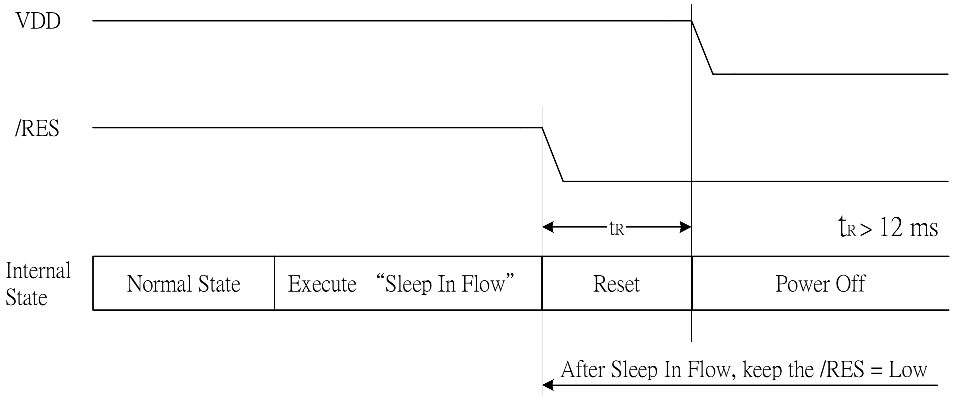


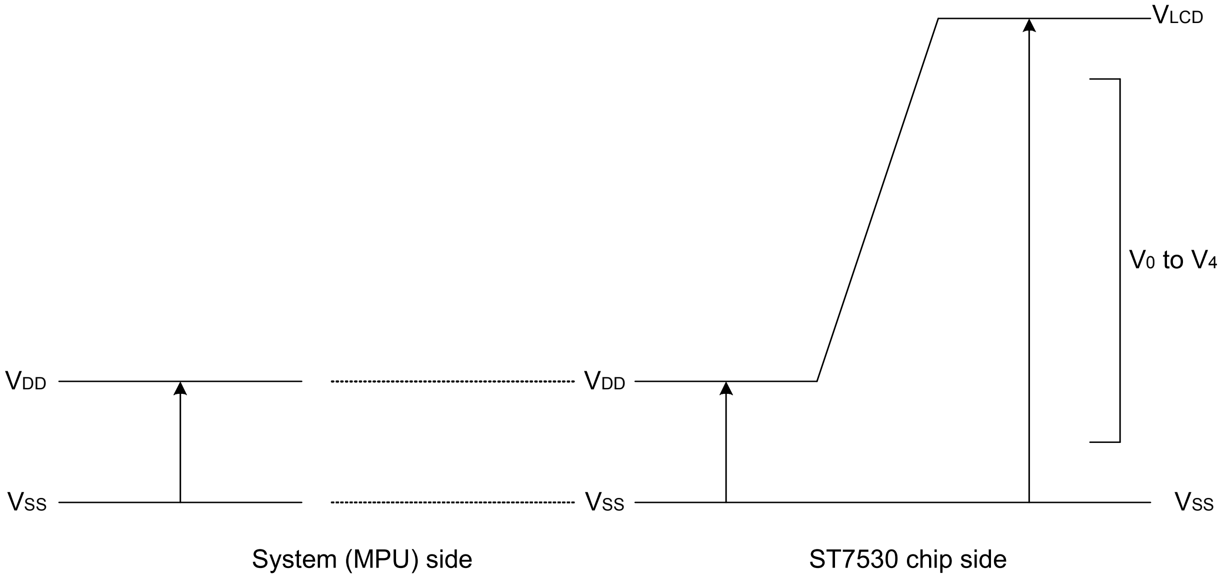
Figure 8.2.7.1 Power off

Note：The sequence is that users must set the VDD to low after keeping the /RES=low time longer than 12ms.

9. LIMITING VALUES

In accordance with the Absolute Maximum Rating System; see notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Power Supply Voltage	VDD, VDD1	–0.5 ~ +4.0	V
Power supply voltage	VDD2, VDD3, VDD4, VDD5	-0.5 ~ +4.0	V
Power supply voltage (VDD standard)	VLCDIN, VLCDOUT	–0.5 ~ +20	V
Power supply voltage (VDD standard)	V0,V1, V2, V3, V4	0.3 to VLCDIN	V
Input voltage	VIN	–0.5 to VDD+0.5	V
Output voltage	VO	–0.5 to VDD+0.5	V
Operating temperature(Die)	TOPR	–30 to +85	°C
Storage temperature(Die)	TSTR	–40 to +125	°C



Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.

2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

3. Insure that the voltage levels of V1, V2, V3, and V4 are always such that

VLCDIN ≧ V0 ≧ V1 ≧ V2 ≧ V3 ≧ V4 ≧ Vss

10. HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see “Handling MOS devices”).

11. DC CHARACTERISTICS

T_a = -30℃ to +85℃

Item		Symbol	Condition	Rating			Units	Applicable Pin
				Min.	Typ.	Max.		
Operating Voltage (1)		VDD VDD1	-	2.4	-	3.3	V	VDD*1 VDD1
Operating Voltage (2)		VDD2 VDD3 VDD4 VDD5	(Relative to VSS)	2.4	-	3.3	V	VDD2 VDD3 VDD4 VDD5
High-level Input Voltage		VIH	-	0.7 VDD	-	VDD	V	*2
Low-level Input Voltage		VIL	-	VSS	-	0.3 VDD	V	*2
High-level Output Current		IOH	VDD=2.7V VOH =2.2V	0.5	-	-	mA	*3
Low-level Output Current		IOL	VDD=2.7V VOL = 0.5V	-	-	-0.5	mA	*3
Input leakage current		ILI	VIN = VDD or VSS	-1.0	-	1.0	µA	*4
Liquid Crystal Driver ON Resistance		RON	Ta = 25°C (Relative To VSS) V0 = 14.0V VDD = 2.7V	-	1.4	2.0	KΩ	SEGn COMn *5
Oscillator Frequency	Internal Oscillator	fOSC	1/160 duty Ta = 25°C VDD = 2.7V CLD = 0	-	12.4	26	kHz	CL*6
	External Input	fCL		-	12.4	26	kHz	CL
	Frame frequency	fFRAME		-	78	160	Hz	SEGn

Item		Symbol	Condition	Rating			Units	Applicable Pin
				Min.	Typ.	Max.		
Internal Power	Input voltage	VDD	(Relative To VSS)	1.8	-	3.3	V	VDD
	Supply Step-up output voltage Circuit	VLCDOUT	(Relative To VSS)	-	-	18	V	VLCDOUT
	Voltage regulator Circuit Operating Voltage	VLCDIN	(Relative To VSS)	-	-	18	V	VLCDIN

*** Recommended LCD V_{OP} voltage is 12V~14V .**

Dynamic Consumption Current : During Display, with the Internal Power Supply OFF Current consumed by total ICs when an external power supply is used . (Used die to measure)

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern (checkerboard)	ISS	VDD = 2.8 V, V0 – VSS = 16.0 V Booster = 6x Bias = 1/12 Duty = 1/160 Bare chip Cap = 1.0uF	-	460	600	μA	*7
Power Down	ISS	Ta = 25°C	-	-	10	μA	-

Notes to the DC characteristics

1. The maximum possible V_{LCD} voltage that may be generated is dependent on voltage, temperature and (display) load, and Internal clock
2. Power-down mode. During power down all static currents are switched off.
3. If external V_{LCD}, the display load current is not transmitted to I_{DD}.
4. V_{LCD} external voltage applied to VLCDIN pin; VLCDIN disconnected from VLCDOUT

References for items marked with *

*1. While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.

*2. The A0, D0 to D5, D6 (SI), D7 (SCL),D8 to D15 /RD(E), /WR(R/W), XCS,CL , RST .

*3. The D0 to D7, D8 to D15 and CL.

*4. The A0,/RD (E), /WR(R/W), XCS, CLS, CL, RST , IF1 to IF3, M0, M1.

*5. These are the resistance values for when a 0.1 V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V1, V2, V3, and V4). These are specified for the operating voltage range.
RON = 0.1 V /ΔI (Where ΔI is the current that flows when 0.1 V is applied while the power supply is ON.)

*6. The relationship between the oscillator frequency and the frame rate frequency.

*7. It indicates the current consumed on ICs alone when the internal oscillator circuit and display are turned on.

ST7531 I/O PIN ITO Resister Limitation

PIN Name	ITO Resister
IF1~IF3, M0, M1, CLS	No Limitation
VREF, T0~T10, TCAP, CL	Floating
VDD,VDD1~5,VSS,VSS1,VSS2,VSS4, V_{LCDIN}, V_{LCDOUT} , CxP, CxN	<100Ω
V0IN, V0OUT, V1, V2, V3, V4	<500Ω
A0, RW_WR, E_RD, XCS, D0 …D15, SCL, SI	<1kΩ
RST	<10kΩ

12. AC CHARACTERISTICS

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

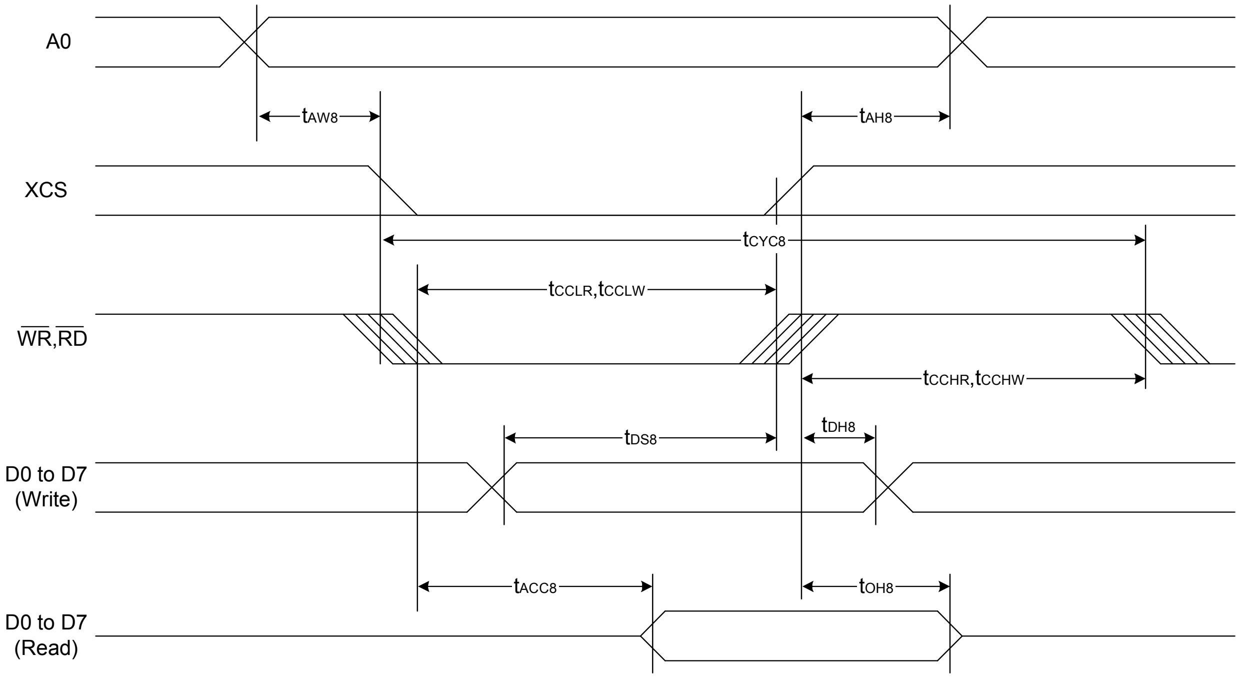


Figure 39.

(VDD = 3.3V , Ta = –30 to 85°C,Die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8	-	20	-	ns
Address setup time		tAW8	-	20	-	
System cycle time		tCYC8	-	200	-	
Enable L pulse width (WRITE)	WR	tCCLW	-	100	-	
Enable H pulse width (WRITE)		tCCHW	-	100	-	
Enable L pulse width (READ)	RD	tCCLR	-	100	-	
Enable H pulse width (READ)		tCCHR	-	100	-	
WRITE Data setup time	D0 to D7	tDS8	-	150	-	
WRITE Data hold time		tDH8	-	20	-	
READ access time		tACC8	CL = 100 pF	-	40	
READ Output disable time		tOH8	CL = 100 pF	-	30	

(VDD = 2.7V , Ta = –30 to 85°C,Die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8	-	20	-	ns
Address setup time		tAW8	-	30	-	
System cycle time		tCYC8	-	250	-	
Enable L pulse width (WRITE)	WR	tCCLW	-	150	-	
Enable H pulse width (WRITE)		tCCHW	-	100	-	
Enable L pulse width (READ)	RD	tCCLR	-	150	-	
Enable H pulse width (READ)		tCCHR	-	100	-	
WRITE Data setup time	D0 to D7	tDS8	-	200	-	
WRITE Data hold time		tDH8	-	20	-	
READ access time		tACC8	CL = 100 pF	-	40	
READ Output disable time		tOH8	CL = 100 pF	-	30	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≦ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≦ (tCYC8 – tCCLR – tCCHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tCCLW and tCCLR are specified as the overlap between XCS being “L” and WR and RD being at the “L” level.

System Bus Read/Write Characteristics 1 (For the 6800 Series MPU)

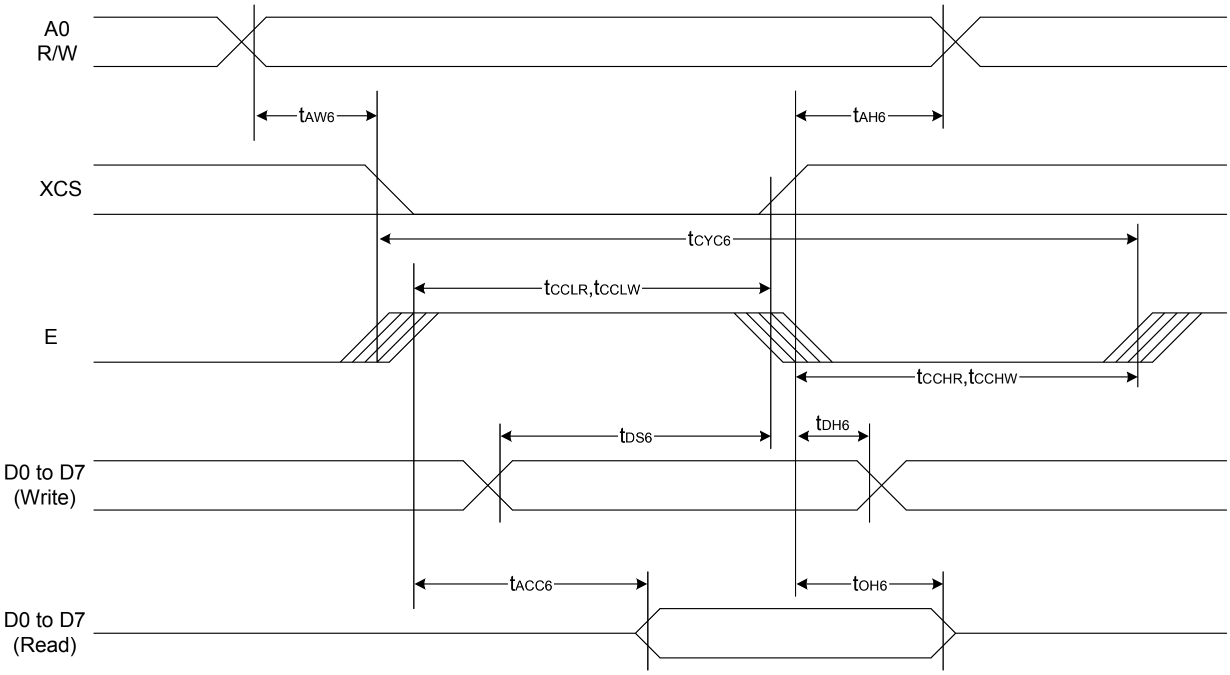


Figure 40.

(VDD = 3.3V , Ta = –30 to 85°C,Die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6	-	20	-	ns
Address setup time		tAW6	-	20	-	
System cycle time		tCYC6	-	200	-	
Enable L pulse width (WRITE)	WR	tEWLW	-	100	-	
Enable H pulse width (WRITE)		tEWHW	-	100	-	
Enable L pulse width (READ)	RD	tEWLR	-	100	-	
Enable H pulse width (READ)		tEWHR	-	100	-	
WRITE Data setup time	D0 to D7	tDS6	-	150	-	
WRITE Data hold time		tDH6	-	20	-	
READ access time		tACC6	CL = 100 pF	-	40	
READ Output disable time		tOH6	CL = 100 pF	-	30	

(VDD = 2.7V , Ta = –30 to 85°C,Die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6	-	20	-	ns
Address setup time		tAW6	-	30	-	
System cycle time		tCYC6	-	250	-	
Enable L pulse width (WRITE)	WR	tEWLW	-	150	-	
Enable H pulse width (WRITE)		tEWHW	-	100	-	
Enable L pulse width (READ)	RD	tEWLR	-	150	-	
Enable H pulse width (READ)		tEWHR	-	100	-	
WRITE Data setup time	D0 to D7	tDS6	-	200	-	
WRITE Data hold time		tDH6	-	20	-	
READ access time		tACC6	CL = 100 pF	-	40	
READ Output disable time		tOH6	CL = 100 pF	-	30	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≦ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≦ (tCYC6 – tEWLR – tEWHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tEWLW and tEWLR are specified as the overlap between XCS being “L” and E.

SERIAL INTERFACE (4-Line Interface)

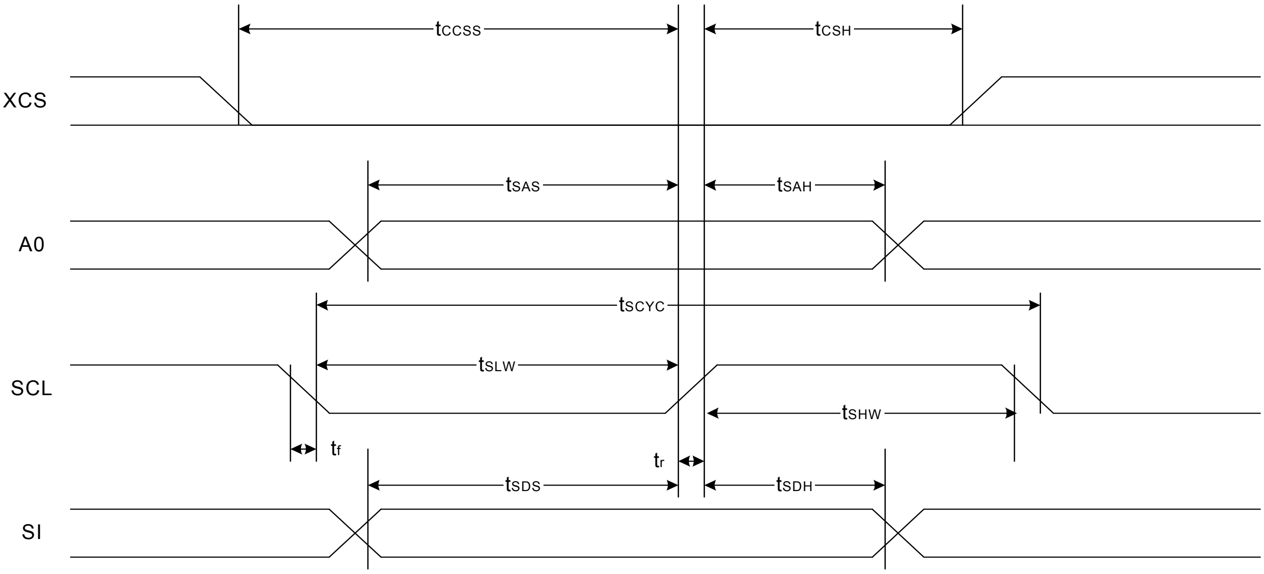


Fig 41.

(VDD = 3.3V , Ta = –30 to 85°C,Die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC	-	100	-	ns
SCL “H” pulse width		tSHW	-	50	-	
SCL “L” pulse width		tSLW	-	50	-	
Address setup time	A0	tSAS	-	40	-	
Address hold time		tSAH	-	30	-	
Data setup time	SI	tSDS	-	30	-	
Data hold time		tSDH	-	30	-	
CS-SCL time	XCS	tCSS	-	20	-	
CS-SCL time		tCSH	-	50	-	

(VDD = 2.7V , Ta = –30 to 85°C,Die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC	-	110	-	ns
SCL “H” pulse width		tSHW	-	60	-	
SCL “L” pulse width		tSLW	-	50	-	
Address setup time	A0	tSAS	-	50	-	
Address hold time		tSAH	-	40	-	
Data setup time	SI	tSDS	-	40	-	
Data hold time		tSDH	-	40	-	
CS-SCL time	XCS	tCSS	-	30	-	
CS-SCL time		tCSH	-	60	-	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

SERIAL INTERFACE (3-Line Interface)

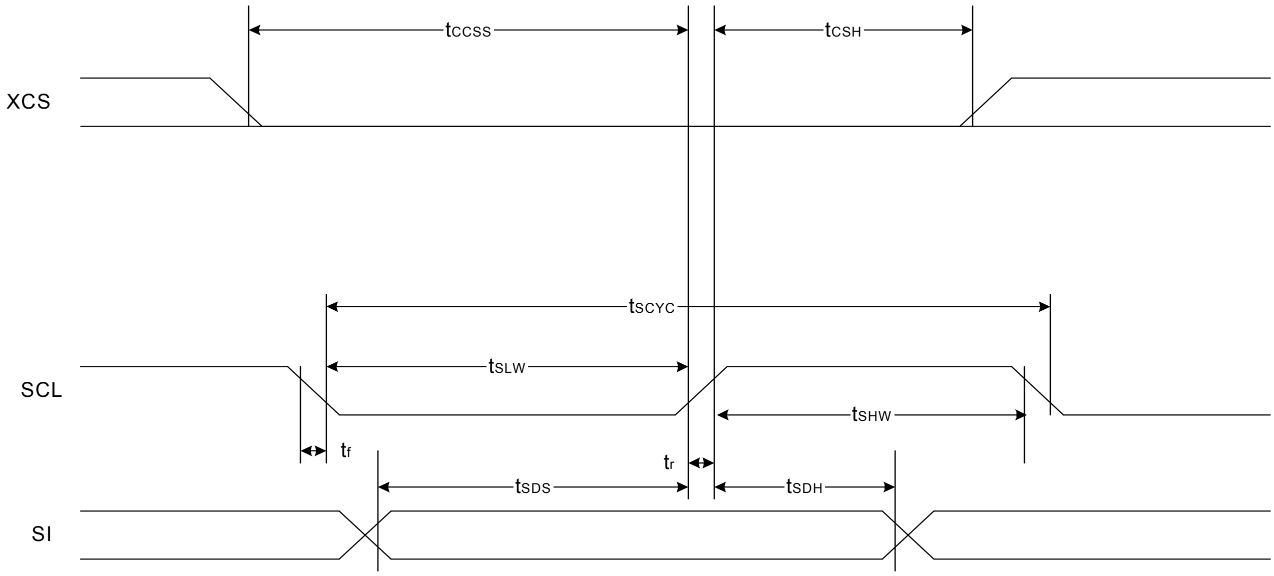


Fig 42.

(VDD = 3.3V , Ta = –30 to 85°C,Die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC	-	100	-	ns
SCL “H” pulse width		tSHW	-	50	-	
SCL “L” pulse width		tSLW	-	50	-	
Data setup time	SI	tSDS	-	30	-	
Data hold time		tSDH	-	30	-	
CS-SCL time	XCS	tCSS	-	20	-	
CS-SCL time		tCSH	-	50	-	

(VDD = 2.7V , Ta = –30 to 85°C,Die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC	-	110	-	ns
SCL “H” pulse width		tSHW	-	60	-	
SCL “L” pulse width		tSLW	-	50	-	
Data setup time	SI	tSDS	-	40	-	
Data hold time		tSDH	-	40	-	
CS-SCL time	XCS	tCSS	-	30	-	
CS-SCL time		tCSH	-	60	-	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

13. RESET TIMING

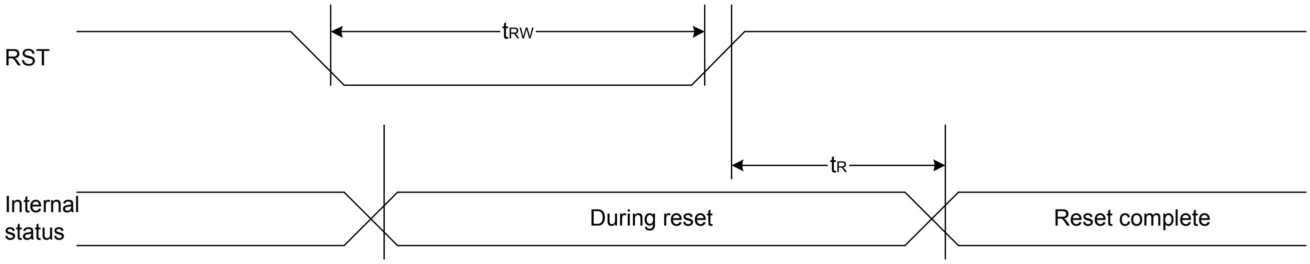


Fig 43.

(VDD = 3.3V , Ta = –30 to 85°C,Die)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR	-	-	-	1	us
Reset “L” pulse width	RST	tRW	-	1	-	-	us

(VDD = 2.7V , Ta = –30 to 85°C,Die)

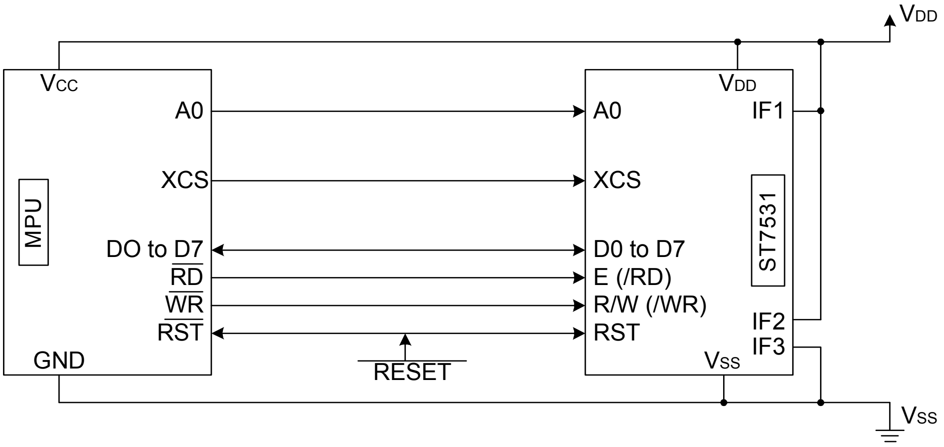
Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR	-	-	-	1.5	us
Reset “L” pulse width	RST	tRW	-	1.5	-	-	us

14. THE MPU INTERFACE (REFERENCE EXAMPLES)

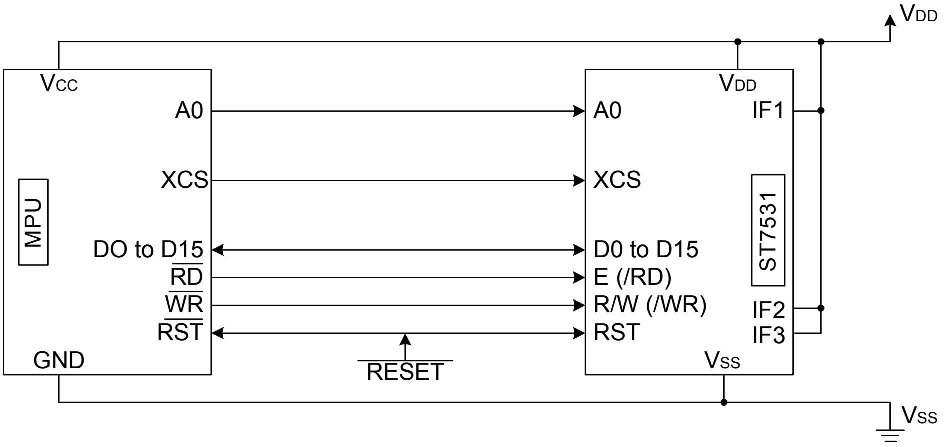
The ST7531 Series can be connected to either 8080 Series MPUs or to 6800 Series MPUs. Moreover, using the serial interface it is possible to operate the ST7531 series chips with fewer signal lines.

The display area can be enlarged by using multiple ST7531 Series chips. When this is done, the chip select signal can be used to select the individual Ics to access.

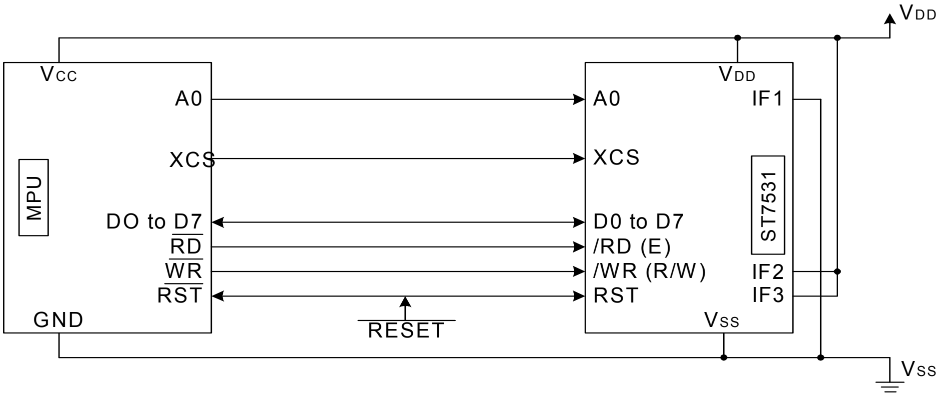
(1) 8080 Series MPUs(8 bit)



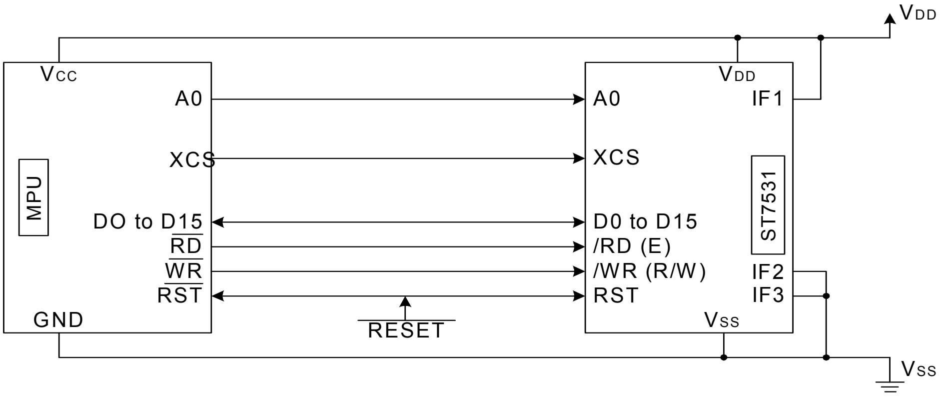
(2) 8080 Series MPUs(16 bit)



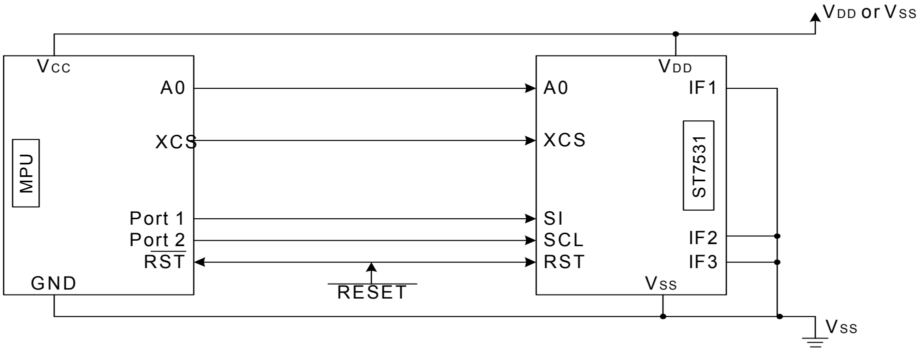
(3) 6800 Series MPUs(8 bit)



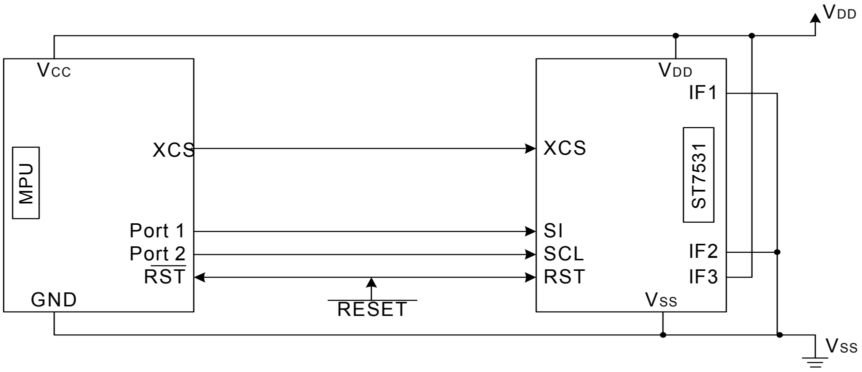
(4) 6800 Series MPUs(16 bit)



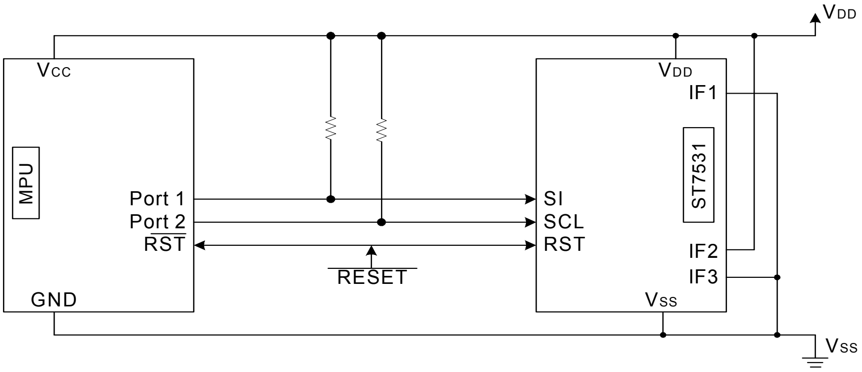
(5) Using the Serial Interface (4-line interface)



(3) Using the Serial Interface (3-line interface)

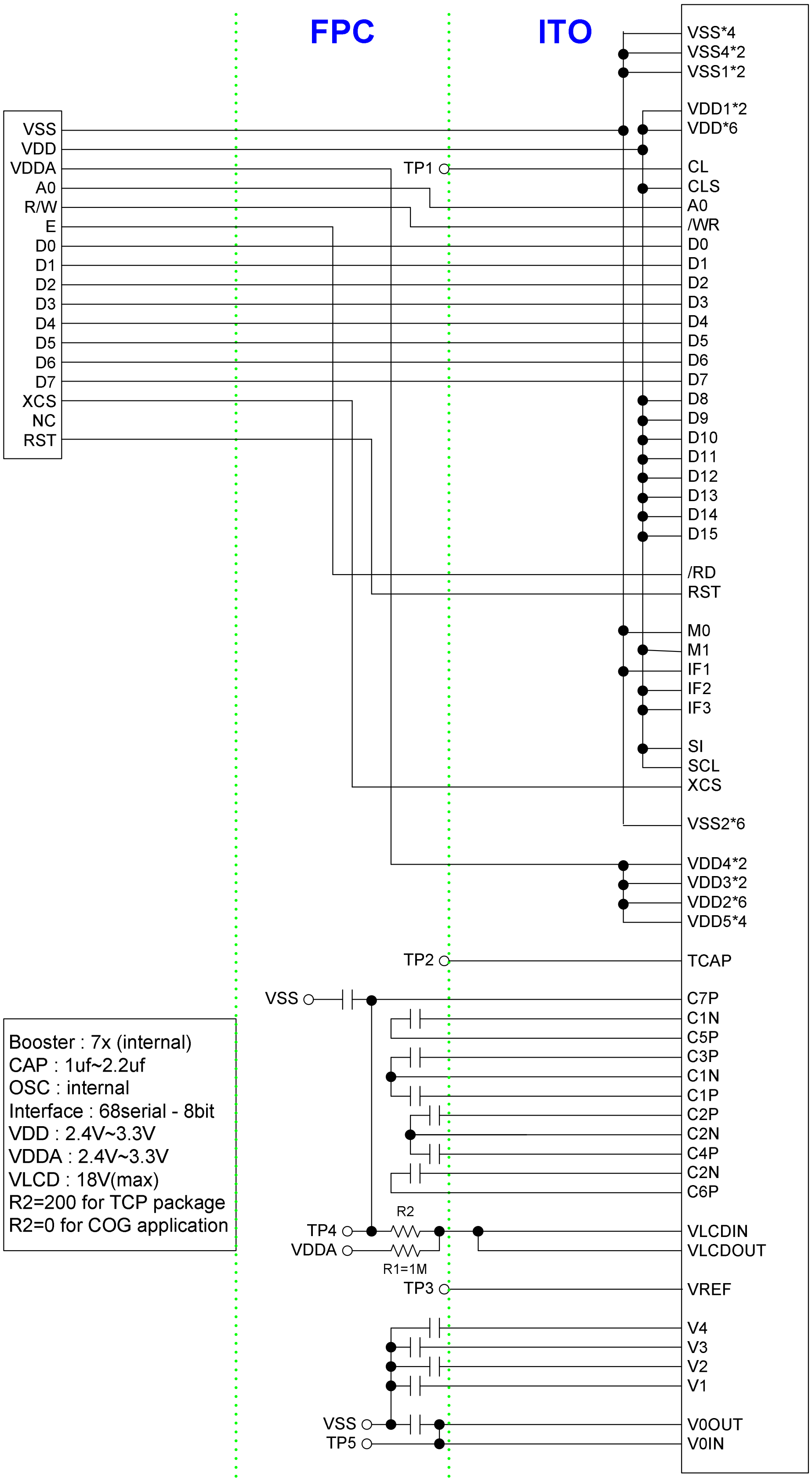


(4) Using the Serial Interface (2-line interface)



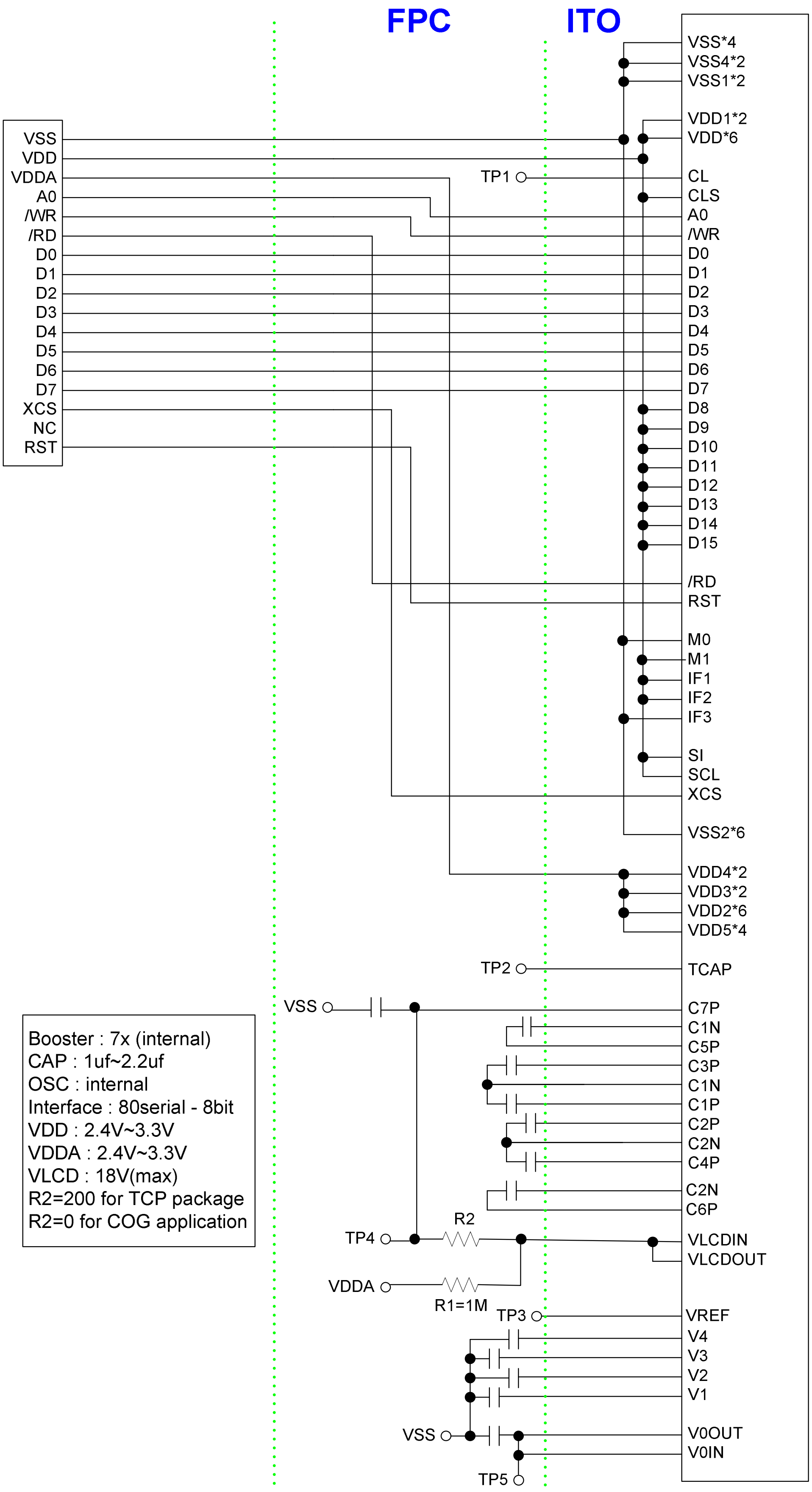
15. Application circuit

ST7531(SPRD-Mode B) / 68serial - 8bit



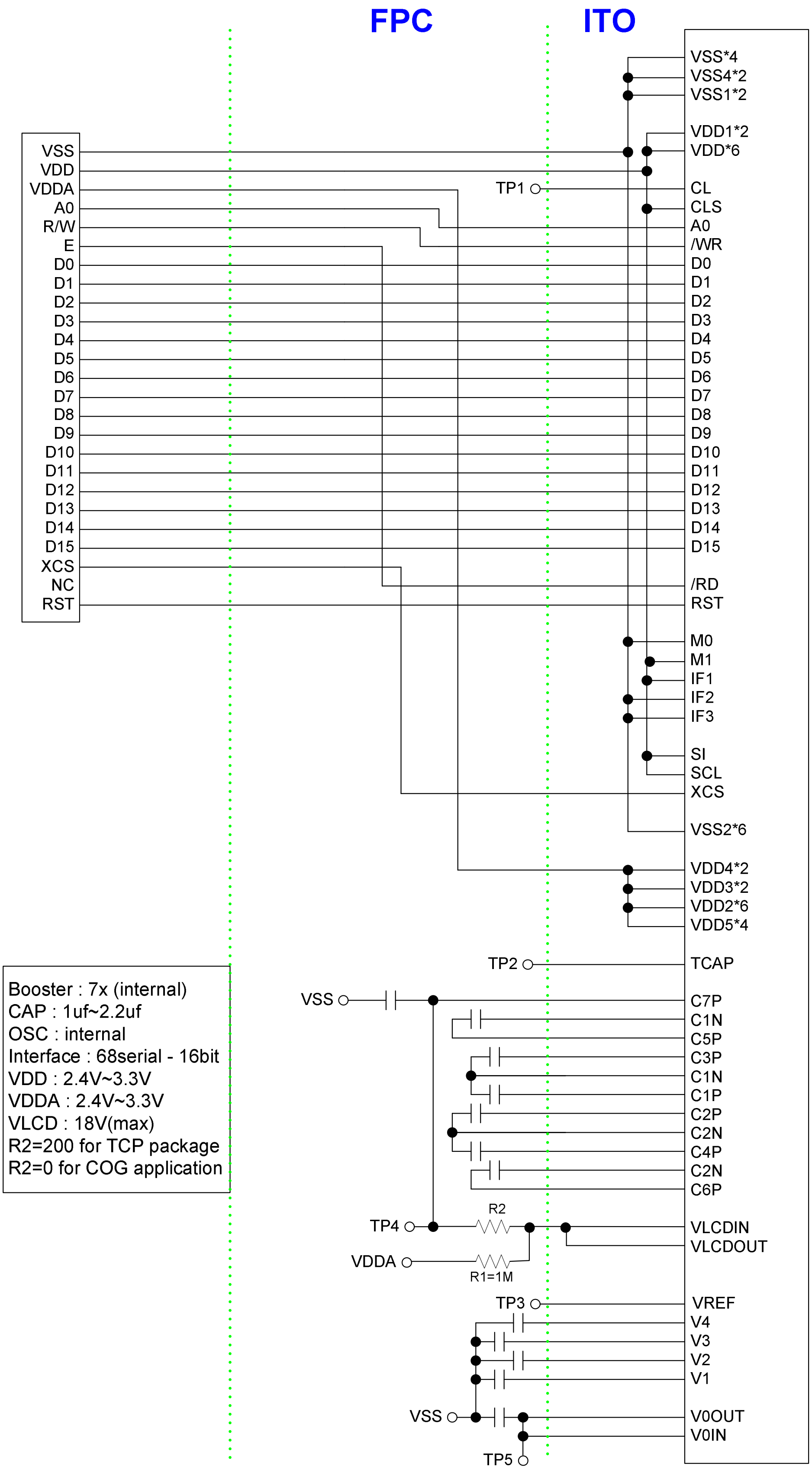
Booster : 7x (internal)
CAP : 1uf~2.2uf
OSC : internal
Interface : 68serial - 8bit
VDD : 2.4V~3.3V
VDDA : 2.4V~3.3V
VLCD : 18V(max)
R2=200 for TCP package
R2=0 for COG application

ST7531(SPRD-Mode B) / 80serial - 8bit



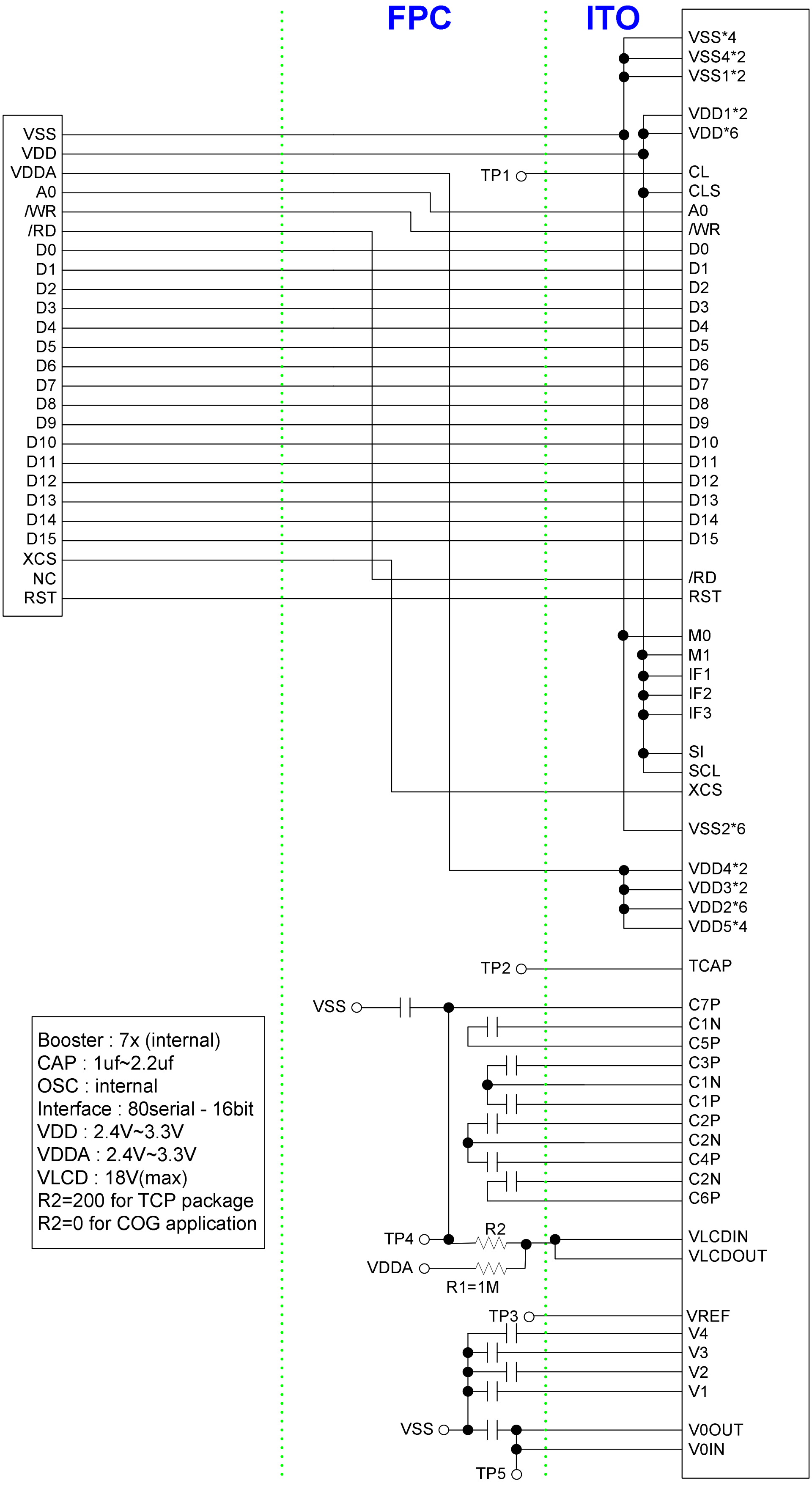
Booster : 7x (internal)
CAP : 1uf~2.2uf
OSC : internal
Interface : 80serial - 8bit
VDD : 2.4V~3.3V
VDDA : 2.4V~3.3V
VLCD : 18V(max)
R2=200 for TCP package
R2=0 for COG application

ST7531(SPRD-Mode B) / 68serial - 16bit



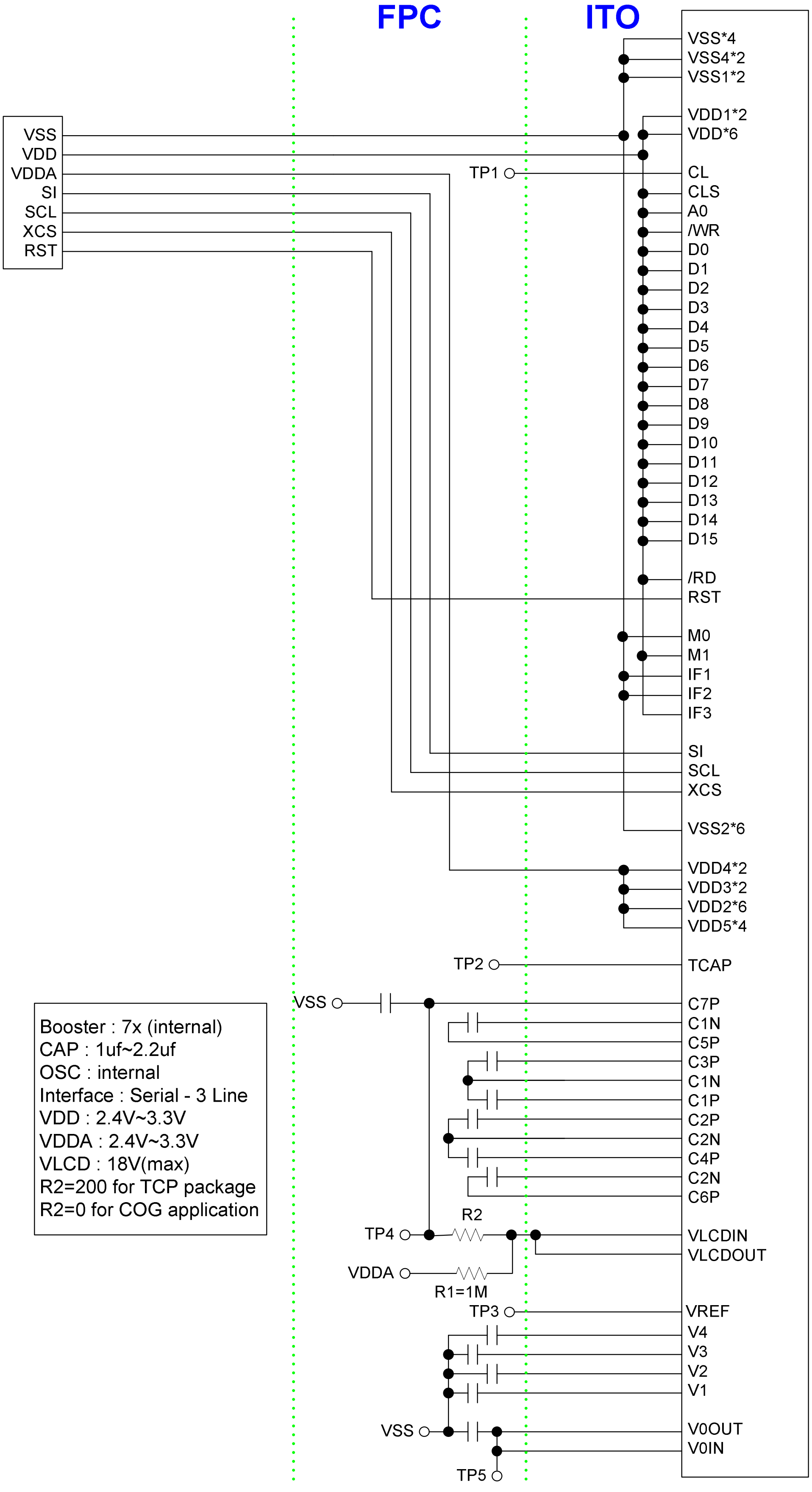
Booster : 7x (internal)
CAP : 1uf~2.2uf
OSC : internal
Interface : 68serial - 16bit
VDD : 2.4V~3.3V
VDDA : 2.4V~3.3V
VLCD : 18V(max)
R2=200 for TCP package
R2=0 for COG application

ST7531 (SPRD-Mode B) / 80serial - 16bit



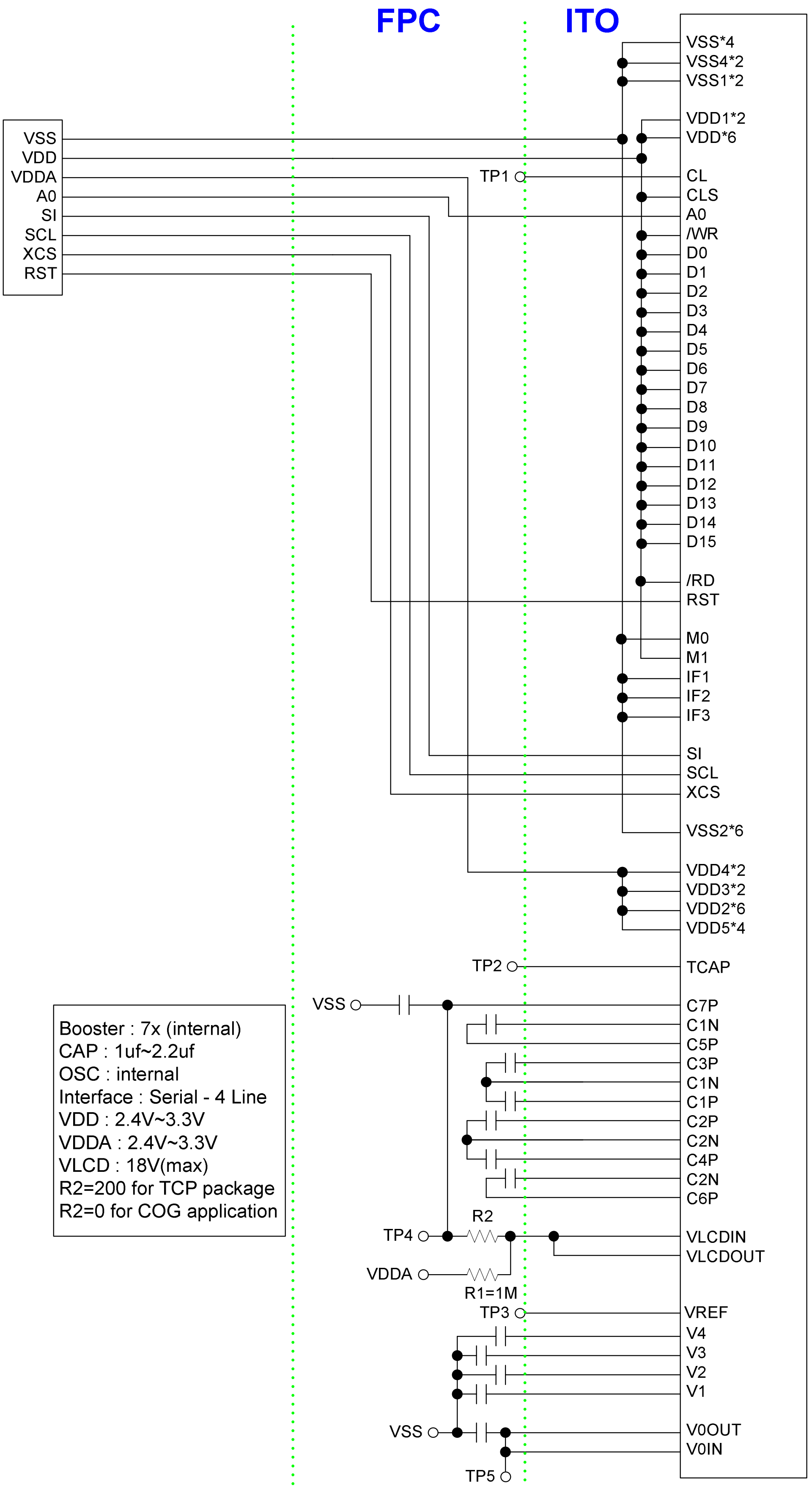
Booster : 7x (internal)
CAP : 1uf~2.2uf
OSC : internal
Interface : 80serial - 16bit
VDD : 2.4V~3.3V
VDDA : 2.4V~3.3V
VLCD : 18V(max)
R2=200 for TCP package
R2=0 for COG application

ST7531(SPRD-Mode B) / Serial - 3 Line



Booster : 7x (internal)
CAP : 1uf~2.2uf
OSC : internal
Interface : Serial - 3 Line
VDD : 2.4V~3.3V
VDDA : 2.4V~3.3V
VLCD : 18V(max)
R2=200 for TCP package
R2=0 for COG application

ST7531(SPRD-Mode B) / Serial - 4 Line



Booster : 7x (internal)
CAP : 1uf~2.2uf
OSC : internal
Interface : Serial - 4 Line
VDD : 2.4V~3.3V
VDDA : 2.4V~3.3V
VLCD : 18V(max)
R2=200 for TCP package
R2=0 for COG application

16. Power Application Note

16.1 Booster Efficiency

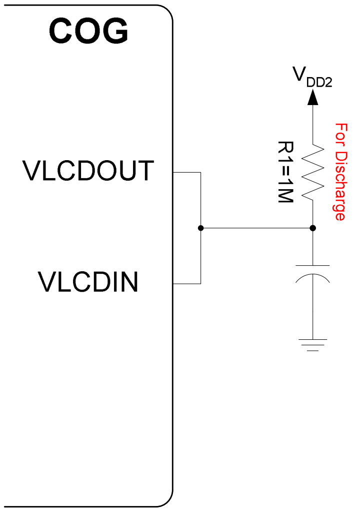
For COG Applications

Please take care about the ITO resistance, especially for the "Booster Capacitors" (CxP & CxN). The ITO trace will let the booster efficiency decrease a little bit when the loading-current flow through it. As the loading-current become larger, the efficiency will drop more. If the booster power source (VDD2) is lower, the ITO resistance control is more important. Therefore, if the loading is heavy or the VDD2 is lower, the ITO resistance should be kept much lower than the recommended value in this datasheet.

16.2 VLCD Discharge

ST7531 has built-in discharge path on VLCD. The discharge path will discharge the VLCD power when power off. The discharge speed is different under different VLCD voltage. In some application, the discharge speed is not enough. To improve this speed, a discharge resistor is needed. Recommend solution is to add the discharge resistor (about 1M Ohm) between VLCD and VDD2. Please note that the resistor value is different from LCD modules. Actual value should be checked according module display quality.

As the result, the recommended application circuit should introduce the circuit listed below on system FPC (COG applications).



ST7531 Series Specification Revision History		
Version	**Date**	**Description**
0.0	2004/4/22	Preliminary version
0.1	2004/6/08	Add SPRD-B mode color filter
0.2	2004/09/22	Pad Arrangement PAD No. in Pad Center Coordinates BLOCK DIAGRAM SETVOP in Voltage Regulator Circuits Description of Weighting Set, Data Scan Direction, Scroll Set, and Power Control in Commands Add Application note Instruction Setup Flow for Initializing with the built-in Power Supply Circuits The recommended value of regulating capacitance The note for 16-bit interface BLOCK DIAGRAM PIN DESCRIPTION FUNCTIONAL DESCRIPTION Referential Instruction Setup Flow LIMITING VALUES DC CHARACTERISTICS TIMING CHARACTERISTICS RESET TIMING
0.3	2005/01/04	Modify Bias setting value
0.4	2005/03/01	Remove 1.8V timing and modify VDD voltage to 2.4V ~ 3.6V
0.5	2005/04/13	Remove IIC interface Remove RAMRD, RMWIN and RMWOUT command Add some example code and flow chart Add EPINT command
1.0	2005/04/29	Release version Change initial code(Booster must be on first)
1.1	2005/06/03	Modify write EEPROM sequence
1.2	2005/08/09	Add Temperature Gradient Coefficient (Page 1) Add Figure 8.1.1 (Page 39), Figure 8.1.2 (Page 42)
1.3	2005/09/15	Modify bump height, chip thickness, limiting value…..
1.4	2005/12/19	Add SPRD warning message in page 2
1.5	2006/01/18	Modify application circuit voltage from 3.6V to 3.3V
1.6	2006/6/16	a. Add Power Application Note.(Page 83) b. Modify Application circuit.(Page 77) c. Modify Voltage Converter circuits.(Page 31) d. Modify Analog circuit set(Oscillator frequency adjustment). (Page 50) e. Modify Initial code flowchart.(Page 56) f. Add Power ON Sequence Note.(Page 55) g. Recommended LCD Vop Voltage.(Page 65)
1.7	2006/7/6	Modify Power Application Note.(Page 83)

1.7a	2006/7/11	Modify Power Application Note.(Page 83)
1.8	2006/9/18	a. Add microprocessor notice item. (page14、56) b. Modify Pad Arrangement.(page 3)