Sitronix

ST7546T

66 x 102 Dot Matrix LCD Controller/Driver

1. INTRODUCTION

The ST7546T is a driver & controller LSI for graphic dot-matrix liquid crystal display systems. It contains 102 segment and 65 common with 1 ICON driver circuits. This chip is connected directly to a microprocessor, accepts 8-bit parallel interface、3-line or 4-line serial peripheral interface (SPI)、I^2C interface, display data can stores in an on-chip display data RAM of 66 x 102 bits. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

Single-chip LCD controller & driver

Driver Output Circuits

102 segment / 65 common + 1 ICON

On-chip Display Data ram

- Capacity: 66X102=6,732 bits

Microprocessor Interface

- 8-bit parallel bi-directional interface with 6800-series or 8080-series
- 4-line SPI (serial peripheral interface) available (only write operation)
- 3-line SPI (serial peripheral interface) available
- I^2C (Inter-Integrated Circuit) Interface

On-chip Low Power Analog Circuit

- Generation of LCD supply voltage (externally Vout voltage supply is possible)
- Generation of intermediate LCD bias voltages
- Oscillator requires no external components (external clock also possible)
- Voltage converter (x4, x5)
- Voltage regulator(temperature gradient -0.11%/°C)
- Voltage follower
- On-chip electronic contrast control function (255 steps)

External RESB (reset) pin

Logic supply voltage range $V_{DD1,2}$ -V_{SS}

- V_{DD1} -V_{SS} : 1.7 to 3.3V
- V_{DD2} -V_{SS} : 2.4 to 3.3V

Display supply voltage range V_{LCD} -V_{SS}

- 4.5 to 13.5V

Temperature range: -40 to +85 degree

ST7546T-G2	**6800 , 8080 , 4-Line , 3-Line interface (without I^2C interface)**	ST
ST7546Ti-G2	**I^2C interface**	I^2C BUS

3. ST7546T-G2 Pad Arrangement (COG)

Chip Size: 8,200 um × 1020 um

Bump Pitch:

PAD NO 1 ~ 11 , 12 ~ 147 , 207 ~ 230 : 55 um ; PAD NO 11 ~ 12 : 56 um ;

PAD NO 148 ~ 216 : max : 175 um , min : 72 um

Bump Size:

PAD NO 188 ~ 193 : 45 (x)um × 60 (y) um ;

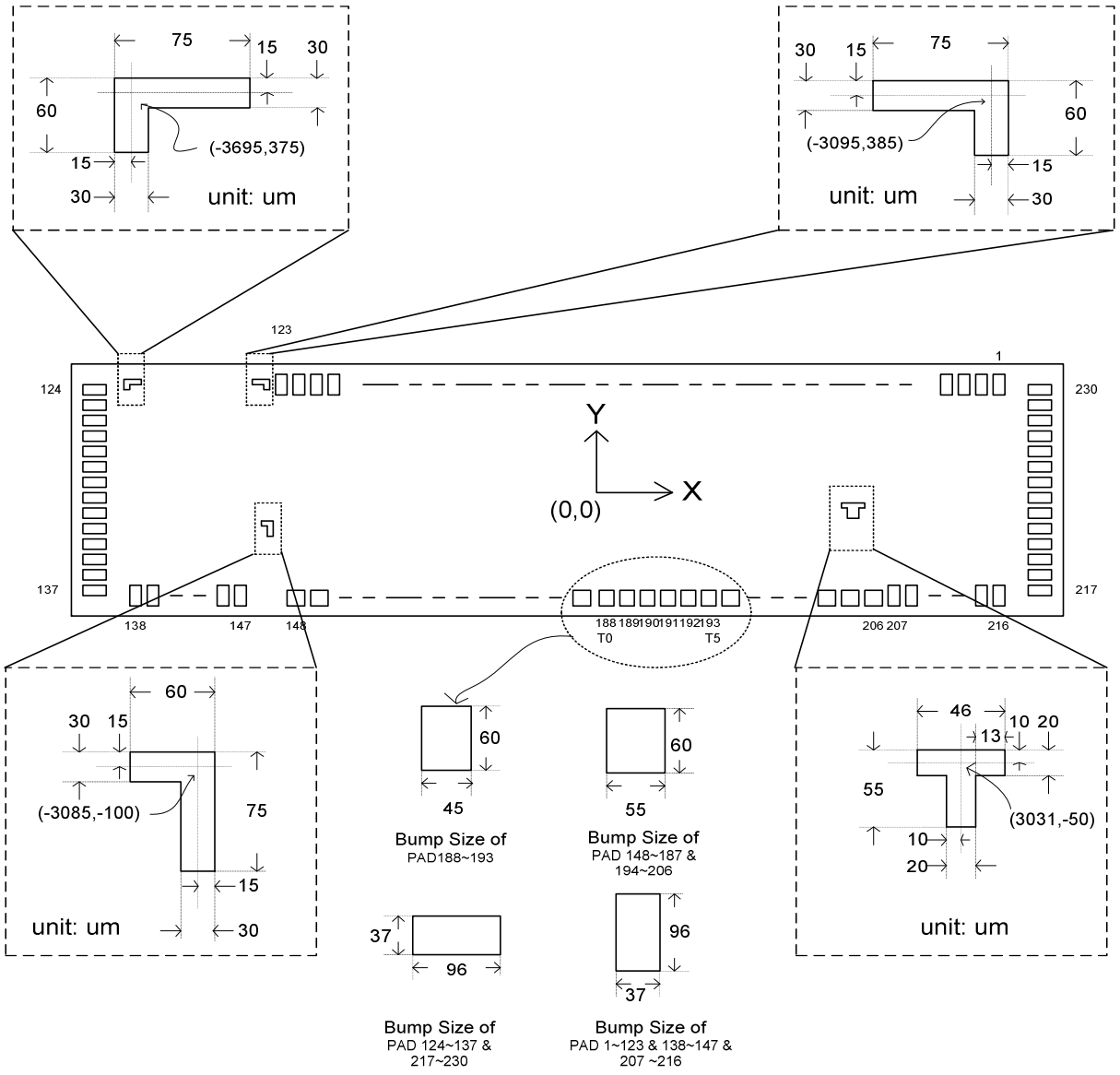
PAD NO 148 ~ 187 , 194 ~ 206 : 55 (x) um × 60 (y) um ;

PAD NO 124 ~ 137 , 217 ~ 230: 96 (x) um × 37 (y) um ;

PAD NO 1 ~ 123 , 138 ~ 147 , 207 ~ 216 : 37 (x) um × 96 (y) um ;

Bump Height: 17 um

Chip Thickness: 480 um



unit: um

Pad Center Coordinates(TMY=0)

PAD NO.	PIN Name	X	Y
1	COM[41]	3677	371
2	COM[40]	3622	371
3	COM[39]	3567	371
4	COM[38]	3512	371
5	COM[37]	3457	371
6	COM[36]	3402	371
7	COM[35]	3347	371
8	COM[34]	3292	371
9	COM[33]	3237	371
10	COM[32]	3182	371
11	Reserved	3127	371
12	SEG[0]	3071	371
13	SEG[1]	3016	371
14	SEG[2]	2961	371
15	SEG[3]	2906	371
16	SEG[4]	2851	371
17	SEG[5]	2796	371
18	SEG[6]	2741	371
19	SEG[7]	2686	371
20	SEG[8]	2631	371
21	SEG[9]	2576	371
22	SEG[10]	2521	371
23	SEG[11]	2466	371
24	SEG[12]	2411	371
25	SEG[13]	2356	371
26	SEG[14]	2301	371
27	SEG[15]	2246	371
28	SEG[16]	2191	371
29	SEG[17]	2136	371
30	SEG[18]	2081	371

PAD NO.	PIN Name	X	Y
31	SEG[19]	2026	371
32	SEG[20]	1971	371
33	SEG[21]	1916	371
34	SEG[22]	1861	371
35	SEG[23]	1806	371
36	SEG[24]	1751	371
37	SEG[25]	1696	371
38	SEG[26]	1641	371
39	SEG[27]	1586	371
40	SEG[28]	1531	371
41	SEG[29]	1476	371
42	SEG[30]	1421	371
43	SEG[31]	1366	371
44	SEG[32]	1311	371
45	SEG[33]	1256	371
46	SEG[34]	1201	371
47	SEG[35]	1146	371
48	SEG[36]	1091	371
49	SEG[37]	1036	371
50	SEG[38]	981	371
51	SEG[39]	926	371
52	SEG[40]	871	371
53	SEG[41]	816	371
54	SEG[42]	761	371
55	SEG[43]	706	371
56	SEG[44]	651	371
57	SEG[45]	596	371
58	SEG[46]	541	371
59	SEG[47]	486	371
60	SEG[48]	431	371

PAD NO.	PIN Name	X	Y
61	SEG[49]	376	371
62	SEG[50]	321	371
63	SEG[51]	266	371
64	SEG[52]	211	371
65	SEG[53]	156	371
66	SEG[54]	101	371
67	SEG[55]	46	371
68	SEG[56]	-9	371
69	SEG[57]	-64	371
70	SEG[58]	-119	371
71	SEG[59]	-174	371
72	SEG[60]	-229	371
73	SEG[61]	-284	371
74	SEG[62]	-339	371
75	SEG[63]	-394	371
76	SEG[64]	-449	371
77	SEG[65]	-504	371
78	SEG[66]	-559	371
79	SEG[67]	-614	371
80	SEG[68]	-669	371
81	SEG[69]	-724	371
82	SEG[70]	-779	371
83	SEG[71]	-834	371
84	SEG[72]	-889	371
85	SEG[73]	-944	371
86	SEG[74]	-999	371
87	SEG[75]	-1054	371
88	SEG[76]	-1109	371
89	SEG[77]	-1164	371
90	SEG[78]	-1219	371

PAD NO.	PIN Name	X	Y
91	SEG[79]	-1274	371
92	SEG[80]	-1329	371
93	SEG[81]	-1384	371
94	SEG[82]	-1439	371
95	SEG[83]	-1494	371
96	SEG[84]	-1549	371
97	SEG[85]	-1604	371
98	SEG[86]	-1659	371
99	SEG[87]	-1714	371
100	SEG[88]	-1769	371
101	SEG[89]	-1824	371
102	SEG[90]	-1879	371
103	SEG[91]	-1934	371
104	SEG[92]	-1989	371
105	SEG[93]	-2044	371
106	SEG[94]	-2099	371
107	SEG[95]	-2154	371
108	SEG[96]	-2209	371
109	SEG[97]	-2264	371
110	SEG[98]	-2319	371
111	SEG[99]	-2374	371
112	SEG[100]	-2429	371
113	SEG[101]	-2484	371
114	COMS	-2540	371
115	COM[0]	-2595	371
116	COM[1]	-2650	371
117	COM[2]	-2705	371
118	COM[3]	-2760	371
119	COM[4]	-2815	371
120	COM[5]	-2870	371

PAD NO.	PIN Name	X	Y
121	COM[6]	-2925	371
122	COM[7]	-2980	371
123	COM[8]	-3035	371
124	COM[9]	-3981	352
125	COM[10]	-3981	297
126	COM[11]	-3981	242
127	COM[12]	-3981	187
128	COM[13]	-3981	132
129	COM[14]	-3981	77
130	COM[15]	-3981	22
131	COM[16]	-3981	-33
132	COM[17]	-3981	-88
133	COM[18]	-3981	-143
134	COM[19]	-3981	-198
135	COM[20]	-3981	-253
136	COM[21]	-3981	-308
137	COM[22]	-3981	-363
138	COM[23]	-3678	-371
139	COM[24]	-3623	-371
140	COM[25]	-3568	-371
141	COM[26]	-3513	-371
142	COM[27]	-3458	-371
143	COM[28]	-3403	-371
144	COM[29]	-3348	-371
145	COM[30]	-3293	-371
146	COM[31]	-3238	-371
147	Reserved	-3183	-371
148	TMX	-2194	-389
149	TMY	-2075	-389
150	VDD1	-2002	-389

PAD NO.	PIN Name	X	Y
151	VDD1	-1929	-389
152	VDD1	-1856	-389
153	VDD1	-1783	-389
154	PS0	-1710	-389
155	PS1	-1591	-389
156	PS2	-1518	-389
157	BR	-1399	-389
158	VSS	-1326	-389
159	T6	-1253	-389
160	T7	-1134	-389
161	CP	-1061	-389
162	T8	-942	-389
163	T9	-869	-389
164	VDD2	-766	-389
165	VDD2	-693	-389
166	VDD2	-620	-389
167	VDD2	-547	-389
168	RESB	-410	-389
169	CSB	-291	-389
170	/WR	-218	-389
171	/RD	-99	-389
172	A0	-26	-389
173	VDD1	77	-389
174	D7	150	-389
175	D6	269	-389
176	D5	342	-389
177	D4	461	-389
178	D3	534	-389
179	D2	653	-389
180	D1	726	-389

PAD NO.	PIN Name	X	Y
181	D0	845	-389
182	OSC	918	-389
183	VSS	1021	-389
184	VSS	1094	-389
185	VSS	1167	-389
186	VSS	1240	-389
187	VRS	1313	-389
188	T0	1385	-389
189	T1	1534	-389
190	T2	1609	-389
191	T3	1784	-389
192	T4	1859	-389
193	T5	2034	-389
194	VSS	2108	-389
195	VSS	2181	-389
196	VSS	2254	-389
197	VSS	2327	-389
198	VLCDOUT	2415	-389
199	VLCDOUT	2488	-389
200	VLCDIN	2561	-389
201	VLCDIN	2634	-389
202	V0	2793	-389
203	V1	2883	-389
204	V2	2956	-389
205	V3	3029	-389
206	V4	3102	-389
207	COMS	3183	-371
208	COM[64]	3238	-371
209	COM[63]	3293	-371
210	COM[62]	3348	-371

PAD NO.	PIN Name	X	Y
211	COM[61]	3403	-371
212	COM[60]	3458	-371
213	COM[59]	3513	-371
214	COM[58]	3568	-371
215	COM[57]	3623	-371
216	COM[56]	3678	-371
217	COM[55]	3981	-363
218	COM[54]	3981	-308
219	COM[53]	3981	-253
220	COM[52]	3981	-198
221	COM[51]	3981	-143
222	COM[50]	3981	-88
223	COM[49]	3981	-33
224	COM[48]	3981	22
225	COM[47]	3981	77
226	COM[46]	3981	132
227	COM[45]	3981	187
228	COM[44]	3981	242
229	COM[43]	3981	297
230	COM[42]	3981	352

Pad Center Coordinates(TMY=1)

PAD NO.	PIN Name	X	Y
1	COM[23]	3677	371
2	COM[24]	3622	371
3	COM[25]	3567	371
4	COM[26]	3512	371
5	COM[27]	3457	371
6	COM[28]	3402	371
7	COM[29]	3347	371
8	COM[30]	3292	371
9	COM[31]	3237	371
10	Reserved	3182	371
11	Reserved	3127	371
12	SEG[0]	3071	371
13	SEG[1]	3016	371
14	SEG[2]	2961	371
15	SEG[3]	2906	371
16	SEG[4]	2851	371
17	SEG[5]	2796	371
18	SEG[6]	2741	371
19	SEG[7]	2686	371
20	SEG[8]	2631	371
21	SEG[9]	2576	371
22	SEG[10]	2521	371
23	SEG[11]	2466	371
24	SEG[12]	2411	371
25	SEG[13]	2356	371
26	SEG[14]	2301	371
27	SEG[15]	2246	371
28	SEG[16]	2191	371
29	SEG[17]	2136	371
30	SEG[18]	2081	371

PAD NO.	PIN Name	X	Y
31	SEG[19]	2026	371
32	SEG[20]	1971	371
33	SEG[21]	1916	371
34	SEG[22]	1861	371
35	SEG[23]	1806	371
36	SEG[24]	1751	371
37	SEG[25]	1696	371
38	SEG[26]	1641	371
39	SEG[27]	1586	371
40	SEG[28]	1531	371
41	SEG[29]	1476	371
42	SEG[30]	1421	371
43	SEG[31]	1366	371
44	SEG[32]	1311	371
45	SEG[33]	1256	371
46	SEG[34]	1201	371
47	SEG[35]	1146	371
48	SEG[36]	1091	371
49	SEG[37]	1036	371
50	SEG[38]	981	371
51	SEG[39]	926	371
52	SEG[40]	871	371
53	SEG[41]	816	371
54	SEG[42]	761	371
55	SEG[43]	706	371
56	SEG[44]	651	371
57	SEG[45]	596	371
58	SEG[46]	541	371
59	SEG[47]	486	371
60	SEG[48]	431	371

PAD NO.	PIN Name	X	Y
61	SEG[49]	376	371
62	SEG[50]	321	371
63	SEG[51]	266	371
64	SEG[52]	211	371
65	SEG[53]	156	371
66	SEG[54]	101	371
67	SEG[55]	46	371
68	SEG[56]	-9	371
69	SEG[57]	-64	371
70	SEG[58]	-119	371
71	SEG[59]	-174	371
72	SEG[60]	-229	371
73	SEG[61]	-284	371
74	SEG[62]	-339	371
75	SEG[63]	-394	371
76	SEG[64]	-449	371
77	SEG[65]	-504	371
78	SEG[66]	-559	371
79	SEG[67]	-614	371
80	SEG[68]	-669	371
81	SEG[69]	-724	371
82	SEG[70]	-779	371
83	SEG[71]	-834	371
84	SEG[72]	-889	371
85	SEG[73]	-944	371
86	SEG[74]	-999	371
87	SEG[75]	-1054	371
88	SEG[76]	-1109	371
89	SEG[77]	-1164	371
90	SEG[78]	-1219	371

PAD NO.	PIN Name	X	Y
91	SEG[79]	-1274	371
92	SEG[80]	-1329	371
93	SEG[81]	-1384	371
94	SEG[82]	-1439	371
95	SEG[83]	-1494	371
96	SEG[84]	-1549	371
97	SEG[85]	-1604	371
98	SEG[86]	-1659	371
99	SEG[87]	-1714	371
100	SEG[88]	-1769	371
101	SEG[89]	-1824	371
102	SEG[90]	-1879	371
103	SEG[91]	-1934	371
104	SEG[92]	-1989	371
105	SEG[93]	-2044	371
106	SEG[94]	-2099	371
107	SEG[95]	-2154	371
108	SEG[96]	-2209	371
109	SEG[97]	-2264	371
110	SEG[98]	-2319	371
111	SEG[99]	-2374	371
112	SEG[100]	-2429	371
113	SEG[101]	-2484	371
114	COMS	-2540	371
115	COM[64]	-2595	371
116	COM[63]	-2650	371
117	COM[62]	-2705	371
118	COM[61]	-2760	371
119	COM[60]	-2815	371
120	COM[59]	-2870	371

PAD NO.	PIN Name	X	Y
121	COM[58]	-2925	371
122	COM[57]	-2980	371
123	COM[56]	-3035	371
124	COM[55]	-3981	352
125	COM[54]	-3981	297
126	COM[53]	-3981	242
127	COM[52]	-3981	187
128	COM[51]	-3981	132
129	COM[50]	-3981	77
130	COM[49]	-3981	22
131	COM[48]	-3981	-33
132	COM[47]	-3981	-88
133	COM[46]	-3981	-143
134	COM[45]	-3981	-198
135	COM[44]	-3981	-253
136	COM[43]	-3981	-308
137	COM[42]	-3981	-363
138	COM[41]	-3678	-371
139	COM[40]	-3623	-371
140	COM[39]	-3568	-371
141	COM[38]	-3513	-371
142	COM[37]	-3458	-371
143	COM[36]	-3403	-371
144	COM[35]	-3348	-371
145	COM[34]	-3293	-371
146	COM[33]	-3238	-371
147	COM[32]	-3183	-371
148	TMX	-2194	-389
149	TMY	-2075	-389
150	VDD1	-2002	-389

PAD NO.	PIN Name	X	Y
151	VDD1	-1929	-389
152	VDD1	-1856	-389
153	VDD1	-1783	-389
154	PS0	-1710	-389
155	PS1	-1591	-389
156	PS2	-1518	-389
157	BR	-1399	-389
158	VSS	-1326	-389
159	T6	-1253	-389
160	T7	-1134	-389
161	CP	-1061	-389
162	T8	-942	-389
163	T9	-869	-389
164	VDD2	-766	-389
165	VDD2	-693	-389
166	VDD2	-620	-389
167	VDD2	-547	-389
168	RESB	-410	-389
169	CSB	-291	-389
170	/WR	-218	-389
171	/RD	-99	-389
172	A0	-26	-389
173	VDD1	77	-389
174	D7	150	-389
175	D6	269	-389
176	D5	342	-389
177	D4	461	-389
178	D3	534	-389
179	D2	653	-389
180	D1	726	-389

PAD NO.	PIN Name	X	Y
181	D0	845	-389
182	OSC	918	-389
183	VSS	1021	-389
184	VSS	1094	-389
185	VSS	1167	-389
186	VSS	1240	-389
187	VRS	1313	-389
188	T0	1385	-389
189	T1	1534	-389
190	T2	1609	-389
191	T3	1784	-389
192	T4	1859	-389
193	T5	2034	-389
194	VSS	2108	-389
195	VSS	2181	-389
196	VSS	2254	-389
197	VSS	2327	-389
198	VLCDOUT	2415	-389
199	VLCDOUT	2488	-389
200	VLCDIN	2561	-389
201	VLCDIN	2634	-389
202	V0	2793	-389
203	V1	2883	-389
204	V2	2956	-389
205	V3	3029	-389
206	V4	3102	-389
207	COMS	3183	-371
208	COM[0]	3238	-371
209	COM[1]	3293	-371
210	COM[2]	3348	-371

PAD NO.	PIN Name	X	Y
211	COM[3]	3403	-371
212	COM[4]	3458	-371
213	COM[5]	3513	-371
214	COM[6]	3568	-371
215	COM[7]	3623	-371
216	COM[8]	3678	-371
217	COM[9]	3981	-363
218	COM[10]	3981	-308
219	COM[11]	3981	-253
220	COM[12]	3981	-198
221	COM[13]	3981	-143
222	COM[14]	3981	-88
223	COM[15]	3981	-33
224	COM[16]	3981	22
225	COM[17]	3981	77
226	COM[18]	3981	132
227	COM[19]	3981	187
228	COM[20]	3981	242
229	COM[21]	3981	297
230	COM[22]	3981	352

4. BLOCK DIAGRAM

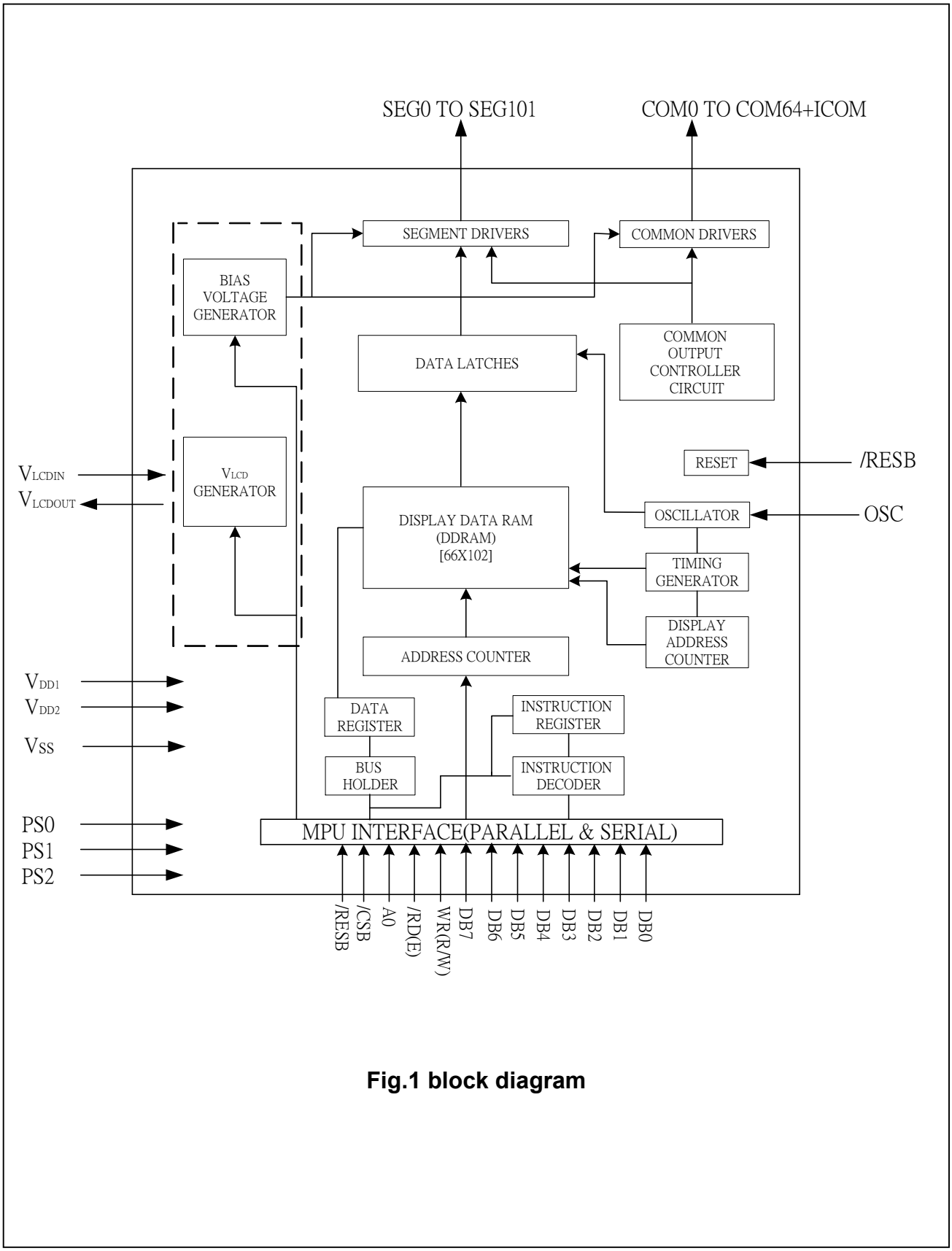


Fig.1 block diagram

5. PINNING DESCRIPTIONS

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td colspan="4">Lcd driver outputs</td></tr>
<tr><td>SEG0 to SEG101</td><td>O</td><td>LCD segment driver outputs
This display data and the M signal control the output voltage of segment driver.
<table>
<tr><td rowspan="2">Display data</td><td rowspan="2">M (Internal)</td><td colspan="2">Segment driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td>V_0</td><td>V_2</td></tr>
<tr><td>H</td><td>L</td><td>V_{SS}</td><td>V_3</td></tr>
<tr><td>L</td><td>H</td><td>V_2</td><td>V_0</td></tr>
<tr><td>L</td><td>L</td><td>V_3</td><td>V_{SS}</td></tr>
<tr><td colspan="2">Power down mode</td><td>V_{SS}</td><td>V_{SS}</td></tr>
</table></td><td>102</td></tr>
<tr><td>COM0 to COM64</td><td>O</td><td>LCD common driver outputs
This internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><td rowspan="2">Display data</td><td rowspan="2">M(Internal)</td><td colspan="2">Common driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td colspan="2">V_{SS}</td></tr>
<tr><td>H</td><td>L</td><td colspan="2">V_0</td></tr>
<tr><td>L</td><td>H</td><td colspan="2">V_1</td></tr>
<tr><td>L</td><td>L</td><td colspan="2">V_4</td></tr>
<tr><td colspan="2">Power down mode</td><td colspan="2">V_{SS}</td></tr>
</table></td><td>65</td></tr>
<tr><td>COMS</td><td>O</td><td>Common output for the icons.
The output signals of two pins are same. When not used, this pin should be left open.</td><td>2</td></tr>
<tr><td colspan="4">MICROPROCESSOR INTERFACE</td></tr>
<tr><td>PS[2:0]</td><td>I</td><td>Microprocessor interface select input pin
<table>
<tr><th>PS0</th><th>PS1</th><th>PS2</th><th>State</th></tr>
<tr><td>" L "</td><td>" L "</td><td>" L "</td><td>4 Pin-SPI MPU interface</td></tr>
<tr><td>" L "</td><td>" L "</td><td>" H "</td><td>3 Pin-SPI MPU interface</td></tr>
<tr><td>" L "</td><td>" H "</td><td>" L "</td><td>8080-series parallel MPU interface</td></tr>
<tr><td>" L "</td><td>" H "</td><td>" H "</td><td>6800-series parallel MPU interface</td></tr>
<tr><td>" H "</td><td>"H"</td><td>" H "</td><td>I^2C interface</td></tr>
</table></td><td>3</td></tr>
<tr><td>CSB</td><td>I</td><td>Chip select input pins
Data/instruction I/O is enabled only when CSB is " L ". When chip select is non-active, DB0 to DB7 is high impedance.
This pin is only used in 8-bit parallel interface.
When using serial interface , this pin must be fixed to “H”</td><td>1</td></tr>
<tr><td>RESB</td><td>I</td><td>Reset input pin
When RESB is " L ", initialization is executed.</td><td>1</td></tr>
<tr><td>A0</td><td>I</td><td>It determines whether the data bits are data or a command.
A0=" H “: Indicates that D0 to D7 are display data.
A0=" L “: Indicates that D0 to D7 are control data.
This pin is only used in 8-bit parallel interface.
When using serial interface , this pin must be fixed to “H”</td><td>1</td></tr>
</table>

<table>
<tr><td>/WR(R/W)</td><td>I</td><td>Read/Write execution control pin (PS[0:1]=[L:H])
<table><tr><th>PS2</th><th>MPU type</th><th>/WR(R/W)</th><th>Description</th></tr><tr><td>H</td><td>6800-series</td><td>R/W</td><td>Read/Write control input pin
R/W=" H ": read
R/W=" L": write</td></tr><tr><td>L</td><td>8080-series</td><td>/WR</td><td>Write enable clock input pin
The data on D0 to D7 are latched at the rising edge of the /WR signal</td></tr></table>When in the serial interface must fix to " H"</td><td>1</td></tr>
<tr><td>/RD (E)</td><td>I</td><td>Read/Write execution control pin (PS[0:1]=[L:H])
<table><tr><th>PS2</th><th>MPU Type</th><th>/RD (E)</th><th>Description</th></tr><tr><td>H</td><td>6800-series</td><td>E</td><td>Read/Write control input pin
R/W=" H ": When E is " H ", D0 to D7 are in an output status.
R/W=" L ": The data on D0 to D7 are latched at the falling edge of the E signal.</td></tr><tr><td>L</td><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is " L ", D0 to D7 are in an output status.</td></tr></table>When in the serial interface must fix to " H"</td><td>1</td></tr>
<tr><td>D7(SCLK)
D6(SDA)
D5(A0)
D4(CSB)
D3 to D0</td><td rowspan="2">I/O</td><td>When using 8-bit parallel interface : 6800 . 8080
8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus.
When chip select is not active, D0 to D7 is high impedance.
When using serial interface: 4-LINE.3-LINE
D7: serial input clock (SCLK) ; D6: serial input data (SDA)
D5: command/data selection (A0) ; D4: chip select pin(CSB)
D3,D2.D1.D0: must fix to " H"
When using 3-line A0 must fix to “H”</td><td rowspan="2">8</td></tr>
<tr><td>D7(SCLK)
D6 (SDA_IN)
D5(X)
D4(X)
D3 to D2 (SDA_OUT)
D1 (SA1)
D0 (SA0)</td><td>When using I^{2}C interface
D7: serial clock input (SCLK)
D6: serial input data (SDA_IN)
D3, D2: (SDA_OUT) serial data acknowledge for the I^{2}C interface. By connecting SDA_OUT to SDA_IN externally, the SDA line becomes fully I^{2}C interface compatible. Having the acknowledge output separated from the serial data line is advantageous in chip on glass (COG) applications. In COG application where the track resistance from the SDA_OUT pad to the system SDA line can be significant, a potential divider is generated by the bus pull-up resistor and the ITO track resistance. It is possible the during the acknowledge cycle the ST7546T will not be able to create a valid logic 0 level. By splitting the SDA_IN input from the SDA_OUT output the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDA_OUT pad to the system SDA line to guarantee a valid low level.
<u>D6, D3,D2 must be connected together (SDA)</u>
D4, D5: must fix to " H"
D1, D0: Is slave address (SA0,SA1), must fix to “H” or “L”
Chip select input pins “CSB” not used must fix to “H”</td></tr>
</table>

LCD DRIVER SUPPLY			
OSC	**I**	**When the on-chip oscillator is used, this input must be connected to VDD**. An external clock signal, if used, is connected to this input. If the oscillator and external clock are both inhibited by connecting the OSC pin to VSS the display is not clocked and may be left in a DC state. To avoid this, the chip should always be put into Power Down Mode before stopping the clock.	**1**
Power Supply Pins			
V_{SS}	**Power Supply**	Ground.	**9**
V_{DD1}	**Power Supply**	Digital Supply voltage. The 2 supply rails V_{DD1} and V_{DD2} could be connected together. If Digital Option pin is high, must be this level	**5**
V_{DD2}	**Power Supply**	Analog Supply voltage. The 2 supply rails V_{DD1} and V_{DD2} could be connected together.	**4**
V_{LCDIN}	**Power Supply**	If the internal voltage generator is used, the V_{LCDIN} & V_{LCDOUT} must be connected together. An external supply voltage can be supplied using the V_{LCDIN} pad. This pad is for external multiple voltage input. In this case, VLCDOUT has to be left open,	**2**
V_{LCDOUT}	**Power Supply**	If the internal voltage generator is used, the V_{LCDIN} & V_{LCDOUT} must be connected together and series one capacitor to VSS If an external supply is used this pin must be left open.	**2**
V0, V1, V2, V3, V4	**Power Supply**	This is a multi-level power supply for the liquid crystal. $V_{LCDIN} \geq V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq VSS$	**5**
VRS	**Power Supply**	Monitor Voltage Regulator level, must be left open.	**1**
Configuration Pins			
TMX	**I**	Mirror X: SEG bi-direction selection TMX connect to VSS : normal direction (SEG0→SEG101) TMX connect to VDD : reverse direction (SEG101→SEG0)	**1**
TMY	**I**	Mirror Y: COM bi-direction selection TMY connect to VSS (TMY=0): normal direction TMY connect to VDD (TMY=1): reverse direction See Pad Center Coordinates at page 3~10.	**1**
CP	**I**	Set Booster stages. (VSS=4X;VDD=5X)	**1**
BR	**I**	Set LCD bias ratio. (VSS=1/7;VDD=1/9) After reset , the bias ratio will be the setting value.	**1**
Test Pin			
T0~T9	**T**	T0~T5 must floating T7.T8 must connect to VDD T6.T9 must connect to VSS	**10**
Reserved	**-**	All Reserved pins must floating	**2**

ST7546T I/O PIN ITO Resister Limitation

PIN Name	ITO Resister
PS[2:0],OSC,CP,BR,T6~T9,TMX,TMY	No Limitation
T0~T5,VRS, V1 , V2 , V3 , V4	Floating
Vdd1, Vdd2, Vss, Vlcdin , Vlcdout	<100Ω
V0	<500Ω
A0,/WR,/RD,CSB, D0 …D7	<1KΩ
RESB	<10KΩ

6. FUNCTIONS DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

There is CSB pin for chip selection. The ST7546T can interface with an MPU when CSB is "L". When CSB is “H”, these pins are set to any other combination, A0, /RD(E), and /WR(R/W) inputs are disabled and D0 to D7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel / Serial Interface

ST7546T has five types of interface with an MPU, which are three serial and two parallel interfaces. This parallel or serial interface is determined by PS [0:2] pin as shown in table 1.

Table 1. Parallel/Serial Interface Mode

PS0	PS1	PS2	State
" L "	" L "	" L "	4 Pin-SPI MPU interface
" L "	" L "	" H "	3 Pin-SPI MPU interface
" L "	" H "	" L "	8080-series parallel MPU interface
" L "	" H "	" H "	6800-series parallel MPU interface
" H "	" H "	" H "	I^2C interface

Parallel Interface (PS[0:1] = "L;H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by PS2 as shown in table 2. The type of data transfer is determined by signals at A0, /RD (E) and /WR(R/W) as shown in table 3.

Table 2. Microprocessor Selection for Parallel Interface

PS0	PS1	PS2	CSB	A0	/RD (E)	/WR (R/W)	DB0 to DB7	MPU bus
L	H	H	CSB	A0	E	R/W	DB0 to DB7	6800-series
L	H	L	CSB	A0	/RD	/WR	DB0 to DB7	8080-series

Table 3. Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	E (/RD)	R/W (/WR)	/RD (E)	/WR (R/W)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

NOTE: When /RD (E) pin is always pulled high for 6800-series interface, it can be used CSB for enable signal. In this case, interface data is latched at the rising edge of CSB and the type of data transfer is determined by signals at A0, /WR(R/W) as in case of 6800-series mode.

Serial Interface

Serial Mode	PS0	PS1	PS2
4-line SPI interface	L	L	L
3-line SPI interface	L	L	H
I^2C interface	H	H	H

PS0=" L ", PS1=" L ", PS2=" L ": 4-line SPI interface

When the ST7546T is active (CSB="L"), serial data (D1) and serial clock (D0) inputs are enabled. And not active, the internal 8-bit shift register and the 3-bit counter are reset. The display data/command indication may be controlled either via software or the Register Select (A0) Pin, based on the setting of PS[2:0]. When the A0 pin is used , data is display data when A0 is high, and command data when A0 is low. When A0 is not used , the LCD Driver will receive command from MCU by default. If messages on the data pin are data rather than command, MCU should send Data direction command to control the data direction and then one more command to define the number of data bytes will be write. After these two continuous commands are sending, the following messages will be data rather than command. Serial data can be read on the rising edge of serial clock going into D0 and processed as 8-bit parallel data on the eighth serial clock. And the DDRAM column address pointer will be increased by one automatically. The next bytes after the display data string are handled as command data.

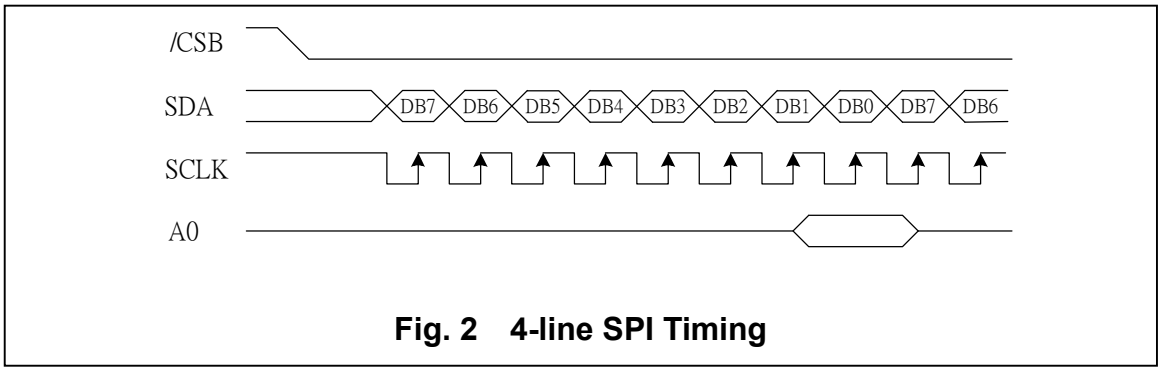


Fig. 2 4-line SPI Timing

PS0=" L ", PS1=" L ", PS2=" H ": 3-line SPI interface

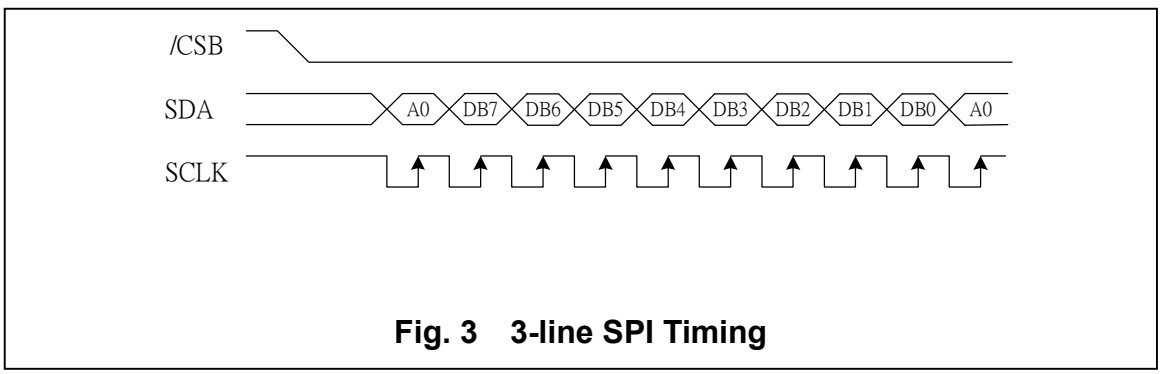


Fig. 3 3-line SPI Timing

PS0=" H ", PS1=" H ", PS2=" H ": I²C Interface

The I²C interface receives and executes the commands sent via the I²C Interface. It also receives RAM data and sends it to the RAM.

The I²C Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCLK). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Fig.4.

START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.5.

SYSTEM CONFIGURATION

The system configuration is illustrated in Fig.6.

· Transmitter: the device, which sends the data to the bus
· Receiver: the device, which receives the data from the bus
· Master: the device, which initiates a transfer, generates clock signals and terminates a transfer
· Slave: the device addressed by a master
· Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message
· Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
· Synchronization: procedure to synchronize the clock signals of two or more devices.

ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I²C Interface is illustrated in Fig.7.

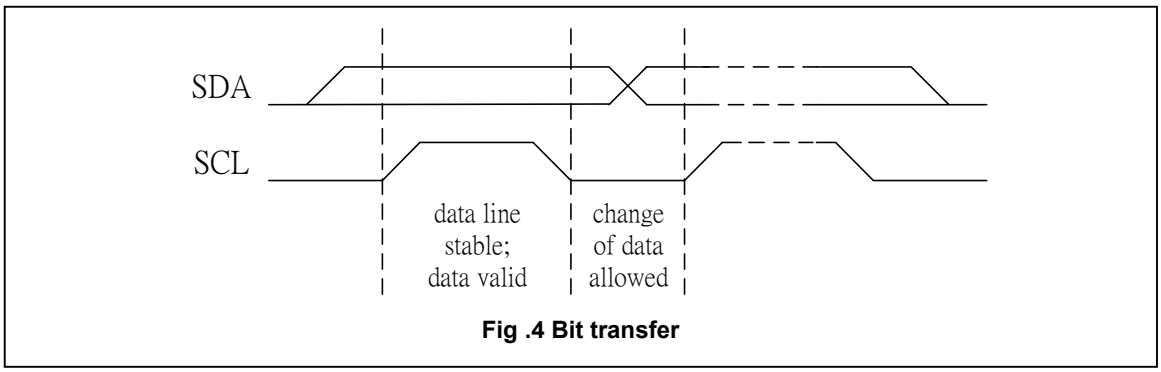


Fig .4 Bit transfer

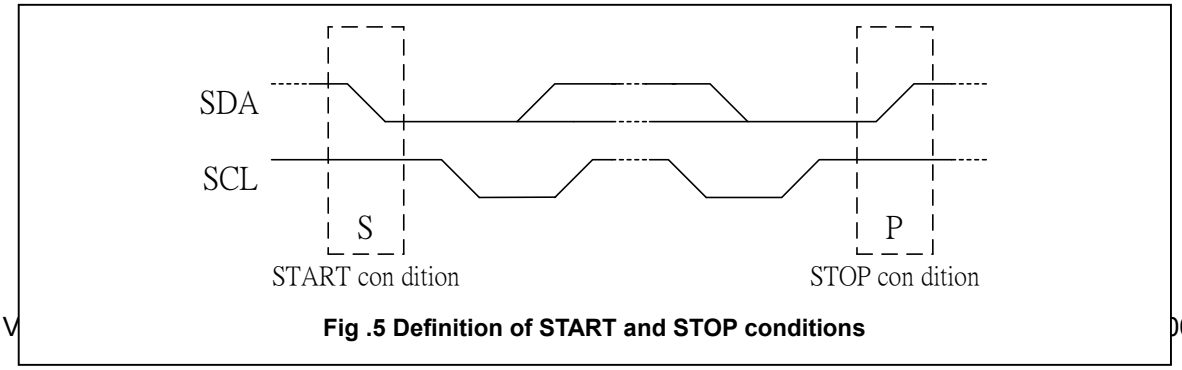


Fig .5 Definition of START and STOP conditions

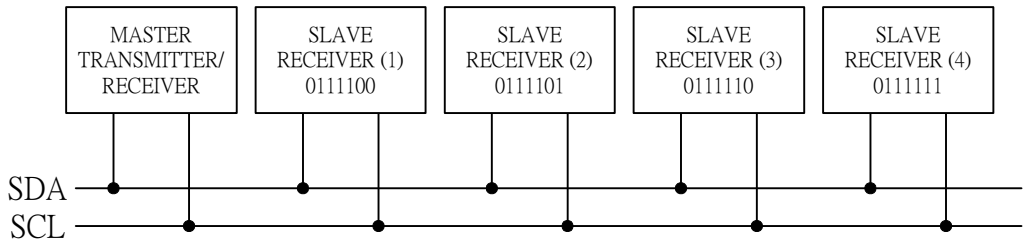


Fig .6 System configuration

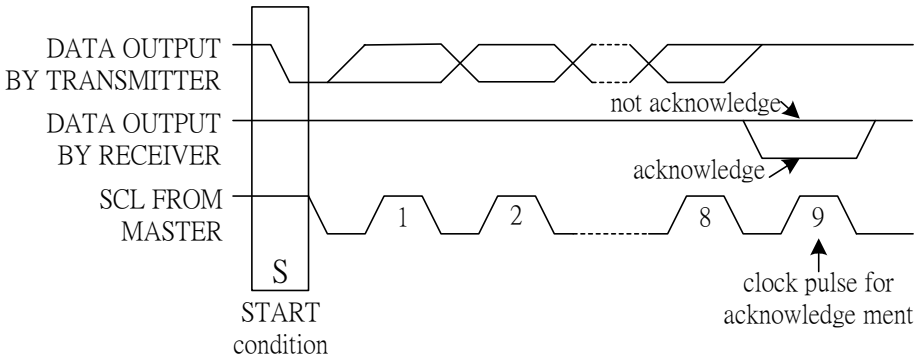


Fig .7 Acknowledgement on the I^2C Interface

I^2C Interface protocol

The ST7546T supports command, data write addressed slaves on the bus.
Before any data is transmitted on the I^2C Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111**100**,0111**101**, 0111**110** and 0111**111**) are reserved for the ST7546T. The least significant bit of the slave address is set by connecting the input SA0 and SA1 to either logic 0 (or logic 1 (VDD1).
The I^2C Interface protocol is illustrated in Fig.8.

The sequence is initiated with a START condition (S) from the I^2C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I^2C Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.
A command word consists of a control byte, which defines Co and A0, plus a data byte.
The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the A0 bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the A0 bit setting; either a series of display data bytes or command data bytes may follow. If the A0 bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended ST7546T device. If the A0 bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the I^2C INTERFACE-bus master issues a STOP condition (P).If the R/W bit is set to logic 1 the chip will output data immediately after the slave address if the A0 bit, which was sent during the last write access, is set to logic 0. If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

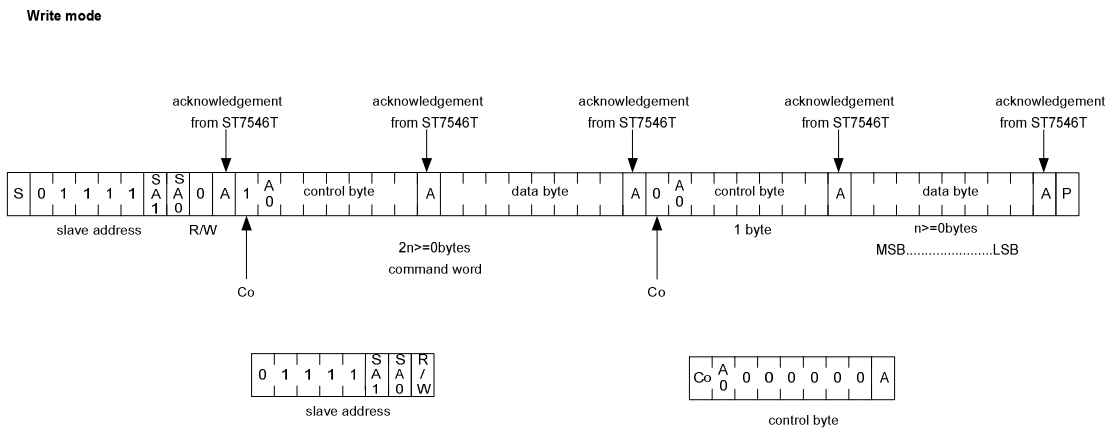


Fig .8 I²C Interface protocol

Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by s STOP or RE-START condition.
	1	Another control byte will follow the data byte unless a STOP or RE-START condition is received.

Data Transfer

The ST7546T uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in figure 9. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 10. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

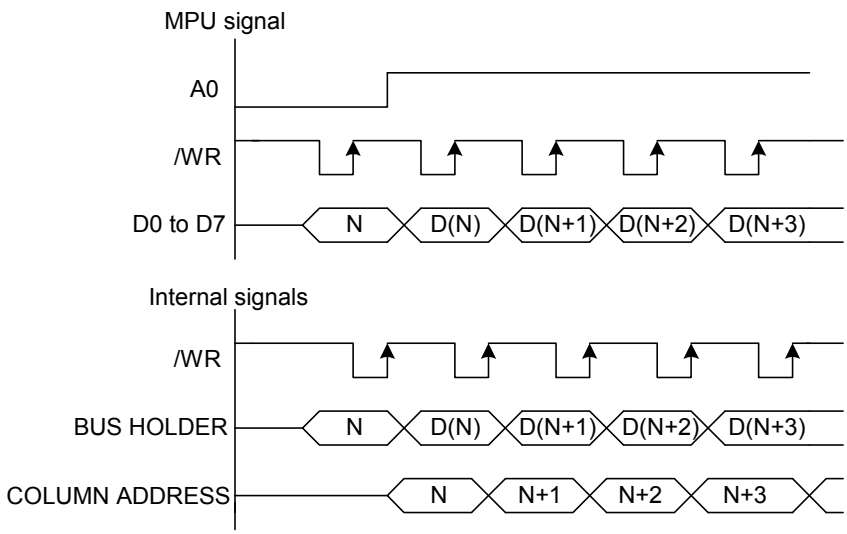


Fig.9 Write Timing

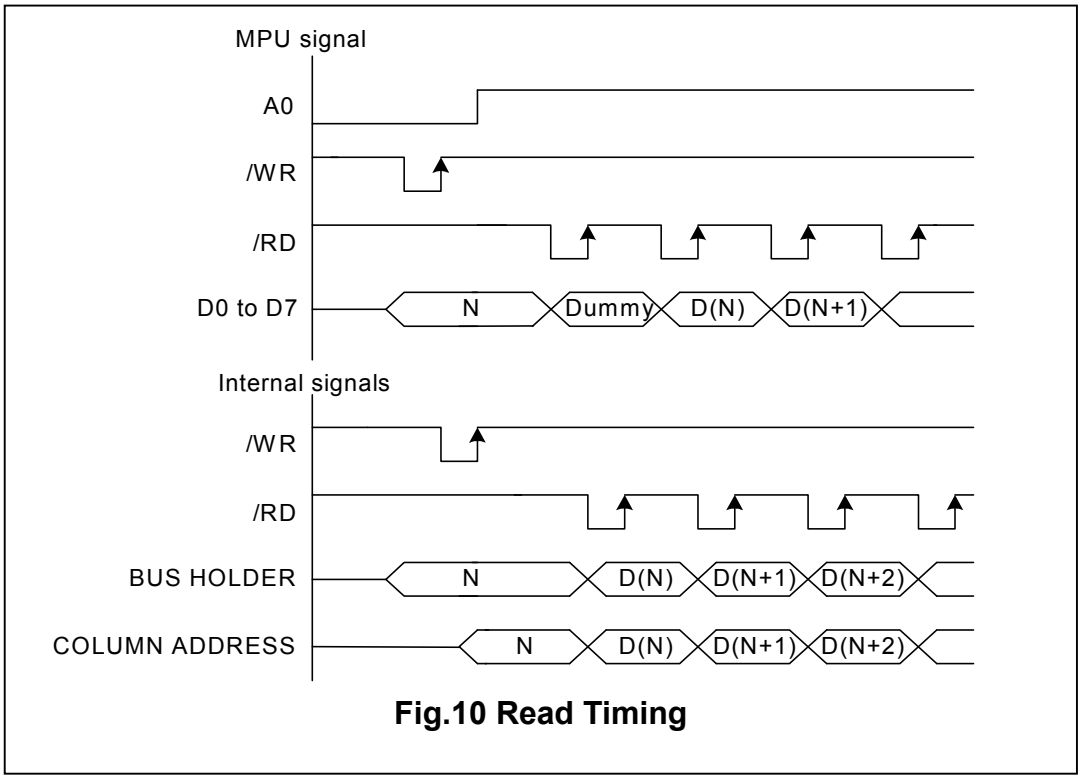


Fig.10 Read Timing

DISPLAY DATA RAM (DDRAM)

The ST7546T contains a 66X102 bit static RAM that stores the display data. The display data RAM store the dot data for the LCD. It has a 66(8 pageX8 bit +1 pageX1 bit +1 pageX1 bit) X 102 . There is a direct correspondence between X-address and column output number. It is 66-row by 102-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 65 rows are divided into 8 pages of 8 lines (0~63 COM) and 8th page with single line (D0) (64COM) and 9th page with a single line (D0) (COMS for ICON). Data is read from or written to the 8 lines of each page directly through D0 to D7. The display data of D0 to D7 from the microprocessor correspond to the LCD common lines. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM. It incorporates 4-bit Page Address register changed by only the “Set Page” instruction. Page Address 9 is a special RAM area for the icons and display data D0 is only valid.

Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting Line Address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM as shown in figure 10. It incorporates 7-bit Line Address register changed by only the initial display line instruction and 7-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the line address for transferring the 102-bit RAM data to the display data latch circuit. When icon is selected by setting icon page address, display data of icons are not scrolled because the MPU cannot access Line Address of icons.

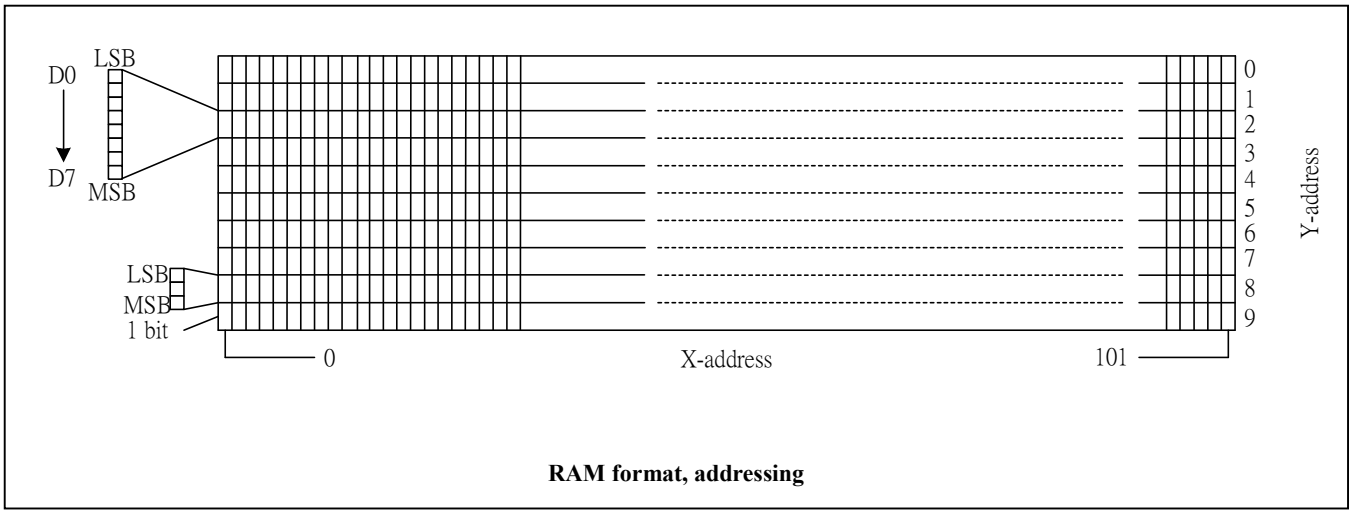
Column Address Circuit

Column Address Circuit has an 8-bit preset counter that provides Column Address to the Display Data RAM. The display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously.

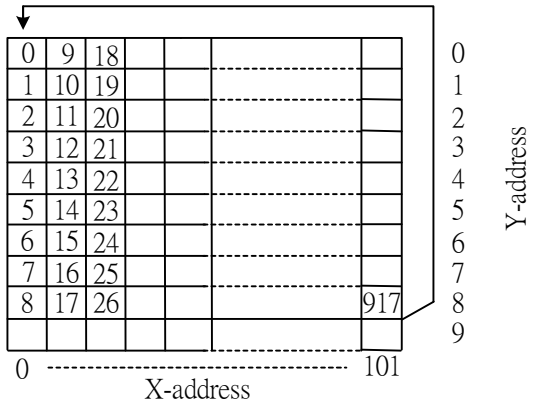
ADDRESSING

Data is downloaded in bytes into the RAM matrix of ST7546T. The display RAM has a matrix of 66 by 102 bits. The address pointer addresses the columns. The address ranges are: X 0 to 101 (1100101),Y 0 to 9 (1001) .Addresses outside these ranges are not allowed.In vertical addressing mode (V=1) the Y address increments after each byte. After the last Y address (Y = 8), Y wraps around to 0 and X increments to address the next column.In horizontal addressing mode (V=0) the X address increments after each byte. After the last X address(X = 101) X wraps around to 0 and Y increments to address the next row.After the very last address (X = 101, Y = 8) the address pointers wrap around to address (X = 0, Y =0)

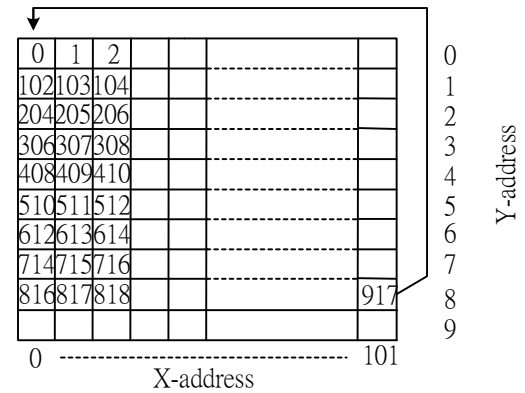
Data structure



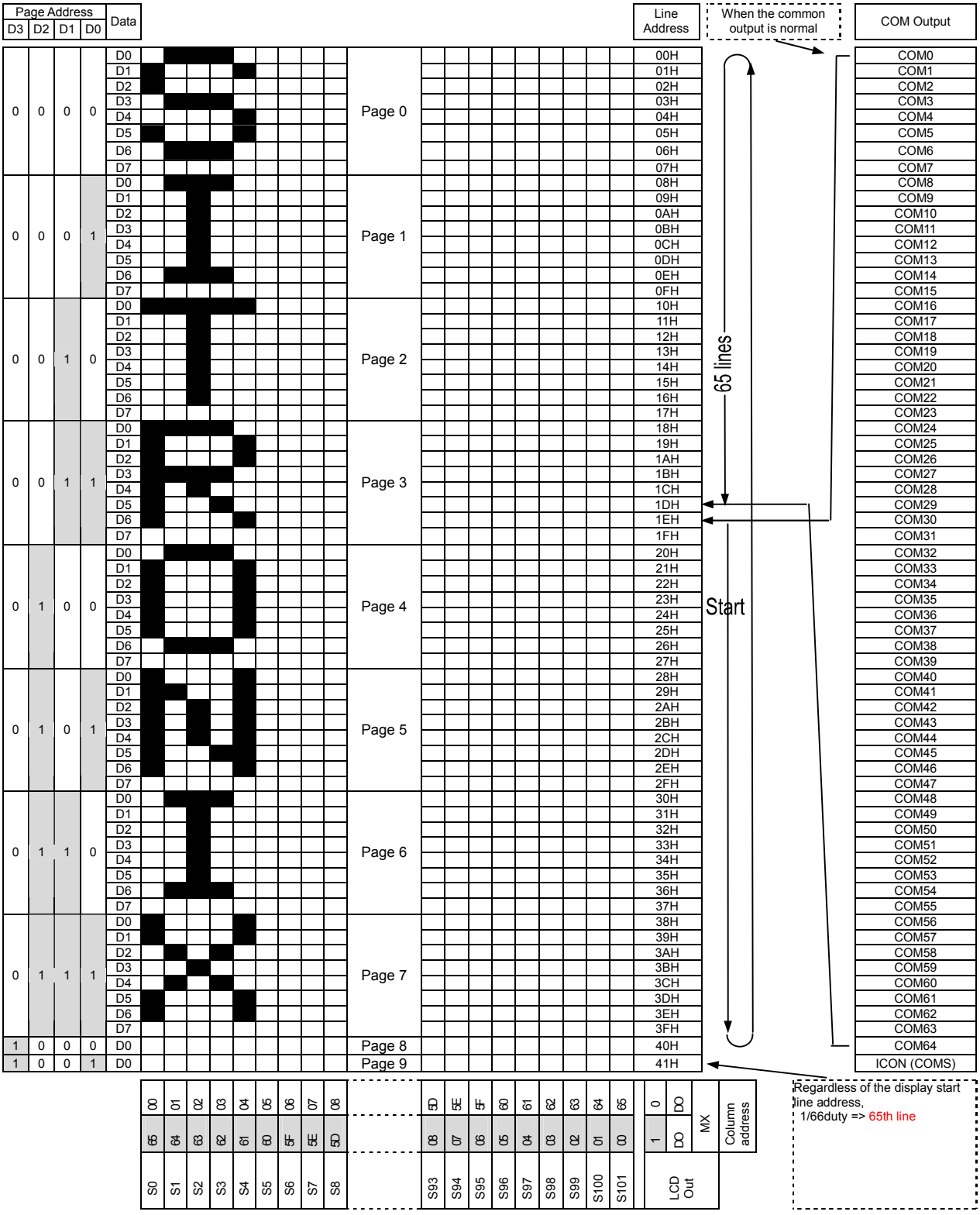
RAM format, addressing



Sequence of writing data bytes into RAM with vertical addressing (V=1)



Sequence of writing data bytes into RAM with horizontal addressing (V=0)



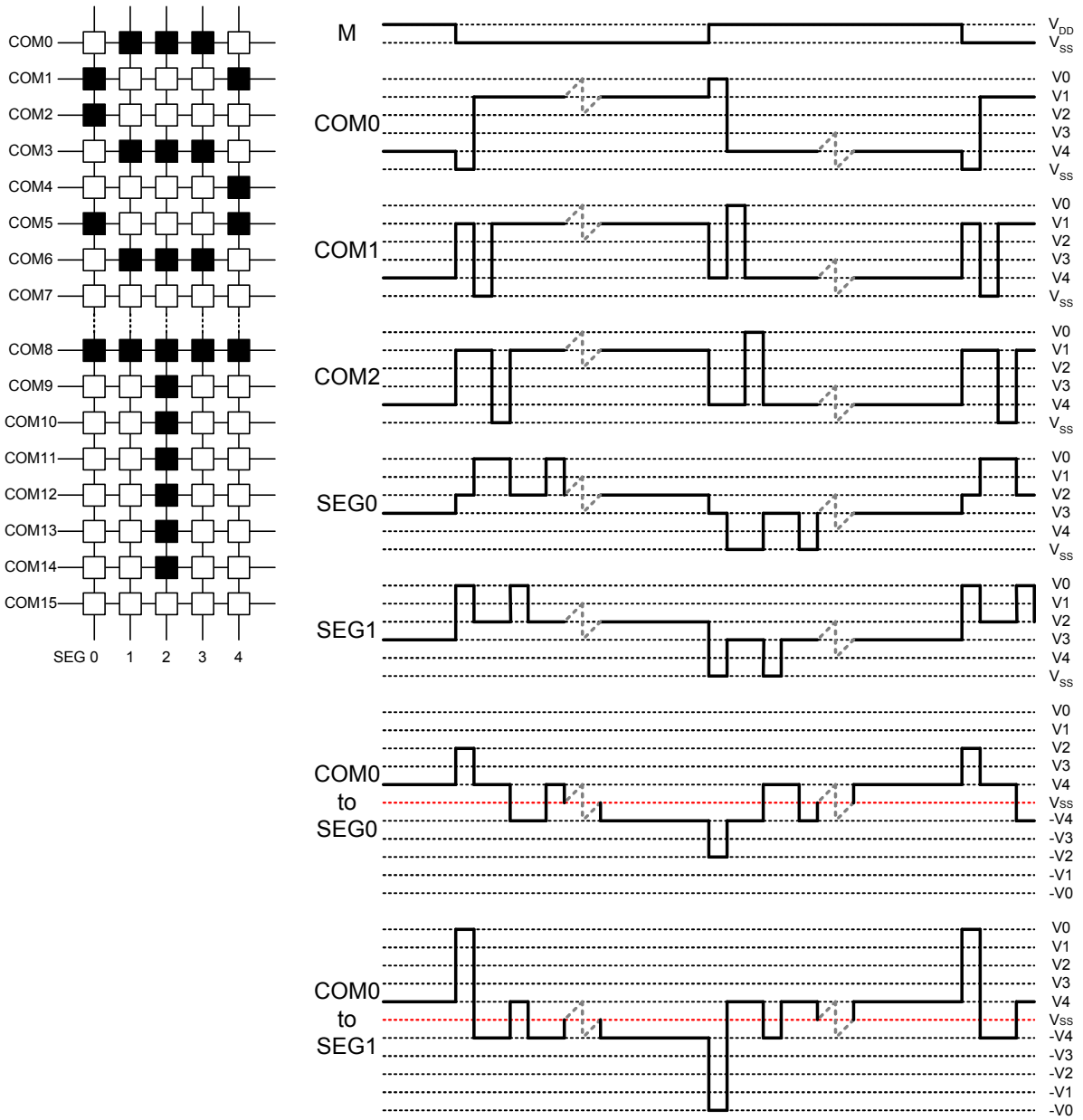
Display Data RAM Map (66 COM)

Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC input must be connected to VDD. An external clock signal, if used, is connected to this input.

LCD DRIVER CIRCUIT

66-channel common drivers and 102-channel segment drivers configure this driver circuit. This LCD panel driver voltage depends on the combination of display data and M signal.



Typical LCD driver waveforms

7. RESET CIRCUIT

Setting RESB to “L” or Reset instruction can initialize internal function.
When RESB becomes “L”, following procedure is occurred.
Page address: 0
Column address: 0
Display control: Display blank
Oscillator: OFF
Power down mode (PD = 1)
Horizontal addressing (V = 0)
Normal instruction set (H = 0)
Display blank (E = D = 0)
Address counter X [6:0] = 0, Y [3:0] = 0
Bias system (BS [2:0] = BR setting)
VLCD is equal to 0; the HV generator is switched off (VOP [6:0] = 0)
After power-on, RAM data are undefined

While RESB is “L” or reset instruction is executed, no instruction except read status can be accepted. Reset status appears at DB0. After DB0 becomes ” L”, any instruction can be accepted. RESB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESB is essential before used.

8. INSTRUCTION TABLE

INSTRUCTION	A0	WR (R/W)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
H=0 or 1											
NOP	0	0	0	0	0	0	0	0	0	0	No operation
Function set	0	0	0	0	1	0	0	PD	V	H	Power-down; entry mode;
Write data	1	0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Write data to RAM

INSTRUCTION	A0	WR (R/W)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
H=0											
Set V_{LCD} range	0	0	0	0	0	1	0	0	0	PRS	V_{LCD} range L/H select
Display control	0	0	0	0	0	0	1	D	0	E	Sets display configuration
Set Y address of RAM	0	0	0	1	0	0	Y_3	Y_2	Y_1	Y_0	Sets Y address of RAM $0 \leqq Y \leqq 9$
Set X address of RAM	0	0	1	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Sets X address of RAM $0 \leqq X \leqq 101$
H=1											
Reserved	0	0	0	0	0	0	0	0	1	X	Do not use
Bias system	0	0	0	0	0	1	0	BS_2	BS_1	BS_0	Sets bias system (BSx)
Reserved	0	0	0	1	X	X	X	X	X	X	Do not use(reserved for test)
Set V_{OP}	0	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}	Write V_{OP} to register

9. INSTRUCTION DESCRIPTION

H= “0” or “1”

Function Set

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	PD	V	H

Flag	Description
PD	All LCD outputs at VSS (display off), bias generator and VLCD generator off, VLCD can be disconnected, oscillator off (external clock possible), RAM contents not cleared; RAM data can be written. PD=0:chip is active PD=1:chip is in power down mode
V	When V = 0, the horizontal addressing is selected. When V = 1, the vertical addressing is selected.
H	When H = 0 the commands ‘display control’, ‘set Y address’ and ‘set X address’ can be performed, when H = 1 the others can be executed. The commands ‘write data’ and ‘function set’ can be executed in both cases.

Write data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	Write data							

H= “0”

Set V_{LCD} range

V_{LCD} range L/H select

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	0	0	PRS

PRS=0: VLCD programming range LOW

PRS=1: VLCD programming range HIGH

Display Control

This bits D and E selects the display mode.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	D	0	E

Flag	Description		
D,E	D	E	The bits D and E select the display mode.
	0	0	Display blank
	1	0	Normal display
	0	1	All display segments on
	1	1	Inverse video mode

Set Y address of RAM

Y [3:0] defines the Y address vector address of the display RAM.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	Y_3	Y_2	Y_1	Y_0

Y_3	Y_2	Y_1	Y_0	CONTENT	ALLOWED X-RANGE
0	0	0	0	Page0 (display RAM)	0 to 101
0	0	0	1	Page1 (display RAM)	0 to 101
0	0	1	0	Page2 (display RAM)	0 to 101
0	0	1	1	Page3 (display RAM)	0 to 101
0	1	0	0	Page4 (display RAM)	0 to 101
0	1	0	1	Page5 (display RAM)	0 to 101
0	1	1	0	Page6 (display RAM)	0 to 101
0	1	1	1	Page7 (display RAM)	0 to 101
1	0	0	0	Page8 (display RAM)	0 to 101
1	0	0	1	Page9 (display RAM)	0 to 101

Set X address of RAM

The X address points to the columns. The range of X is 0…101.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	X_6	X_5	X_4	X_3	X_2	X_1	X_0

X_6	X_5	X_4	X_3	X_2	X_1	X_0	Column address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:
1	1	0	0	0	1	0	98
1	1	0	0	0	1	1	99
1	1	0	0	1	0	0	100
1	1	0	0	1	0	1	101

H= “1”

System Bias

Select LCD bias ratio of the voltage required for driving the LCD.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	BS_2	BS_1	BS_0

BS_2	BS_1	BS_0	Bias	Recommend Duty
0	0	0	11	1:100
0	0	1	10	1:81
0	1	0	9	1:65/1:68
0	1	1	8	1:49
1	0	0	7	1/40:1/36
1	0	1	6	1/24
1	1	0	5	1:18/1:16
1	1	1	4	1:10/1:9/1:8

Set VOP value

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}

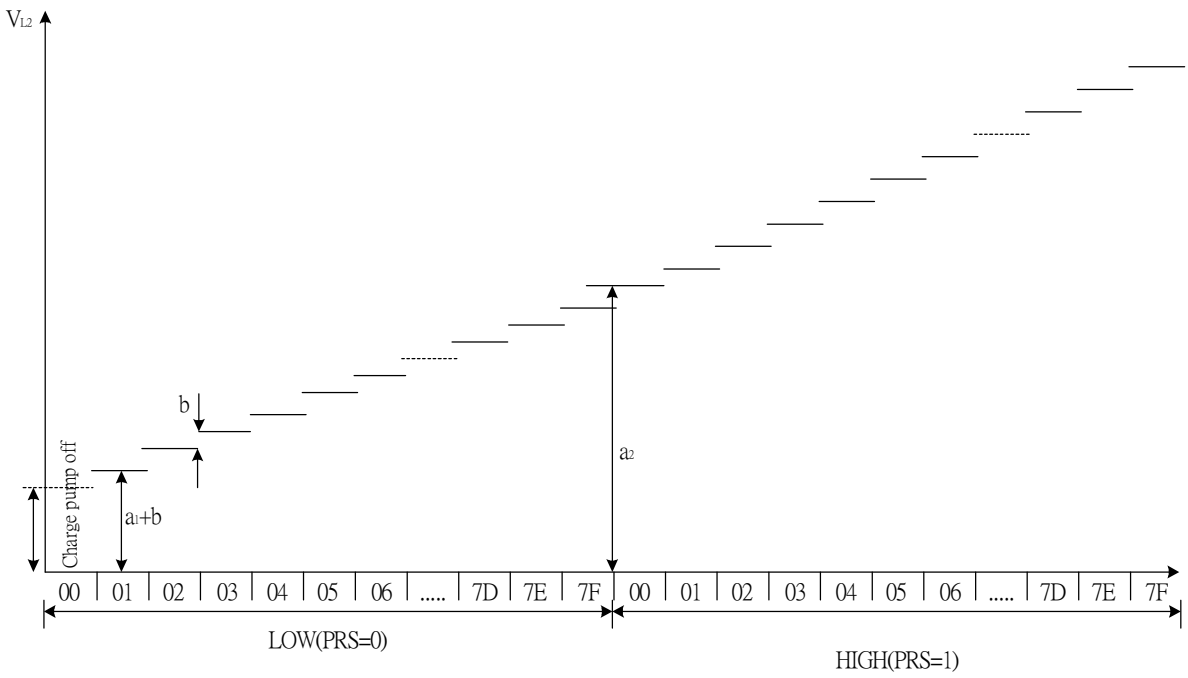
The operation voltage V_{LCD} can be set by software.

$$V_{LCD}=(a + V_{OP} x b) \quad (1)$$

The maximum voltage that can be generated is depending on the VDD1 voltage and the display load current. Two overlapping VLCD ranges are selectable via the command "Booster control". For the LOW (PRS=0) range a=a1 and for the HIGH (PRS=1) range a=a2 with steps equal to "b" in both ranges. Note that the charge pump is turned off if VOP [6;0] and the bit PRS are all set to zero

Table 4 Typical values for parameter for the HV-Generator programming

SYMBOL	VALUE	UNIT
a1	2.94(PRS=0)	V
a2	6.75(PRS=1)	V
b	0.03	V

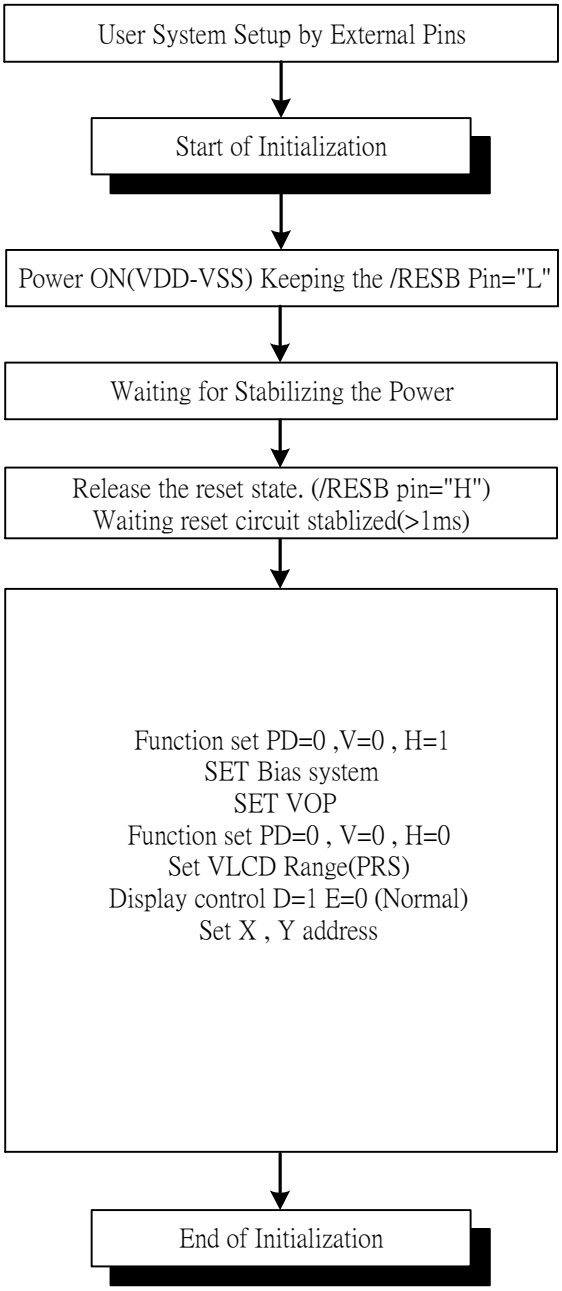


VOP [6:0](programmed) {00 hex… 7F hex}

Fig.23 V_{OP} programming of ST7546T

10. COMMAND DESCRIPTION

Referential Instruction Setup Flow: Initializing with the built-in Power Supply Circuits

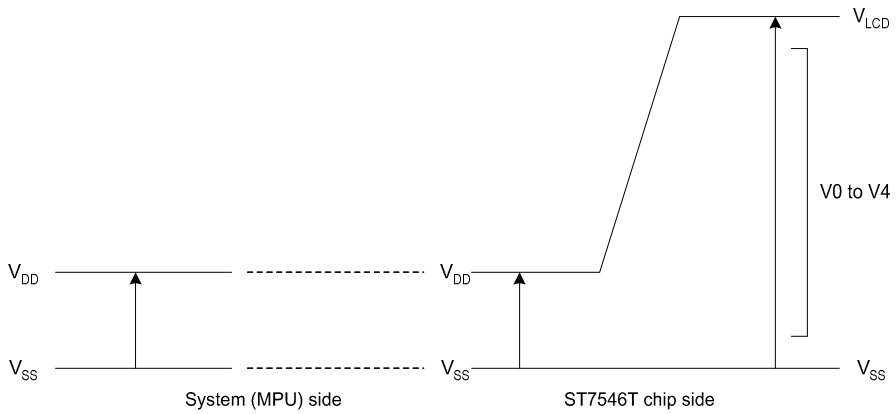


Initializing with the Built-in Power Supply Circuits

11. LIMITING VALUES

In accordance with the Absolute Maximum Rating System; see notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Power Supply Voltage	VDD1	-0.5 ~ 5	V
Power supply voltage	VDD2	-0.5 ~ 5	V
Power supply voltage (VDD standard)	VLCDIN	4.5~13.5	V
Power supply voltage (VDD standard)	V1, V2, V3, V4	0.3 to Vlcdin	V
Operating temperature	TOPR	–40 to +85	°C
Storage temperature	TSTR	–65 to +150	°C



Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
3. Insure that the voltage levels of V0, V1, V2, V3, and V4 are always such that

   VLCDIN ≧ V0 ≧ V1 ≧ V2 ≧ V3 ≧ V4 ≧ Vss

12. HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see “Handling MOS devices”).

13. DC CHARACTERISTICS

V_{DD1} = 1.7 V to 3.3V; V_{SS} = 0 V; Vout = 3.0 to 13.0V; T_{amb} = -40℃ to +85℃; unless otherwise specified.

Item	Symbol	Condition		Rating			Units	Applicable Pin
				Min.	Typ.	Max.		
Operating Voltage (1)	VDD1			1.7	—	3.3	V	Vss
Operating Voltage (2)	VDD2	(Relative to VSS)		2.4	—	3.3	V	VSS
High-level Input Voltage	VIHC			0.7 x VDD	—	VDD	V	
Low-level Input Voltage	VILC			VSS	—	0.3 x VDD	V	
High-level Output Voltage	VOHC			0.7 x VDD	—	VDD	V	
Low-level Output Voltage	VOLC			VSS	—	0.3 x VDD	V	
Input leakage current	ILI			–1.0	—	1.0	μA	
Output leakage current	ILO			–3.0	—	3.0	μA	
Liquid Crystal Driver ON Resistance	RON	Ta = 25°C (Relative To VSS)	VLCDIN = 13.0 V	—	2.0	3.5	KΩ	SEGn COMn *6
			VLCDIN = 8.0 V	—	3.2	5.4		
Frame frequency	FR			65.7	73	80.3	Hz	

Item		Symbol	Condition	Rating			Units	Applicable Pin
				Min.	Typ.	Max.		
Internal Power	Input voltage	VDD1	(Relative To VSS)	1.7	—	3.3	V	
	Supply Step-up output voltage Circuit	VLCDOUT	(Relative To VSS)	—	—	13.5	V	VLCDOUT
	Voltage regulator Circuit Operating Voltage	VLCDIN	(Relative To VSS)	—	—	13.5	V	VLCDIN

Dynamic Consumption Current : During Display, with the Internal Power Supply OFF Current consumed by total ICs(bare die)

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern SNOW	ISS	VDD = 3.0 V, Booster X4 V0 – VSS = 9.0 V	—	300	—	μA	
Power Down	ISS	Ta = 25°C	—	0.01	2	μA	

Notes to the DC characteristics

1. The maximum possible V_{LCD} voltage that may be generated is dependent on voltage, temperature and (display) load.
2. Internal clock
3. Power-down mode. During power down all static currents are switched off.
4. If external V_{LCDIN}, the display load current is not transmitted to I_{DD}.
5. V_{OUT} external voltage applied to VLCDIN pin; VLCDIN disconnected from VLCDOUT (no connect)

14. TIMING CHARACTERISTICS

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

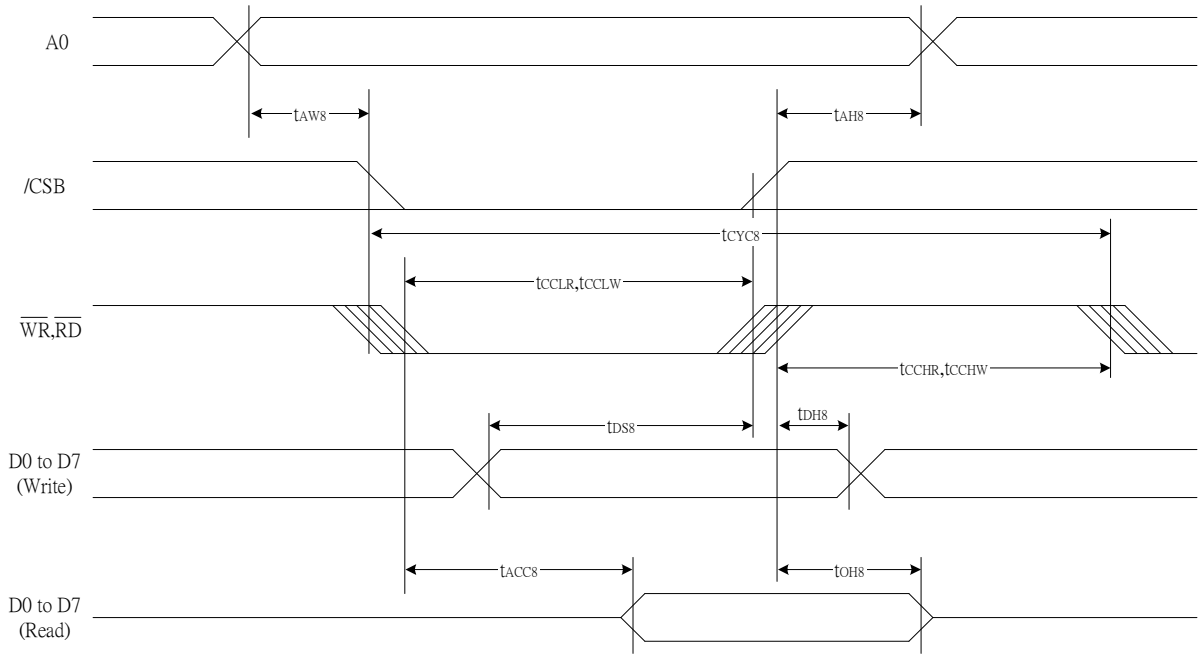


Figure 26.

(VDD = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		10	—	ns
Address setup time		tAW8		100	—	
System cycle time		tCYC8		400	—	
Enable L pulse width (WRITE)	WR	tCCLW		80	—	
Enable H pulse width (WRITE)		tCCHW		80	—	
Enable L pulse width (READ)	RD	tCCLR		140	—	
Enable H pulse width (READ)		tCCHR		80		
WRITE Data setup time	D0 to D7	tDS8		80	—	
WRITE Address hold time		tDH8		10	—	
READ access time		tACC8	CL = 100 pF	—	70	
READ Output disable time		tOH8	CL = 100 pF	5	50	

(VDD = 2.7 V , Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		15	—	ns
Address setup time		tAW8		150	—	
System cycle time		tCYC8		600	—	
Enable L pulse width (WRITE)	WR	tCCLW		220	—	
Enable H pulse width (WRITE)		tCCHW		180	—	
Enable L pulse width (READ)	RD	tCCLR		220	—	
Enable H pulse width (READ)		tCCHR		180	—	
WRITE Data setup time	D0 to D7	tDS8		120	—	
WRITE Address hold time		tDH8		15	—	
READ access time		tACC8	CL = 100 pF	—	140	
READ Output disable time		tOH8	CL = 100 pF	10	100	

(VDD = 1.8V , Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		30	—	ns
Address setup time		tAW8		200	—	
System cycle time		tCYC8		1000	—	
Enable L pulse width (WRITE)	WR	tCCLW		360	—	
Enable H pulse width (WRITE)		tCCHW		280	—	
Enable L pulse width (READ)	RD	tCCLR		360	—	
Enable H pulse width (READ)		tCCHR		280		
WRITE Data setup time	D0 to D7	tDS8		200	—	
WRITE Address hold time		tDH8		30	—	
READ access time		tACC8	CL = 100 pF	—	240	
READ Output disable time		tOH8	CL = 100 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) $\leqq$ (tCYC8 – tCCLW – tCCHW) for (tr + tf) $\leqq$ (tCYC8 – tCCLR – tCCHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tCCLW and tCCLR are specified as the overlap between CSB being “L” and WR and RD being at the “L” level.

System Bus Read/Write Characteristics 1 (For the 6800 Series MPU)

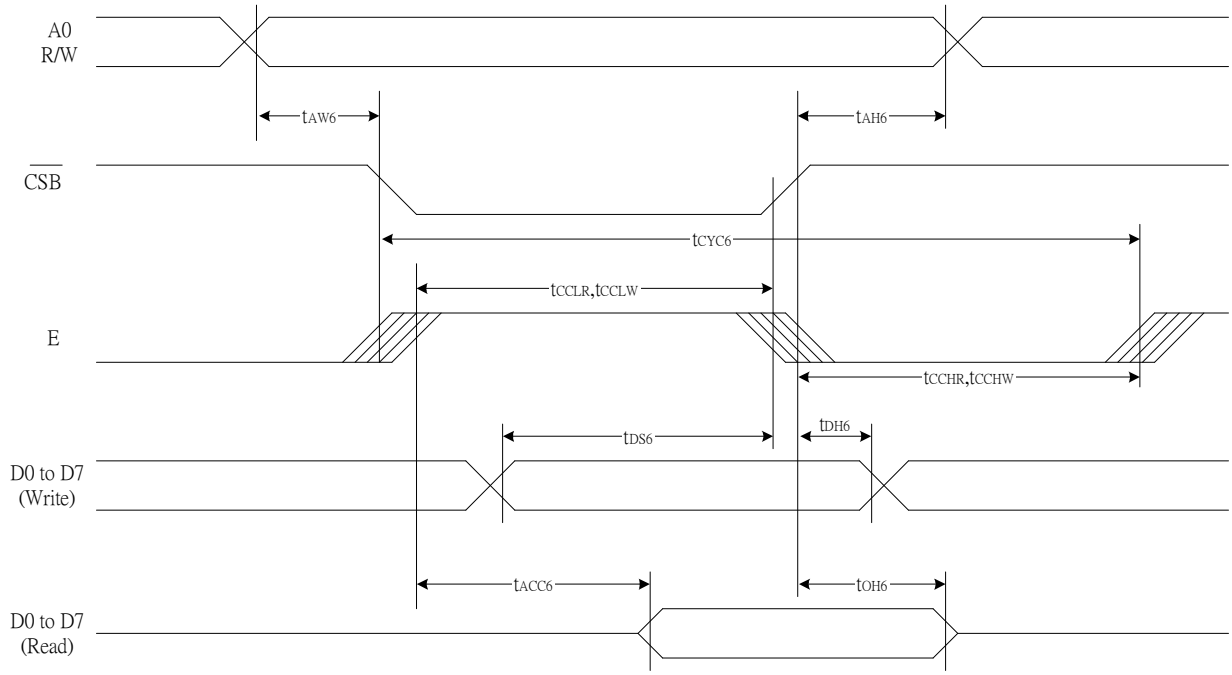


Figure 27.

(V_{DD} = 3.3 V , Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		10	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		240	—	
Enable L pulse width (WRITE)	WR	tEWLW		80	—	
Enable H pulse width (WRITE)		tEWHW		80	—	
Enable L pulse width (READ)	RD	tEWLR		80	—	
Enable H pulse width (READ)		tEWHR		140		
WRITE Data setup time	D0 to D7	tDS6		80	—	
WRITE Address hold time		tDH6		10	—	
READ access time		tACC6	CL = 100 pF	—	70	
READ Output disable time		tOH6	CL = 100 pF	5	50	

(VDD = 2.7V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		15	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		400	—	
Enable L pulse width (WRITE)	WR	tEWLW		220	—	
Enable H pulse width (WRITE)		tEWHW		180	—	
Enable L pulse width (READ)	RD	tEWLR		220	—	
Enable H pulse width (READ)		tEWHR		180	—	
WRITE Data setup time	D0 to D7	tDS6		120	—	
WRITE Address hold time		tDH6		15	—	
READ access time		tACC6	CL = 100 pF	—	140	
READ Output disable time		tOH6	CL = 100 pF	10	100	

(VDD =1.8V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		30	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		640	—	
Enable L pulse width (WRITE)	WR	tEWLW		360	—	
Enable H pulse width (WRITE)		tEWHW		280	—	
Enable L pulse width (READ)	RD	tEWLR		360	—	
Enable H pulse width (READ)		tEWHR		280	—	
WRITE Data setup time	D0 to D7	tDS6		200	—	
WRITE Address hold time		tDH6		30	—	
READ access time		tACC6	CL = 100 pF	—	240	
READ Output disable time		tOH6	CL = 100 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≦ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≦ (tCYC6 – tEWLR – tEWHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tEWLW and tEWLR are specified as the overlap between CSB being “L” and E.

SERIAL INTERFACE(4-Line Interface)

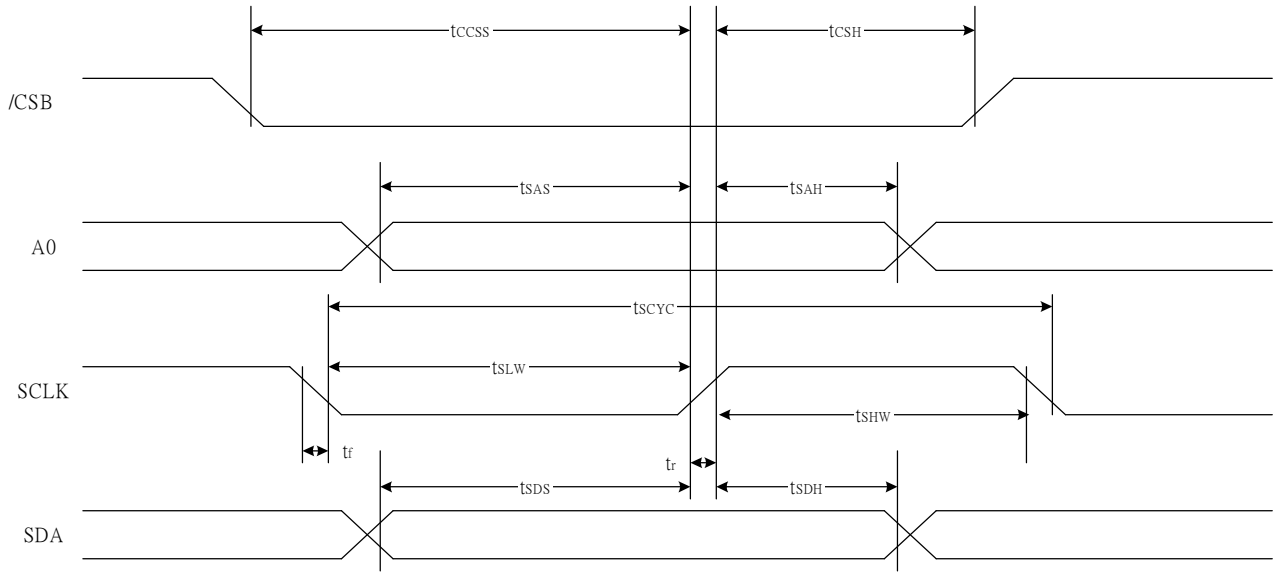


Fig 28.

(V_{DD}=3.3V,Ta=25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		150	—	ns
SCL “H” pulse width		tSHW		75	—	
SCL “L” pulse width		tSLW		75	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		100	—	
Data setup time	SI	tSDS		20	—	
Data hold time		tSDH		10	—	
CS-SCL time	CSB	tCSS		20	—	
CS-SCL time		tCSH		140	—	

(V_{DD}=2.7V,Ta=25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		300	—	ns
SCL “H” pulse width		tSHW		150	—	
SCL “L” pulse width		tSLW		150	—	
Address setup time	A0	tSAS		30	—	
Address hold time		tSAH		150	—	
Data setup time	SI	tSDS		30	—	
Data hold time		tSDH		20	—	
CS-SCL time	CSB	tCSS		30	—	
CS-SCL time		tCSH		200	—	

(V_{DD}=1.8V,Ta=25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		500	—	ns
SCL “H” pulse width		tSHW		250	—	
SCL “L” pulse width		tSLW		250	—	
Address setup time	A0	tSAS		60	—	
Address hold time		tSAH		250	—	
Data setup time	SI	tSDS		60	—	
Data hold time		tSDH		50	—	
CS-SCL time	CSB	tCSS		40	—	
CS-SCL time		tCSH		350	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

SERIAL INTERFACE(3-Line Interface)

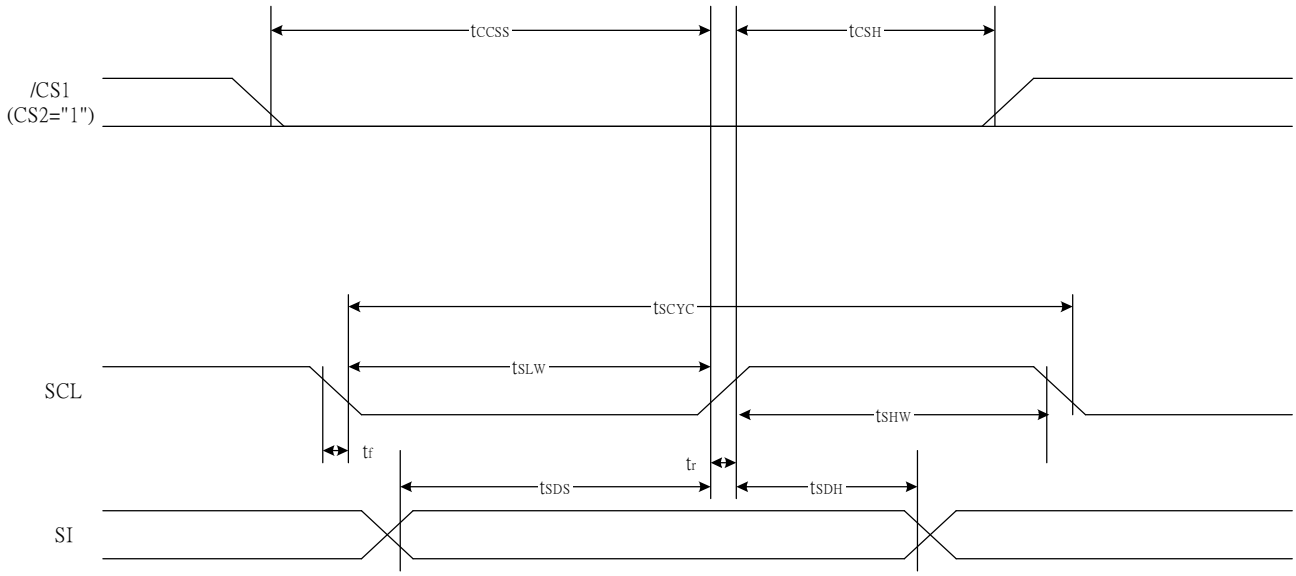


Fig 28.

(V_{DD}=3.3V,Ta=25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		150	—	ns
SCL “H” pulse width		tSHW		75	—	
SCL “L” pulse width		tSLW		75	—	
Data setup time	SI	tSDS		20	—	
Data hold time		tSDH		10	—	
CS-SCL time	CSB	tCSS		20	—	
CS-SCL time		tCSH		140	—	

(V_{DD}=2.7V,Ta=25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		300	—	ns
SCL “H” pulse width		tSHW		150	—	
SCL “L” pulse width		tSLW		150	—	
Data setup time	SI	tSDS		30	—	
Data hold time		tSDH		20	—	
CS-SCL time	CSB	tCSS		30	—	
CS-SCL time		tCSH		200	—	

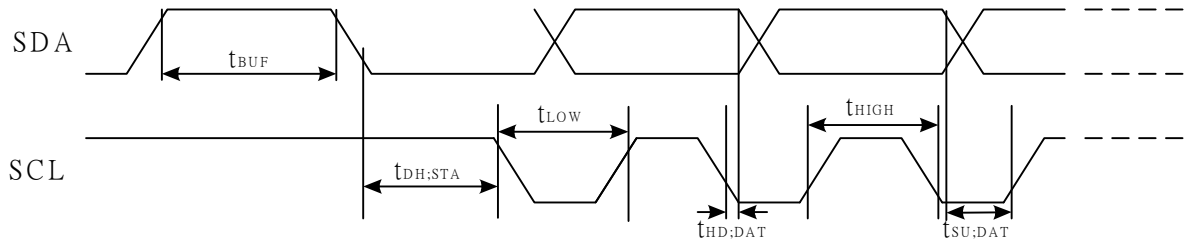
(V_{DD}=1.8V,Ta=25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		500	—	ns
SCL “H” pulse width		tSHW		250	—	
SCL “L” pulse width		tSLW		250	—	
Data setup time	SI	tSDS		60	—	
Data hold time		tSDH		50	—	
CS-SCL time	CSB	tCSS		40	—	
CS-SCL time		tCSH		350	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

SERIAL INTERFACE(I²C Interface)



(V_{DD}=3.3V,Ta=25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
SCL clock frequency	SCL	FSCLK		-	400	kHZ
SCL clock low period	SCL	TLOW		1.3	-	us
SCL clock high period	SCL	THIGH		0.6	-	us
Data set-up time	SI	TSU;Data		100	-	ns
Data hold time	SI	THD;Data		0	0.9	us
SCL,SDA rise time	SCL	TR		20+0.1Cb	300	ns
SCL,SDA fall time	SCL	TF		20+0.1Cb	300	ns
Capacitive load represented by each bus line		Cb		-	400	pF
Setup time for a repeated START condition	SI	TSU;SUA		0.6	-	us
Start condition hold time	SI	THD;STA		0.6	-	us
Setup time for STOP condition		TSU;STO		0.6	-	us
Tolerable spike width on bus		TSW		-	50	ns
BUS free time between a STOP and START condition	SCL	TBUF		1.3		us

15. RESET TIMING

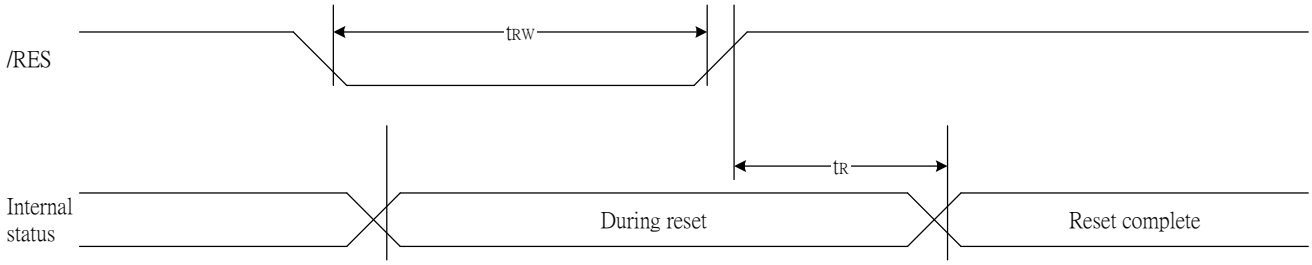


Fig 29.

(VDD = 3.3V , Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	1	us
Reset “L” pulse width	RESB	tRW		1	—	—	us

(VDD = 2.7V , Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	2.0	us
Reset “L” pulse width	RESB	tRW		2.0	—	—	us

(VDD = 1.8V , Ta = –40 to 85°C)

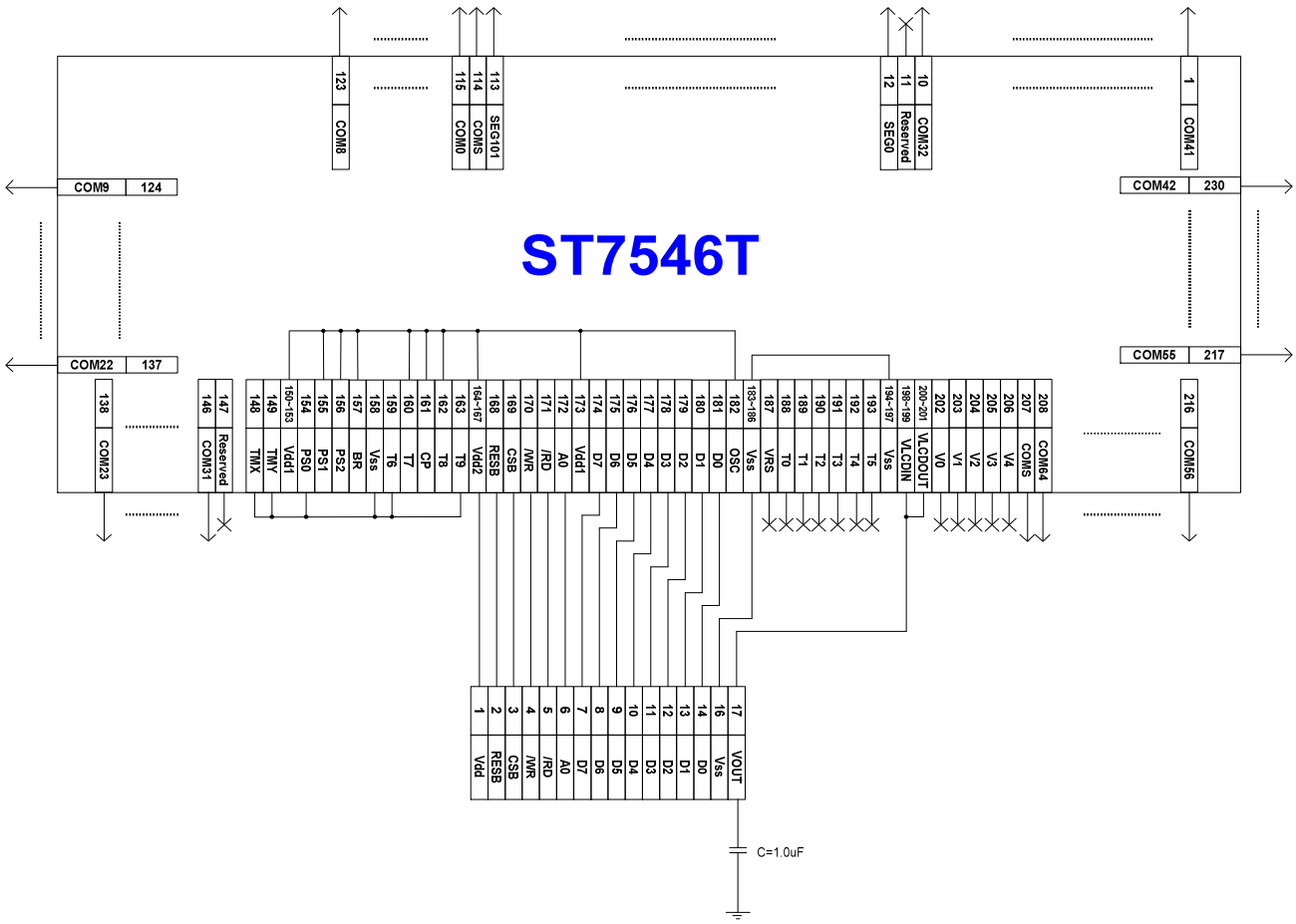
Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	3.0	us
Reset “L” pulse width	RESB	tRW		3.0	—	—	us

APPICATION NOTE

ST7546T (TMY=0)

Resolution : 66(65COM+ICON)*102(SEG)
Interface : 6800 series
Internal analog circuit
Internal OSC
Booster : X5
Bias ratio default : 1/9
(bias ratio can be changed by instruction)
C=1.0 uF

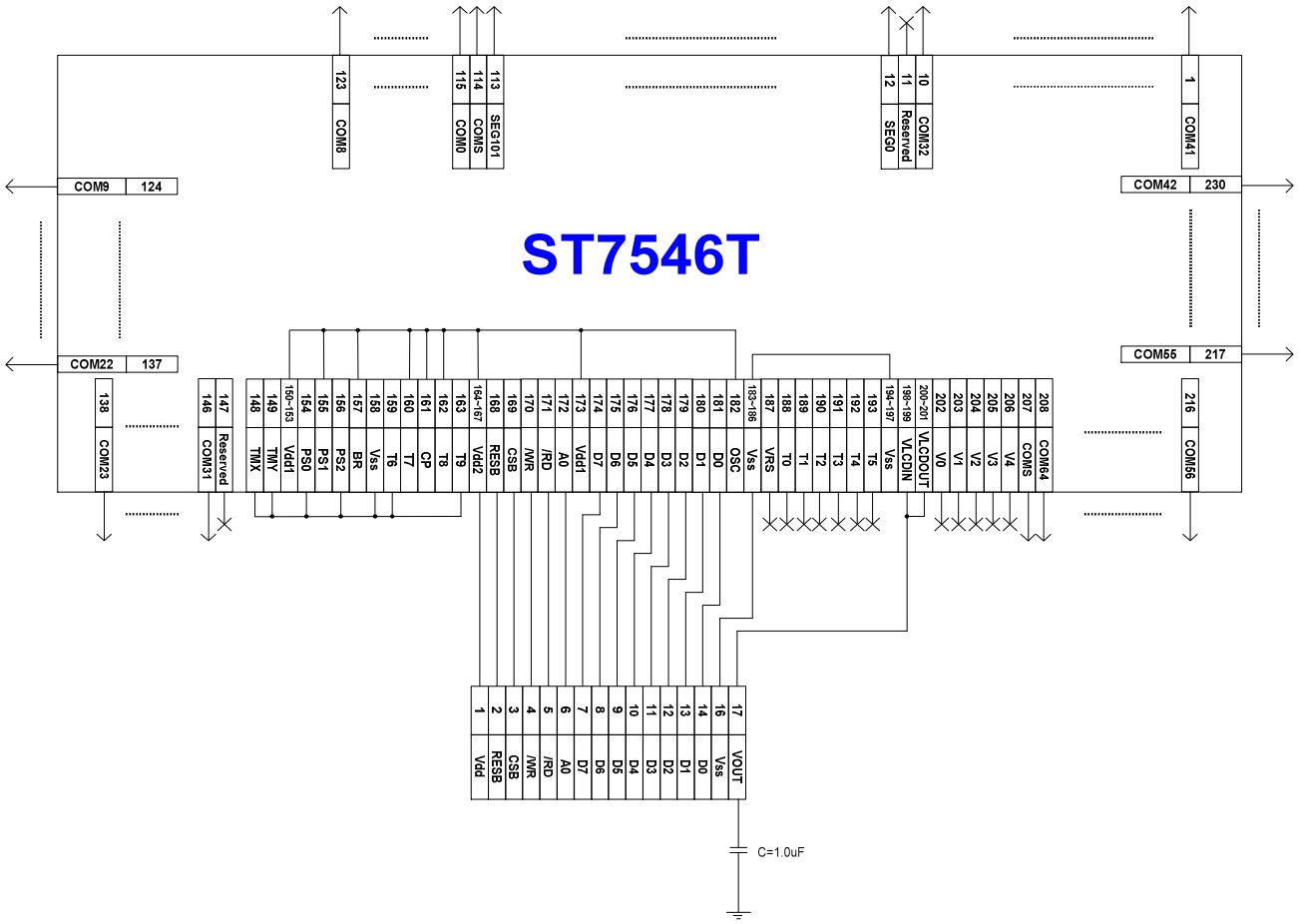
OSC : Vdd
T6 : Vss
T7 : Vdd
T8 : Vdd
T9 : Vss
PS0 : Vss
PS1 : Vdd
PS2 : Vdd
CP : Vdd
BR : Vdd



ST7546T (TMY=0)

Resolution : 66(65COM+ICON)*102(SEG)
Interface : 8080 series
Internal analog circuit
Internal OSC
Booster : X5
Bias ratio default : 1/9
(bias ratio can be changed by instruction)
C=1.0 uF

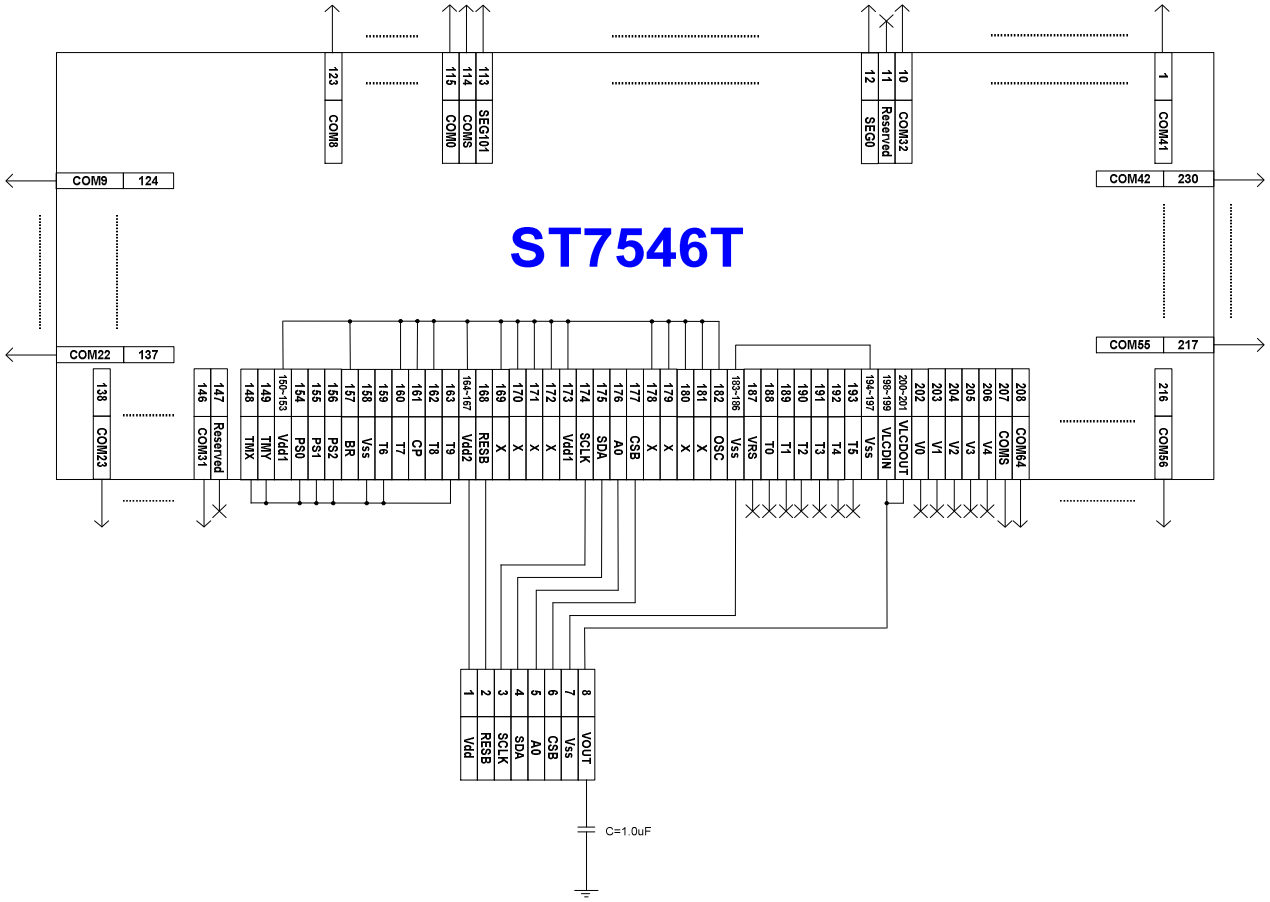
OSC : Vdd
T6 : Vss
T7 : Vdd
T8 : Vdd
T9 : Vss
PS0 : Vss
PS1 : Vdd
PS2 : Vss
CP : Vdd
BR : Vdd



ST7546T (MY=0)

Resolution : 66(65COM+ICON)*102(SEG)
Interface : 4-Line
Internal analog circuit
Internal OSC
Booster : X5
Bias ratio default : 1/9
(bias ratio can be changed by instruction)
C=1.0 uF

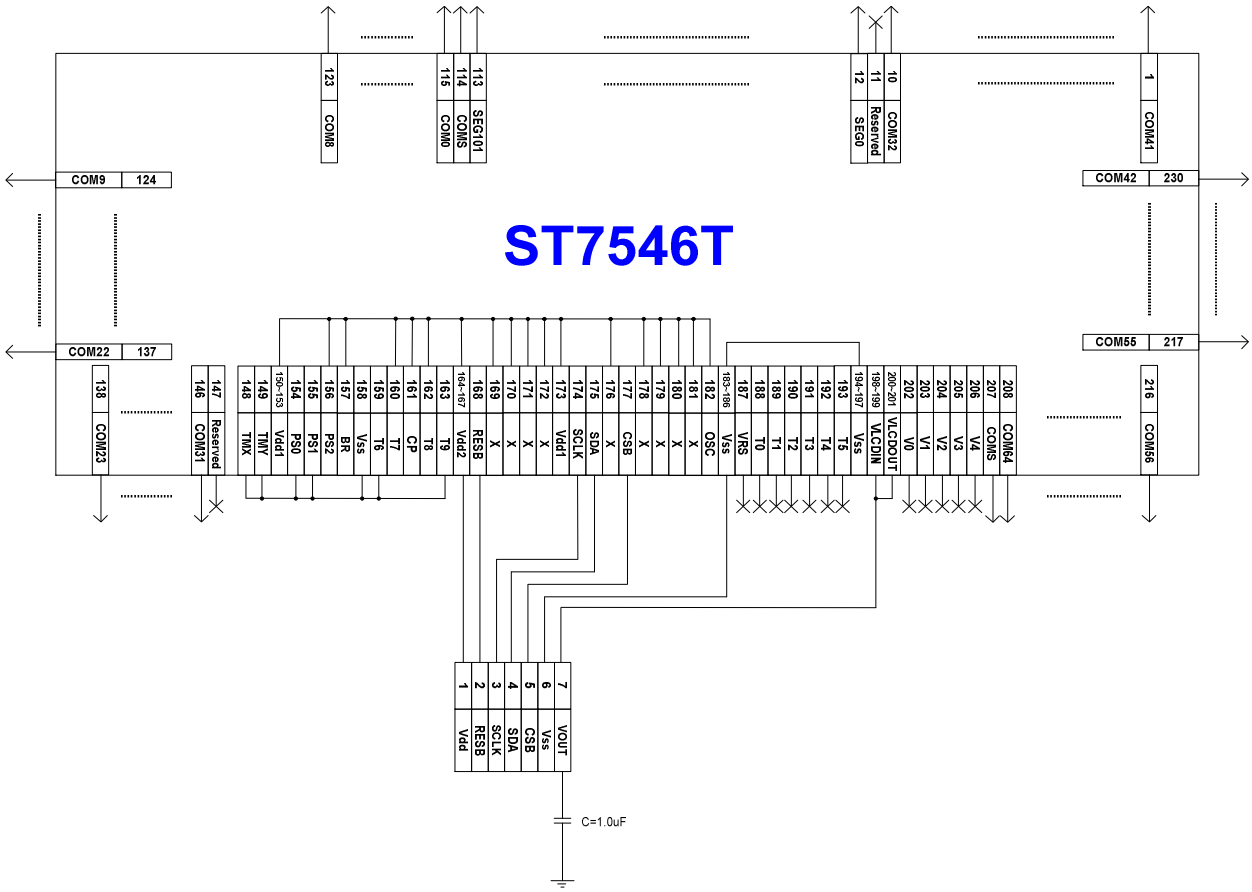
OSC : Vdd
T6 : Vss
T7 : Vdd
T8 : Vdd
T9 : Vss
PS0 : Vss
PS1 : Vss
PS2 : Vss
CP : Vdd
BR : Vdd



ST7546T (MY=0)

Resolution : 66(65COM+ICON)*102(SEG)
Interface : 3-Line
Internal analog circuit
Internal OSC
Booster : X5
Bias ratio default : 1/9
(bias ratio can be changed by instruction)
C=1.0 uF

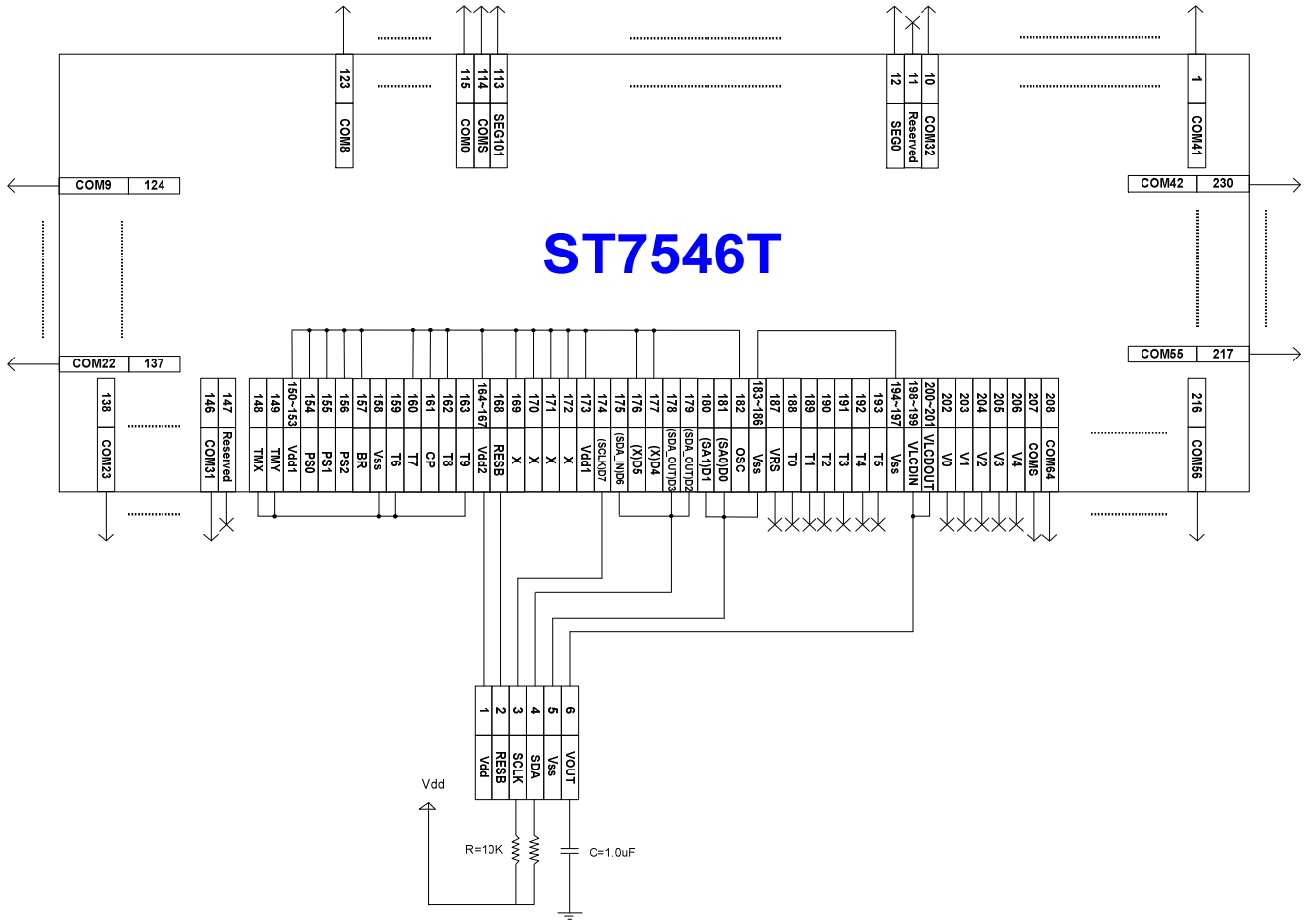
OSC : Vdd
T6 : Vss
T7 : Vdd
T8 : Vdd
T9 : Vss
PS0 : Vss
PS1 : Vss
PS2 : Vdd
CP : Vdd
BR : Vdd



ST7546Ti (MY=0)

Resolution : 66(65COM+ICON)*102(SEG)
Interface : I2C
Internal analog circuit
Internal OSC
Booster : X5
Bias ratio default : 1/9
(bias ratio can be changed by instruction)
SA[1:0]:(0,0)
(SA[1:0] are slave address of I2C)
C=1.0 uF ; R=10K ohm

OSC : Vdd
T6 : Vss
T7 : Vdd
T8 : Vdd
T9 : Vss
PS0 : Vdd
PS1 : Vdd
PS2 : Vdd
CP : Vdd
BR : Vdd



History

Version	History	Notes
V0.x	Preliminary	
V1.0	Complete release Revise I2C pin description	 P13,P47
V1.1	Change Thickness to be 480um Add Frame Rate maximum and minimum value.	
V1.2	Change –G2 definition: Model Name: ST7546T Part Number: ST7546T-G2 and ST7546Ti-G2	