Sitronix

ST7558

65 x 102 Dot Matrix LCD Controller/Driver

1. INTRODUCTION

The ST7558 is a driver & controller LSI for graphic dot-matrix liquid crystal display systems. It contains 102 segment and 65 common with 1 ICOM driver circuits. This chip is connected directly to a microprocessor, accepts 4-line serial interface (SPI), I^2C interface or 8-bit parallel interface, display data can stores in an on-chip display data RAM of 66 x 102 bits. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

Driver Output Circuits

102 segment outputs / 65 common outputs

On-chip Display Data Ram

- Capacity: 66X102=6732 bits

Microprocessor Interface

- 8-bit parallel bi-directional interface with 6800-series or 8080-series
- 4-line SPI (serial peripheral interface) available (only write operation)
- I^2C (Inter-Integrated Circuit) Interface

On-chip Low Power Analog Circuit

- Generation of LCD supply voltage (externally Vout voltage supply is possible)
- Generation of intermediate LCD bias voltages
- Oscillator requires no external components (external clock also possible)
- Voltage converter (x2, x3, x4, x5)
- Voltage regulator (temperature gradient -0.05%/°C)
- Voltage follower
- On-chip electronic contrast control function (128 stepsX2)
- Liquid crystal driving voltage : V0 -VSS = max 12 V (external power supply)

External RESB (reset) pin

Logic supply voltage range V_{DD} -V_{SS}

- 1.8 to 3.3V

Temperature range: -30 to +85 degree

ST7558	**6800 , 8080 , 4-Line (without I^2C interface)**	ST
ST7558i	**I^2C interface**	I²C BUS

3. PAD Arrangement (COG)

Chip Size: 10,220 um × 1000 um

Bump Pitch:

PAD NO 1 ~ 148 , 250 ~ 272 : 75.5 um (com/seg) PAD NO 149 ~ 248 : 75 um (I/O) PAD NO 148 ~ 149 : 114 um

PAD NO 248 ~ 249 : 93.5 um PAD NO 249 ~ 250 : 95.9 um

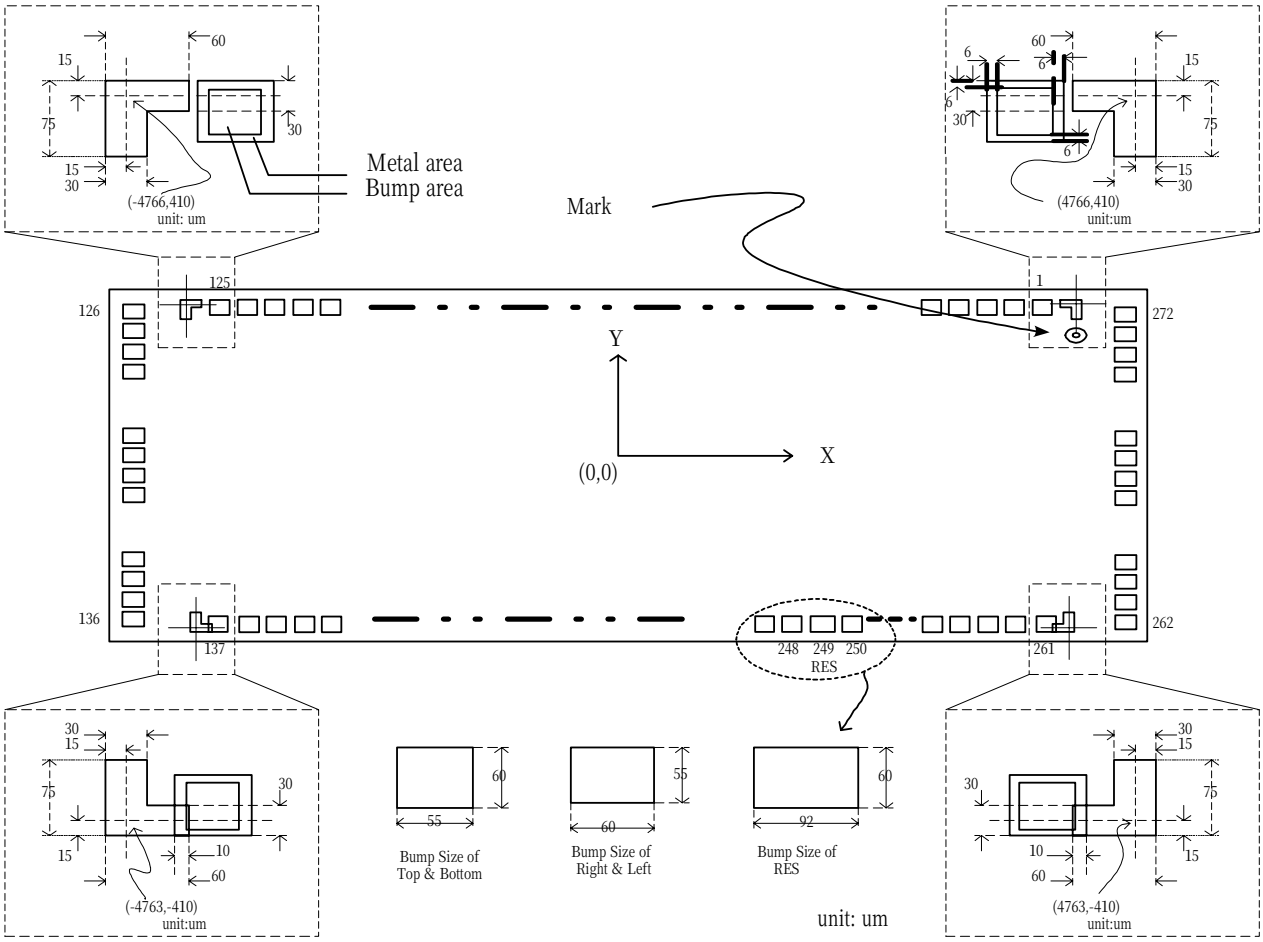
Bump Size:

PAD NO 1 ~ 125 , 137 ~ 248 , 250 ~ 261 : 55(x) um ㄨ 60(y) um PAD NO 249 : 92(x) um ㄨ 60(y) um

PAD NO 126 ~ 136 , 262 ~ 272 : 60(x)um ㄨ 55(y) um

Bump Height: 17 um

Chip Thickness: 635 um



Pad Center Coordinates(NORMAL,MY=0)

PAD NO.	PIN Name	X	Y
1	COM[42]	4681.0	389.0
2	COM[41]	4605.5	389.0
3	COM[40]	4530.0	389.0
4	COM[39]	4454.5	389.0
5	COM[38]	4379.0	389.0
6	COM[37]	4303.5	389.0
7	COM[36]	4228.0	389.0
8	COM[35]	4152.5	389.0
9	COM[34]	4077.0	389.0
10	COM[33]	4001.5	389.0
11	COM[32]	3926.0	389.0
12	Reserve	3850.5	389.0
13	SEG[0]	3775.0	389.0
14	SEG[1]	3699.5	389.0
15	SEG[2]	3624.0	389.0
16	SEG[3]	3548.5	389.0
17	SEG[4]	3473.0	389.0
18	SEG[5]	3397.5	389.0
19	SEG[6]	3322.0	389.0
20	SEG[7]	3246.5	389.0
21	SEG[8]	3171.0	389.0
22	SEG[9]	3095.5	389.0
23	SEG[10]	3020.0	389.0
24	SEG[11]	2944.5	389.0
25	SEG[12]	2869.0	389.0
26	SEG[13]	2793.5	389.0
27	SEG[14]	2718.0	389.0
28	SEG[15]	2642.5	389.0
29	SEG[16]	2567.0	389.0
30	SEG[17]	2491.5	389.0
31	SEG[18]	2416.0	389.0
32	SEG[19]	2340.5	389.0
33	SEG[20]	2265.0	389.0
34	SEG[21]	2189.5	389.0
35	SEG[22]	2114.0	389.0

PAD NO.	PIN Name	X	Y
36	SEG[23]	2038.5	389.0
37	SEG[24]	1963.0	389.0
38	SEG[25]	1887.5	389.0
39	SEG[26]	1812.0	389.0
40	SEG[27]	1736.5	389.0
41	SEG[28]	1661.0	389.0
42	SEG[29]	1585.5	389.0
43	SEG[30]	1510.0	389.0
44	SEG[31]	1434.5	389.0
45	SEG[32]	1359.0	389.0
46	SEG[33]	1283.5	389.0
47	SEG[34]	1208.0	389.0
48	SEG[35]	1132.5	389.0
49	SEG[36]	1057.0	389.0
50	SEG[37]	981.5	389.0
51	SEG[38]	906.0	389.0
52	SEG[39]	830.5	389.0
53	SEG[40]	755.0	389.0
54	SEG[41]	679.5	389.0
55	SEG[42]	604.0	389.0
56	SEG[43]	528.5	389.0
57	SEG[44]	453.0	389.0
58	SEG[45]	377.5	389.0
59	SEG[46]	302.0	389.0
60	SEG[47]	226.5	389.0
61	SEG[48]	151.0	389.0
62	SEG[49]	75.5	389.0
63	SEG[50]	0.0	389.0
64	SEG[51]	-75.5	389.0
65	SEG[52]	-151.0	389.0
66	SEG[53]	-226.5	389.0
67	SEG[54]	-302.0	389.0
68	SEG[55]	-377.5	389.0
69	SEG[56]	-453.0	389.0
70	SEG[57]	-528.5	389.0

PAD NO.	PIN Name	X	Y
71	SEG[58]	-604.0	389.0
72	SEG[59]	-679.5	389.0
73	SEG[60]	-755.0	389.0
74	SEG[61]	-830.5	389.0
75	SEG[62]	-906.0	389.0
76	SEG[63]	-981.5	389.0
77	SEG[64]	-1057.0	389.0
78	SEG[65]	-1132.5	389.0
79	SEG[66]	-1208.0	389.0
80	SEG[67]	-1283.5	389.0
81	SEG[68]	-1359.0	389.0
82	SEG[69]	-1434.5	389.0
83	SEG[70]	-1510.0	389.0
84	SEG[71]	-1585.5	389.0
85	SEG[72]	-1661.0	389.0
86	SEG[73]	-1736.5	389.0
87	SEG[74]	-1812.0	389.0
88	SEG[75]	-1887.5	389.0
89	SEG[76]	-1963.0	389.0
90	SEG[77]	-2038.5	389.0
91	SEG[78]	-2114.0	389.0
92	SEG[79]	-2189.5	389.0
93	SEG[80]	-2265.0	389.0
94	SEG[81]	-2340.5	389.0
95	SEG[82]	-2416.0	389.0
96	SEG[83]	-2491.5	389.0
97	SEG[84]	-2567.0	389.0
98	SEG[85]	-2642.5	389.0
99	SEG[86]	-2718.0	389.0
100	SEG[87]	-2793.5	389.0
101	SEG[88]	-2869.0	389.0
102	SEG[89]	-2944.5	389.0
103	SEG[90]	-3020.0	389.0
104	SEG[91]	-3095.5	389.0
105	SEG[92]	-3171.0	389.0
106	SEG[93]	-3246.5	389.0

PAD NO.	PIN Name	X	Y
107	SEG[94]	-3322.0	389.0
108	SEG[95]	-3397.5	389.0
109	SEG[96]	-3473.0	389.0
110	SEG[97]	-3548.5	389.0
111	SEG[98]	-3624.0	389.0
112	SEG[99]	-3699.5	389.0
113	SEG[100]	-3775.0	389.0
114	SEG[101]	-3850.5	389.0
115	COMS1	-3926.0	389.0
116	COM[0]	-4001.5	389.0
117	COM[1]	-4077.0	389.0
118	COM[2]	-4152.5	389.0
119	COM[3]	-4228.0	389.0
120	COM[4]	-4303.5	389.0
121	COM[5]	-4379.0	389.0
122	COM[6]	-4454.5	389.0
123	COM[7]	-4530.0	389.0
124	COM[8]	-4605.5	389.0
125	COM[9]	-4681.0	389.0
126	COM[10]	-4998.5	381.5
127	COM[11]	-4998.5	306.0
128	COM[12]	-4998.5	230.5
129	COM[13]	-4998.5	155.0
130	COM[14]	-4998.5	79.5
131	COM[15]	-4998.5	4.0
132	COM[16]	-4998.5	-71.5
133	COM[17]	-4998.5	-147.0
134	COM[18]	-4998.5	-222.5
135	COM[19]	-4998.5	-298.0
136	COM[20]	-4998.5	-373.5
137	COM[21]	-4694.5	-389.0
138	COM[22]	-4619.0	-389.0
139	COM[23]	-4543.5	-389.0
140	COM[24]	-4468.0	-389.0
141	COM[25]	-4392.5	-389.0
142	COM[26]	-4317.0	-389.0

PAD NO.	PIN Name	X	Y
143	COM[27]	-4241.5	-389.0
144	COM[28]	-4166.0	-389.0
145	COM[29]	-4090.5	-389.0
146	COM[30]	-4015.0	-389.0
147	COM[31]	-3939.5	-389.0
148	Reserve	-3864.0	-389.0
149	T9	-3750.0	-389.0
150	VDD	-3675.0	-389.0
151	VDD	-3600.0	-389.0
152	VDD	-3525.0	-389.0
153	VDD	-3450.0	-389.0
154	VDD	-3375.0	-389.0
155	VDD	-3300.0	-389.0
156	VDD2	-3225.0	-389.0
157	VDD2	-3150.0	-389.0
158	VDD2	-3075.0	-389.0
159	VDD2	-3000.0	-389.0
160	VDD2	-2925.0	-389.0
161	VDD2	-2850.0	-389.0
162	VDD2	-2775.0	-389.0
163	VDD2	-2700.0	-389.0
164	VDD2	-2625.0	-389.0
165	VDD2	-2550.0	-389.0
166	VDD2	-2475.0	-389.0
167	VDD2	-2400.0	-389.0
168	D7	-2325.0	-389.0
169	D7	-2250.0	-389.0
170	D6	-2175.0	-389.0
171	D6	-2100.0	-389.0
172	D5	-2025.0	-389.0
173	D5	-1950.0	-389.0
174	D4	-1875.0	-389.0
175	D4	-1800.0	-389.0
176	D3	-1725.0	-389.0
177	D3	-1650.0	-389.0
178	D2	-1575.0	-389.0

PAD NO.	PIN Name	X	Y
179	D2	-1500.0	-389.0
180	D1	-1425.0	-389.0
181	D1	-1350.0	-389.0
182	D0	-1275.0	-389.0
183	D0	-1200.0	-389.0
184	VDD	-1125.0	-389.0
185	T0	-1050.0	-389.0
186	T1	-975.0	-389.0
187	T2	-900.0	-389.0
188	T3	-825.0	-389.0
189	T4	-750.0	-389.0
190	T5	-675.0	-389.0
191	T6	-600.0	-389.0
192	T7	-525.0	-389.0
193	T8	-450.0	-389.0
194	VRS	-375.0	-389.0
195	ERD	-300.0	-389.0
196	ERD	-225.0	-389.0
197	RWR	-150.0	-389.0
198	RWR	-75.0	-389.0
199	A0	0.0	-389.0
200	A0	75.0	-389.0
201	CS	150.0	-389.0
202	CS	225.0	-389.0
203	IMS	300.0	-389.0
204	VDD	375.0	-389.0
205	PS	450.0	-389.0
206	T11	525.0	-389.0
207	T10	600.0	-389.0
208	VDD	675.0	-389.0
209	OSC	750.0	-389.0
210	OSC	825.0	-389.0
211	V0	900.0	-389.0
212	V0	975.0	-389.0
213	V0	1050.0	-389.0
214	V0	1125.0	-389.0

PAD NO.	PIN Name	X	Y
215	V1	1200.0	-389.0
216	V2	1275.0	-389.0
217	V3	1350.0	-389.0
218	V4	1425.0	-389.0
219	VSS2	1500.0	-389.0
220	VSS2	1575.0	-389.0
221	VSS2	1650.0	-389.0
222	VSS2	1725.0	-389.0
223	VSS2	1800.0	-389.0
224	VSS2	1875.0	-389.0
225	VSS2	1950.0	-389.0
226	VSS2	2025.0	-389.0
227	VSS2	2100.0	-389.0
228	VSS2	2175.0	-389.0
229	VSS2	2250.0	-389.0
230	VSS2	2325.0	-389.0
231	VSS	2400.0	-389.0
232	VSS	2475.0	-389.0
233	VSS	2550.0	-389.0
234	VSS	2625.0	-389.0
235	VSS	2700.0	-389.0
236	VSS	2775.0	-389.0
237	VLCDIN	2850.0	-389.0
238	VLCDIN	2925.0	-389.0
239	VLCDIN	3000.0	-389.0
240	VLCDIN	3075.0	-389.0
241	VLCDIN	3150.0	-389.0
242	VLCDIN	3225.0	-389.0
243	VLCDOUT	3300.0	-389.0

PAD NO.	PIN Name	X	Y
244	VLCDOUT	3375.0	-389.0
245	VLCDOUT	3450.0	-389.0
246	VLCDOUT	3525.0	-389.0
247	VLCDOUT	3600.0	-389.0
248	VLCDOUT	3675.0	-389.0
249	RES	3768.5	-389.0
250	COMS2	3864.5	-389.0
251	COM[64]	3940.0	-389.0
252	COM[63]	4015.5	-389.0
253	COM[62]	4091.0	-389.0
254	COM[61]	4166.5	-389.0
255	COM[60]	4242.0	-389.0
256	COM[59]	4317.5	-389.0
257	COM[58]	4393.0	-389.0
258	COM[57]	4468.5	-389.0
259	COM[56]	4544.0	-389.0
260	COM[55]	4619.5	-389.0
261	COM[54]	4695.0	-389.0
262	COM[53]	4998.5	-373.5
263	COM[52]	4998.5	-298.0
264	COM[51]	4998.5	-222.5
265	COM[50]	4998.5	-147.0
266	COM[49]	4998.5	-71.5
267	COM[48]	4998.5	4.0
268	COM[47]	4998.5	79.5
269	COM[46]	4998.5	155.0
270	COM[45]	4998.5	230.5
271	COM[44]	4998.5	306.0
272	COM[43]	4998.5	381.5

Pad Center Coordinates(REVERSE,MY=1)

PAD NO.	PIN Name	X	Y
1	COM[22]	4681.0	389.0
2	COM[23]	4605.5	389.0
3	COM[24]	4530.0	389.0
4	COM[25]	4454.5	389.0
5	COM[26]	4379.0	389.0
6	COM[27]	4303.5	389.0
7	COM[28]	4228.0	389.0
8	COM[29]	4152.5	389.0
9	COM[30]	4077.0	389.0
10	COM[31]	4001.5	389.0
11	Reserve	3926.0	389.0
12	Reserve	3850.5	389.0
13	SEG[0]	3775.0	389.0
14	SEG[1]	3699.5	389.0
15	SEG[2]	3624.0	389.0
16	SEG[3]	3548.5	389.0
17	SEG[4]	3473.0	389.0
18	SEG[5]	3397.5	389.0
19	SEG[6]	3322.0	389.0
20	SEG[7]	3246.5	389.0
21	SEG[8]	3171.0	389.0
22	SEG[9]	3095.5	389.0
23	SEG[10]	3020.0	389.0
24	SEG[11]	2944.5	389.0
25	SEG[12]	2869.0	389.0
26	SEG[13]	2793.5	389.0
27	SEG[14]	2718.0	389.0
28	SEG[15]	2642.5	389.0
29	SEG[16]	2567.0	389.0
30	SEG[17]	2491.5	389.0
31	SEG[18]	2416.0	389.0
32	SEG[19]	2340.5	389.0
33	SEG[20]	2265.0	389.0
34	SEG[21]	2189.5	389.0
35	SEG[22]	2114.0	389.0

PAD NO.	PIN Name	X	Y
36	SEG[23]	2038.5	389.0
37	SEG[24]	1963.0	389.0
38	SEG[25]	1887.5	389.0
39	SEG[26]	1812.0	389.0
40	SEG[27]	1736.5	389.0
41	SEG[28]	1661.0	389.0
42	SEG[29]	1585.5	389.0
43	SEG[30]	1510.0	389.0
44	SEG[31]	1434.5	389.0
45	SEG[32]	1359.0	389.0
46	SEG[33]	1283.5	389.0
47	SEG[34]	1208.0	389.0
48	SEG[35]	1132.5	389.0
49	SEG[36]	1057.0	389.0
50	SEG[37]	981.5	389.0
51	SEG[38]	906.0	389.0
52	SEG[39]	830.5	389.0
53	SEG[40]	755.0	389.0
54	SEG[41]	679.5	389.0
55	SEG[42]	604.0	389.0
56	SEG[43]	528.5	389.0
57	SEG[44]	453.0	389.0
58	SEG[45]	377.5	389.0
59	SEG[46]	302.0	389.0
60	SEG[47]	226.5	389.0
61	SEG[48]	151.0	389.0
62	SEG[49]	75.5	389.0
63	SEG[50]	0.0	389.0
64	SEG[51]	-75.5	389.0
65	SEG[52]	-151.0	389.0
66	SEG[53]	-226.5	389.0
67	SEG[54]	-302.0	389.0
68	SEG[55]	-377.5	389.0
69	SEG[56]	-453.0	389.0
70	SEG[57]	-528.5	389.0

PAD NO.	PIN Name	X	Y
71	SEG[58]	-604.0	389.0
72	SEG[59]	-679.5	389.0
73	SEG[60]	-755.0	389.0
74	SEG[61]	-830.5	389.0
75	SEG[62]	-906.0	389.0
76	SEG[63]	-981.5	389.0
77	SEG[64]	-1057.0	389.0
78	SEG[65]	-1132.5	389.0
79	SEG[66]	-1208.0	389.0
80	SEG[67]	-1283.5	389.0
81	SEG[68]	-1359.0	389.0
82	SEG[69]	-1434.5	389.0
83	SEG[70]	-1510.0	389.0
84	SEG[71]	-1585.5	389.0
85	SEG[72]	-1661.0	389.0
86	SEG[73]	-1736.5	389.0
87	SEG[74]	-1812.0	389.0
88	SEG[75]	-1887.5	389.0
89	SEG[76]	-1963.0	389.0
90	SEG[77]	-2038.5	389.0
91	SEG[78]	-2114.0	389.0
92	SEG[79]	-2189.5	389.0
93	SEG[80]	-2265.0	389.0
94	SEG[81]	-2340.5	389.0
95	SEG[82]	-2416.0	389.0
96	SEG[83]	-2491.5	389.0
97	SEG[84]	-2567.0	389.0
98	SEG[85]	-2642.5	389.0
99	SEG[86]	-2718.0	389.0
100	SEG[87]	-2793.5	389.0
101	SEG[88]	-2869.0	389.0
102	SEG[89]	-2944.5	389.0
103	SEG[90]	-3020.0	389.0
104	SEG[91]	-3095.5	389.0
105	SEG[92]	-3171.0	389.0
106	SEG[93]	-3246.5	389.0

PAD NO.	PIN Name	X	Y
107	SEG[94]	-3322.0	389.0
108	SEG[95]	-3397.5	389.0
109	SEG[96]	-3473.0	389.0
110	SEG[97]	-3548.5	389.0
111	SEG[98]	-3624.0	389.0
112	SEG[99]	-3699.5	389.0
113	SEG[100]	-3775.0	389.0
114	SEG[101]	-3850.5	389.0
115	COMS1	-3926.0	389.0
116	COM[64]	-4001.5	389.0
117	COM[63]	-4077.0	389.0
118	COM[62]	-4152.5	389.0
119	COM[61]	-4228.0	389.0
120	COM[60]	-4303.5	389.0
121	COM[59]	-4379.0	389.0
122	COM[58]	-4454.5	389.0
123	COM[57]	-4530.0	389.0
124	COM[56]	-4605.5	389.0
125	COM[55]	-4681.0	389.0
126	COM[54]	-4998.5	381.5
127	COM[53]	-4998.5	306.0
128	COM[52]	-4998.5	230.5
129	COM[51]	-4998.5	155.0
130	COM[50]	-4998.5	79.5
131	COM[49]	-4998.5	4.0
132	COM[48]	-4998.5	-71.5
133	COM[47]	-4998.5	-147.0
134	COM[46]	-4998.5	-222.5
135	COM[45]	-4998.5	-298.0
136	COM[44]	-4998.5	-373.5
137	COM[43]	-4694.5	-389.0
138	COM[42]	-4619.0	-389.0
139	COM[41]	-4543.5	-389.0
140	COM[40]	-4468.0	-389.0
141	COM[39]	-4392.5	-389.0
142	COM[38]	-4317.0	-389.0

PAD NO.	PIN Name	X	Y
143	COM[37]	-4241.5	-389.0
144	COM[36]	-4166.0	-389.0
145	COM[35]	-4090.5	-389.0
146	COM[34]	-4015.0	-389.0
147	COM[33]	-3939.5	-389.0
148	COM[32]	-3864.0	-389.0
149	T9	-3750.0	-389.0
150	VDD	-3675.0	-389.0
151	VDD	-3600.0	-389.0
152	VDD	-3525.0	-389.0
153	VDD	-3450.0	-389.0
154	VDD	-3375.0	-389.0
155	VDD	-3300.0	-389.0
156	VDD2	-3225.0	-389.0
157	VDD2	-3150.0	-389.0
158	VDD2	-3075.0	-389.0
159	VDD2	-3000.0	-389.0
160	VDD2	-2925.0	-389.0
161	VDD2	-2850.0	-389.0
162	VDD2	-2775.0	-389.0
163	VDD2	-2700.0	-389.0
164	VDD2	-2625.0	-389.0
165	VDD2	-2550.0	-389.0
166	VDD2	-2475.0	-389.0
167	VDD2	-2400.0	-389.0
168	D7	-2325.0	-389.0
169	D7	-2250.0	-389.0
170	D6	-2175.0	-389.0
171	D6	-2100.0	-389.0
172	D5	-2025.0	-389.0
173	D5	-1950.0	-389.0
174	D4	-1875.0	-389.0
175	D4	-1800.0	-389.0
176	D3	-1725.0	-389.0
177	D3	-1650.0	-389.0
178	D2	-1575.0	-389.0

PAD NO.	PIN Name	X	Y
179	D2	-1500.0	-389.0
180	D1	-1425.0	-389.0
181	D1	-1350.0	-389.0
182	D0	-1275.0	-389.0
183	D0	-1200.0	-389.0
184	VDD	-1125.0	-389.0
185	T0	-1050.0	-389.0
186	T1	-975.0	-389.0
187	T2	-900.0	-389.0
188	T3	-825.0	-389.0
189	T4	-750.0	-389.0
190	T5	-675.0	-389.0
191	T6	-600.0	-389.0
192	T7	-525.0	-389.0
193	T8	-450.0	-389.0
194	VRS	-375.0	-389.0
195	ERD	-300.0	-389.0
196	ERD	-225.0	-389.0
197	RWR	-150.0	-389.0
198	RWR	-75.0	-389.0
199	A0	0.0	-389.0
200	A0	75.0	-389.0
201	CS	150.0	-389.0
202	CS	225.0	-389.0
203	IMS	300.0	-389.0
204	VDD	375.0	-389.0
205	PS	450.0	-389.0
206	T11	525.0	-389.0
207	T10	600.0	-389.0
208	VDD	675.0	-389.0
209	OSC	750.0	-389.0
210	OSC	825.0	-389.0
211	V0	900.0	-389.0
212	V0	975.0	-389.0
213	V0	1050.0	-389.0
214	V0	1125.0	-389.0

PAD NO.	PIN Name	X	Y
215	V1	1200.0	-389.0
216	V2	1275.0	-389.0
217	V3	1350.0	-389.0
218	V4	1425.0	-389.0
219	VSS2	1500.0	-389.0
220	VSS2	1575.0	-389.0
221	VSS2	1650.0	-389.0
222	VSS2	1725.0	-389.0
223	VSS2	1800.0	-389.0
224	VSS2	1875.0	-389.0
225	VSS2	1950.0	-389.0
226	VSS2	2025.0	-389.0
227	VSS2	2100.0	-389.0
228	VSS2	2175.0	-389.0
229	VSS2	2250.0	-389.0
230	VSS2	2325.0	-389.0
231	VSS	2400.0	-389.0
232	VSS	2475.0	-389.0
233	VSS	2550.0	-389.0
234	VSS	2625.0	-389.0
235	VSS	2700.0	-389.0
236	VSS	2775.0	-389.0
237	VLCDIN	2850.0	-389.0
238	VLCDIN	2925.0	-389.0
239	VLCDIN	3000.0	-389.0
240	VLCDIN	3075.0	-389.0
241	VLCDIN	3150.0	-389.0
242	VLCDIN	3225.0	-389.0
243	VLCDOUT	3300.0	-389.0

PAD NO.	PIN Name	X	Y
244	VLCDOUT	3375.0	-389.0
245	VLCDOUT	3450.0	-389.0
246	VLCDOUT	3525.0	-389.0
247	VLCDOUT	3600.0	-389.0
248	VLCDOUT	3675.0	-389.0
249	RES	3768.5	-389.0
250	COMS2	3864.5	-389.0
251	COM[0]	3940.0	-389.0
252	COM[1]	4015.5	-389.0
253	COM[2]	4091.0	-389.0
254	COM[3]	4166.5	-389.0
255	COM[4]	4242.0	-389.0
256	COM[5]	4317.5	-389.0
257	COM[6]	4393.0	-389.0
258	COM[7]	4468.5	-389.0
259	COM[8]	4544.0	-389.0
260	COM[9]	4619.5	-389.0
261	COM[10]	4695.0	-389.0
262	COM[11]	4998.5	-373.5
263	COM[12]	4998.5	-298.0
264	COM[13]	4998.5	-222.5
265	COM[14]	4998.5	-147.0
266	COM[15]	4998.5	-71.5
267	COM[16]	4998.5	4.0
268	COM[17]	4998.5	79.5
269	COM[18]	4998.5	155.0
270	COM[19]	4998.5	230.5
271	COM[20]	4998.5	306.0
272	COM[21]	4998.5	381.5

4. BLOCK DIAGRAM

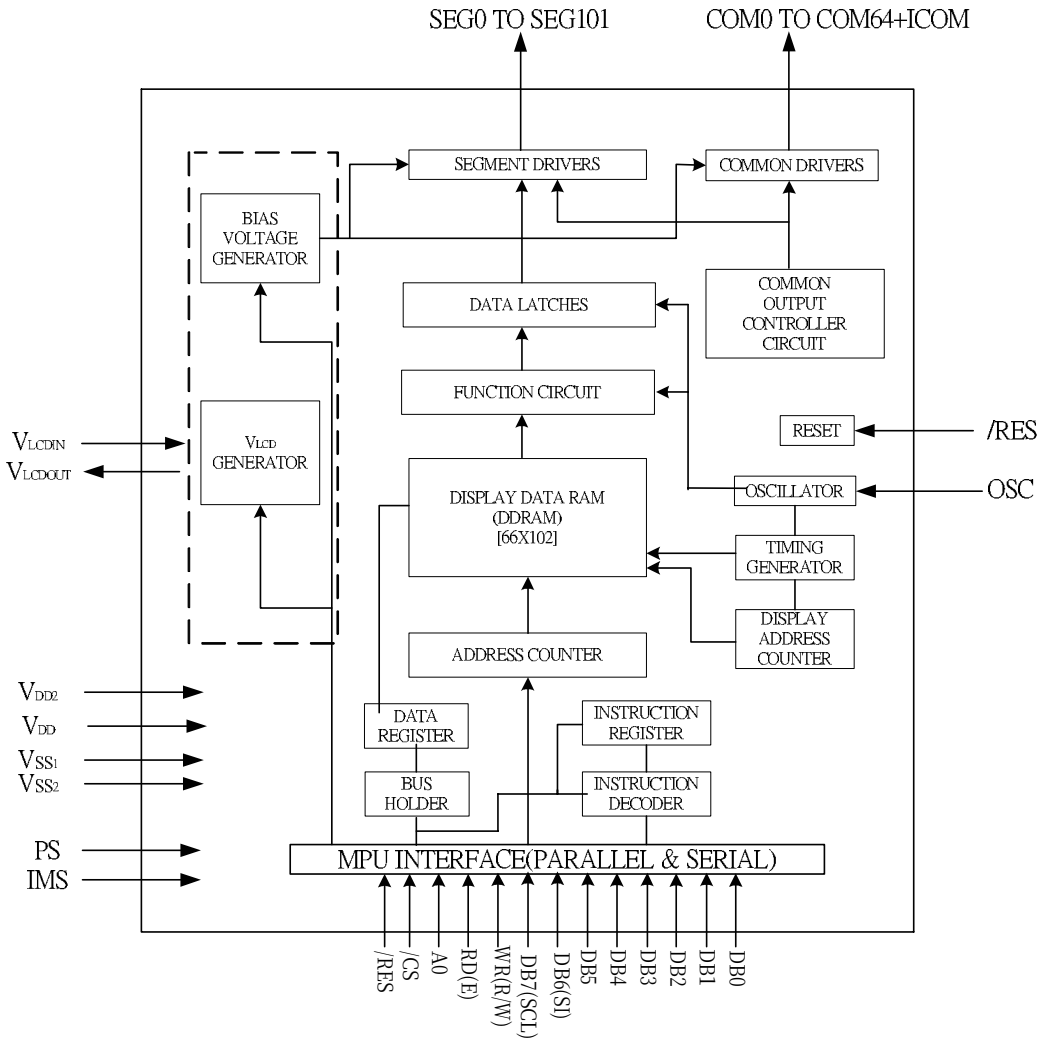


Fig.1 block diagram

5. PINNING DESCRIPTIONS

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td colspan="4">Lcd driver outputs</td></tr>
<tr><td>SEG0 to SEG101</td><td>O</td><td>LCD segment driver outputs
This display data and the M signal control the output voltage of segment driver.
<table>
<tr><td rowspan="2">Display data</td><td rowspan="2">M (Internal)</td><td colspan="2">Segment driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td>VLCD</td><td>V_2</td></tr>
<tr><td>H</td><td>L</td><td>V_{SS}</td><td>V_3</td></tr>
<tr><td>L</td><td>H</td><td>V_2</td><td>VLCD</td></tr>
<tr><td>L</td><td>L</td><td>V_3</td><td>V_{SS}</td></tr>
<tr><td colspan="2">Power save mode</td><td>V_{SS}</td><td>V_{SS}</td></tr>
</table></td><td>102</td></tr>
<tr><td>COM0 to COM64</td><td>O</td><td>LCD column driver outputs
This internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><td rowspan="2">Display data</td><td rowspan="2">M(Internal)</td><td colspan="2">Common driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td colspan="2">V_{SS}</td></tr>
<tr><td>H</td><td>L</td><td colspan="2">VLCD</td></tr>
<tr><td>L</td><td>H</td><td colspan="2">V_1</td></tr>
<tr><td>L</td><td>L</td><td colspan="2">V_4</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">V_{SS}</td></tr>
</table></td><td>65</td></tr>
<tr><td>COMS</td><td>O</td><td>Common output for the icons
The output signals of two pins are same. When not used, this pin should be left open.</td><td>2</td></tr>
<tr><td colspan="4">MICROPROCESSOR INTERFACE</td></tr>
<tr><td>P/S</td><td>I</td><td>Microprocessor interface select input pin

P/S= " H ": parallel data input.
P/S= " L ": serial data input.
When P/S=" L ",D0 to D5 are fixed to " H ".
RD (E) and WR(R/W) are fixed to " H ".</td><td>1</td></tr>
<tr><td>IMS</td><td>I</td><td>Input mode select
<table>
<tr><td>P/S</td><td>IMS</td><td>State</td></tr>
<tr><td>" H "</td><td>" H "</td><td>6800-series parallel MPU interface</td></tr>
<tr><td>" H "</td><td>" L "</td><td>8080-series parallel MPU interface</td></tr>
<tr><td>" L "</td><td>" H "</td><td>4 Pin-SPI MPU interface</td></tr>
<tr><td>" L "</td><td>" L "</td><td>I^2C interface</td></tr>
</table></td><td>1</td></tr>
<tr><td>CSB</td><td>I</td><td>Chip select input pins
Data/instruction I/O is enabled only when CSB is " L ". When chip select is non-active, DB0 to DB7 is high impedance.
When CSB pin in two line interface, this pin should fix to ” H”</td><td>2</td></tr>
<tr><td>RESB</td><td>I</td><td>Reset input pin
When RESET is " L ", initialization is executed.</td><td>1</td></tr>
<tr><td>A0</td><td>I</td><td>It determines whether the data bits are data or a command.
A0=" H ": Indicates that D0 to D7 are display data.
A0=" L ": Indicates that D0 to D7 are control data.
A0 pin in I^2C interface, this pin should fix to ” H”</td><td>2</td></tr>
</table>

<table>
<tr><td>/WR(R/W)</td><td>I</td><td>Read/Write execution control pin
<table>
<tr><th>IMS</th><th>MPU type</th><th>/WR(R/W)</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>R/W</td><td>Read/Write control input pin
R/W=" H ": read
R/W=" L": write</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WR</td><td>Write enable clock input pin
The data on D0 to D7 are latched at the rising edge of the /WR signal</td></tr>
</table>
When in the serial interface must fixed to " H ".</td><td>2</td></tr>
<tr><td>/RD (E)</td><td>I</td><td>Read/Write execution control pin
<table>
<tr><th>IMS</th><th>MPU Type</th><th>/RD (E)</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read/Write control input pin
R/W=" H ": When E is " H ", D0 to D7 are in an output status.
R/W=" L ": The data on D0 to D7 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is " L ", D0 to D7 are in an output status.</td></tr>
</table>
When in the serial interface must fixed to " H ".</td><td>2</td></tr>
<tr><td>D5 to D0
D6 (SI)
D7 (SCL)</td><td rowspan="2">I/O</td><td>When the parallel interface selected (P/S=" H "): 8-bit interface
8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus.
When chip select is not active, D0 to D7 is high impedance.
When the serial interface selected (P/S=" L " & IMS=”H”):4-line
D7: serial input clock (SCL)
D6: serial input data (SI)
D5, D4, D3, D2, D1, D0: must fix to “H”..
When chip select is not active, D0 to D7 is high impedance.</td><td rowspan="2">16</td></tr>
<tr><td>D0 to D1 (SA)
D2 to D3 (SDA_OUT)
D4 to D6 (SDA_IN)
D7 (SCL)</td><td>When the serial interface selected (P/S=" L " & IMS=”L”): I²C
D7: serial clock input (SCL)
D6 , D5 , D4: serial input data (SDA_IN)
D3, D2: (SDA_OUT) serial data acknowledge for the I²C interface. By connecting SDA_OUT to SDA_IN externally, the SDA line becomes fully I²C interface compatible. Having the acknowledge output separated from the serial data line is advantageous in chip on glass (COG) applications. In COG application where the track resistance from the SDA_OUT pad to the system SDA line can be significant, a potential divider is generated by the bus pull-up resistor and the ITO track resistance. It is possible the during the acknowledge cycle the ST7558 will not be able to create a valid logic 0 level. By splitting the SDA_IN input from the SDA_OUT output the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDA_OUT pad to the system SDA line to guarantee a valid low level.
<u>D6, D5, ….D2 must be connected together (SDA)</u>
D1, D0: Is slave address (SA) bit1, 0, must fix to “H” or “L”
Chip select input pins “CSB” not used must fix to “H”</td></tr>
</table>

LCD DRIVER SUPPLY			
OSC	**I**	**When the on-chip oscillator is used, this input must be connected to VDD.** An external clock signal, if used, is connected to this input. If the oscillator and external clock are both inhibited by connecting the OSC pin to VSS the display is not clocked and may be left in a DC state. To avoid this, the chip should always be put into Power Down Mode before stopping the clock.	**2**
Power Supply Pins			
V_{SS1}	**Power Supply**	Digital Ground. The 2 supply rails V_{SS1} and V_{SS2} must be connected together.	**6**
V_{SS2}	**Power Supply**	Analog Ground. The 2 supply rails V_{SS1} and V_{SS2} must be connected together.	**12**
VDD	**Power Supply**	Digital Supply voltage. The 2 supply rails VDD and V_{DD2} could be connected together. If Digital Option pin is high, must be this level	**9**
V_{DD2}	**Power Supply**	Analog Supply voltage. The 2 supply rails VDD and V_{DD2} could be connected together.	**12**
V_{LCDOUT}	**Power Supply**	If the internal voltage generator is used, the V_{LCDIN} & V_{LCDOUT} must be connected together and series one capacitor to VSS2. If an external supply is used this pin must be left open.	**6**
V_{LCDIN}	**Power Supply**	If the internal voltage generator is used, the V_{LCDIN} & V_{LCDOUT} must be connected together. An external supply voltage can be supplied using the V_{LCDIN} pad. This pad is for external multiple voltage input. In this case, VLCDOUT has to be left open,	**6**
V0,V1, V2, V3, V4	**Power Supply**	This is a multi-level power supply for the liquid crystal. $V_{LCDIN} \geq V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq VSS$	**8**
VRS	**Power Supply**	Monitor Voltage Regulator level, must be left open.	**1**
Test Pin			
Test0~Test11	**T**	To test used. Test0~Test8 must floating Test9 could be connected out for monitor the VLCD(V0) voltage Test10 must connect to VSS Test11 must connect to VDD	**11**
Reserve Pin		ALL Reserve Pin must floating	

ST7558 I/O PIN ITO Resister Limitation

PIN Name	ITO Resister
PS,IMS,OSC	**No Limitation**
T1~T8, VRS, V1 , V2 , V3 , V4	**Floating**
VDD, Vdd2, Vss1, Vss2 , Vlcdin , Vlcdout	**<100Ω**
T9,V0	**<500Ω**
A0,/WR,/RD,CSB, D0 …D7(68/80, 4L-SPI interface)	**<1KΩ**
RESB	**<10KΩ**

In IIC interface: SDA , SCL ITO resister recommend to less than 100 ohm

6. FUNCTIONS DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

There is CSB pin for chip selection. The ST7558 can interface with an MPU when CSB is "L". When CSB is “H”, these pins are set to any other combination, A0, /RD(E), and /WR(R/W) inputs are disabled and D0 to D7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel / Serial Interface

ST7558 has four types of interface with an MPU, which are two serial and two parallel interfaces. This parallel or serial interface is determined by P/S pin as shown in table 1.

Table 1. Parallel/Serial Interface Mode

Type	P/S	IMS	CSB	Interface mode
Parallel	H	H	CSB	6800-series MPU interface
		L		8080-series MPU interface
Serial	L	H	CSB	4-pin SPI interface
		L	---	I^2C interface

Parallel Interface (P/S = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by IMS as shown in table 2. The type of data transfer is determined by signals at A0, /RD (E) and /WR(R/W) as shown in table 3.

Table 2. Microprocessor Selection for Parallel Interface

IMS	CSB	A0	/RD (E)	/WR (R/W)	DB0 to DB7	MPU bus
H	CSB	A0	E	R/W	DB0 to DB7	6800-series
L	CSB	A0	/RD	/WR	DB0 to DB7	8080-series

Table 3. Parallel Data Transfer

Common	6800-series		8080-series		Description
RS	E (/RD)	R/W (/WR)	/RD (E)	/WR (R/W)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

NOTE: When /RD (E) pin is always pulled high for 6800-series interface, it can be used CSB for enable signal. In this case, interface data is latched at the rising edge of CSB and the type of data transfer is determined by signals at A0, /WR(R/W) as in case of 6800-series mode.

Serial Interface (P/S=" L ")

Serial Mode	P/S	IMS	CSB	A0	Description
4-line SPI interface	L	H	CSB	Used	Write only
I^2C interface	L	L	Not Used Fix to “H”	Not Used Fix to “H”	Write only

IMS=” L “, P/S=” H “: 4-line SPI interface

When the ST7558 is active (CSB=”L”), serial data (D6) and serial clock (D7) inputs are enabled. And not active, the internal 8-bit shift register and the 3-bit counter are reset. The display data/command indication may be controlled either via software or the Register Select (A0) Pin, based on the setting of P/S. When the A0 pin is used (IMS = “H”), data is display data when A0 is high, and command data when A0 is low. When A0 is not used (IMS = “L”), the LCD Driver will receive command from MCU by default. If messages on the data pin are data rather than command, MCU should send Data direction command to control the data direction and then one more command to define the number of data bytes will be write. After these two continuous commands are sending, the following messages will be data rather than command. Serial data can be read on the rising edge of serial clock going into D7 and processed as 8-bit parallel data on the eighth serial clock. And the DDRAM column address pointer will be increased by one automatically. The next bytes after the display data string are handled as command data.

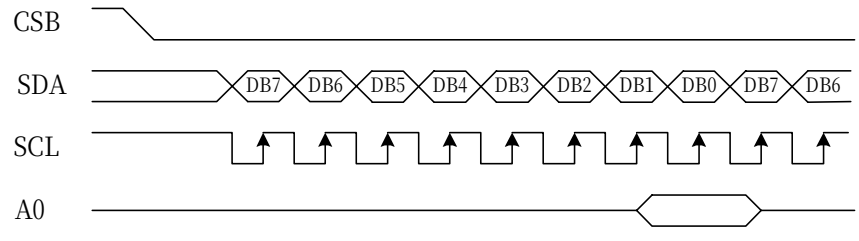


Fig. 2 4-line SPI Timing

IMS=" L ", P/S=" L ": I²C Interface
It could not read Data or Instruction from ST7558 (except Acknowledge signal).

SCL: serial clock input
SDA_IN: serial data input
SDA_OUT: acknowledge response output
Slave address could set from "0111100" to "0111111".

The I²C interface send RAM data and executes the commands sent via the I²C Interface. It could send data in to the RAM. The I²C Interface is two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

BIT TRANSFER
One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Fig.3.

START AND STOP CONDITIONS
Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.4.

SYSTEM CONFIGURATION
The system configuration is illustrated in Fig.5.
· Transmitter: the device, which sends the data to the bus
· Master: the device, which initiates a transfer, generates clock signals and terminates a transfer
· Slave: the device addressed by a master
· Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message
· Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
· Synchronization: procedure to synchronize the clock signals of two or more devices.

ACKNOWLEDGE

Acknowledge signal (ACK) is not BF signal in parallel interface.
Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I²C Interface is illustrated in Fig.6.

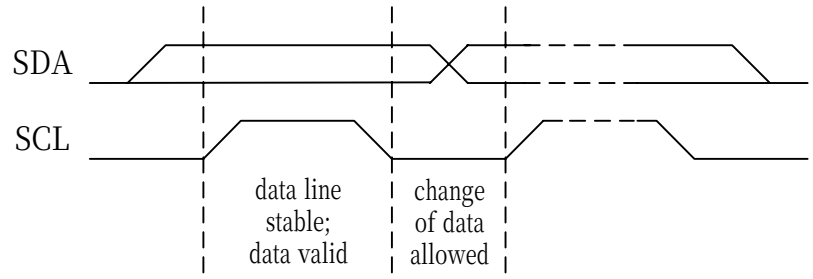


Fig .3 Bit transfer

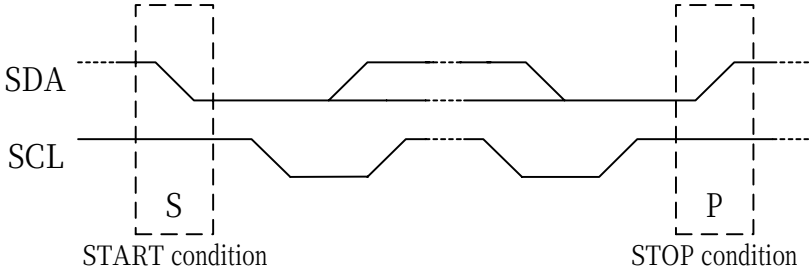


Fig .4 Definition of START and STOP conditions

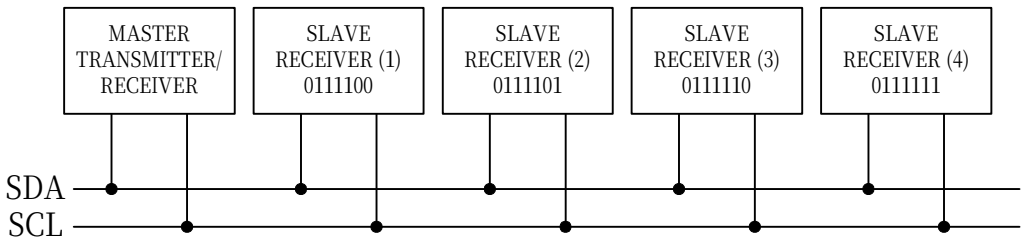


Fig .5 System configuration

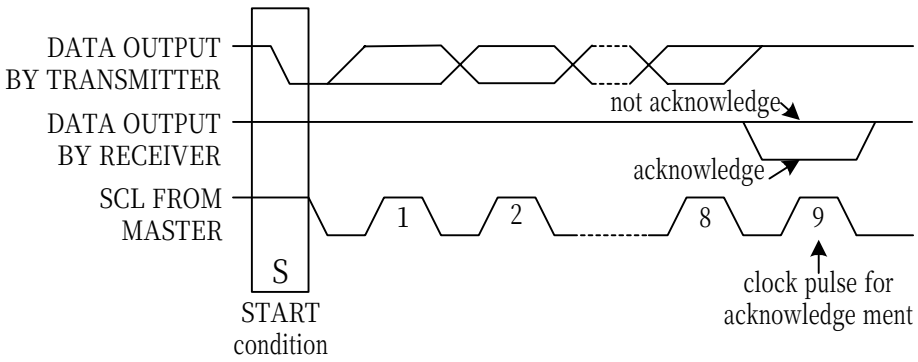


Fig .6 Acknowledgement on the I²C Interface

I²C Interface protocol

The ST7558 supports command, data write addressed slaves on the bus.
Before any data is transmitted on the I²C Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111100 to 0111111) are reserved for the ST7558. The R/W is assigned to 0 for Write only.
The I²C Interface protocol is illustrated in Fig.7.

The sequence is initiated with a START condition (S) from the I²C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.
A command word consists of a control byte, which defines Co and RS, plus a data byte.
The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the RS bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the RS bit setting; either a series of display data bytes or command data bytes may follow. If the RS bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended ST558 device. If the RS bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the I²C INTERFACE-bus master issues a STOP condition (P).If the R/W bit is set to logic 1 the chip will output data immediately after the slave address if the RS bit, which was sent during the last write access, is set to logic 0. If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

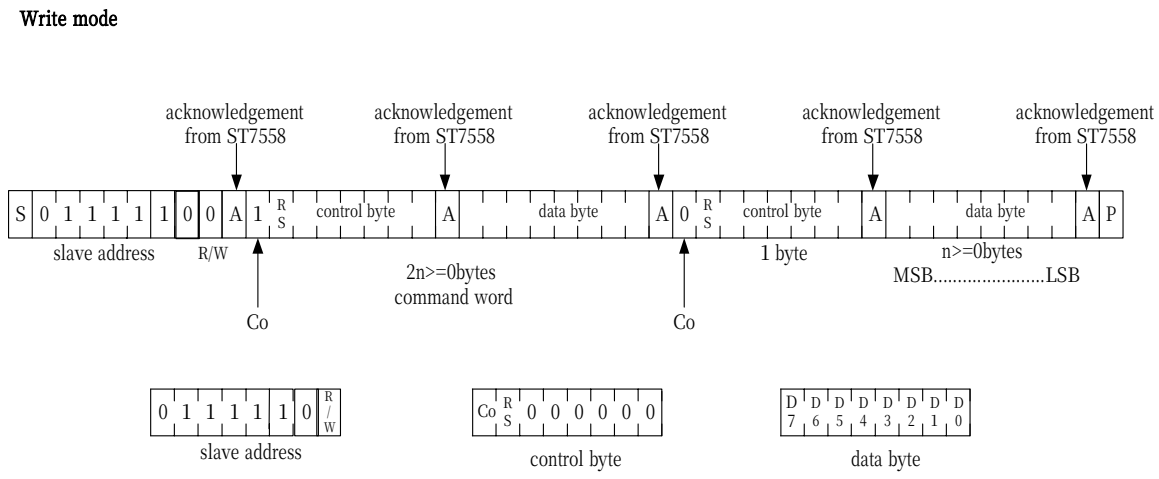


Fig .7 I²C Interface protocol

Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by a STOP condition.

Busy Flag

The Busy Flag indicates whether the ST7558 is operating or not. When D7 is "H" in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

Data Transfer

The ST7558 uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in figure 8. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 9. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

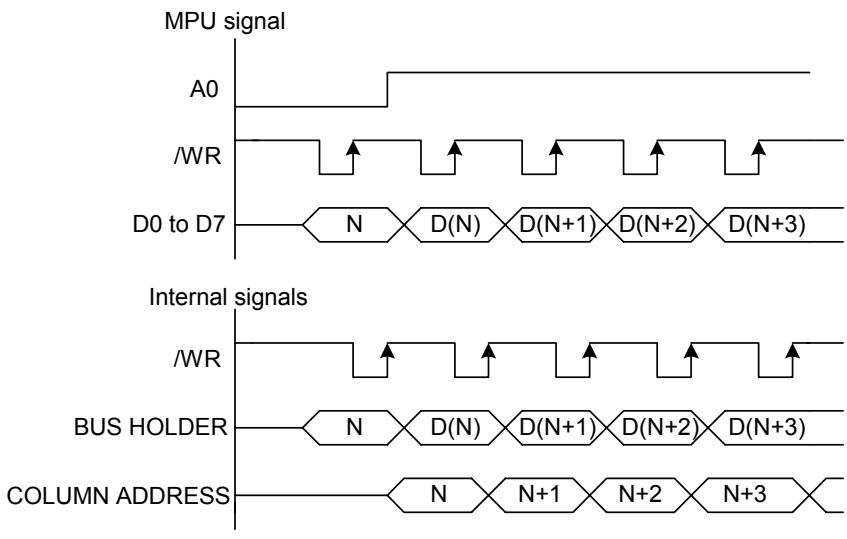


Fig.8 Write Timing

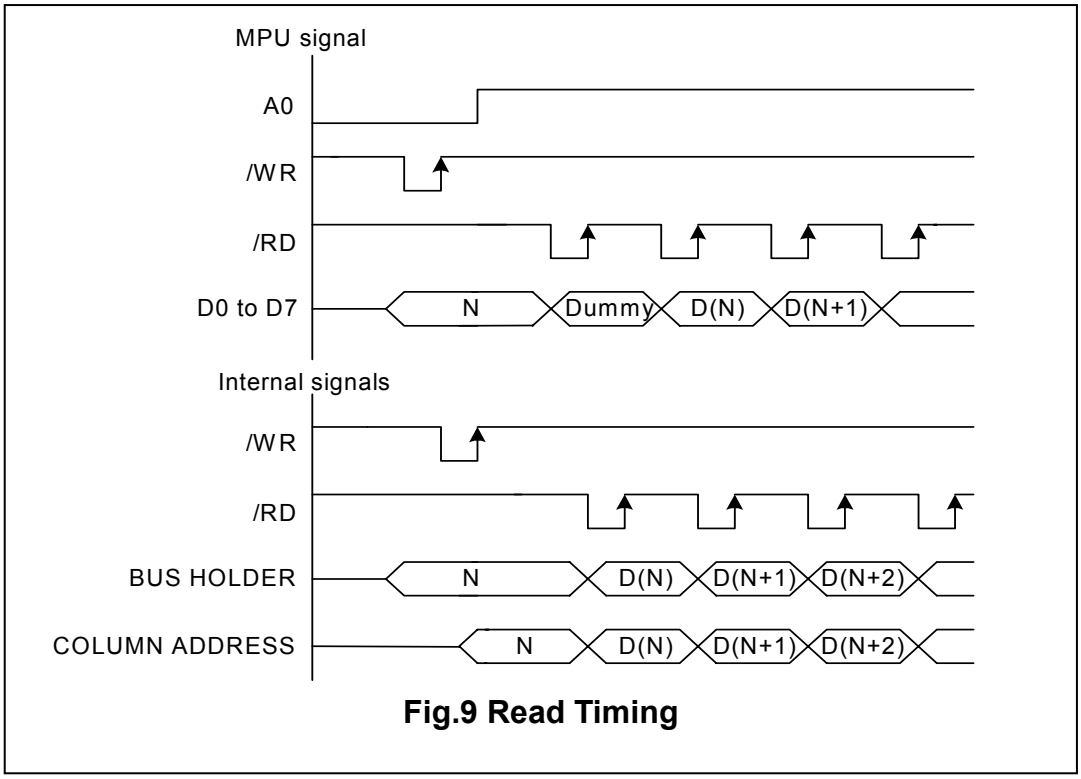


Fig.9 Read Timing

DISPLAY DATA RAM (DDRAM)

The ST7558 contains a 65X102 bit static RAM that stores the display data. The display data RAM store the dot data for the LCD. It has a 65(8 pageX8 +1) X102, and extra ICOM. There is a direct correspondence between X-address and column output number. It is 65-row by 102-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 65 rows are divided into 8 pages of 8 lines and 1 page of 1 line. Data is read from or written to the 8 lines of each page directly through D0 to D7. The display data of D0 to D7 from the microprocessor correspond to the LCD common lines. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM shown in figure 10. It incorporates 4-bit Page Address register changed by only the “Set Page” instruction. Page Address 9 is a special RAM area for the icons and display data D0 is only valid.

Column Address Circuit

Column Address Circuit has an 8-bit preset counter that provides Column Address to the Display Data RAM as shown in figure10. The display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously.

Register MX and MY selection instruction makes it possible to invert the relationship between the Column Address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing MX select instruction.

SEG Output

SEG Output MX	SEG0 SEG101
“0”	seg0 → Segment Address → seg101
“1”	seg101 ← Segment Address ← seg0

Com Output

COM Output MY	Com0 Com64
“0”	com0 → Common Address → com64
“1”	com64 ← Common Address ← com0

ADDRESSING

Data is downloaded in bytes into the RAM matrix of ST7558 as indicated in Figs.10, 11,12. The display RAM has a matrix of 65 by 102 bits. The address pointer addresses the columns. The address ranges are: X 0 to 101 (1100101), Y 0 to 8 (1000). Addresses outside these ranges are not allowed.

In vertical addressing mode (V=1) the Y address increments after each byte (see Fig.11). After the last Y address (Y = 8) Y wraps around to 0 and X increments to address the next column.

In horizontal addressing mode (V=0) the X address increments after each byte (see Fig.12). After the last X address (X = 101) X wraps around to 0 and Y increments to address the next row.

After the very last address (X = 101, Y = 8) the address pointers wrap around to address (X = 0, Y =0)

Data structure

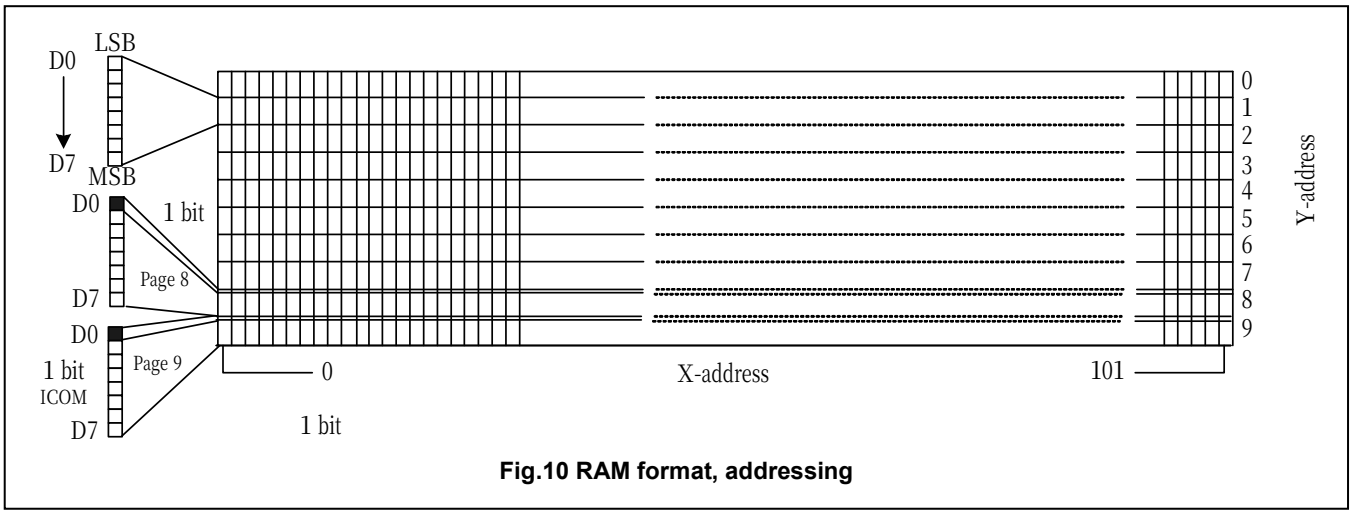


Fig.10 RAM format, addressing

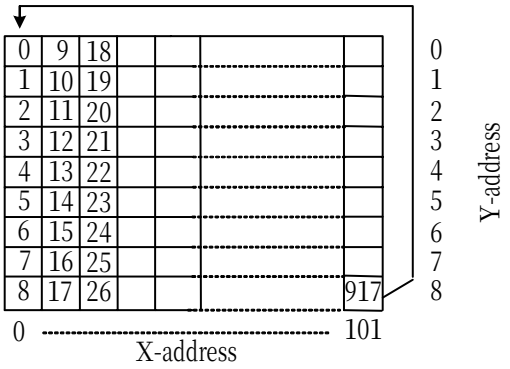


Fig.11 Sequence of writing data bytes into RAM with vertical addressing (V=1)

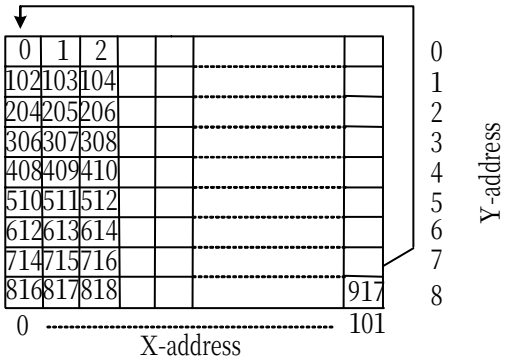


Fig.12 sequence of writing data bytes into RAM with horizontal addressing (V=0)

Page Address D3	D2	D1	D0	Data										Line Address		COM Output
0	0	0	0	D0		■	■	■						00H		COM0
				D1	■				■					01H		COM1
				D2	■									02H		COM2
				D3		■	■	■						03H		COM3
				D4					■					04H		COM4
				D5	■				■					05H		COM5
				D6		■	■	■						06H		COM6
				D7										07H		COM7
0	0	0	1	D0		■	■	■						08H		COM8
				D1			■							09H		COM9
				D2			■							0AH		COM10
				D3			■							0BH		COM11
				D4			■							0CH		COM12
				D5			■							0DH		COM13
				D6		■	■	■						0EH		COM14
				D7										0FH		COM15
0	0	1	0	D0	■	■	■	■	■					10H		COM16
				D1			■							11H		COM17
				D2			■							12H		COM18
				D3			■							13H		COM19
				D4			■							14H		COM20
				D5			■							15H		COM21
				D6			■							16H		COM22
				D7										17H		COM23
0	0	1	1	D0	■	■	■	■						18H		COM24
				D1	■				■					19H		COM25
				D2	■				■					1AH		COM26
				D3	■	■	■	■						1BH		COM27
				D4	■		■							1CH		COM28
				D5	■			■						1DH		COM29
				D6	■				■					1EH		COM30
				D7										1FH		COM31
0	1	0	0	D0		■	■	■						20H		COM32
				D1	■				■					21H		COM33
				D2	■				■					22H		COM34
				D3	■				■					23H		COM35
				D4	■				■					24H		COM36
				D5	■				■					25H		COM37
				D6		■	■	■	■					26H		COM38
				D7										27H		COM39
0	1	0	1	D0	■				■					28H		COM40
				D1	■	■			■					29H		COM41
				D2	■		■		■					2AH		COM42
				D3	■		■		■					2BH		COM43
				D4	■				■					2CH		COM44
				D5	■			■	■					2DH		COM45
				D6	■				■					2EH		COM46
				D7										2FH		COM47
0	1	1	0	D0		■	■	■						30H		COM48
				D1			■							31H		COM49
				D2			■							32H		COM50
				D3			■							33H		COM51
				D4			■							34H		COM52
				D5			■							35H		COM53
				D6		■	■	■						36H		COM54
				D7										37H		COM55
0	1	1	1	D0	■				■					38H		COM56
				D1	■				■					39H		COM57
				D2		■		■						3AH		COM58
				D3			■							3BH		COM59
				D4		■		■						3CH		COM60
				D5	■				■					3DH		COM61
				D6	■				■					3EH		COM62
				D7										3FH		COM63
1	0	0	0	D0										40H		COM64
1	0	0	1	D0										43H		ICON(COMS)

	00	01	02	03	04	05	06	07	08		5D	5E	5F	60	61	62	63	64	65
	65	64	63	62	61	60	5F	5E	5D		08	07	06	05	04	03	02	01	00
LCD Out	S0	S1	S2	S3	S4	S5	S6	S7	S8		S93	S94	S95	S96	S97	S98	S99	S100	S101

0	D0	MX	Column address
1	D0		

Display Data RAM Map (65 Duty + ICOM)

Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC input must be connected to VDD. An external clock signal, if used, is connected to this input.

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL (internal), generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 102-bit display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M) which enables the LCD driver to make a AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. Driving waveform and internal timing signal are shown in Figure 13.

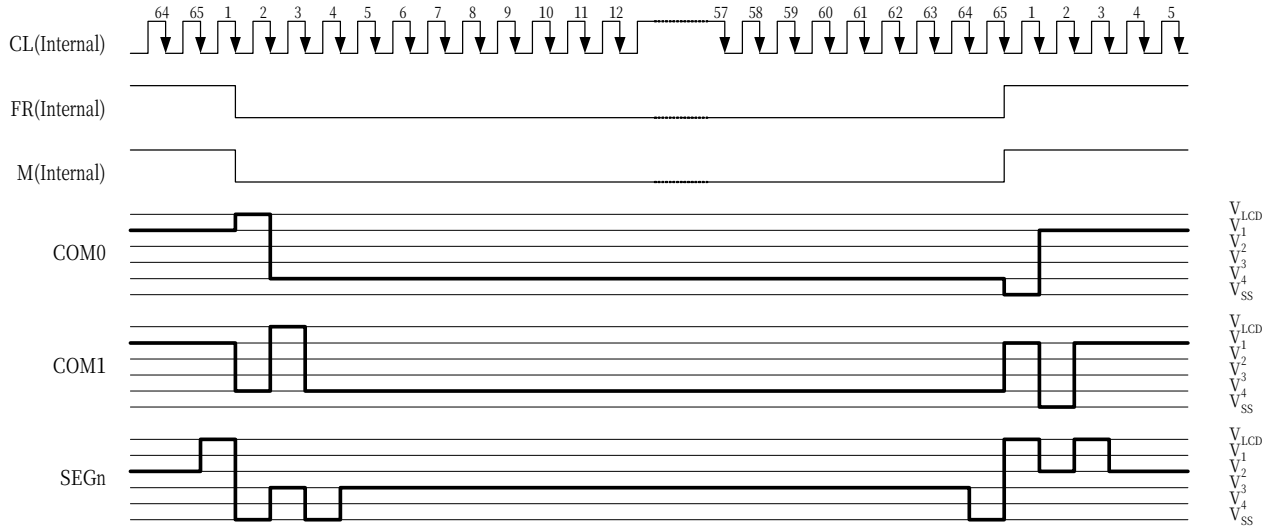


Fig.13 2-frame AC Driving Waveform (Duty Ratio: 1/65)

LCD DRIVER CIRCUIT

65-channel common drivers and 102-channel segment drivers configure this driver circuit. This LCD panel driver voltage depends on the combination of display data and M signal.

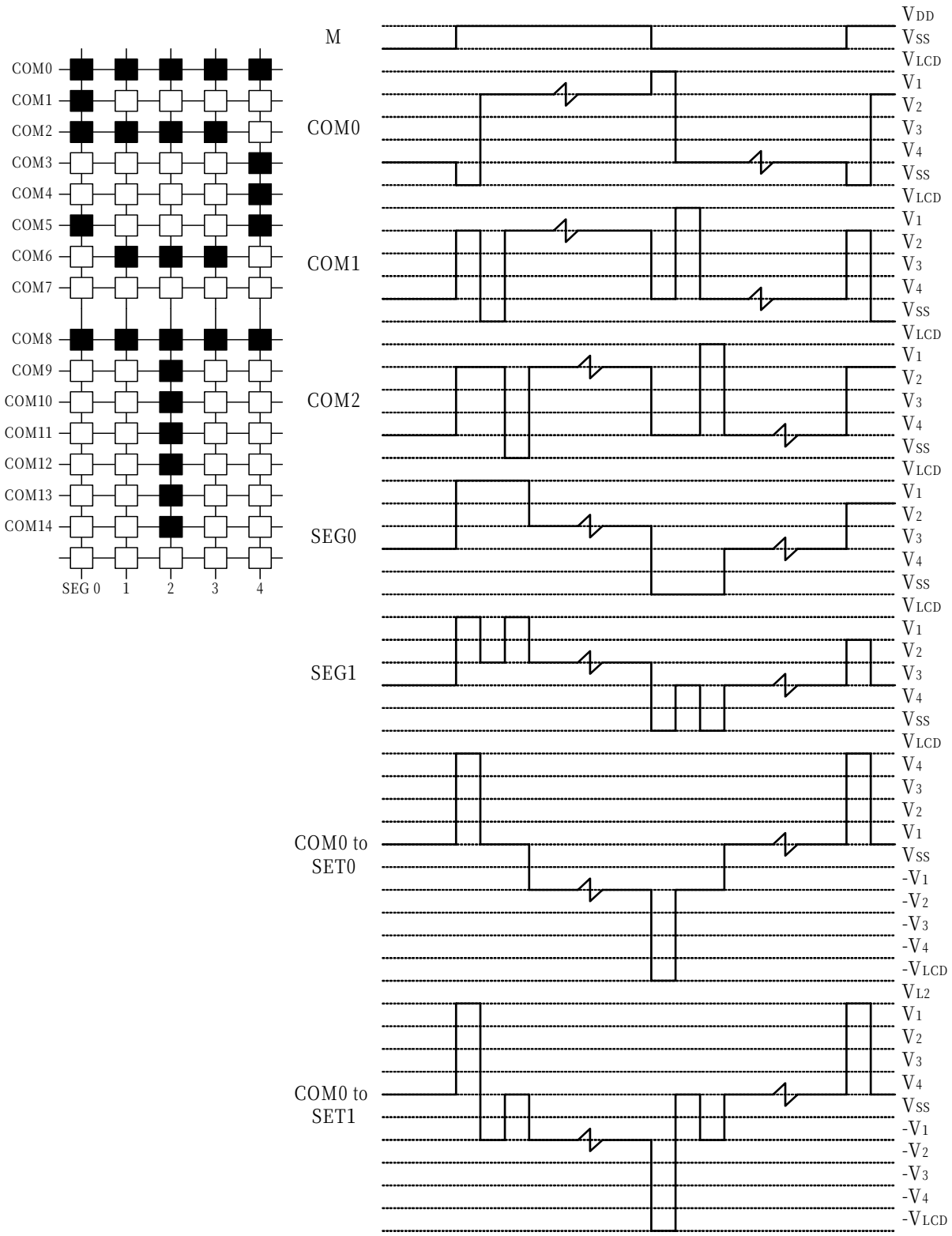


Fig.15 Typical LCD driver waveforms

7. RESET CIRCUIT

Setting RESB to “L” or Reset instruction can initialize internal function.
When RESB becomes “L”, following procedure is executed
Page address: 0
Column address: 0
COM Scan Direction MY: 0
SEG Select Direction MX: 0
Oscillator: OFF
Power down mode (PD = 1)
Horizontal addressing (V = 0)
normal instruction set (H = 0)
Display OFF (D = E = 0)
Address counter X [6:0] = 0, Y [2:0] = 0
Bias system (BS [2:0] = 0)
VLCD is equal to 0; the HV generator is switched off (VOP [6:0] = 0)
After power-on, RAM data are undefined

While RESB is “L” or reset instruction is executed, no instruction except read status can be accepted. Reset status appears at DB6. After DB6 becomes ”L”, any instruction can be accepted. RESB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESB is essential before used.

8. INSTRUCTION TABLE

INSTRUCTION	A0	WR (R/W)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
H=0 or 1											
NOP	0	0	0	0	0	0	0	0	0	0	No operation
Reset	0	0	0	0	0	0	0	0	1	1	Internal reset
Function set	0	0	0	0	1	0	0	PD	V	H	Power-down; entry mode; Extended instruction control
Ext. display control	0	0	0	0	1	0	1	MX	MY	0	Mirror X, Mirror Y
Read status byte	0	1	PD	RST	BUSY	D	E	1	0	1	Read status byte
Read data	1	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Read data from RAM
Write data	1	0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Write data to RAM

INSTRUCTION	A0	WR (R/W)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
H=0											
Set V_{LCD} range	0	0	0	0	0	1	0	0	0	PRS	V_{LCD} range L/H select
Display control	0	0	0	0	0	0	1	D	0	E	Set display configuration
Set Y address of RAM	0	0	0	1	0	0	Y_3	Y_2	Y_1	Y_0	Sets Y address of RAM $0 \leqq Y \leqq 9$
Set X address of RAM	0	0	1	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Sets X address of RAM $0 \leqq X \leqq 101$
Loading Control	0	0	0 0	0 0	0 0	0 0	1 1	1 0	1 0	1 1	Loading Control
H=1											
Booster stages	0	0	0	0	0	0	1	0	PC_1	PC_0	booster voltage multiplication
S/W Internal register initial	0 0	0 0	0 0	0 0	0 0	0 1	1 0	1 0	1 1	0 0	S/W Internal register initial
Bias system	0	0	0	0	0	1	0	BS_2	BS_1	BS_0	Sets bias system (BSx)
Reserved	0	0	0	1	X	X	X	X	X	X	Do not use
Set V_{OP}	0	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}	Write V_{OP} to register

9. INSTRUCTION DESCRIPTION

H="0" or "1"

Reset

This instruction resets initial display line, column address, page address, and common output status select to their initial status. This instruction cannot initialize the LCD power supply, which is initialized by the RESB pin.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	1	1

!!!caution: this instruction cannot be used when using I^2C interface

Function Set

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	PD	V	H

Flag	Description
PD	All LCD outputs at VSS (display off), bias generator and VLCD generator off, VLCD can be disconnected, oscillator off (external clock possible), RAM contents not cleared; RAM data can be written. PD=0:chip is active PD=1:chip is in power down mode
V	When V = 0, the horizontal addressing is selected. The data is written into the DDRAM as shown in Fig13. When V = 1, the vertical addressing is selected. The data is written into the DDRAM as shown in Fig12
H	When H = 0 the commands ' display control ', ' set Y address ' and ' set X address ' can be performed, when H = 1 the others can be executed. The commands ' write data ' and ' function set ' can be executed in both cases. H=0:use basic instruction set H=1:use extended instruction set

Ext. display control

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	MX	MY	0

Flag	Description
MX	SEG bi-direction selection MX=0:normal direction (SEG0→SEG101) MX=1:reverse direction (SEG101→SEG0)
MY	COM bi-direction selection See Pad Center Coordinates at page 3~10 when using this register

!!!Caution:the common output pad should be care.

The normal direction of common and reverse direction of common have different pad location, only one can be used. On the other hand, you must choose one kind, NORMAL or REVERSE, and these two have different ITO layout. Moreover, using the NORMAL layout, must set MY=0; using the REVERSE layout ,must set MY=1.

PS. The NORMAL and REVERSE pad location table are at page3 ~ page10

Read status byte

Indicates the internal status of the ST7558

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	PD	RST	BUSY	D	E	1	0	1

Flag	Description		
PD	PD=0:chip is active PD=1:chip is in power down mode		
RST	Indicates the initialization is in progress by RESET signal 0: chip is active,1:chip is being reset		
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes LOW. 0:chip is active 1:chip is being busy		
D,E	D	E	The bits D and E select the display mode.
	0	0	Display blank
	0	1	All display segments on
	1	0	Normal mode
	1	1	Inverse video mode
D2~D0	ST7558 will return the fix data “101” as identification bit		

Write data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	Write data							

H=”0”

Set V_{LCD} range

V_{LCD} range L/H select

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	0	0	PRS

PRS=0:VLCD programming range LOW

PRS=1: VLCD programming range HIGH

Display Control

This bits D and E selects the display mode.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	D	0	E

Flag	Description		
D,E	D	E	The bits D and E select the display mode.
	0	0	Display off
	1	0	Normal display
	0	1	All display segments on
	1	1	Inverse video mode

Set Y address of RAM

Y [3:0] defines the Y address vector address of the display RAM.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	Y_3	Y_2	Y_1	Y_0

X/Y Address range

Y_3	Y_2	Y_1	Y_0	CONTENT	ALLOWED X-RANGE
0	0	0	0	Page0 (display RAM)	0 to 101
0	0	0	1	Page1 (display RAM)	0 to 101
0	0	1	0	Page2 (display RAM)	0 to 101
0	0	1	1	Page3 (display RAM)	0 to 101
0	1	0	0	Page4 (display RAM)	0 to 101
0	1	0	1	Page5 (display RAM)	0 to 101
0	1	1	0	Page6 (display RAM)	0 to 101
0	1	1	1	Page7 (display RAM)	0 to 101
1	0	0	0	Page8 (display RAM)	0 to 101
1	0	0	1	Page9 (display RAM)	0 to 101

Set X address of RAM

The X address points to the columns. The range of X is 0…101.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	X_6	X_5	X_4	X_3	X_2	X_1	X_0

X_6	X_5	X_4	X_3	X_2	X_1	X_0	Column address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:
1	1	0	0	0	1	0	98
1	1	0	0	0	1	1	99
1	1	0	0	1	0	0	100
1	1	0	0	1	0	1	101

Set Loading Control

Improve Out Put Driving in Heavy Loading

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	1	1	1
0	0	0	0	0	0	1	0	0	1

H="1"

Booster stages

The ST7558 incorporates a software configurable voltage multiplier. After reset (RESB), the default voltage multiplier is set to 2*VDD2. Other voltage multiplier factors are set via the command "Set Booster stages".

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	0	PC_1	PC_0

Flag	Description		
	PC_1	PC_0	
PC_1, PC0	0	0	2*voltage multiplier
	0	1	3*voltage multiplier
	1	0	4*voltage multiplier
	1	1	5*voltage multiplier

S/W initial Internal register

The 1st Instruction

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	1	1	0

The 2nd Instruction

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	0	1	0

System Bias

Select LCD bias ratio of the voltage required for driving the LCD.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	BS_2	BS_1	BS_0

BS_2	BS_1	BS_0	Bias	Recommend Duty
0	0	0	11	1:100
0	0	1	10	1:80
0	1	0	9	1:65/1:68
0	1	1	8	1:48
1	0	0	7	1/40:1/34
1	0	1	6	1/24
1	1	0	5	1:18/1:16
1	1	1	4	1:10/1:9/1:8

LCD bias voltage

Symbol	Bias voltage for 1/8 bias	Symbol	Bias voltage for 1/8 bias
VLCDIN	VLCDIN	V3	2/8 X VLCDIN
V1	7/8 X VLCDIN	V4	1/8 X VLCDIN
V2	6/8 X VLCDIN	VSS	VSS

Set VOP value:

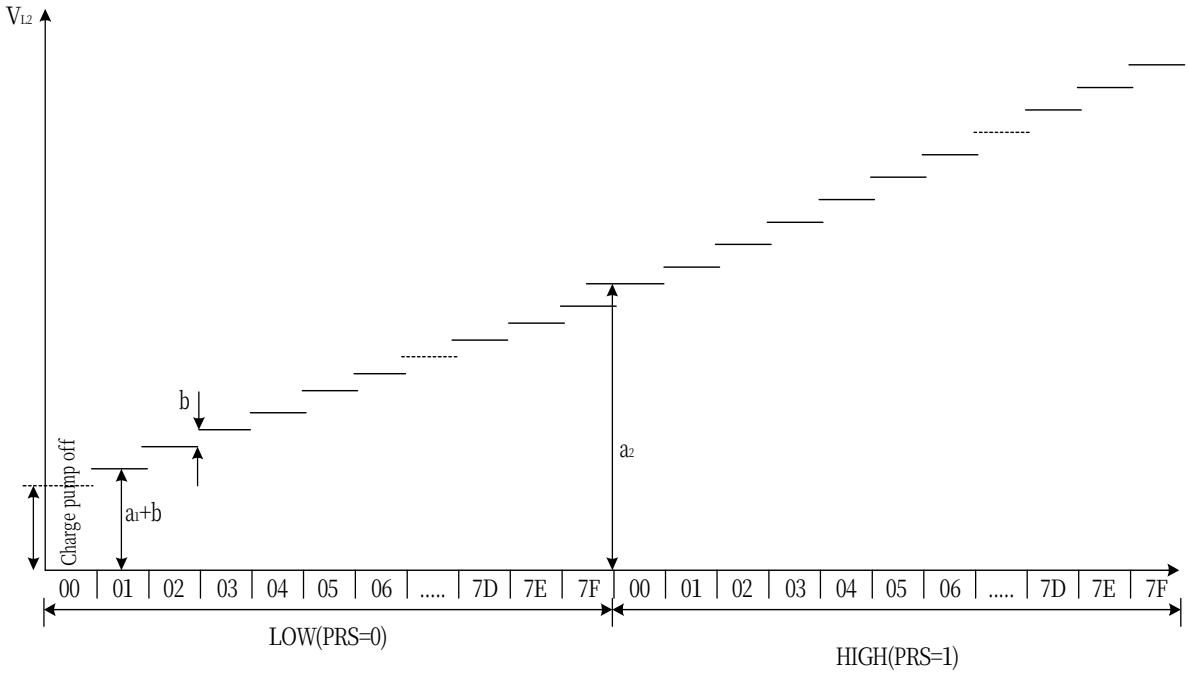
The operation voltage V_{LCD} can be set by software.

$$V_0=(a + V_{OP} X b) \quad (1)$$

The parameters are explained in table 4.The maximum voltage that can be generated is depending on the VDD voltage and the display load current. Two overlapping VLCD ranges are selectable via the command “Booster control”. For the LOW (PS=0) range a=a1 and for the HIGH (PRS=1) range a=a2 with steps equal to “b” in both ranges. Note that the charge pump is turned off if VOP [6;0] and the bit PRS are all set to zero.

Table 4 Typical values for parameter for the HV-Generator programming

SYMBOL	VALUE	UNIT
a1	2.94(PRS=0)	V
a2	6.75(PRS=1)	V
b	0.03	V



VOP [6:0](programmed) {00 hex… 7F hex}

Fig.19 V_{OP} programming of ST7558

Caution

As the programming range for the internally generated VLCDIN allows values above the max allowed VLCDIN, the customer has to ensure while setting the VOP register that under all condition and including all tolerances the VLCD limit of max. 13V will never be exceeded. As VLCDIN increases with lower temperatures, care must be taken not to set a Vop generating a VLCDIN voltage that will exceed the maximum of 10.6V when operating at –40 ℃.

10. COMMAND DESCRIPTION

Referential Instruction Setup Flow: Initializing with the built-in Power Supply Circuits

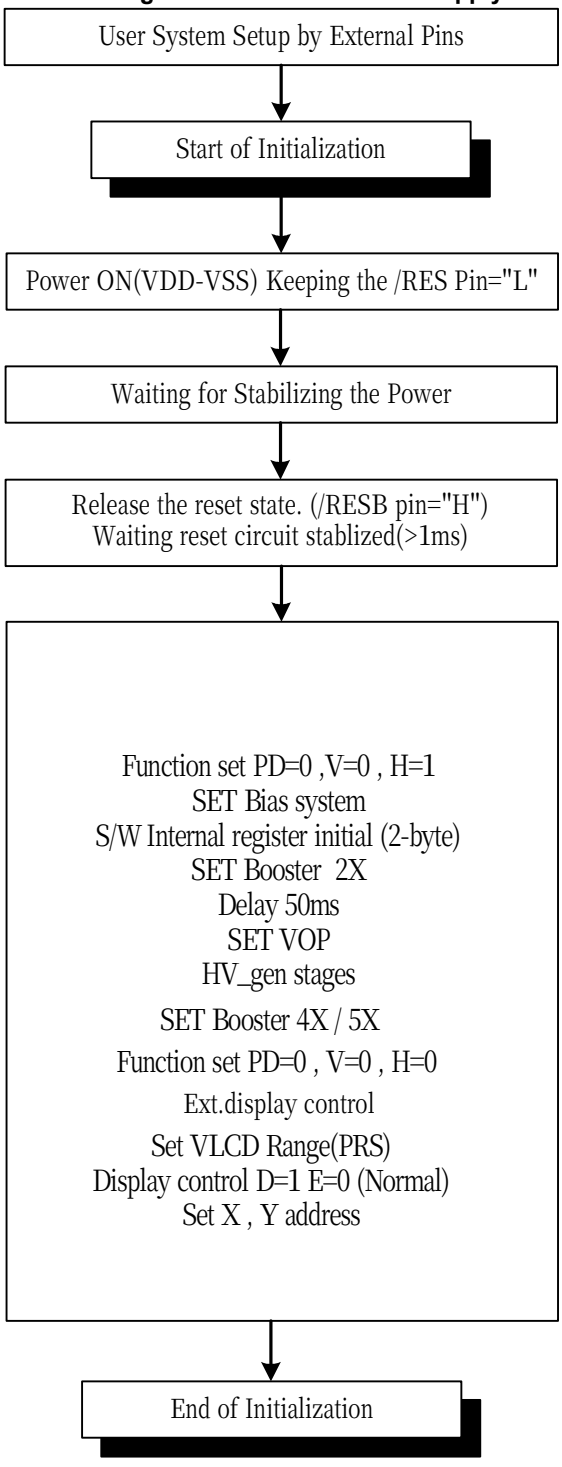


Fig.20 Initializing with the Built-in Power Supply Circuits

Referential Instruction Setup Flow: Initializing without the built-in Power Supply Circuits

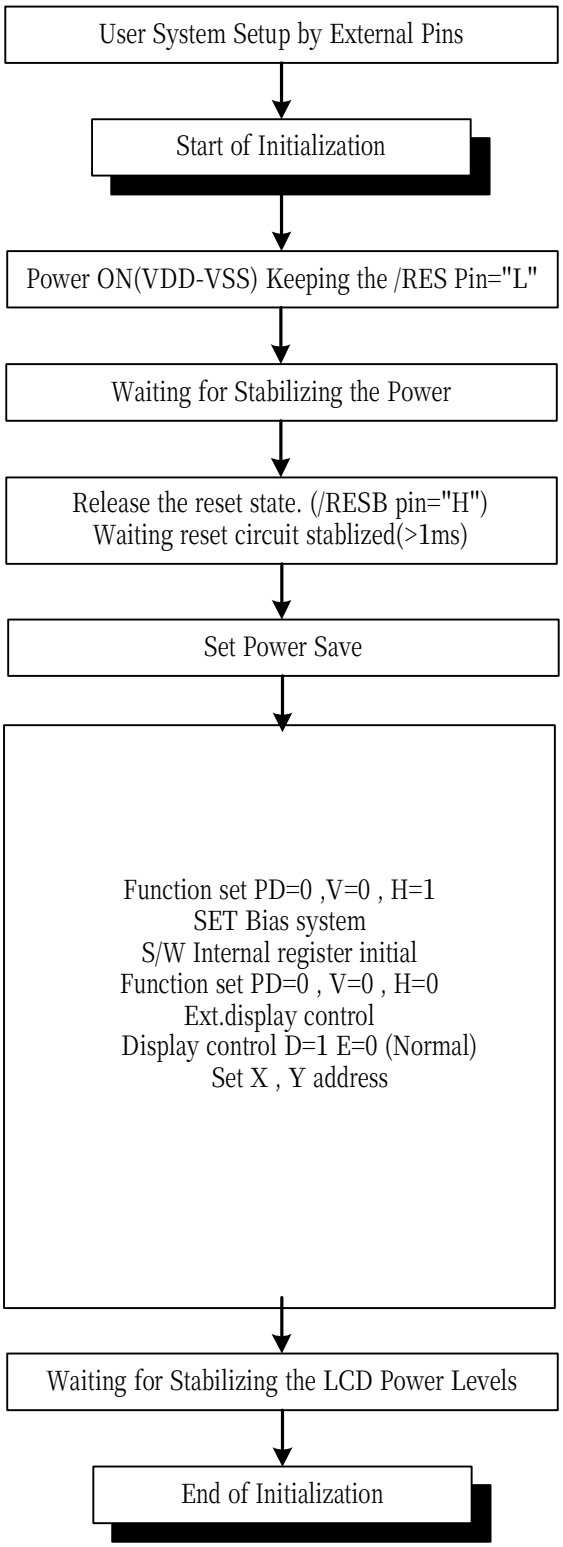


Fig.21 Initializing without Built-in Power Supply Circuits

Referential Instruction Setup Flow: Data Displaying

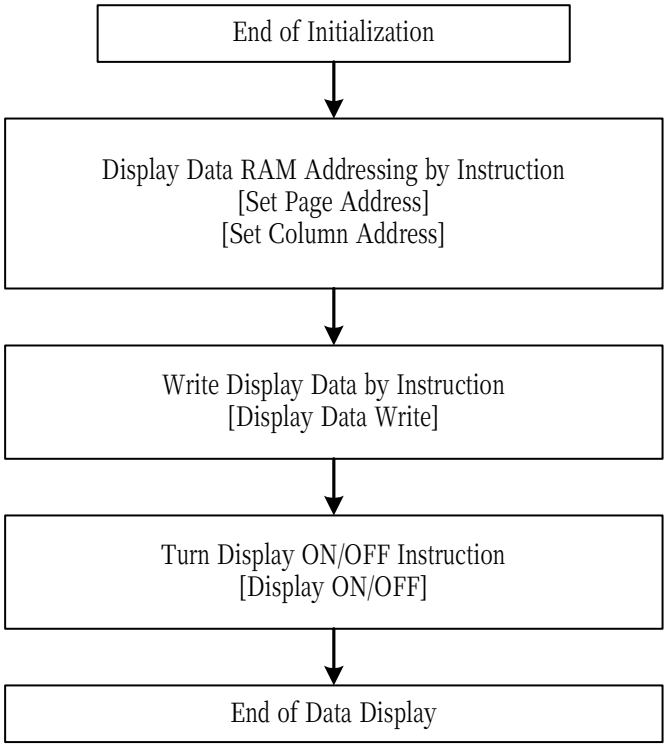


Fig.22 Data Displaying

Referential Instruction Setup Flow: Power OFF

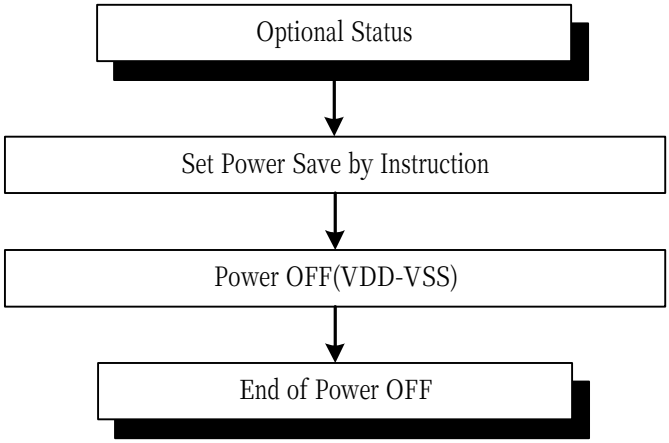
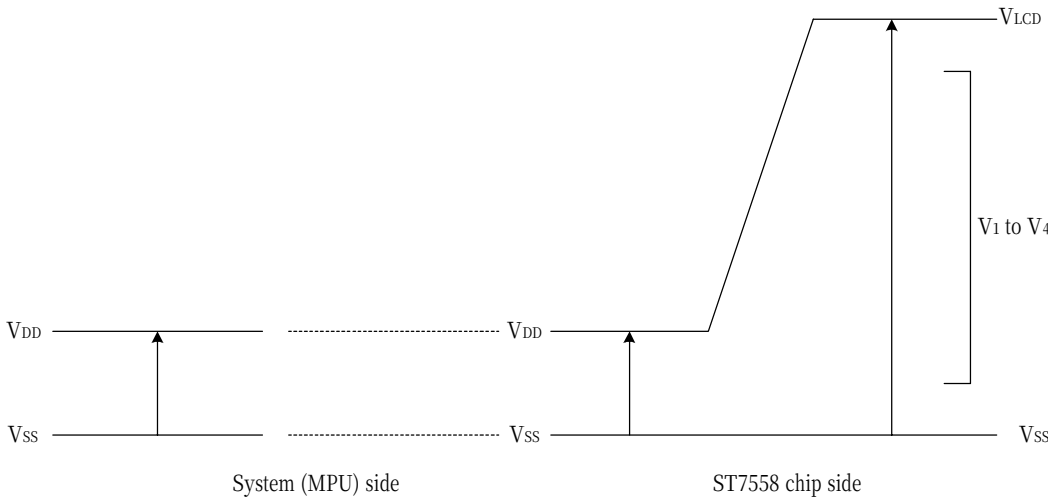


Fig.23 Power OFF

11. LIMITING VALUES

In accordance with the Absolute Maximum Rating System; see notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Power Supply Voltage	VDD	–0.5 ~ +5.0	V
Power supply voltage	V0	3.0 ~ 12	V
Power supply voltage	VLCDIN	–0.3 ~ +13.5	V
Power supply voltage	V1, V2, V3, V4	0.3 to VLCDIN	V
Input voltage	VIN	–0.5 to VDD+0.5	V
Output voltage	VO	–0.5 to VDD+0.5	V
Operating temperature	TOPR	–30 to +85	°C
Storage temperature	TSTR	–65 to +150	°C



Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
3. Insure that the voltage levels of V1, V2, V3, and V4 are always such that

   Vout ≧ V0 ≧ V1 ≧ V2 ≧ V3 ≧ V4 ≧ Vss

12. DC CHARACTERISTICS

V_{DD} = 1.8 V to 3.3V; V_{SS} = 0 V; V_{LCD} = 3.0 to 13.0V; T_{amb} = -30℃ to +85℃; unless otherwise specified.

Item		Symbol	Condition		Rating			Units	Applicable Pin
					Min.	Typ.	Max.		
Operating Voltage (1)		VDD			1.8	—	3.3	V	Vss*1
Operating Voltage (2)		VDD2	(Relative to VSS)		1.8	—	3.3	V	VSS2
High-level Input Voltage		VIHC			0.7 x VDD	—	VDD	V	*2
Low-level Input Voltage		VILC			VSS	—	0.3 x VDD	V	*2
High-level Output Voltage		VOHC			0.7 x VDD	—	VDD	V	*3
Low-level Output Voltage		VOLC			VSS	—	0.3 x VDD	V	*3
Input leakage current		ILI	VIN = VDD or VSS		–1.0	—	1.0	μA	*4
Output leakage current		ILO	VIN = VDD or VSS		–3.0	—	3.0	μA	*5
Liquid Crystal Driver ON Resistance		RON	Ta = 25°C (Relative To VSS)	VLCDIN = 13.0 V	—	2.0	3.5	KΩ	SEGn COMn *6
				VLCDIN = 8.0 V	—	3.2	5.4		
Oscillator Frequency	Internal Oscillator	fOSC	1/65 duty Ta = 25°C		—	80	84	kHz	*7
	External Input	fCL			—	80	84	kHz	OSC
	Frame frequency	fFRAME			—	77	80.3	Hz	

Item		Symbol	Condition	Rating			Units	Applicable Pin
				Min.	Typ.	Max.		
Internal Power	Input voltage	VDD	(Relative To VSS)	1.8	—	3.3	V	
	Supply Step-up output voltage Circuit	VLCDOUT	(Relative To VSS)	—	—	13.5	V	VLCDOUT
	Voltage regulator Circuit Operating Voltage	VLCDIN	(Relative To VSS)	—	—	13.5	V	VLCDIN

Bare Dice Consumption Current : During Display, with the Internal Power Supply, Current consumed by total ICs when an external power supply(VDD,VDD2) is used .

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern SNOW	ISS	VDD,VDD2 = 3.0 V, V0 – VSS = 9.0 V 4X Booster 1/9 Bias	—	300	400	μA	*8
Power Down	ISS	VDD=3.0V Ta = 25°C	—	0.01	2	μA	

Notes to the DC characteristics

1. The maximum possible V_{LCD} voltage that may be generated is dependent on voltage, temperature and (display) load.
2. Internal clock
3. Power-down mode. During power down all static currents are switched off.
4. If external V_{LCDIN}, the display load current is not transmitted to I_{DD}.
5. V_{OUT} external voltage applied to VLCDIN pin; VLCDIN disconnected from VLCDOUT (no connect)

References for items market with *

*1 While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.

*2 The A0, D0 to D5, D6 (SI), D7 (SCL), /RD (E), /WR ,/(R/W), CSB, IMS, OSC, P/S, /DOF, RESB ,and MODE terminals.

*3 The D0 to D7, and OSC terminals.

*4 The A0,/RD (E), /WR ,/(R/W), CSB, IMS, OSC, P/S, /DOF, RESB ,and MODE terminals.

*5 Applies when the D0 to D5, D6 (SI), D7 (SCL) terminals are in a high impedance state.

*6 These are the resistance values for when a 0.1 V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V1, V2, V3, and V4). These are specified for the operating voltage range.
RON = 0.1 V /ΔI (Where ΔI is the current that flows when 0.1 V is applied while the power supply is ON.)

*7 The relationship between the oscillator frequency and the frame rate frequency.

*8,9It indicates the current consumed on ICs alone when the internal oscillator circuit and display are turned on.

13. TIMING CHARACTERISTICS

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

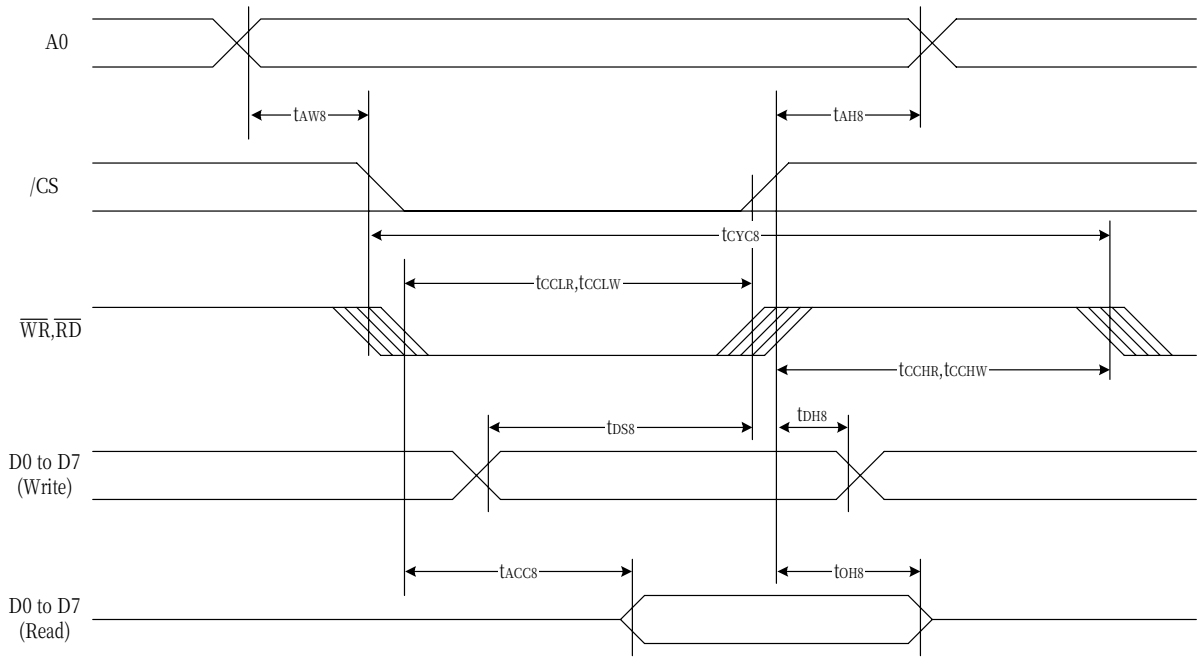


Fig 24.

(VDD = 3.3V , Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		10	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		240	—	
Enable L pulse width (WRITE)	WR	tCCLW		80	—	
Enable H pulse width (WRITE)		tCCHW		80	—	
Enable L pulse width (READ)	RD	tCCLR		140	—	
Enable H pulse width (READ)		tCCHR		80		
WRITE Data setup time	D0 to D7	tDS8		40	—	
WRITE Address hold time		tDH8		0	—	
READ access time		tACC8	CL = 100 pF	—	70	
READ Output disable time		tOH8	CL = 100 pF	5	50	

(VDD = 2.7 V , Ta = -30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		15	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		400	—	
Enable L pulse width (WRITE)	WR	tCCLW		220	—	
Enable H pulse width (WRITE)		tCCHW		180	—	
Enable L pulse width (READ)	RD	tCCLR		220	—	
Enable H pulse width (READ)		tCCHR		180	—	
WRITE Data setup time	D0 to D7	tDS8		40	—	
WRITE Address hold time		tDH8		0	—	
READ access time		tACC8	CL = 100 pF	—	140	
READ Output disable time		tOH8	CL = 100 pF	10	100	

(VDD = 1.8V , Ta = -30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		30	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		640	—	
Enable L pulse width (WRITE)	WR	tCCLW		360	—	
Enable H pulse width (WRITE)		tCCHW		280	—	
Enable L pulse width (READ)	RD	tCCLR		360	—	
Enable H pulse width (READ)		tCCHR		280		
WRITE Data setup time	D0 to D7	tDS8		80	—	
WRITE Address hold time		tDH8		30	—	
READ access time		tACC8	CL = 100 pF	—	240	
READ Output disable time		tOH8	CL = 100 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) $\leqq$ (tCYC8 – tCCLW – tCCHW) for (tr + tf) $\leqq$ (tCYC8 – tCCLR – tCCHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tCCLW and tCCLR are specified as the overlap between CSB being “L” and WR and RD being at the “L” level.

System Bus Read/Write Characteristics 1 (For the 6800 Series MPU)

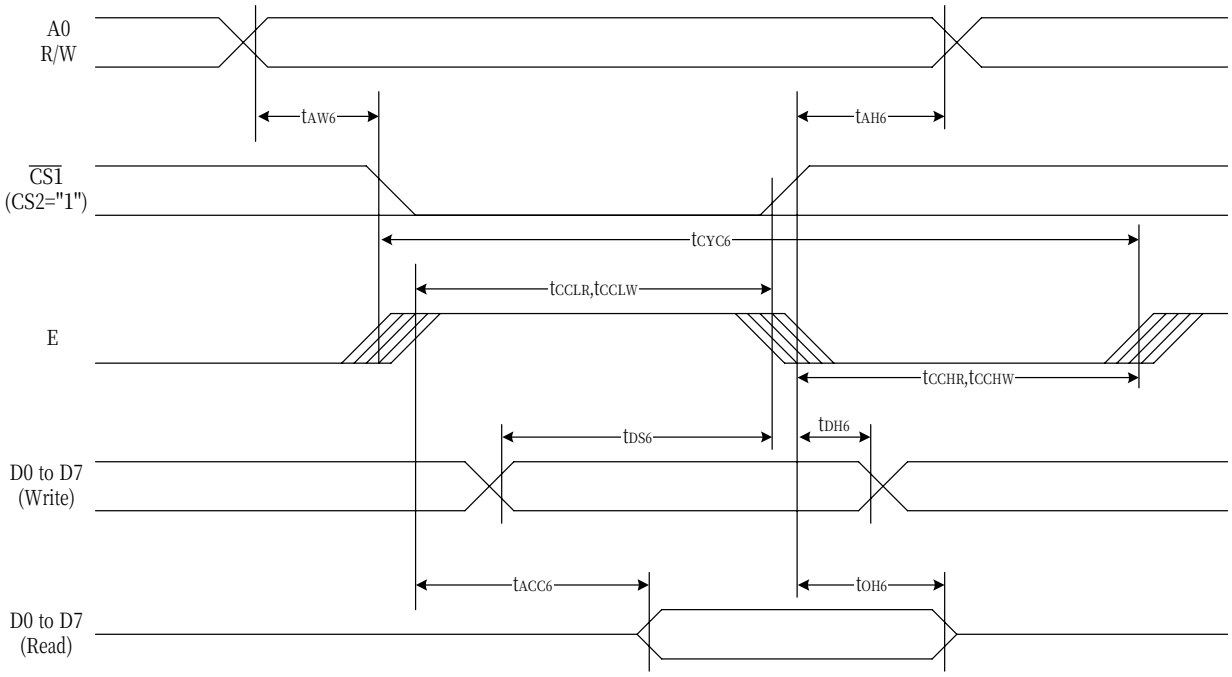


Fig 25.

(V_{DD} = 3.3 V , Ta = -30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		10	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		240	—	
Enable L pulse width (WRITE)	WR	tEWLW		80	—	
Enable H pulse width (WRITE)		tEWHW		80	—	
Enable L pulse width (READ)	RD	tEWLR		80	—	
Enable H pulse width (READ)		tEWHR		140		
WRITE Data setup time	D0 to D7	tDS6		40	—	
WRITE Address hold time		tDH6		0	—	
READ access time		tACC6	CL = 100 pF	—	70	
READ Output disable time		tOH6	CL = 100 pF	5	50	

(VDD = 2.7V , Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		15	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		400	—	
Enable L pulse width (WRITE)	WR	tEWLW		220	—	
Enable H pulse width (WRITE)		tEWHW		180	—	
Enable L pulse width (READ)	RD	tEWLR		220	—	
Enable H pulse width (READ)		tEWHR		180	—	
WRITE Data setup time	D0 to D7	tDS6		40	—	
WRITE Address hold time		tDH6		0	—	
READ access time		tACC6	CL = 100 pF	—	140	
READ Output disable time		tOH6	CL = 100 pF	10	100	

(VDD =1.8V , Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		30	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		640	—	
Enable L pulse width (WRITE)	WR	tEWLW		360	—	
Enable H pulse width (WRITE)		tEWHW		280	—	
Enable L pulse width (READ)	RD	tEWLR		360	—	
Enable H pulse width (READ)		tEWHR		280	—	
WRITE Data setup time	D0 to D7	tDS6		80	—	
WRITE Address hold time		tDH6		30	—	
READ access time		tACC6	CL = 100 pF	—	240	
READ Output disable time		tOH6	CL = 100 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) $\leqq$ (tCYC6 – tEWLW – tEWHW) for (tr + tf) $\leqq$ (tCYC6 – tEWLR – tEWHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tEWLW and tEWLR are specified as the overlap between CSB being “L” and E.

SERIAL INTERFACE(4-Line Interface)

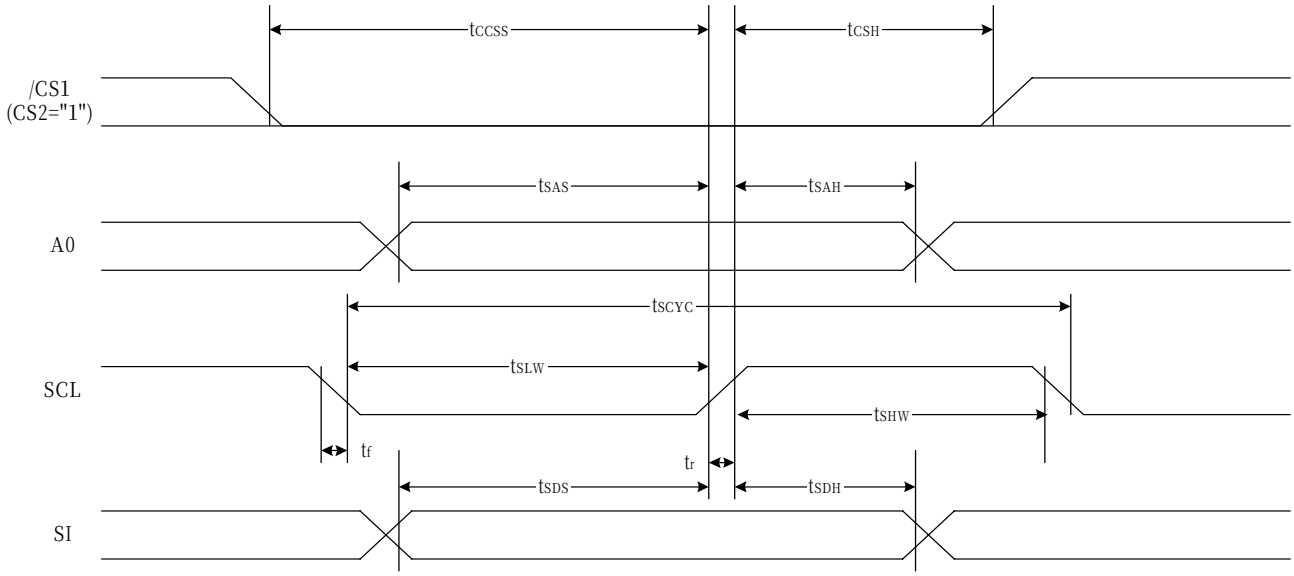


Fig 26.

(V_{DD}=3.3V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		50	—	ns
SCL “H” pulse width		tSHW		25	—	
SCL “L” pulse width		tSLW		25	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		10	—	
Data setup time	SI	tSDS		20	—	
Data hold time		tSDH		10	—	
CS-SCL time	CSB	tCSS		20	—	
CS-SCL time		tCSH		140	—	

(V_{DD}=2.7V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		100	—	ns
SCL “H” pulse width		tSHW		50	—	
SCL “L” pulse width		tSLW		50	—	
Address setup time	A0	tSAS		30	—	
Address hold time		tSAH		20	—	
Data setup time	SI	tSDS		30	—	
Data hold time		tSDH		20	—	
CS-SCL time	CSB	tCSS		30	—	
CS-SCL time		tCSH		160	—	

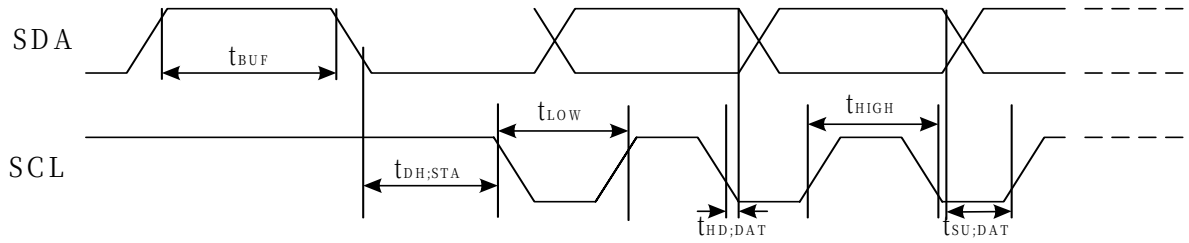
(V_{DD}=1.8V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		200	—	ns
SCL “H” pulse width		tSHW		80	—	
SCL “L” pulse width		tSLW		80	—	
Address setup time	A0	tSAS		60	—	
Address hold time		tSAH		30	—	
Data setup time	SI	tSDS		60	—	
Data hold time		tSDH		30	—	
CS-SCL time	CSB	tCSS		40	—	
CS-SCL time		tCSH		200	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

SERIAL INTERFACE(I²C Interface)



(V_{DD}= 1.8V~3.3V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
SCL clock frequency	SCL	FSCLK		-	200	kHZ
SCL clock low period	SCL	TLOW		2.5	-	us
SCL clock high period	SCL	THIGH		2.5	-	us
Data set-up time	SI	TSU;Data		0.1	-	us
Data hold time	SI	THD;Data		0	0.9	us
SCL,SDA rise time	SCL	TR		20+0.1Cb	300	ns
SCL,SDA fall time	SCL	TF		20+0.1Cb	300	ns
Capacitive load represented by each bus line		Cb		-	400	pF
Setup time for a repeated START condition	SI	TSU;SUA		0.6	-	us
Start condition hold time	SI	THD;STA		0.6	-	us
Setup time for STOP ondition		TSU;STO		0.6	-	us
Tolerable spike width on bus		TSW		-	50	ns
BUS free time between a STOP and StART condition	SCL	TBUF		2.5		us

14. RESET TIMING

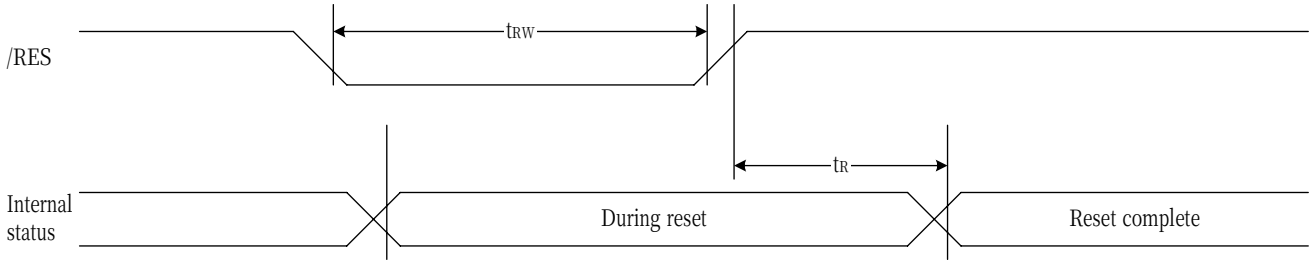


Fig 27.

(VDD = 3.3V , Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	1	us
Reset “L” pulse width	RESB	tRW		1	—	—	us

(VDD = 2.7V , Ta = –30 to 85°C)

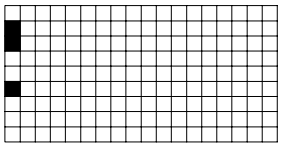
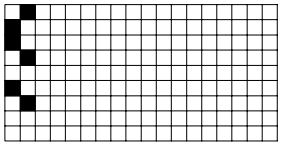
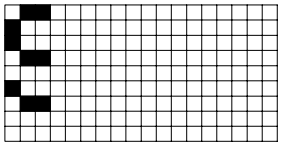
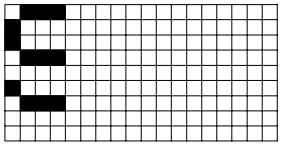
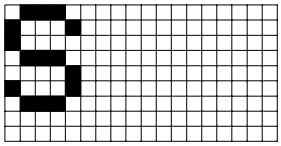
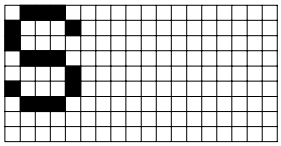
Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	1.5	us
Reset “L” pulse width	RESB	tRW		1.5	—	—	us

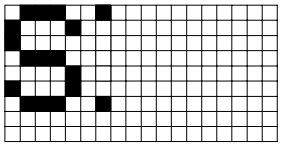
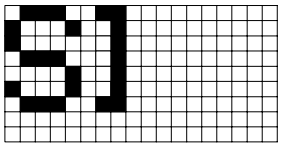
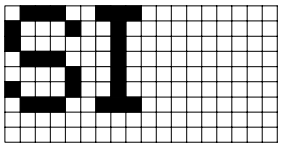
(VDD = 1.8V , Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	2.0	us
Reset “L” pulse width	RESB	tRW		2.0	—	—	us

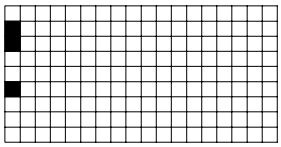
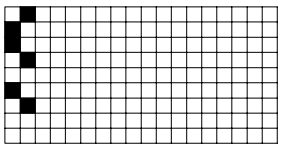
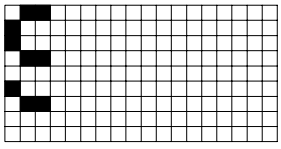
15. APPLICATION INFORMATION

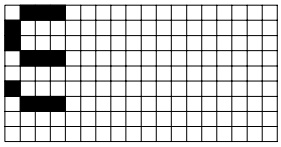
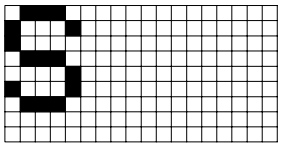
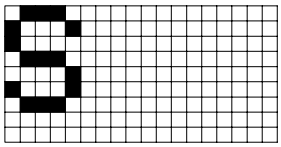
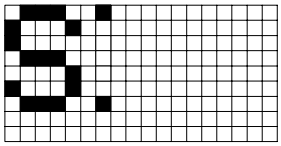
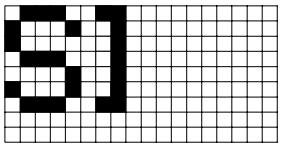
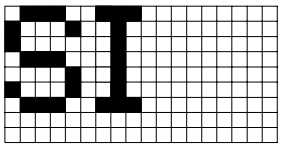
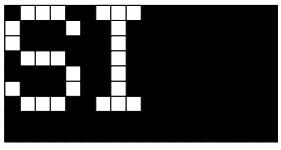
Table 5 programming example for ST7558

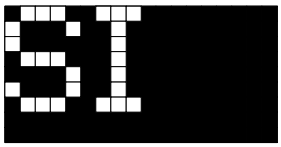
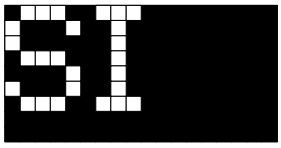
SETP	SERIAL BUS BYTE	DISPLAY	OPERATION
1	Start		CSB IS going low.
2	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 1 0 0 0 0 0		Function Set. PD=0,V=0,select extended Instruction set(H=0 mode)
3	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 1 0 0 0 0		Set V_{OP} V_{OP} is set to a+16*b[V]
4	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 1 0 0 0 0 0		Function Set. PD=0,V=0,select normal Instruction set(H=0 mode).
5	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 0 1 0 0		Display control. Set normal mode(D=1,E=0)
6	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 1 0 0 1 1 0		Data Write. Y,X are initialized to 0 by default, so they aren't set here…
7	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 1 0 0 1		Data Write.
8	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 1 0 0 1		Data Write.
9	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 1 0 0 1		Data Write.
10	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 1 1 0 0 1 0		Data Write.
11	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0 0		Data Write.

12	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 0 0 0 1		Data Write.
13	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 1 1 1 1 1 1		Data Write.
14	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 0 0 0 1		Data Write.
15	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 1 1 0 1		Display Control. Set inverse video mode (D=1,E=1).
16	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 0 0 0 0 0		Set X address of RAM. Set address to “0000000”.
17	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0 0		Data Write.

programming example for ST7558(Use I^2C Interface)

SETP	SERIAL BUS BYTE	DISPLAY	OPERATION
1	I^2C INTERFACE Start		
2	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0		Slave address for write
3	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 0 0 0		Control byte with cleared Co bit and A0 set to logic 0
4	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 0 0 0 0 1		Function Set. PD=0,V=0,select extended Instruction set(H=1 mode)
5	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 1 0 0 1 0		Set bias system
6	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 1 0 0 0 0		Set V_{OP} V_{OP} is set to a+16*b[V]
7	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 0 0 0 0 0		Function Set. PD=0,V=0,select normal Instruction set(H=0 mode).
8	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 1 0 0		Display control. Set normal mode(D=1,E=0)
9	I^2C INTERFACE Start		restart
10	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0		Slave address for write
11	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 1 0 0 0 0 0 0		Control byte with set Co bit and A0 set to logic 1
12	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 0 0 1 1 0		Data Write. Y,X are initialized to 0 by default, so they aren't set here…
13	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 1 0 0 1		Data Write.
14	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 1 0 0 1		Data Write.

15	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 1 0 0 1		Data Write.
16	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 1 0 0 1 0		Data Write.
17	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 0 0 0		Data Write.
18	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 0 0 0 1		Data Write.
19	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 1 1 1 1 1 1		Data Write.
20	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 0 0 0 1		Data Write.
21	I^2C INTERFACE start		restart
22	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0		Slave address for write
23	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0		Control byte with cleared Co bit and A0 set to logic 1
24	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 1		Display Control. Set inverse video mode (D=1,E=1).
25	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0		Control byte with cleared Co bit and A0 set to logic 1

26	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0		Set X address of RAM. Set address to “0000000”.
27	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 0 0 0 0		Control byte with set Co bit and A0 set to logic 0
28	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		Data Write.
29	I^2C INTERFACE start		restart
30	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0		Slave address for write
31	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 1 0 0 0 0 0 0		Control byte with set Co bit and A0 set to logic 1
32	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0		Set X address of RAM. Set address to “0000000”.
33	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0		Control byte with cleared Co bit and A0 set to logic 0

The pinning of the ST7558 is optimized for single plane wiring e.g. for chip-on-glass display modules. Display size: 65x102 pixels.

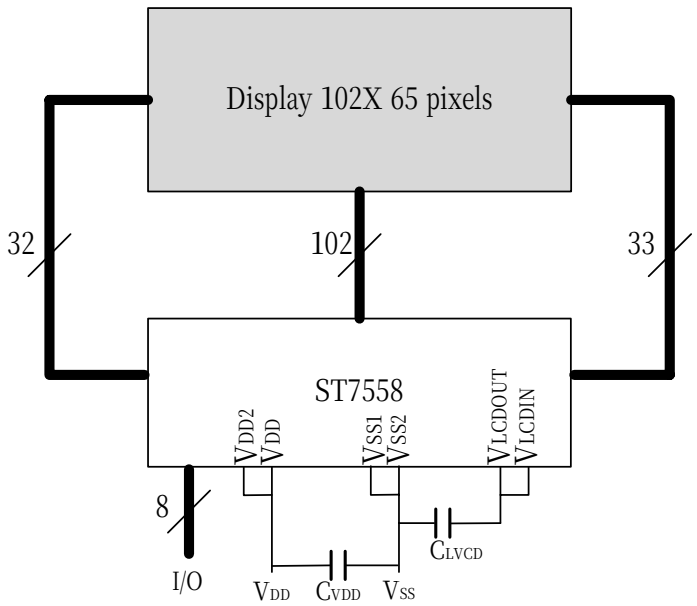


Fig 28. Application diagram: internal charge pump is used and single V_{DD}

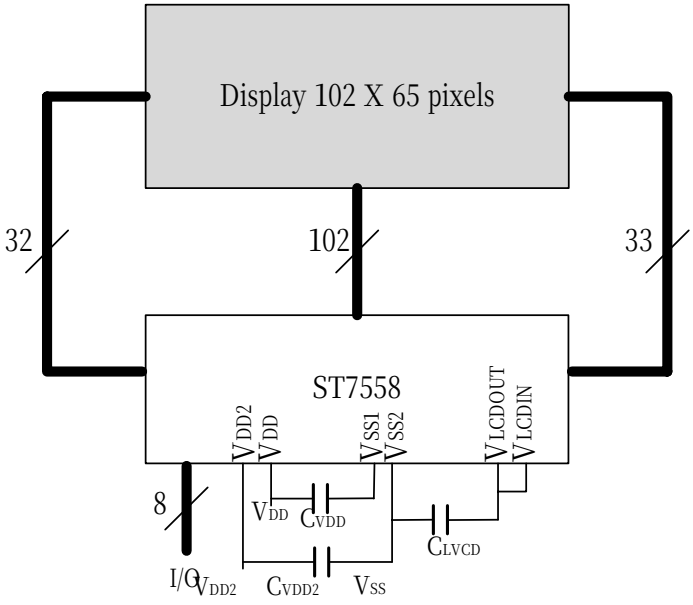


Fig 29. Application diagram: Internal charge pump is used and two separate VDD(V_{DD2})

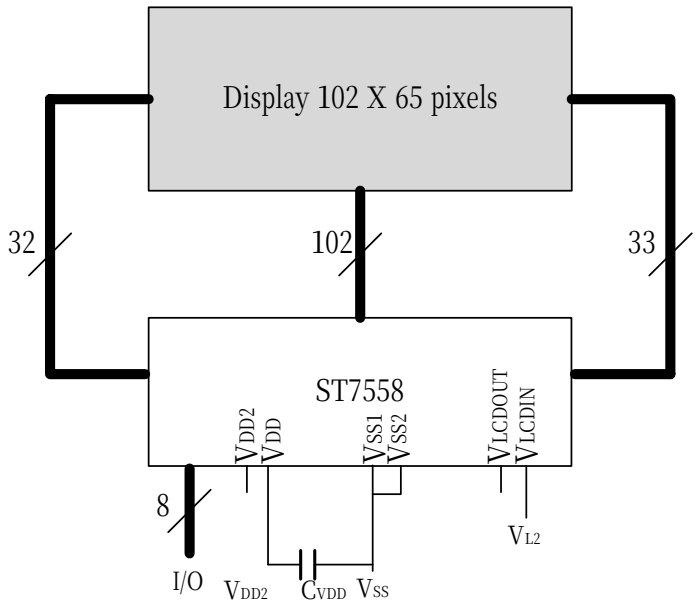


Fig 30. application diagram : External high voltage generation is used

The required minimum value for the external capacitors in an application with the ST7558 are:

C_{VLCD} = min. 100nF $C_{VDD,2}$= min. 1.0 µF

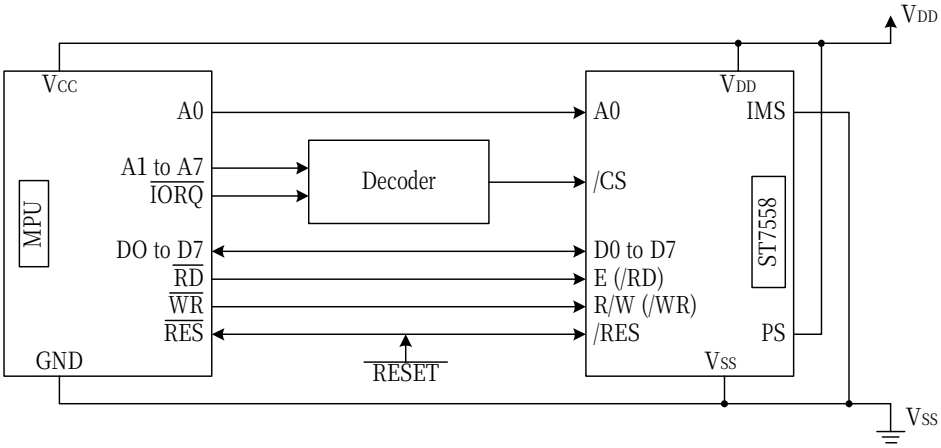
Higher capacitor values are recommended for ripple reduction.

16.THE MPU INTERFACE (REFERENCE EXAMPLES)

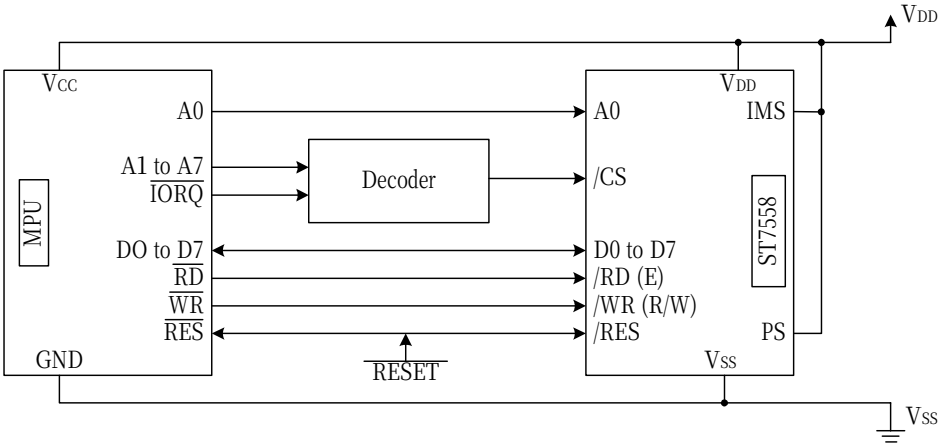
The ST7558 Series can be connected to either 80X86 Series MPUs or to 6800 Series MPUs. Moreover, using the serial interface it is possible to operate the ST7558 series chips with fewer signal lines.

The display area can be enlarged by using multiple ST7558 Series chips. When this is done, the chip select signal can be used to select the individual Ics to access.

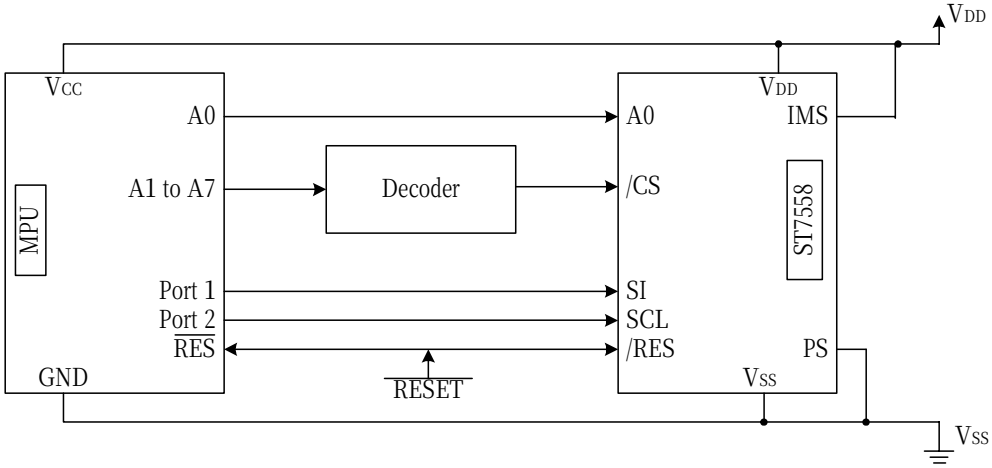
(1) 8080 Series MPUs



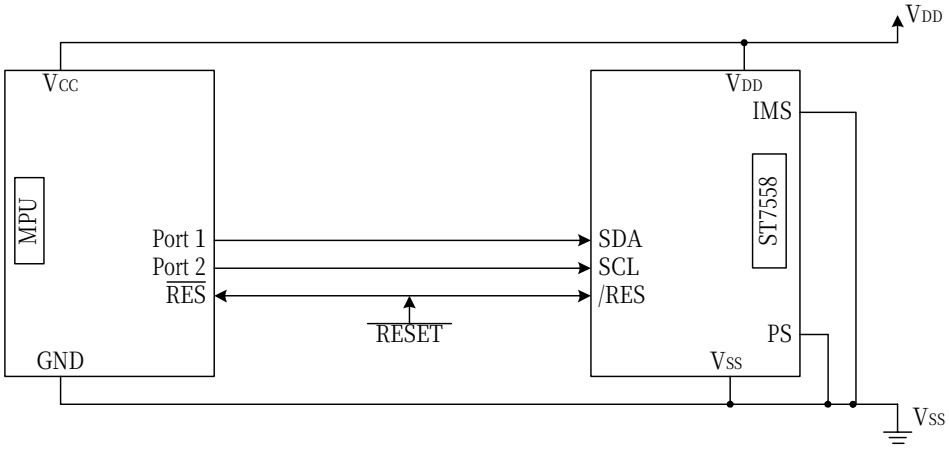
(2) 6800 Series MPUs



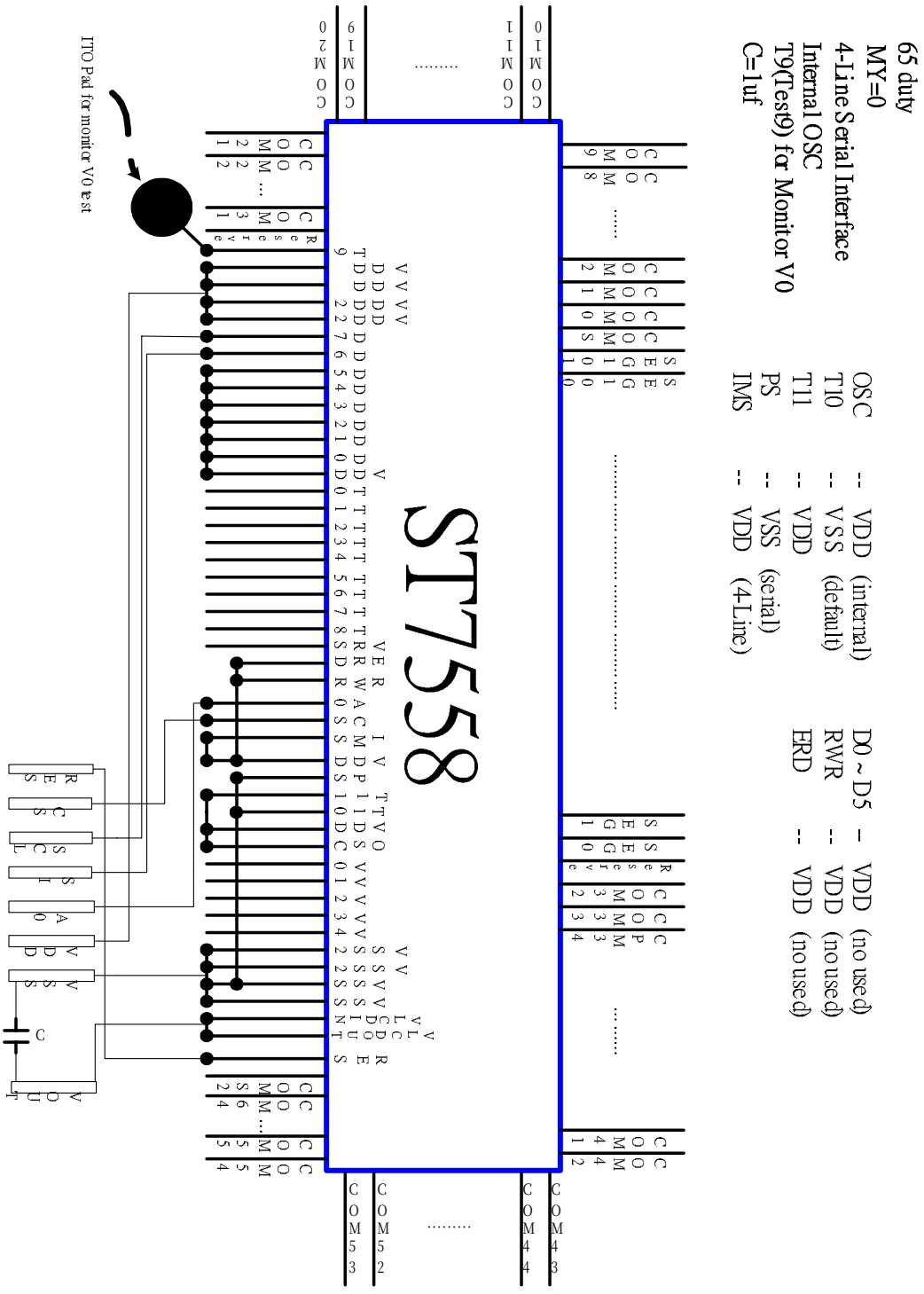
(3) Using the Serial Interface (4-line interface)



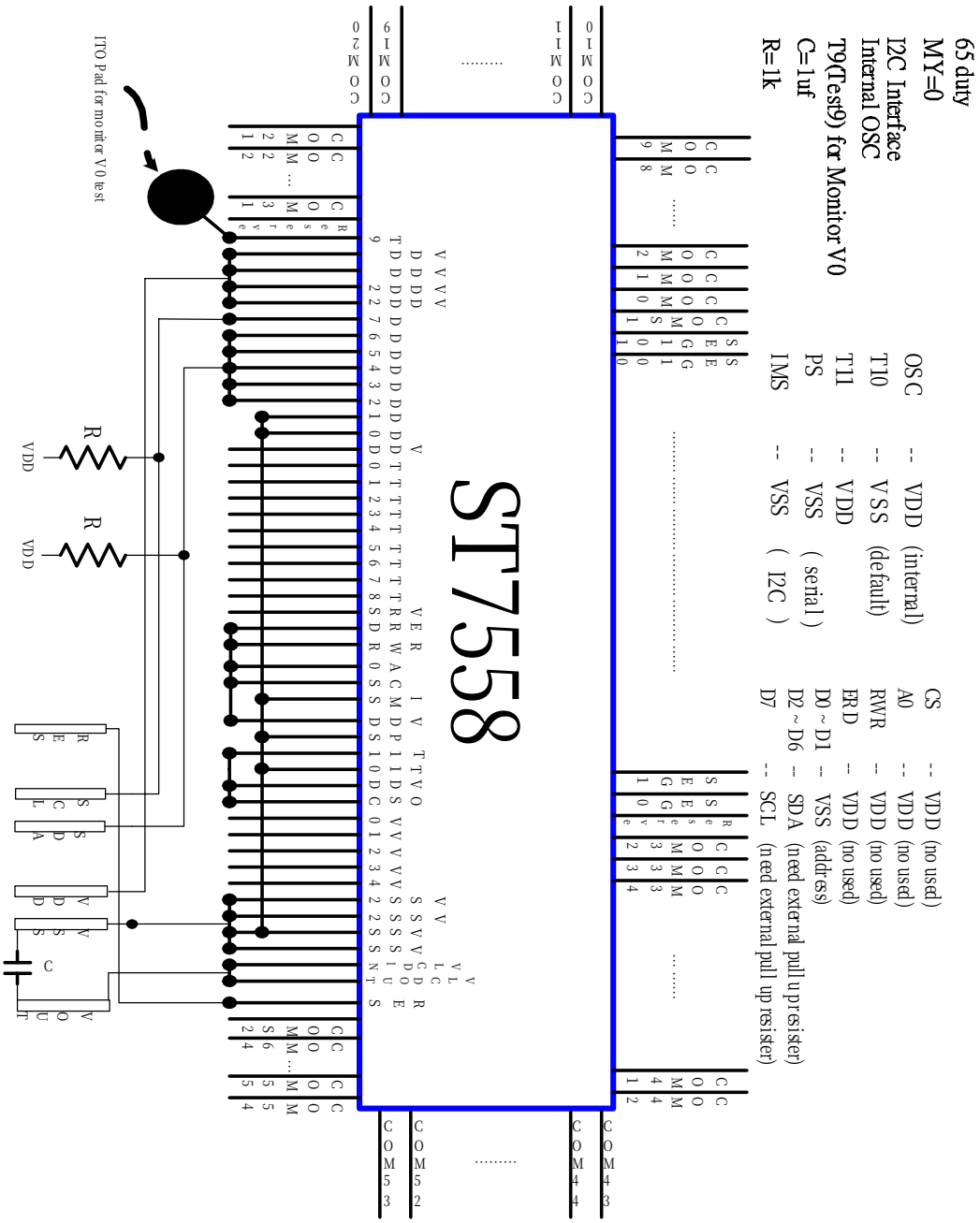
(4) Using the Serial Interface (I^2C interface)



65-duty/serial-4Line/VLCDIN-internal/VDD2=VDD/internal-OSC



65-duty/serial-I2C/VLCDIN-internal/VDD2=VDD/internal-OSC


65 duty
MY=0
I2C Interface
Internal OSC
T9(Test9) for Monitor V0
C= 1uf
R= 1k
OSC -- VDD (internal)
T10 -- VSS (default)
T11 -- VDD
PS -- VSS (serial)
IMS -- VSS (I2C)
CS -- VDD (no used)
A0 -- VDD (no used)
RWR -- VDD (no used)
ERD -- VDD (no used)
D0 ~ D1 -- VSS (address)
D2 ~ D6 -- SDA (need external pull up resister)
D7 -- SCL (need external pull up resister)
ST7558
ITO Pad for monitor V0 test
R
VDD
C