Sitronix

ST7568

68 x 102 Dot Matrix LCD Controller/Driver

1. INTERODUCTION

The ST7568 is a driver & controller LSI for 4-level gray scale graphic dot-matrix liquid crystal display systems. It contains 102 segment and 68 common driver circuits. This chip is connected directly to a microprocessor, accepts. 4-line serial interface(SPI) or 8-bit parallel interface or IIC serial interface, display data can stores in an on-chip display data RAM of 68 x 102 x 2 bits. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

Single chip LCD controller/driver for 4 GRAY SCALE STN LCD

4-level (White, Light Gray, Dark Gray, Black) Gray Scale Display with PWM and FRC Methods

DDRAM data [2n: 2n+1]	00	01	10	11
Gray scale	White	Light gray	Dark gray	Dark

(Accessible column address=0,1,2…99,100,101)

Driver Output Circuits

102 segment outputs / 68 common outputs

On-chip Display Data ram

- Capacity: 68X102X2=13,872 bits

Microprocessor Interface

- 8-bit parallel bi-directional interface with 6800-series or 8080-series
- 4-line SPI (serial peripheral interface) available (only write operation)
- IIC serial interface (only write operation)

On-chip Low Power Analog Circuit

- Generation of LCD supply voltage (externally Vout voltage supply is possible)
- Generation of intermediate LCD bias voltages
- Oscillator requires no external components (external clock also possible)
- Voltage converter (x2, x3, x4, x5)
- Voltage regulator
- Voltage follower
- On-chip electronic contrast control function (128 steps)

External RESB (reset) pin

Logic supply voltage range V_{DD} -V_{SS}

- 1.8V to 3.3V

Temperature range: -30 to +85 degree

ST7568	**6800 , 8080 , 4-Line Interface (without IIC interface)**	ST
ST7568i	**IIC interface**	I²C BUS

3. ST7568 Pad Arrangement (COG)

Chip Size: 10,220 um × 1000 um

Bump Pitch:

PAD NO 1 ~ 148 , 250 ~ 272 : 75.5 um (com/seg) PAD NO 149 ~ 248 : 75 um (I/O) PAD NO 148 ~ 149 : 114 um

PAD NO 248 ~ 249 : 93.5 um PAD NO 249 ~ 250 : 95.9 um

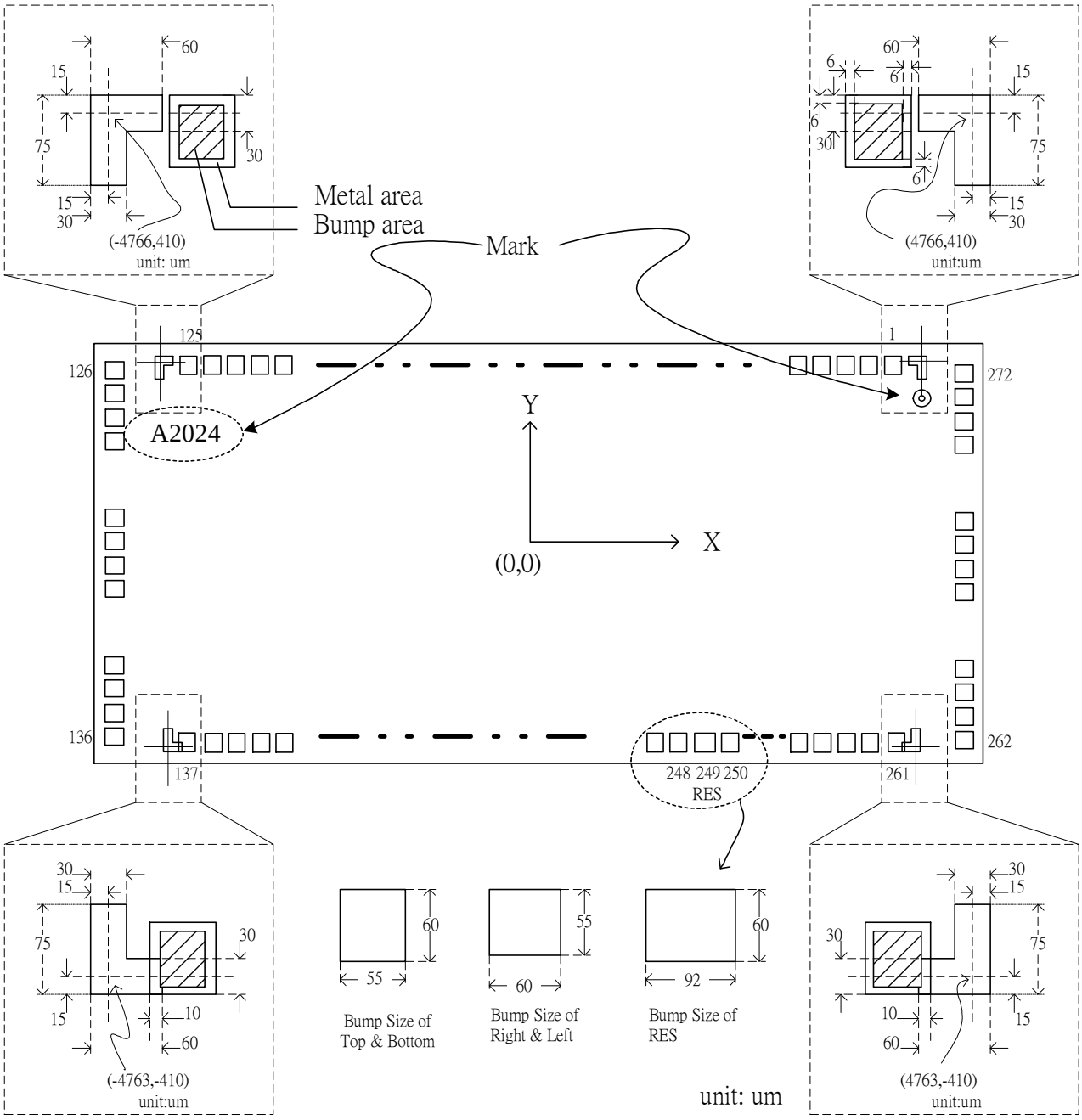
Bump Size:

PAD NO 1 ~ 125 , 137 ~ 248 , 250 ~ 261 : 55(x) um × 60(y) um PAD NO 249 : 92(x) um × 60(y) um

PAD NO 126 ~ 136 , 262 ~ 272 : 60(x)um × 55(y) um

Bump Height: 17 um

Chip Thickness: 635 um



Pad Center Coordinates(68 Duty)

PAD NO.	PIN Name	X	Y
1	COM[44]	4681.0	389.0
2	COM[43]	4605.5	389.0
3	COM[42]	4530.0	389.0
4	COM[41]	4454.5	389.0
5	COM[40]	4379.0	389.0
6	COM[39]	4303.5	389.0
7	COM[38]	4228.0	389.0
8	COM[37]	4152.5	389.0
9	COM[36]	4077.0	389.0
10	COM[35]	4001.5	389.0
11	COM[34]	3926.0	389.0
12	COM[33]	3850.5	389.0
13	SEG[0]	3775.0	389.0
14	SEG[1]	3699.5	389.0
15	SEG[2]	3624.0	389.0
16	SEG[3]	3548.5	389.0
17	SEG[4]	3473.0	389.0
18	SEG[5]	3397.5	389.0
19	SEG[6]	3322.0	389.0
20	SEG[7]	3246.5	389.0
21	SEG[8]	3171.0	389.0
22	SEG[9]	3095.5	389.0
23	SEG[10]	3020.0	389.0
24	SEG[11]	2944.5	389.0
25	SEG[12]	2869.0	389.0
26	SEG[13]	2793.5	389.0
27	SEG[14]	2718.0	389.0
28	SEG[15]	2642.5	389.0
29	SEG[16]	2567.0	389.0
30	SEG[17]	2491.5	389.0
31	SEG[18]	2416.0	389.0
32	SEG[19]	2340.5	389.0
33	SEG[20]	2265.0	389.0
34	SEG[21]	2189.5	389.0
35	SEG[22]	2114.0	389.0

PAD NO.	PIN Name	X	Y
36	SEG[23]	2038.5	389.0
37	SEG[24]	1963.0	389.0
38	SEG[25]	1887.5	389.0
39	SEG[26]	1812.0	389.0
40	SEG[27]	1736.5	389.0
41	SEG[28]	1661.0	389.0
42	SEG[29]	1585.5	389.0
43	SEG[30]	1510.0	389.0
44	SEG[31]	1434.5	389.0
45	SEG[32]	1359.0	389.0
46	SEG[33]	1283.5	389.0
47	SEG[34]	1208.0	389.0
48	SEG[35]	1132.5	389.0
49	SEG[36]	1057.0	389.0
50	SEG[37]	981.5	389.0
51	SEG[38]	906.0	389.0
52	SEG[39]	830.5	389.0
53	SEG[40]	755.0	389.0
54	SEG[41]	679.5	389.0
55	SEG[42]	604.0	389.0
56	SEG[43]	528.5	389.0
57	SEG[44]	453.0	389.0
58	SEG[45]	377.5	389.0
59	SEG[46]	302.0	389.0
60	SEG[47]	226.5	389.0
61	SEG[48]	151.0	389.0
62	SEG[49]	75.5	389.0
63	SEG[50]	0.0	389.0
64	SEG[51]	-75.5	389.0
65	SEG[52]	-151.0	389.0
66	SEG[53]	-226.5	389.0
67	SEG[54]	-302.0	389.0
68	SEG[55]	-377.5	389.0
69	SEG[56]	-453.0	389.0
70	SEG[57]	-528.5	389.0

PAD NO.	PIN Name	X	Y
71	SEG[58]	-604.0	389.0
72	SEG[59]	-679.5	389.0
73	SEG[60]	-755.0	389.0
74	SEG[61]	-830.5	389.0
75	SEG[62]	-906.0	389.0
76	SEG[63]	-981.5	389.0
77	SEG[64]	-1057.0	389.0
78	SEG[65]	-1132.5	389.0
79	SEG[66]	-1208.0	389.0
80	SEG[67]	-1283.5	389.0
81	SEG[68]	-1359.0	389.0
82	SEG[69]	-1434.5	389.0
83	SEG[70]	-1510.0	389.0
84	SEG[71]	-1585.5	389.0
85	SEG[72]	-1661.0	389.0
86	SEG[73]	-1736.5	389.0
87	SEG[74]	-1812.0	389.0
88	SEG[75]	-1887.5	389.0
89	SEG[76]	-1963.0	389.0
90	SEG[77]	-2038.5	389.0
91	SEG[78]	-2114.0	389.0
92	SEG[79]	-2189.5	389.0
93	SEG[80]	-2265.0	389.0
94	SEG[81]	-2340.5	389.0
95	SEG[82]	-2416.0	389.0
96	SEG[83]	-2491.5	389.0
97	SEG[84]	-2567.0	389.0
98	SEG[85]	-2642.5	389.0
99	SEG[86]	-2718.0	389.0
100	SEG[87]	-2793.5	389.0
101	SEG[88]	-2869.0	389.0
102	SEG[89]	-2944.5	389.0
103	SEG[90]	-3020.0	389.0
104	SEG[91]	-3095.5	389.0
105	SEG[92]	-3171.0	389.0
106	SEG[93]	-3246.5	389.0

PAD NO.	PIN Name	X	Y
107	SEG[94]	-3322.0	389.0
108	SEG[95]	-3397.5	389.0
109	SEG[96]	-3473.0	389.0
110	SEG[97]	-3548.5	389.0
111	SEG[98]	-3624.0	389.0
112	SEG[99]	-3699.5	389.0
113	SEG[100]	-3775.0	389.0
114	SEG[101]	-3850.5	389.0
115	COMS1	-3926.0	389.0
116	COM[0]	-4001.5	389.0
117	COM[1]	-4077.0	389.0
118	COM[2]	-4152.5	389.0
119	COM[3]	-4228.0	389.0
120	COM[4]	-4303.5	389.0
121	COM[5]	-4379.0	389.0
122	COM[6]	-4454.5	389.0
123	COM[7]	-4530.0	389.0
124	COM[8]	-4605.5	389.0
125	COM[9]	-4681.0	389.0
126	COM[10]	-4998.5	381.5
127	COM[11]	-4998.5	306.0
128	COM[12]	-4998.5	230.5
129	COM[13]	-4998.5	155.0
130	COM[14]	-4998.5	79.5
131	COM[15]	-4998.5	4.0
132	COM[16]	-4998.5	-71.5
133	COM[17]	-4998.5	-147.0
134	COM[18]	-4998.5	-222.5
135	COM[19]	-4998.5	-298.0
136	COM[20]	-4998.5	-373.5
137	COM[21]	-4694.5	-389.0
138	COM[22]	-4619.0	-389.0
139	COM[23]	-4543.5	-389.0
140	COM[24]	-4468.0	-389.0
141	COM[25]	-4392.5	-389.0
142	COM[26]	-4317.0	-389.0

PAD NO.	PIN Name	X	Y
143	COM[27]	-4241.5	-389.0
144	COM[28]	-4166.0	-389.0
145	COM[29]	-4090.5	-389.0
146	COM[30]	-4015.0	-389.0
147	COM[31]	-3939.5	-389.0
148	COM[32]	-3864.0	-389.0
149	T9	-3750.0	-389.0
150	VDD	-3675.0	-389.0
151	VDD	-3600.0	-389.0
152	VDD	-3525.0	-389.0
153	VDD	-3450.0	-389.0
154	VDD	-3375.0	-389.0
155	VDD	-3300.0	-389.0
156	VDD2	-3225.0	-389.0
157	VDD2	-3150.0	-389.0
158	VDD2	-3075.0	-389.0
159	VDD2	-3000.0	-389.0
160	VDD2	-2925.0	-389.0
161	VDD2	-2850.0	-389.0
162	VDD2	-2775.0	-389.0
163	VDD2	-2700.0	-389.0
164	VDD2	-2625.0	-389.0
165	VDD2	-2550.0	-389.0
166	VDD2	-2475.0	-389.0
167	VDD2	-2400.0	-389.0
168	D7	-2325.0	-389.0
169	D7	-2250.0	-389.0
170	D6	-2175.0	-389.0
171	D6	-2100.0	-389.0
172	D5	-2025.0	-389.0
173	D5	-1950.0	-389.0
174	D4	-1875.0	-389.0
175	D4	-1800.0	-389.0
176	D3	-1725.0	-389.0
177	D3	-1650.0	-389.0
178	D2	-1575.0	-389.0

PAD NO.	PIN Name	X	Y
179	D2	-1500.0	-389.0
180	D1	-1425.0	-389.0
181	D1	-1350.0	-389.0
182	D0	-1275.0	-389.0
183	D0	-1200.0	-389.0
184	VDD	-1125.0	-389.0
185	T0	-1050.0	-389.0
186	T1	-975.0	-389.0
187	T2	-900.0	-389.0
188	T3	-825.0	-389.0
189	T4	-750.0	-389.0
190	T5	-675.0	-389.0
191	T6	-600.0	-389.0
192	T7	-525.0	-389.0
193	T8	-450.0	-389.0
194	VRS	-375.0	-389.0
195	ERD	-300.0	-389.0
196	ERD	-225.0	-389.0
197	RWR	-150.0	-389.0
198	RWR	-75.0	-389.0
199	A0	0.0	-389.0
200	A0	75.0	-389.0
201	CS	150.0	-389.0
202	CS	225.0	-389.0
203	IMS	300.0	-389.0
204	VDD	375.0	-389.0
205	PS	450.0	-389.0
206	MODE	525.0	-389.0
207	T10	600.0	-389.0
208	VDD	675.0	-389.0
209	OSC	750.0	-389.0
210	OSC	825.0	-389.0
211	V0	900.0	-389.0
212	V0	975.0	-389.0
213	V0	1050.0	-389.0
214	V0	1125.0	-389.0

PAD NO.	PIN Name	X	Y
215	V1	1200.0	-389.0
216	V2	1275.0	-389.0
217	V3	1350.0	-389.0
218	V4	1425.0	-389.0
219	VSS2	1500.0	-389.0
220	VSS2	1575.0	-389.0
221	VSS2	1650.0	-389.0
222	VSS2	1725.0	-389.0
223	VSS2	1800.0	-389.0
224	VSS2	1875.0	-389.0
225	VSS2	1950.0	-389.0
226	VSS2	2025.0	-389.0
227	VSS2	2100.0	-389.0
228	VSS2	2175.0	-389.0
229	VSS2	2250.0	-389.0
230	VSS2	2325.0	-389.0
231	VSS	2400.0	-389.0
232	VSS	2475.0	-389.0
233	VSS	2550.0	-389.0
234	VSS	2625.0	-389.0
235	VSS	2700.0	-389.0
236	VSS	2775.0	-389.0
237	VLCDIN	2850.0	-389.0
238	VLCDIN	2925.0	-389.0
239	VLCDIN	3000.0	-389.0
240	VLCDIN	3075.0	-389.0
241	VLCDIN	3150.0	-389.0
242	VLCDIN	3225.0	-389.0
243	VLCDOUT	3300.0	-389.0

PAD NO.	PIN Name	X	Y
244	VLCDOUT	3375.0	-389.0
245	VLCDOUT	3450.0	-389.0
246	VLCDOUT	3525.0	-389.0
247	VLCDOUT	3600.0	-389.0
248	VLCDOUT	3675.0	-389.0
249	RES	3768.5	-389.0
250	COMS2	3864.5	-389.0
251	COM[66]	3940.0	-389.0
252	COM[65]	4015.5	-389.0
253	COM[64]	4091.0	-389.0
254	COM[63]	4166.5	-389.0
255	COM[62]	4242.0	-389.0
256	COM[61]	4317.5	-389.0
257	COM[60]	4393.0	-389.0
258	COM[59]	4468.5	-389.0
259	COM[58]	4544.0	-389.0
260	COM[57]	4619.5	-389.0
261	COM[56]	4695.0	-389.0
262	COM[55]	4998.5	-373.5
263	COM[54]	4998.5	-298.0
264	COM[53]	4998.5	-222.5
265	COM[52]	4998.5	-147.0
266	COM[51]	4998.5	-71.5
267	COM[50]	4998.5	4.0
268	COM[49]	4998.5	79.5
269	COM[48]	4998.5	155.0
270	COM[47]	4998.5	230.5
271	COM[46]	4998.5	306.0
272	COM[45]	4998.5	381.5

Pad Center Coordinates(65 Duty)

PAD NO.	PIN Name	X	Y
1	COM[41]	4681.0	389.0
2	COM[40]	4605.5	389.0
3	COM[39]	4530.0	389.0
4	COM[38]	4454.5	389.0
5	COM[37]	4379.0	389.0
6	COM[36]	4303.5	389.0
7	COM[35]	4228.0	389.0
8	COM[34]	4152.5	389.0
9	COM[33]	4077.0	389.0
10	COM[32]	4001.5	389.0
11	Reserve	3926.0	389.0
12	Reserve	3850.5	389.0
13	SEG[0]	3775.0	389.0
14	SEG[1]	3699.5	389.0
15	SEG[2]	3624.0	389.0
16	SEG[3]	3548.5	389.0
17	SEG[4]	3473.0	389.0
18	SEG[5]	3397.5	389.0
19	SEG[6]	3322.0	389.0
20	SEG[7]	3246.5	389.0
21	SEG[8]	3171.0	389.0
22	SEG[9]	3095.5	389.0
23	SEG[10]	3020.0	389.0
24	SEG[11]	2944.5	389.0
25	SEG[12]	2869.0	389.0
26	SEG[13]	2793.5	389.0
27	SEG[14]	2718.0	389.0
28	SEG[15]	2642.5	389.0
29	SEG[16]	2567.0	389.0
30	SEG[17]	2491.5	389.0
31	SEG[18]	2416.0	389.0
32	SEG[19]	2340.5	389.0
33	SEG[20]	2265.0	389.0
34	SEG[21]	2189.5	389.0
35	SEG[22]	2114.0	389.0

PAD NO.	PIN Name	X	Y
36	SEG[23]	2038.5	389.0
37	SEG[24]	1963.0	389.0
38	SEG[25]	1887.5	389.0
39	SEG[26]	1812.0	389.0
40	SEG[27]	1736.5	389.0
41	SEG[28]	1661.0	389.0
42	SEG[29]	1585.5	389.0
43	SEG[30]	1510.0	389.0
44	SEG[31]	1434.5	389.0
45	SEG[32]	1359.0	389.0
46	SEG[33]	1283.5	389.0
47	SEG[34]	1208.0	389.0
48	SEG[35]	1132.5	389.0
49	SEG[36]	1057.0	389.0
50	SEG[37]	981.5	389.0
51	SEG[38]	906.0	389.0
52	SEG[39]	830.5	389.0
53	SEG[40]	755.0	389.0
54	SEG[41]	679.5	389.0
55	SEG[42]	604.0	389.0
56	SEG[43]	528.5	389.0
57	SEG[44]	453.0	389.0
58	SEG[45]	377.5	389.0
59	SEG[46]	302.0	389.0
60	SEG[47]	226.5	389.0
61	SEG[48]	151.0	389.0
62	SEG[49]	75.5	389.0
63	SEG[50]	0.0	389.0
64	SEG[51]	-75.5	389.0
65	SEG[52]	-151.0	389.0
66	SEG[53]	-226.5	389.0
67	SEG[54]	-302.0	389.0
68	SEG[55]	-377.5	389.0
69	SEG[56]	-453.0	389.0
70	SEG[57]	-528.5	389.0

PAD NO.	PIN Name	X	Y
71	SEG[58]	-604.0	389.0
72	SEG[59]	-679.5	389.0
73	SEG[60]	-755.0	389.0
74	SEG[61]	-830.5	389.0
75	SEG[62]	-906.0	389.0
76	SEG[63]	-981.5	389.0
77	SEG[64]	-1057.0	389.0
78	SEG[65]	-1132.5	389.0
79	SEG[66]	-1208.0	389.0
80	SEG[67]	-1283.5	389.0
81	SEG[68]	-1359.0	389.0
82	SEG[69]	-1434.5	389.0
83	SEG[70]	-1510.0	389.0
84	SEG[71]	-1585.5	389.0
85	SEG[72]	-1661.0	389.0
86	SEG[73]	-1736.5	389.0
87	SEG[74]	-1812.0	389.0
88	SEG[75]	-1887.5	389.0
89	SEG[76]	-1963.0	389.0
90	SEG[77]	-2038.5	389.0
91	SEG[78]	-2114.0	389.0
92	SEG[79]	-2189.5	389.0
93	SEG[80]	-2265.0	389.0
94	SEG[81]	-2340.5	389.0
95	SEG[82]	-2416.0	389.0
96	SEG[83]	-2491.5	389.0
97	SEG[84]	-2567.0	389.0
98	SEG[85]	-2642.5	389.0
99	SEG[86]	-2718.0	389.0
100	SEG[87]	-2793.5	389.0
101	SEG[88]	-2869.0	389.0
102	SEG[89]	-2944.5	389.0
103	SEG[90]	-3020.0	389.0
104	SEG[91]	-3095.5	389.0
105	SEG[92]	-3171.0	389.0
106	SEG[93]	-3246.5	389.0

PAD NO.	PIN Name	X	Y
107	SEG[94]	-3322.0	389.0
108	SEG[95]	-3397.5	389.0
109	SEG[96]	-3473.0	389.0
110	SEG[97]	-3548.5	389.0
111	SEG[98]	-3624.0	389.0
112	SEG[99]	-3699.5	389.0
113	SEG[100]	-3775.0	389.0
114	SEG[101]	-3850.5	389.0
115	COMS1	-3926.0	389.0
116	COM[0]	-4001.5	389.0
117	COM[1]	-4077.0	389.0
118	COM[2]	-4152.5	389.0
119	COM[3]	-4228.0	389.0
120	COM[4]	-4303.5	389.0
121	COM[5]	-4379.0	389.0
122	COM[6]	-4454.5	389.0
123	COM[7]	-4530.0	389.0
124	COM[8]	-4605.5	389.0
125	COM[9]	-4681.0	389.0
126	COM[10]	-4998.5	381.5
127	COM[11]	-4998.5	306.0
128	COM[12]	-4998.5	230.5
129	COM[13]	-4998.5	155.0
130	COM[14]	-4998.5	79.5
131	COM[15]	-4998.5	4.0
132	COM[16]	-4998.5	-71.5
133	COM[17]	-4998.5	-147.0
134	COM[18]	-4998.5	-222.5
135	COM[19]	-4998.5	-298.0
136	COM[20]	-4998.5	-373.5
137	COM[21]	-4694.5	-389.0
138	COM[22]	-4619.0	-389.0
139	COM[23]	-4543.5	-389.0
140	COM[24]	-4468.0	-389.0
141	COM[25]	-4392.5	-389.0
142	COM[26]	-4317.0	-389.0

PAD NO.	PIN Name	X	Y
143	COM[27]	-4241.5	-389.0
144	COM[28]	-4166.0	-389.0
145	COM[29]	-4090.5	-389.0
146	COM[30]	-4015.0	-389.0
147	COM[31]	-3939.5	-389.0
148	Reserve	-3864.0	-389.0
149	T9	-3750.0	-389.0
150	VDD	-3675.0	-389.0
151	VDD	-3600.0	-389.0
152	VDD	-3525.0	-389.0
153	VDD	-3450.0	-389.0
154	VDD	-3375.0	-389.0
155	VDD	-3300.0	-389.0
156	VDD2	-3225.0	-389.0
157	VDD2	-3150.0	-389.0
158	VDD2	-3075.0	-389.0
159	VDD2	-3000.0	-389.0
160	VDD2	-2925.0	-389.0
161	VDD2	-2850.0	-389.0
162	VDD2	-2775.0	-389.0
163	VDD2	-2700.0	-389.0
164	VDD2	-2625.0	-389.0
165	VDD2	-2550.0	-389.0
166	VDD2	-2475.0	-389.0
167	VDD2	-2400.0	-389.0
168	D7	-2325.0	-389.0
169	D7	-2250.0	-389.0
170	D6	-2175.0	-389.0
171	D6	-2100.0	-389.0
172	D5	-2025.0	-389.0
173	D5	-1950.0	-389.0
174	D4	-1875.0	-389.0
175	D4	-1800.0	-389.0
176	D3	-1725.0	-389.0
177	D3	-1650.0	-389.0
178	D2	-1575.0	-389.0

PAD NO.	PIN Name	X	Y
179	D2	-1500.0	-389.0
180	D1	-1425.0	-389.0
181	D1	-1350.0	-389.0
182	D0	-1275.0	-389.0
183	D0	-1200.0	-389.0
184	VDD	-1125.0	-389.0
185	T0	-1050.0	-389.0
186	T1	-975.0	-389.0
187	T2	-900.0	-389.0
188	T3	-825.0	-389.0
189	T4	-750.0	-389.0
190	T5	-675.0	-389.0
191	T6	-600.0	-389.0
192	T7	-525.0	-389.0
193	T8	-450.0	-389.0
194	VRS	-375.0	-389.0
195	ERD	-300.0	-389.0
196	ERD	-225.0	-389.0
197	RWR	-150.0	-389.0
198	RWR	-75.0	-389.0
199	A0	0.0	-389.0
200	A0	75.0	-389.0
201	CS	150.0	-389.0
202	CS	225.0	-389.0
203	IMS	300.0	-389.0
204	VDD	375.0	-389.0
205	PS	450.0	-389.0
206	MODE	525.0	-389.0
207	T10	600.0	-389.0
208	VDD	675.0	-389.0
209	OSC	750.0	-389.0
210	OSC	825.0	-389.0
211	V0	900.0	-389.0
212	V0	975.0	-389.0
213	V0	1050.0	-389.0
214	V0	1125.0	-389.0

PAD NO.	PIN Name	X	Y
215	V1	1200.0	-389.0
216	V2	1275.0	-389.0
217	V3	1350.0	-389.0
218	V4	1425.0	-389.0
219	VSS2	1500.0	-389.0
220	VSS2	1575.0	-389.0
221	VSS2	1650.0	-389.0
222	VSS2	1725.0	-389.0
223	VSS2	1800.0	-389.0
224	VSS2	1875.0	-389.0
225	VSS2	1950.0	-389.0
226	VSS2	2025.0	-389.0
227	VSS2	2100.0	-389.0
228	VSS2	2175.0	-389.0
229	VSS2	2250.0	-389.0
230	VSS2	2325.0	-389.0
231	VSS	2400.0	-389.0
232	VSS	2475.0	-389.0
233	VSS	2550.0	-389.0
234	VSS	2625.0	-389.0
235	VSS	2700.0	-389.0
236	VSS	2775.0	-389.0
237	VLCDIN	2850.0	-389.0
238	VLCDIN	2925.0	-389.0
239	VLCDIN	3000.0	-389.0
240	VLCDIN	3075.0	-389.0
241	VLCDIN	3150.0	-389.0
242	VLCDIN	3225.0	-389.0
243	VLCDOUT	3300.0	-389.0

PAD NO.	PIN Name	X	Y
244	VLCDOUT	3375.0	-389.0
245	VLCDOUT	3450.0	-389.0
246	VLCDOUT	3525.0	-389.0
247	VLCDOUT	3600.0	-389.0
248	VLCDOUT	3675.0	-389.0
249	RES	3768.5	-389.0
250	COMS2	3864.5	-389.0
251	COM[63]	3940.0	-389.0
252	COM[62]	4015.5	-389.0
253	COM[61]	4091.0	-389.0
254	COM[60]	4166.5	-389.0
255	COM[59]	4242.0	-389.0
256	COM[58]	4317.5	-389.0
257	COM[57]	4393.0	-389.0
258	COM[56]	4468.5	-389.0
259	COM[55]	4544.0	-389.0
260	COM[54]	4619.5	-389.0
261	COM[53]	4695.0	-389.0
262	COM[52]	4998.5	-373.5
263	COM[51]	4998.5	-298.0
264	COM[50]	4998.5	-222.5
265	COM[49]	4998.5	-147.0
266	COM[48]	4998.5	-71.5
267	COM[47]	4998.5	4.0
268	COM[46]	4998.5	79.5
269	COM[45]	4998.5	155.0
270	COM[44]	4998.5	230.5
271	COM[43]	4998.5	306.0
272	COM[42]	4998.5	381.5

4. BLOCK DIAGRAM

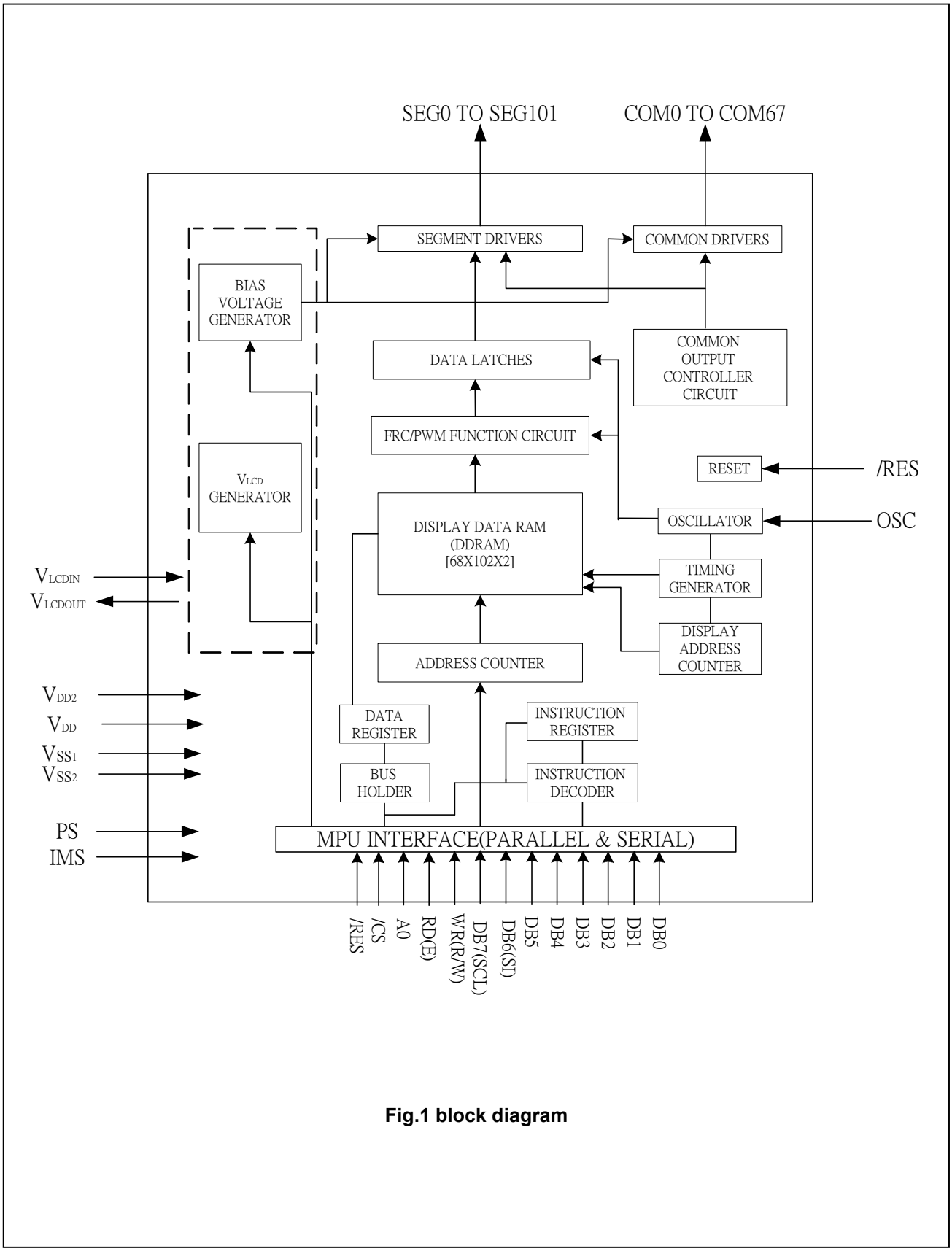


Fig.1 block diagram

5. PINNING DESCRIPTIONS

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td colspan="4">Lcd driver outputs</td></tr>
<tr><td>SEG0 to SEG101</td><td>O</td><td>LCD segment driver outputs
This display data and the M signal control the output voltage of segment driver.
<table>
<tr><td rowspan="2">Display data</td><td rowspan="2">M (Internal)</td><td colspan="2">Segment drover output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td>VLCD</td><td>V_2</td></tr>
<tr><td>H</td><td>L</td><td>V_{SS}</td><td>V_3</td></tr>
<tr><td>L</td><td>H</td><td>V_2</td><td>VLCD</td></tr>
<tr><td>L</td><td>L</td><td>V_3</td><td>V_{SS}</td></tr>
<tr><td colspan="2">Power save mode</td><td>V_{SS}</td><td>V_{SS}</td></tr>
</table></td><td>102</td></tr>
<tr><td>COM0 to COM66</td><td>O</td><td>LCD column driver outputs
This internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><td rowspan="2">Display data</td><td rowspan="2">M(Internal)</td><td colspan="2">Common drover output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td colspan="2">V_{SS}</td></tr>
<tr><td>H</td><td>L</td><td colspan="2">VLCD</td></tr>
<tr><td>L</td><td>H</td><td colspan="2">V_1</td></tr>
<tr><td>L</td><td>L</td><td colspan="2">V_4</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">V_{SS}</td></tr>
</table></td><td>67</td></tr>
<tr><td>COMS</td><td>O</td><td>Common output for the icons
The output signals of two pins are same. When not used, this pin should be left open.</td><td>2</td></tr>
<tr><td colspan="4">MICROPROCESSOR INTERFACE</td></tr>
<tr><td>P/S</td><td>I</td><td>Microprocessor interface select input pin

P/S= " H “: parallel data input.
P/S= " L “: serial data input. (4-line serial or IIC serial interface)
When 4-line serial interface is applied,
D0 to D5 are fixed to " H ".
RD (E) and WR(R/W) are fixed to " H ".</td><td>1</td></tr>
<tr><td>IMS</td><td>I</td><td>Input mode select
<table>
<tr><td>P/S</td><td>IMS</td><td>State</td></tr>
<tr><td>" H "</td><td>" H "</td><td>6800-series parallel MPU interface</td></tr>
<tr><td>" H "</td><td>" L "</td><td>8080-series parallel MPU interface</td></tr>
<tr><td>" L "</td><td>" H "</td><td>4 Pin-SPI MPU interface</td></tr>
<tr><td>" L "</td><td>" L "</td><td>IIC serial interface</td></tr>
</table></td><td>1</td></tr>
<tr><td>CSB</td><td>I</td><td>Chip select input pins
Data/instruction I/O is enabled only when CSB is " L ". When chip select is non-active, DB0 to DB7 is high impedance.
There is no CSB pin in two line interface, so this pin can fix to ” H” or “L”.</td><td>2</td></tr>
<tr><td>RESB</td><td>I</td><td>Reset input pin
When RESET is " L ", initialization is executed.</td><td>1</td></tr>
<tr><td>A0</td><td>I</td><td>It determines whether the data bits are data or a command.
A0=" H “: Indicates that D0 to D7 are display data.
A0=" L “: Indicates that D0 to D7 are control data.
There is no A0 pin in two line interface, so this pin can fix to ” H” or “L”</td><td>2</td></tr>
</table>

<table>
<tr><td>/WR(R/W)</td><td>I</td><td>Read/Write execution control pin
<table>
<tr><th>IMS</th><th>MPU type</th><th>/WR(R/W)</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>R/W</td><td>Read/Write control input pin
R/W=" H ": read
R/W=" L": write</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WR</td><td>Write enable clock input pin
The data on D0 to D7 are latched at the rising edge of the /WR signal</td></tr>
</table>
When in the serial interface must fixed to " H ".</td><td>2</td></tr>
<tr><td>/RD (E)</td><td>I</td><td>Read/Write execution control pin
<table>
<tr><th>IMS</th><th>MPU Type</th><th>/RD (E)</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read/Write control input pin
R/W=" H ": When E is " H ", D0 to D7 are in an output status.
R/W=" L ": The data on D0 to D7 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is " L ", D0 to D7 are in an output status.</td></tr>
</table>
When in the serial interface must fixed to " H ".</td><td>2</td></tr>
<tr><td>D5 to D0
D6 (SI)
D7 (SCL)</td><td>I/O</td><td>When the Parallel interface is selected (P/S=" H "): 8-bit interface
8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus.
When chip select is not active, D0 to D7 is high impedance.
When the serial interface is selected (P/S=" L " & IMS=”H”):4-line
D7: serial input clock (SCL)
D6: serial input data (SI)
D5, D4, D3, D2, D1, D0: must fix to “H”..
When chip select is not active, D0 to D7 is high impedance.
When the IIC serial interface is selected (P/S=" L " & IMS=”L”)
D0 is SA0
D1 is SA1
D2,D3 are SDA_IN
D4,D5,D6 are SDA_OUT
D7 is SCL
SA1, SA0: Is slave address (SA) bit1, 0, must fix to “H” or “L”
SDA_IN: serial input data
SDA_OUT: serial data acknowledge output for the I^2C interface.
SCL: serial clock input
By connecting SDA_OUT to SDA_IN externally, the SDA line becomes fully 2-line interface compatible. Having the acknowledge output separated from the serial data line is advantageous in chip on glass (COG) applications. In COG application where the track resistance from the SDA_OUT pad to the system SDA line can be significant, a potential divider is generated by the bus pull-up resistor and the ITO track resistance. It is possible the during the acknowledge cycle the ST7568 will not be able to create a valid logic 0 level. By splitting the SDA_IN input from the SDA_OUT output the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDA_OUT pad to the system SDA line to guarantee a valid low level.
All Pad of SDA_IN, SDA_OUT must be connected together (SDA)</td><td>16</td></tr>
</table>

MODE	**I**	Use this pin can select 65 duty or 68 duty mode When MODE='L': select 65 duty (64 com + coms) When MODE='H': select 68 duty (67 com + coms)	**1**
LCD DRIVER SUPPLY			
OSC	**I**	Oscillator When the on-chip oscillator is used, this input must be connected to VDD. An external clock signal, if used, is connected to this input. If the oscillator and external clock are both inhibited by connecting the OSC pin to VSS the display is not clocked and may be left in a DC state. To avoid this, the chip should always be put into Power Down Mode before stopping the clock.	**2**
Power Supply Pins			
V_{SS1}	**Power Supply**	Digital Ground. The 2 supply rails V_{SS1} and V_{SS2} must be connected together.	**6**
V_{SS2}	**Power Supply**	Analog Ground. The 2 supply rails V_{SS1} and V_{SS2} must be connected together.	**12**
VDD	**Power Supply**	Digital Supply voltage. The 2 supply rails VDD and V_{DD2} could be connected together. If Digital Option pin is high, must be this level	**9**
V_{DD2}	**Power Supply**	Analog Supply voltage. The 2 supply rails VDD and V_{DD2} could be connected together.	**12**
V_{LCDOUT}	**Power Supply**	If the internal voltage generator is used, the V_{LCDIN} & V_{LCDOUT} must be connected together and series one capacitor to VSS2. If an external supply is used this pin must be left open.	**6**
V_{LCDIN}	**Power Supply**	If the internal voltage generator is used, the V_{LCDIN} & V_{LCDOUT} must be connected together. An external supply voltage can be supplied using the V_{LCDIN} pad. This pad is for external multiple voltage input. In this case, VLCDOUT has to be left open,	**6**
V1, V2, V3, V4	**Power Supply**	This is a multi-level power supply for the liquid crystal. $V_{LCDIN} \geq V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq VSS$	**8**
VRS	**Power Supply**	Monitor Voltage Regulator level, must be left open.	**1**
Test Pin			
Test0~Test10	**T**	To test used. Test0~Test8 must floating Test9 could be connected out for monitor the VLCD(V0) voltage Test10 must connect to VDD	**11**

Recommend ITO Resistance Value

PIN Name	ITO Resistance
P/S, IMS, MODE, OSC, Test9, Test10	No Limitation
Test[0:8]	Floating
VDD, VDD2, VSS1, VSS2, VRS, VLCD	<100Ω
CSB, E, R/W, A0, D0…D7	<1KΩ
V0, V1 , V2 , V3 , V4	<500Ω
RESB	<10KΩ

6. FUNCTIONS DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

There is CSB pin for chip selection. The ST7568 can interface with an MPU when CSB is "L". When CSB is “H”, these pins are set to any other combination, A0, /RD(E), and /WR(R/W) inputs are disabled and D0 to D7 are to be high impedance. And, in case of 4-line serial interface, the internal shift register and the counter are reset. In case of IIC serial interface CSB is a no use pin which must be fixed to high or low

Parallel / Serial Interface

ST7568 has four types of interface with an MPU, which are two serial and two parallel interfaces. This parallel or serial interface is determined by P/S pin as shown in table 1.

Table 1. Parallel/Serial Interface Mode

Type	P/S	IMS	CSB	Interface mode
Parallel	H	H	CSB	6800-series MPU interface
		L		8080-series MPU interface
Serial	L	H	CSB	4-pin SPI interface
		L	No use	IIC serial interface

Parallel Interface (P/S = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by IMS as shown in table 2. The type of data transfer is determined by signals at A0, /RD (E) and /WR(R/W) as shown in table 3.

Table 2. Microprocessor Selection for Parallel Interface

IMS	CSB	A0	/RD (E)	/WR (R/W)	DB0 to DB7	MPU bus
H	CSB	A0	E	R/W	DB0 to DB7	6800-series
L	CSB	A0	/RD	/WR	DB0 to DB7	8080-series

Table 3. Parallel Data Transfer

Common	6800-series		8080-series		Description
RS	E (/RD)	R/W (/WR)	/RD (E)	/WR (R/W)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

NOTE: When /RD (E) pin is always pulled high for 6800-series interface, it can be used CSB for enable signal. In this case, interface data is latched at the rising edge of CSB and the type of data transfer is determined by signals at A0, /WR(R/W) as in case of 6800-series mode.

Serial Interface (P/S=" L ")

Serial Mode	P/S	IMS	CSB	A0	/RD (E)	/WR (R/W)
4-line SPI interface	L	H	CSB	A0	No Used	No Used
IIC serial interface	L	L	No Used	No Used	No Used	No Used

IMS=” L “, P/S=” H “: 4-line SPI interface

When the ST7568 is active (CSB=”L”), serial data (D7) and serial clock (D6) inputs are enabled. And not active, the internal 8-bit shift register and the 3-bit counter are reset. The display data/command indication may be controlled either via software or the Register Select (A0) Pin, based on the setting of P/S. When the A0 pin is used (IMS = “H”), data is display data when A0 is high, and command data when A0 is low. If messages on the data pin are data rather than command, MCU should send Data direction to the SI data signal pin,. And the DDRAM column address pointer will be increased by one pixel data (2 bits) automatically. The next bytes after the display data string are handled as command data.

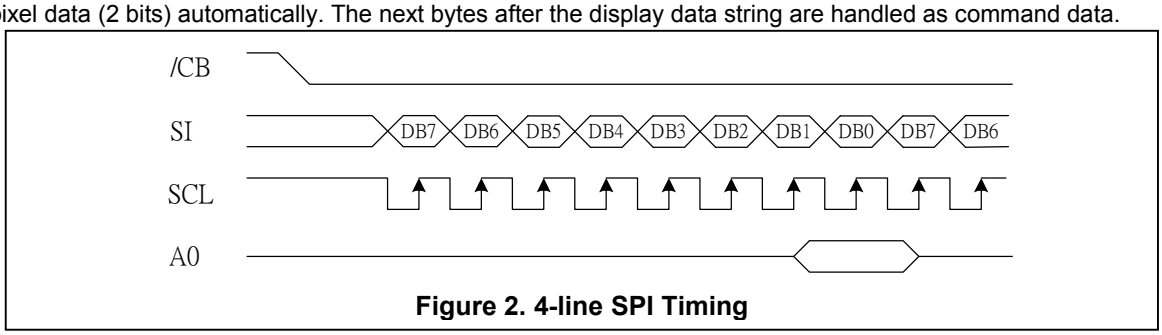


Figure 2. 4-line SPI Timing

IMS=" L ", P/S=" L ":I²C Interface

The I²C interface send RAM data and executes the commands sent via the I²C Interface. It could send data it to the RAM. The I²C Interface is two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Fig.3.

START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.4.

SYSTEM CONFIGURATION

The system configuration is illustrated in Fig.5.

· Transmitter: the device, which sends the data to the bus
· Master: the device, which initiates a transfer, generates clock signals and terminates a transfer
· Slave: the device addressed by a master
· Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message
· Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
· Synchronization: procedure to synchronize the clock signals of two or more devices.

ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I²C Interface is illustrated in Fig.6.

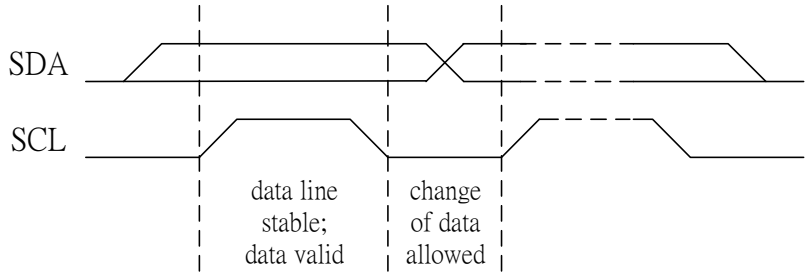


Fig .3 Bit transfer

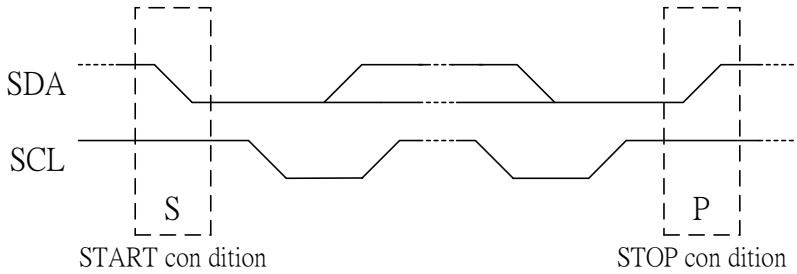


Fig .4 Definition of START and STOP conditions

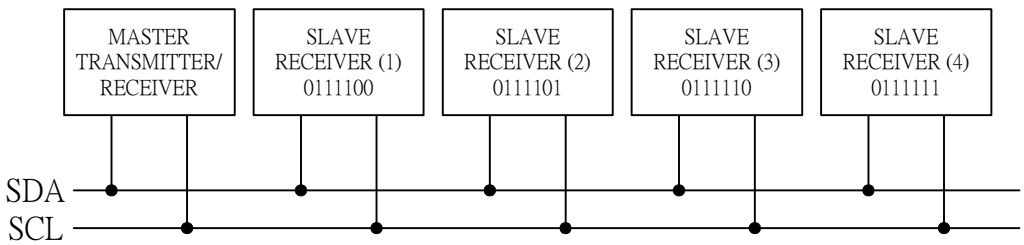


Fig .5 System configuration

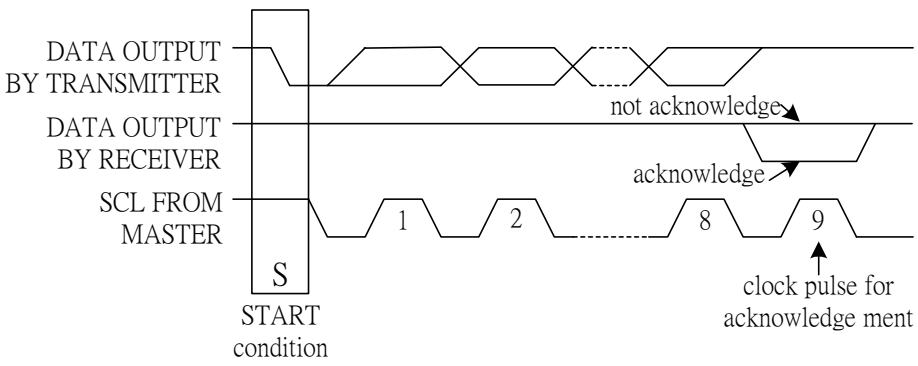


Fig .6 Acknowledgement on the 2-line Interface

I²C Interface protocol

The ST7568 supports command, data write addressed slaves on the bus.
Before any data is transmitted on the I²C Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111100,0111101, 0111110 and 0111111) are reserved for the ST7568. The least significant bit of the slave address is set by connecting the input SA0 and SA1 to either logic 0 (or logic 1 (VDD).
The I²C Interface protocol is illustrated in Fig.7.

The sequence is initiated with a START condition (S) from the I²C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.
A command word consists of a control byte, which defines Co and A0, plus a data byte.
The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the A0 bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the A0 bit setting; either a series of display data bytes or command data bytes may follow. If the A0 bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended ST7568i device. If the A0 bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the I²C INTERFACE-bus master issues a STOP condition (P).If the R/W bit is set to logic 1 the chip will output data immediately after the slave address if the A0 bit, which was sent during the last write access, is set to logic 0. If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

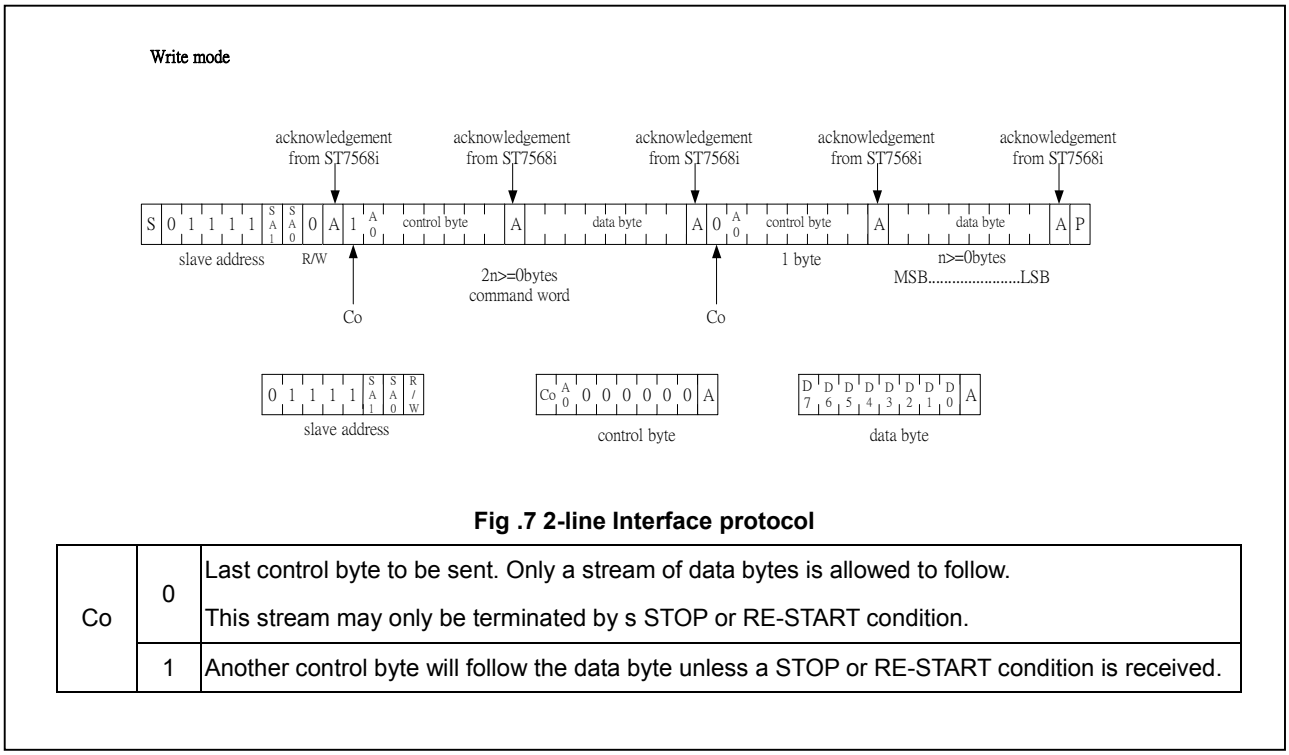


Fig .7 2-line Interface protocol

Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by s STOP or RE-START condition.
	1	Another control byte will follow the data byte unless a STOP or RE-START condition is received.

Busy Flag

The Busy Flag indicates whether the ST7568 is operating or not. When D7 is "H" in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

Data Transfer

The ST7568 uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in figure 8. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 9. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

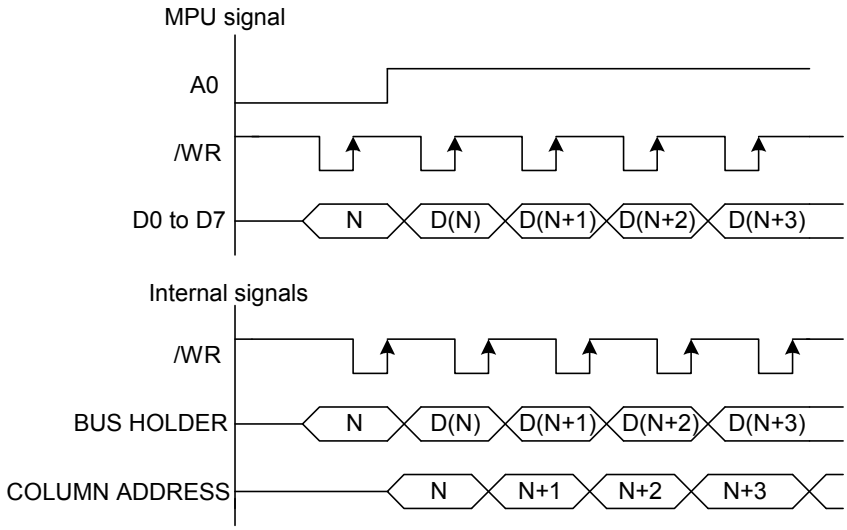


Figure 8. Write Timing

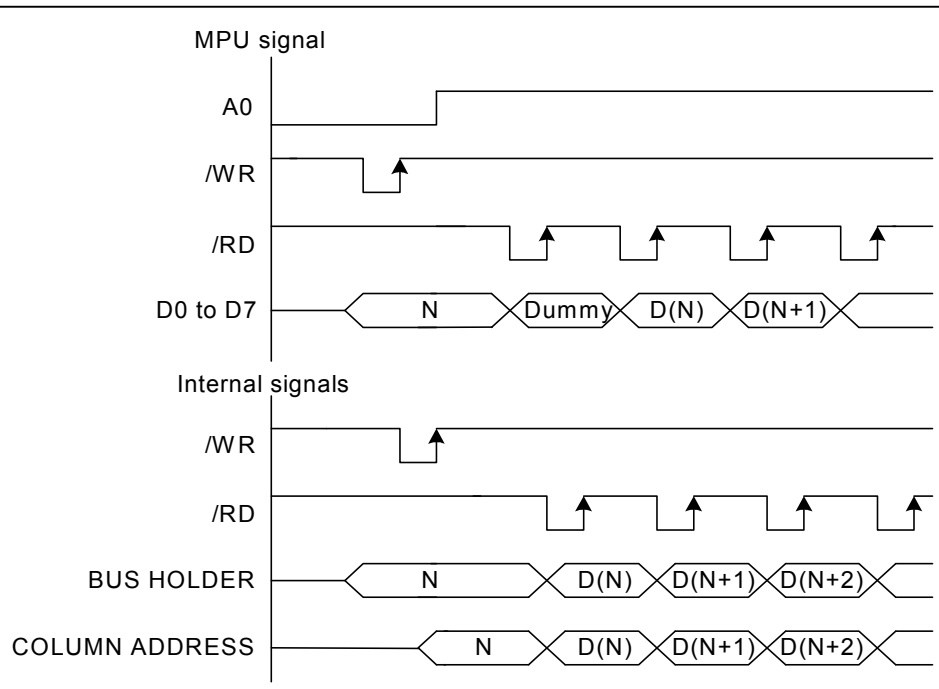


Figure 9.Read Timing

DISPLAY DATA RAM (DDRAM)

The ST7568 contains a 68X102X2 bit static RAM that stores the display data. The display data RAM store the dot data for the LCD. It has a 68(8 pageX8 bit +1 pageX3 bit +1 pageX1 bit) X102 X2. There is a direct correspondence between X-address and column output number. It is 68-row by 102-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 65 rows are divided into 8 pages of 8 lines (0~63 COM) and 8th page with three line (D0 ~D2)(64~ 66 COM) and 9th page with a single line (D0 only)(67 row—COMS (ICON). Data is read from or written to the 8 lines of each page directly through D0 to D7. The display data of D0 to D7 from the microprocessor correspond to the LCD common lines. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM shown in figure 6. It incorporates 4-bit Page Address register changed by only the “Set Page” instruction. Page Address 9 is a special RAM area for the icons and display data D0 is only valid.

Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting Line Address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM as shown in figure 10. It incorporates 7-bit Line Address register changed by only the initial display line instruction and 7-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the line address for transferring the 102-bit RAM data to the display data latch circuit. When icon is selected by setting icon page address, display data of icons are not scrolled because the MPU cannot access Line Address of icons.

Column Address Circuit

Column Address Circuit has an 8-bit preset counter that provides Column Address to the Display Data RAM as shown in figure11. The display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously.

Register MX and MY selection instruction makes it possible to invert the relationship between the Column Address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing MX select instruction. Refer to the following figure 12.

SEG Output

SEG Output MX	SEG0 SEG101
“0”	seg0 → Segment Address → seg101
“1”	seg101 ← Segment Address ← seg0

Com Output

SEG Output MY	Com0 Com66	Coms
“0”	com0 → Common Address → com66	Coms
“1”	com66 ← Common Address ← com0	Coms

Status	COM Scan Direction	
	1/65 DUTY	1/68 DUTY
Normal	COM0 → COM63	COM0 → COM66
Reverse	COM63 → COM0	COM66 → COM0

Duty	MY	Common output pins			
		Com [0:31]	Com [32:34]	Com [35:66]	Coms
1/68	0	Com [0:66]			Coms
	1	Com [66:0]			Coms
1/65	0	Com [0:31]	Reverse	Com [32:63]	Coms
	1	Com [63:32]	Reverse	Com [31:0]	Coms

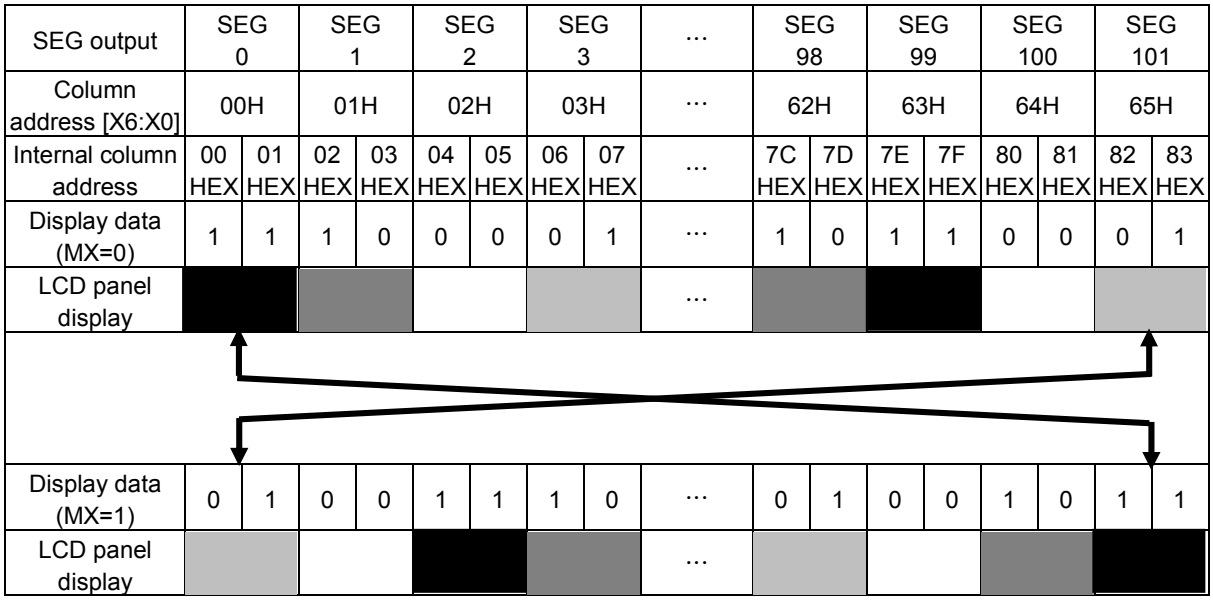


Figure10.The Relationship between the Column Address and The Segment Outputs

ADDRESSING

Data is downloaded in bytes into the RAM matrix of ST7568 as indicated in Figs.11, 12,13. The display RAM has a matrix of 68 by 102 × 2 bits. The address pointer addresses the columns. The address ranges are: X 0 to 101 (1100101), Y 0 to 9 (1001). Addresses outside these ranges are not allowed.

In vertical addressing mode (V=1) the Y address increments after each byte (see Fig.13). After the last Y address (Y = 9) Y wraps around to 0 and X increments to address the next column.

In horizontal addressing mode (V=0) the X address increments after each byte (see Fig.12). After the last X address (X = 101) X wraps around to 0 and Y increments to address the next row.

After the very last address (X = 101, Y = 9) the address pointers wrap around to address (X = 0, Y =0)

Data structure

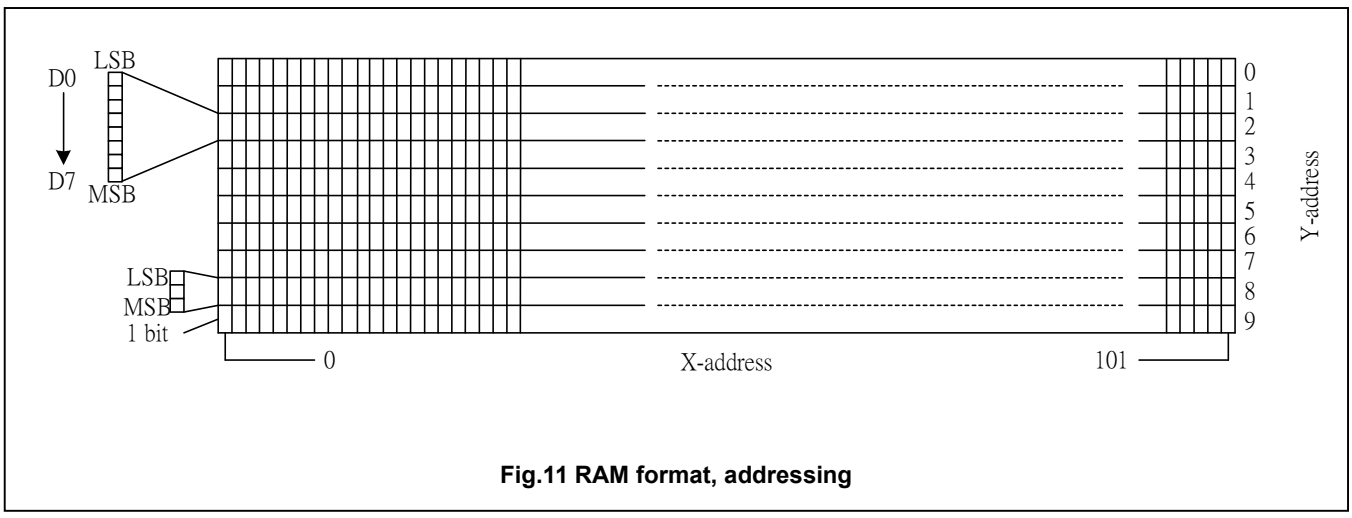


Fig.11 RAM format, addressing

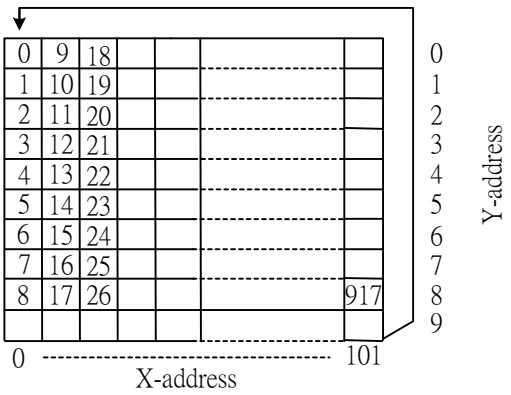


Fig.12 Sequence of writing data bytes into RAM with vertical addressing (V=1)

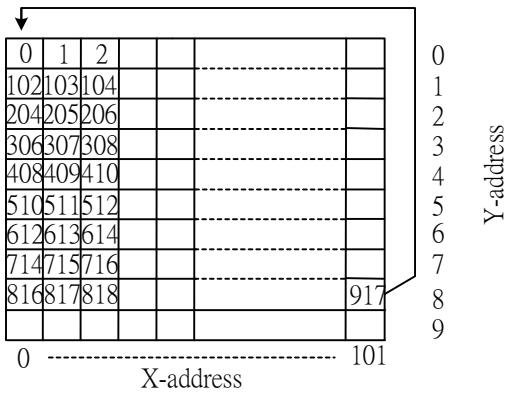


Fig.13 sequence of writing data bytes into RAM with horizontal addressing (V=0)

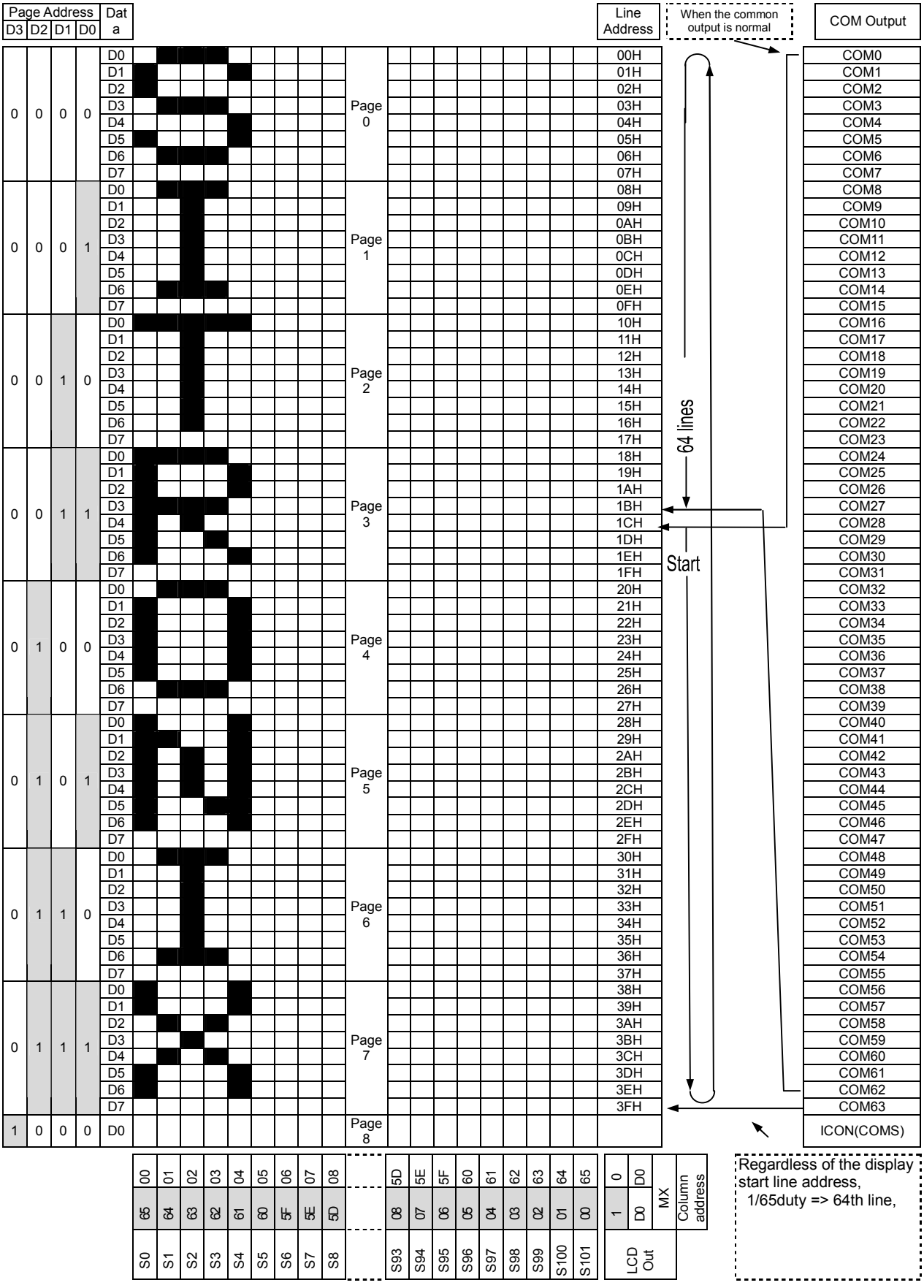
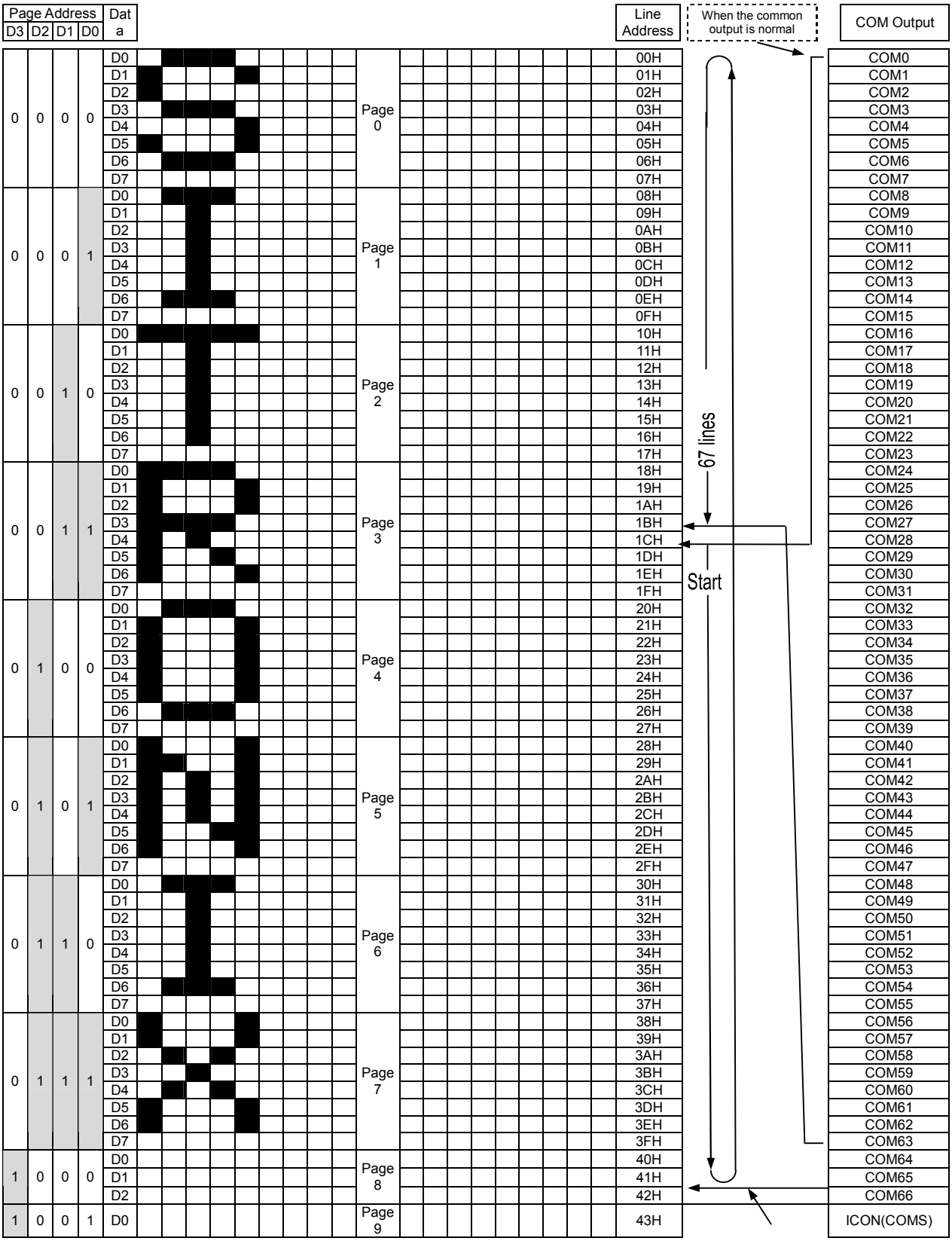


Figure 14. Display Data RAM Map (65 COM)



Display Data RAM Map (68 COM)

LCD DISPLAY CIRCUITS

FRC (Frame Rate Control) and PWM (Pulse Width Modulation) Function Circuit

The ST7568 incorporates an FRC function and a PWM function circuit to display a 4-level gray scale. The FRC function and PWM utilize liquid crystal characteristics whose transmittance is changed by an effective value of applied voltage. The ST7568 provides four 4-bit palette-registers to assign the desired gray level. The instructions and the RESB Pin set these registers.

-Gray Scale Table of 4 FRC (Frame Rate Control)

Gray scale level	MSB (D7 TO D4)	LSB (D3 TO D0)
White	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)
Light gray	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)
Dark gray	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)
Black	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)

-Gray Scale Table of 3 FRC (Frame Rate Control)

Gray scale level	MSB (D7 TO D4)	LSB (D3 TO D0)
White	2nd FR (FR2)	1st FR (FR1)
	XXXX	3rd FR (FR3)
Light gray	2nd FR (FR2)	1st FR (FR1)
	XXXX	3rd FR (FR3)
Dark gray	2nd FR (FR2)	1st FR (FR1)
	XXXX	3rd FR (FR3)
Black	2nd FR (FR2)	1st FR (FR1)
	XXXX	3rd FR (FR3)

-Gray Scale Table of 15 PWM (Pulse Width Modulation)

Dec	Hex	4-bits	PWM (on width)	Note
0	00	0000	0(0/15)	Brighter
1	01	0001	1/15	↑
2	02	0010	2/15	
3	03	0011	3/15	
4	04	0100	4/15	
5	05	0101	5/15	
6	06	0110	6/15	
7	07	0111	7/15	
8	08	1000	8/15	
9	09	1001	9/15	
10	0A	1010	10/15	
11	0B	1011	11/15	
12	0C	1100	12/15	
13	0D	1101	13/15	
14	0E	1110	14/15	↓
15	0F	1111	1(15/15)	Darker

-Gray Scale Table of 12 PWM (Pulse Width Modulation)

Dec	Hex	4-bits	PWM (on width)	Note
0	00	0000	0(0/12)	Brighter
1	01	0001	1/12	
2	02	0010	2/12	
3	03	0011	3/12	
4	04	0100	4/12	
5	05	0101	5/12	
6	06	0110	6/12	
7	07	0111	7/12	
8	08	1000	8/12	
9	09	1001	9/12	
10	0A	1010	10/12	
11	0B	1011	11/12	
12	0C	1100	1(12/12)	Darker
13	0D	1101	0/12	This area is selected to OFF level (0/12 level)
14	0E	1110	0/12	
15	0F	1111	0/12	

-Gray Scale Table of 9 PWM (Pulse Width Modulation)

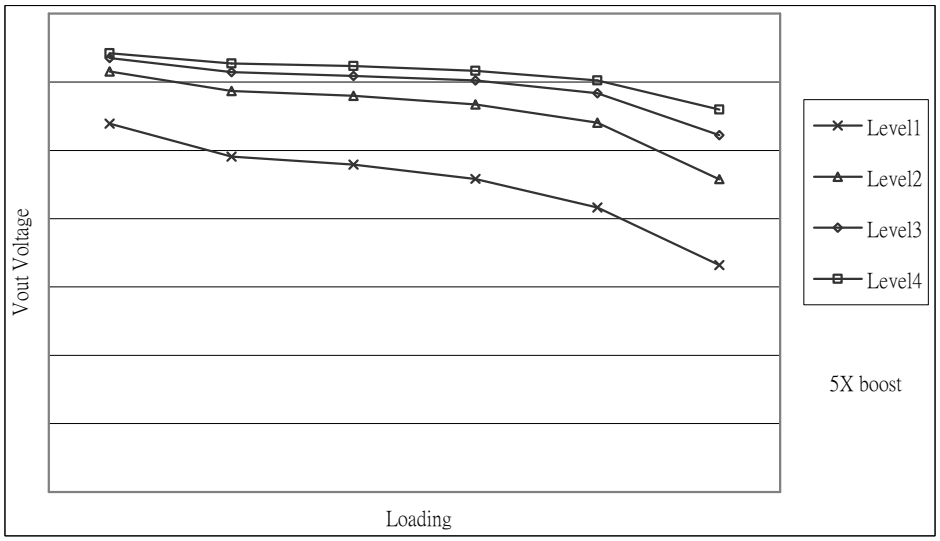
Dec	Hex	4-bits	PWM (on width)	Note
0	00	0000	0(0/9)	Brighter
1	01	0001	1/9	
2	02	0010	2/9	
3	03	0011	3/9	
4	04	0100	4/9	
5	05	0101	5/9	
6	06	0110	6/9	
7	07	0111	7/9	
8	08	1000	8/9	
9	09	1001	1(9/9)	Darker
10	0A	1010	0/9	This area is selected to OFF level (0/9 level)
11	0B	1011	0/9	
12	0C	1100	0/9	
13	0D	1101	0/9	
14	0E	1110	0/9	
15	0F	1111	0/9	

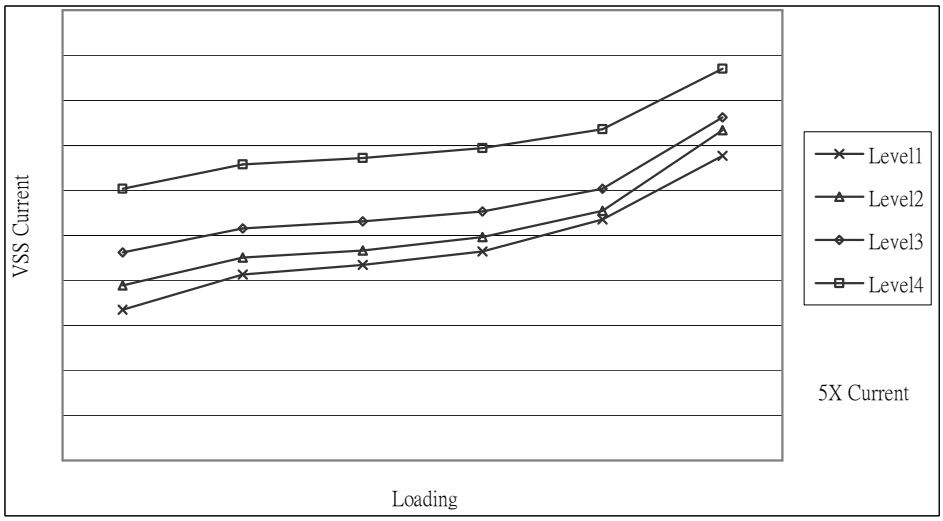
Booster Efficiency

By Booster Stages (2X, 3X, 4X, 5X) and Booster Efficiency (Level1~4) commands, we could easily set the best Booster performance with suitable current consumption. If the Booster Efficiency is set to higher level (level4 is higher than level1), The Boost Efficiency is better than lower level, and it just need few more power consumption current. It could be applied to each multiple voltage Condition.

When the LCD Panel loading is heavier. Then the Performance of Booster will be not in a good working condition. We could set the BE level to be higher. We do not need to change to higher Booster Stage, and just need few more current.

The Booster Efficiency Command could be used together with Booster Stage Command to choose one best Boost output condition. We could see the Boost Stage Command as a large scale operation, and see the Booster Efficiency Command as a small scale operation. These commands are very convenient for using





Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC input must be connected to VDD. An external clock signal, if used, is connected to this input.

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL (internal), generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 102-bit display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M) which enables the LCD driver to make a AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Figure 15.

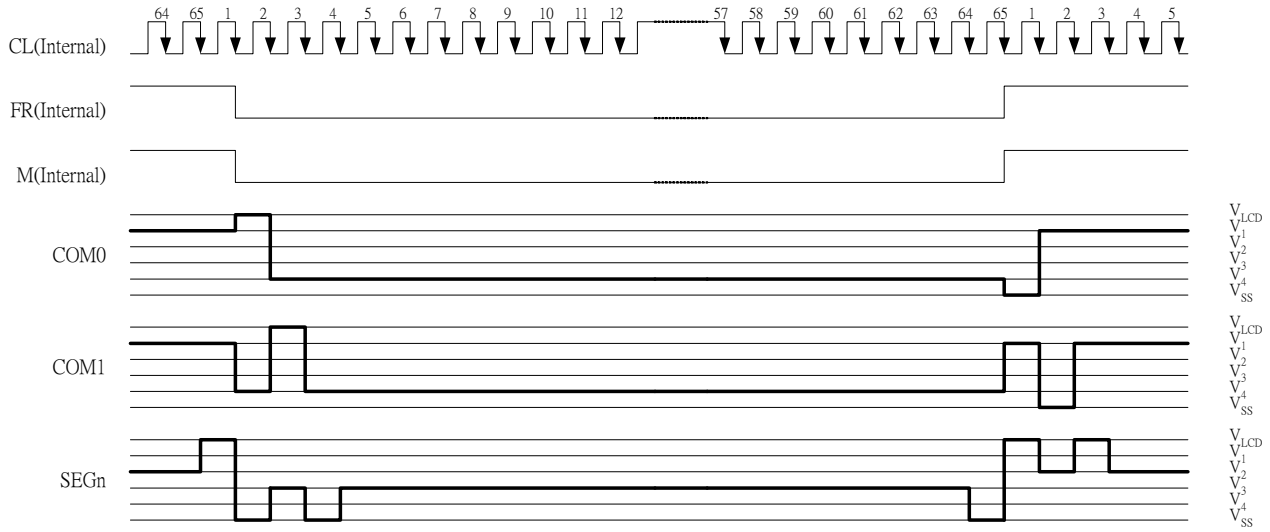


Figure 15 2-frame AC Driving Waveform (Duty Ratio: 1/65)

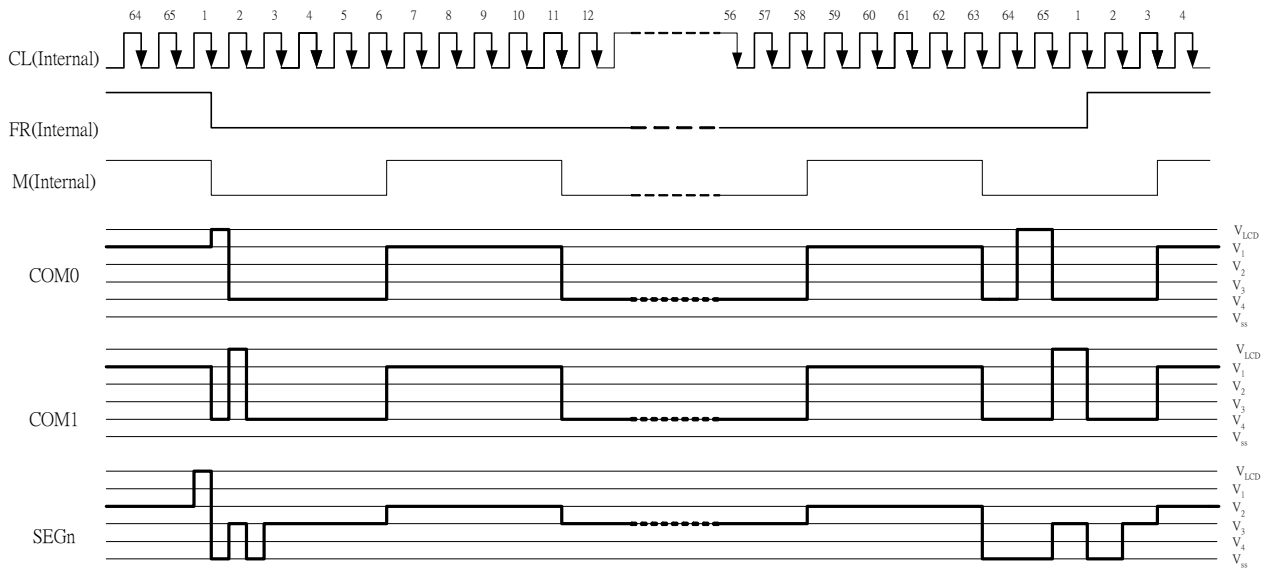


Figure 16. N-Line Inversion Driving Waveform (N=5,Duty Ratio=1/65)

LCD DRIVER CIRCUIT

68-channel common drivers and 102-channel segment drivers configure this driver circuit. This LCD panel driver voltage depends on the combination of display data and M signal.

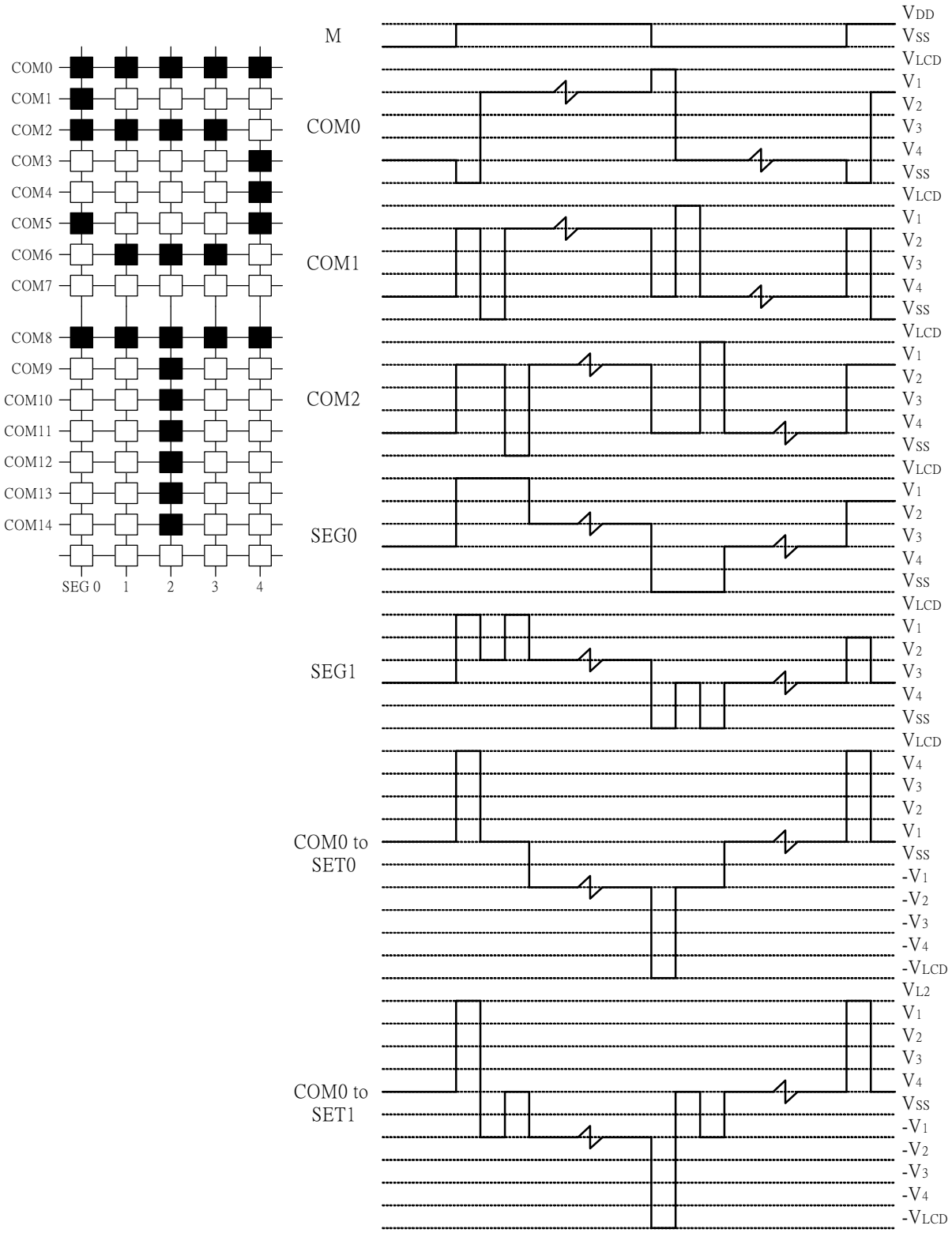


Fig.17 Typical LCD driver waveforms

Partial Display on LCD

The ST7568 realizes the Partial Display function on LCD with low-duty driving for saving power consumption and showing the various display duty. To show the various display duty on LCD, LCD driving duty and bias are programmable via the instruction. And, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages.

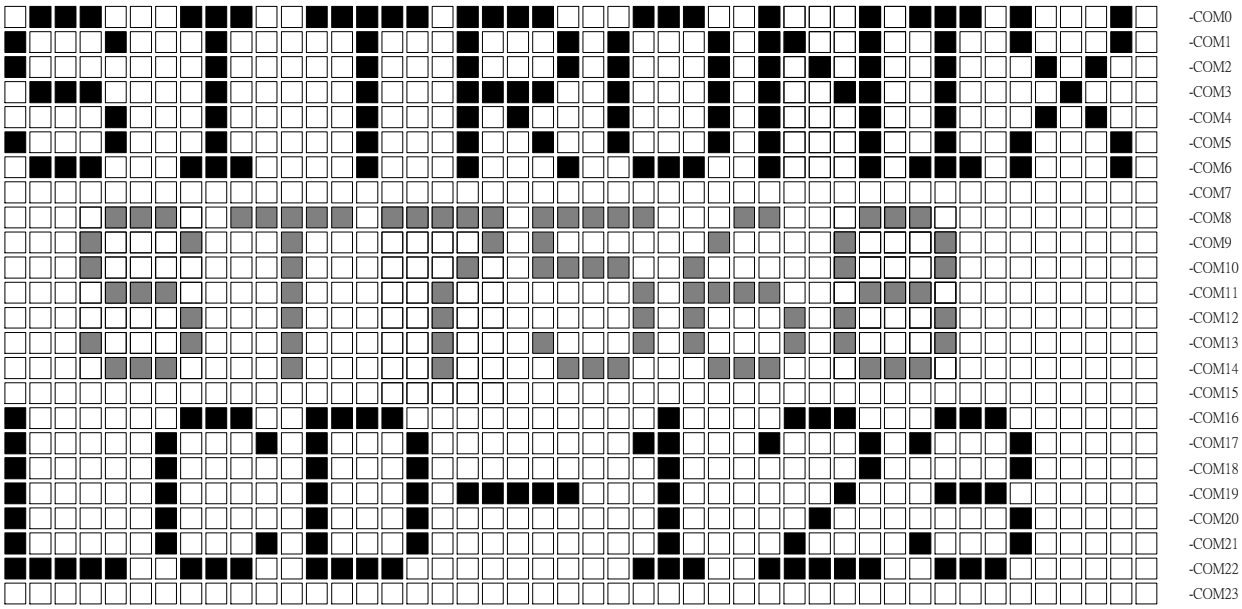


Figure 18.Reference Example for Partial Display

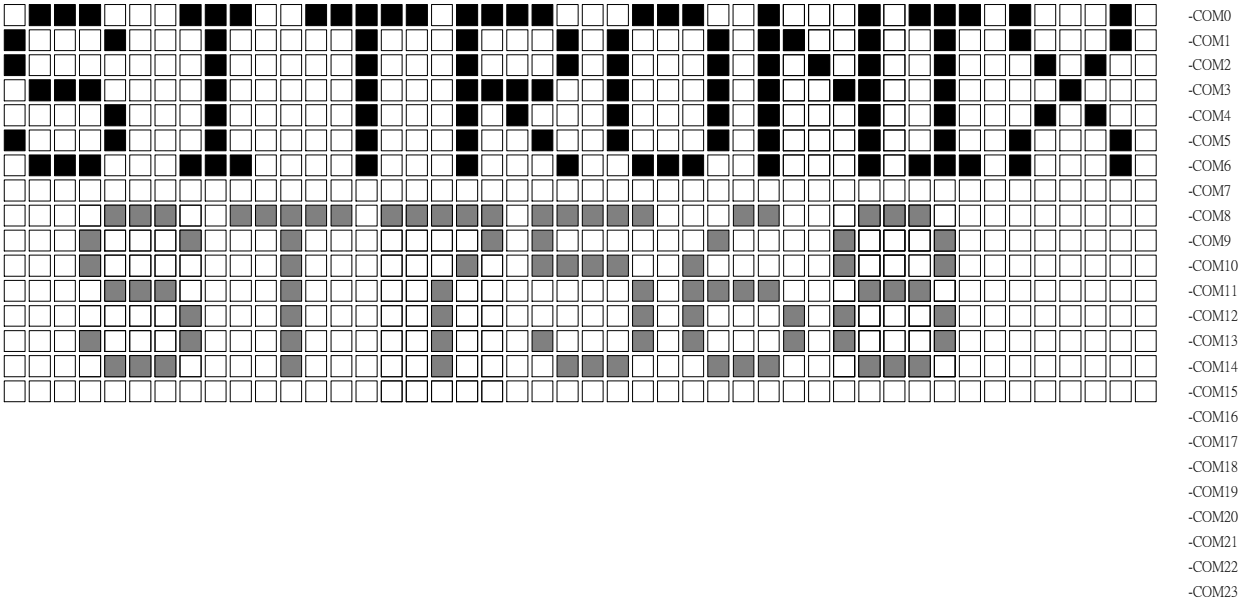


Figure 19.Partial Display (Partial Display Duty=16,initial COM0=0)

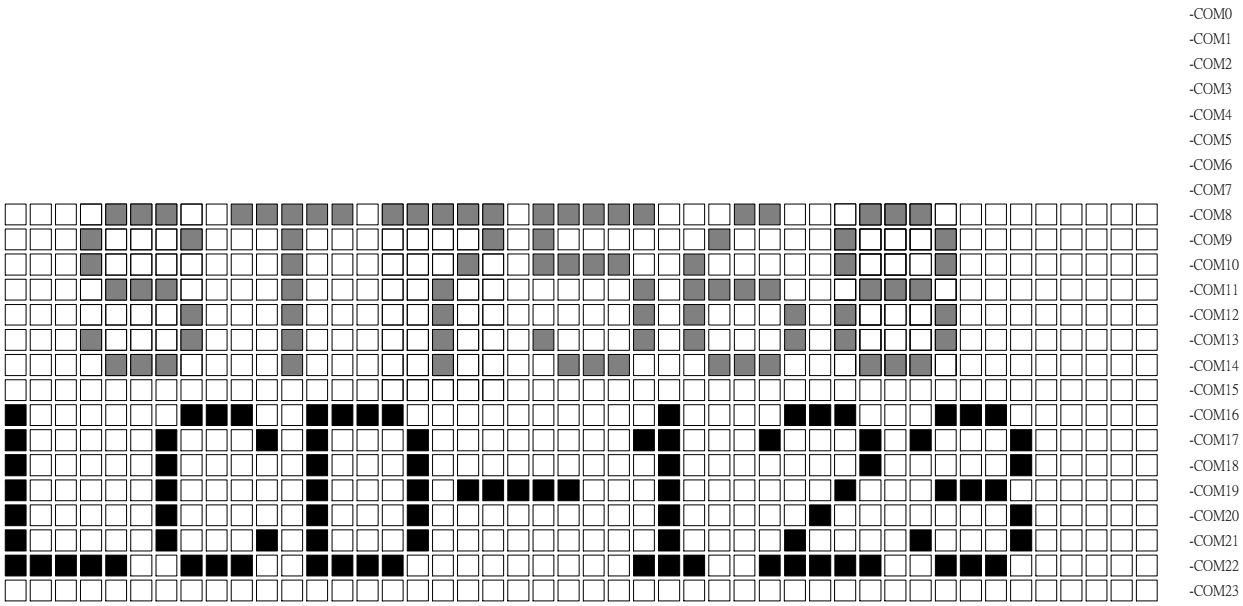


Figure 20.Moving Display (Partial Display Duty=16,Initial COM0=8)

7. RESET CIRCUIT

Setting RESB to “L” or Reset instruction can initialize internal function.
When RESB becomes “L”, following procedure is occurred.
Page address: 0
Column address: 0
Read-modify-write: OFF
Display ON / OFF: OFF
Initial display line: 0 (first)
Initial COM0 register: 0 (COM0)
Reverse display ON / OFF: OFF (normal)
N-line inversion register: 0 (disable)
Entire Display ON/OFF: OFF
ICON Control Register ON/OFF: OFF (ICON disable)
COM Scan Direction MY: 0
SEG Select Direction MX: 0
Oscillator: OFF
Power Save Mode: Release
Display Data Length register: 0 (for SPI mode)
White mode set: OFF
White palette register (WG3, WG2, WG1, WG0) = (0, 0, 0, 0)
Light gray mode set: OFF
Light gray palette register (LG3, LG2, LG1, LG0) = (0, 0, 0, 0)
Dark gray mode set: OFF
Dark gray palette register (DG3, DG2, DG1, DG0) = (1, 1, 1, 1)
Black mode set: OFF
Black palette register (BG3, BG2, BG1, BG0) = (1, 1, 1, 1)
FRC, PWM mode: 4FRC, 9PWM
Power down mode (PD = 1)
Horizontal addressing (V = 0) normal instruction set (H = 0)
Display blank (E = D = 0)
Address counter X [6:0] = 0, Y [2:0] = 0
Bias system (BS [2:0] = 0)
VLCD is equal to 0; the HV generator is switched off (VOP [6:0] = 0)
After power-on, RAM data are undefined

While RESB is “L” or reset instruction is executed, no instruction except read status can be accepted. Reset status appears at DB6. After DB6 becomes ”L”, any instruction can be accepted. RESB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESB is essential before used.

8. INSTRUCTION TABLE

INSTRUCTION	A0	WR (R/W)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
H=0 or 1											
NOP	0	0	0	0	0	0	0	0	0	0	No operation
Reset	0	0	0	0	0	0	0	0	1	1	Internal reset
Function set	0	0	0	0	1	0	0	PD	V	H	Power-down; entry mode; Extended instruction control
Ext. display control	0	0	0	0	1	0	1	MX	MY	PS	Mirror X, Mirror Y, partial screen mode
Window size for Partial screen	0	0	0	0	1	1	0	0	0	WS	Partial screen size 0:8 row, 1:16 row
Display part	0	0	0	0	1	1	1	DP_2	DP_1	DP_0	Sets display part for partial screen mode
Read status byte	0	1	PD	RST	BUSY	D	E	1	0	1	Read status byte
Read data	1	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Read data from RAM
Write data	1	0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Write data to RAM

* Reset instruction could not applied on IIC serial interface

INSTRUCTION	A0	WR (R/W)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
H=0											
Set V_{LCD} range	0	0	0	0	0	0	0	1	0	PRS	V_{LCD} range L/H select
END	0	0	0	0	0	0	0	1	1	0	Release read/modify/write
Read/modify/write	0	0	0	0	0	0	0	1	1	1	RAM address at R:+0 , W:+1
Display control	0	0	0	0	0	0	1	D	0	E	Set display configuration
Set Y address of RAM	0	0	0	0	0	1	Y_3	Y_2	Y_1	Y_0	Sets Y address of RAM $0 \leqq Y \leqq 9$
Start line set	0	0	0	1	S_5	S_4	S_3	S_2	S_1	S_0	Specify the initial display line to realize vertical scrolling
Set X address of RAM	0	0	1	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Sets X address of RAM $0 \leqq X \leqq 101$
H=1											
Booster Efficiency	0	0	0	0	0	0	0	1	BE1	BE0	Booster Efficiency Set
Booster stages	0	0	0	0	0	0	1	0	PC_1	PC_0	# of booster voltage multiplication
Release N-line inversion	0	0	0	0	0	0	1	1	0	0	Release N-line inversion
Set N-line inversion	0 0	0 0	0 X	0 X	0 X	0 N_4	1 N_3	1 N_2	0 N_1	1 N_0	Sets N-line inversion
S/W Internal register initial	0 0	0 0	0 0	0 0	0 0	0 1	1 0	1 0	1 1	0 0	S/W Internal register initial
Frame freq. Adjust and set FRC, PWM	0 0	0 0	0 X	0 FR_2	0 FR_1	0 FR_0	1 X	1 FRC	1 PWM_1	1 PWM_0	Adjust frame frequency and FRC and PWM mode
Bias system	0	0	0	0	0	1	0	BS_2	BS_1	BS_0	Sets bias system (BSx)
Set white mode and $1^{st}/2^{nd}$ frame	0 0	0 0	0 WB_3	0 WB_2	0 WB_1	1 WB_0	1 WA_3	0 WA_2	0 WA_1	0 WA_0	Set white mode and $1^{st}/2^{nd}$ frame, set pulse width
Set white mode and $3^{rd}/4^{th}$ frame	0 0	0 0	0 WD_3	0 WD_2	0 WD_1	1 WD_0	1 WC_3	0 WC_2	0 WC_1	1 WC_0	Set white mode and $3^{rd}/4^{th}$ frame, set pulse width
Set light gray mode $1^{st}/2^{nd}$ frame	0 0	0 0	0 LB_3	0 LB_2	0 LB_1	1 LB_0	1 LA_3	0 LA_2	1 LA_1	0 LA_0	Set light gray mode and $1^{st}/2^{nd}$ frame set pulse width
Set light gray mode $3^{rd}/4^{th}$ frame	0 0	0 0	0 LD_3	0 LD_2	0 LD_1	1 LD_0	1 LC_3	0 LC_2	1 LC_1	1 LC_0	Set light gray mode and $3^{rd}/4^{th}$ frame, set pulse width
Set dark gray mode and $1^{st}/2^{nd}$ frame	0 0	0 0	0 DB_3	0 DB_2	0 DB_1	1 DB_0	1 DA_3	1 DA_2	0 DA_1	0 DA_0	Set dark gray mode and $1^{st}/2^{nd}$ frame, set pulse width
Set dark gray and $3^{rd}/4^{th}$ frame	0 0	0 0	0 DD_3	0 DD_2	0 DD_1	1 DD_0	1 DC_3	1 DC_2	0 DC_1	1 DC_0	Set dark gray mode and $3^{rd}/4^{th}$ frame, set pulse width
Set block mode and $1^{st}/2^{nd}$ frame	0 0	0 0	0 BB_3	0 BB_2	0 BB_1	1 BB_0	1 BA_3	1 BA_2	1 BA_1	0 BA_0	Set black mode and $1^{st}/2^{nd}$ Frame, set pulse width
Set block mode and $3^{rd}/4^{th}$ frame	0 0	0 0	0 DB_3	0 DB_2	0 DB_1	0 DB_0	1 BC_3	1 BC_2	1 BC_1	1 BC_0	Set black mode and $3^{rd}/4^{th}$ frame, set pulse width
Reserved	0	0	0	1	X	X	X	X	X	X	Do not use
Set V_{OP}	0	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}	Write V_{OP} to register

9. INSTRUCTION DESCRIPTION

H="0" or "1"

Reset

This instruction resets initial display line, column address, page address, and common output status select to their initial status.This instruction cannot initialize the LCD power supply, which is initialized by the RESB pin.
Note: This instruction is invalid in IIC serial interface

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	1	1

Function Set

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	PD	V	H

Flag	Description
PD	All LCD outputs at VSS (display off), bias generator and VLCD generator off, VLCD can be disconnected, oscillator off (external clock possible), RAM contents not cleared; RAM data can be written. PD=0:chip is active PD=1:chip is in power down mode
V	When V = 0, the horizontal addressing is selected. The data is written into the DDRAM as shown in Fig13. When V = 1, the vertical addressing is selected. The data is written into the DDRAM as shown in Fig12
H	When H = 0 the commands 'display control', 'set Y address' and 'set X address' can be performed, when H = 1 the others can be executed. The commands 'write data' and 'function set' can be executed in both cases. H=0:use basic instruction set H=1:use extended instruction set

Ext. display byte

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	MX	MY	PS

Flag	Description
MX	SEG bi-direction selection MY=0:normal direction (SEG0→SEG101) MY=1:reverse direction (SEG101→SEG0)
MY	COM bi-direction selection MY=0:normal direction (COM0→COM67) MY=1:reverse direction (COM67→COM0)
PS	Full display mode or partial screen mode selection PS=0:Full display mode with MUX 1:68 PS=1:Partial screen mode with MUX 1:8 or MUX 1:16

Window sizes for partial scan

This instruction can select partial screen size, partial screen 8 rows when WS is low and partial screen 16 rows when WS is height.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	0	0	WS

Display part

This instruction can select partial screen modes

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	1	DP_2	DP_1	DP_0

Flag	Status			Description
DP_2 DP_1 DP_0	0	0	0	RAM bank 0 to 1 (row0~row7)
	0	0	1	RAM bank 1 to 2 (row8~row15)
	0	1	0	RAM bank 2 to 3 (row16~row23)
	0	1	1	RAM bank 3 to 4 (row24~row31)
	1	0	0	RAM bank 4 to 5 (row32~row39)
	1	0	1	RAM bank 5 to 6 (row40~row47)
	1	1	0	RAM bank 6 to 7 (row48~row55)
	1	1	1	RAM bank 7 to 8 (row56~row63)

Read status byte

Indicates the internal status of the ST7568

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	PD	RST	BUSY	D	E	1	0	1

Flag	Description		
PD	PD=0:chip is active PD=1:chip is in power down mode		
RST	Indicates the initialization is in progress by RESET signal 0: chip is active,1:chip is being reset		
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes LOW. 0:chip is active 1:chip is being busy		
D,E	D	E	The bits D and E select the display mode.
	0	0	Display blank
	0	1	All display segments on
	1	0	Normal mode
	1	1	Inverse video mode
D2~D0	ST7568 will return the fix data “101” as identification bit		

Write data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	Write data							

H=”0”

Set V_{LCD} range

V_{LCD} range L/H select

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	0	PRS

PRS=0:VLCD programming range LOW

PRS=1: VLCD programming range HIGH

END

This command releases the read/modify/write mode, and returns the column and row address to the address it was at when the mode was entered.

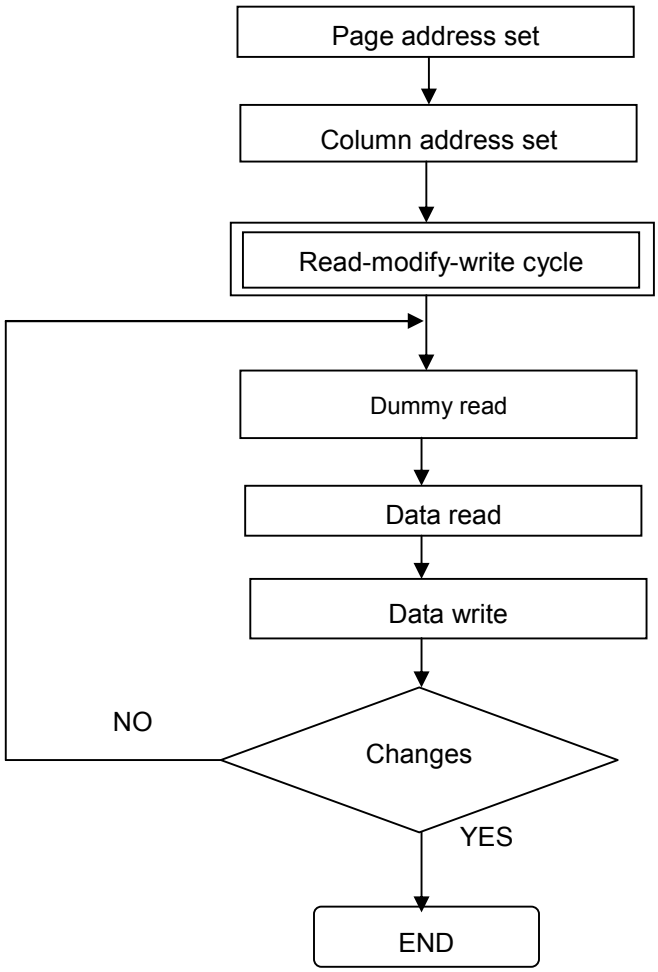
A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	1	0

Read/modify/write

This command is used paired with the "END" command. Once this command has been input, the display data read command does not change the column and row address, but only the display data write command increments (+1) the address depend on V register setting. This mode is maintained until the END command is input. When the END command is input, the address returns to the address it was at when the read/modify/write command was entered. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blanking cursor.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	1	1

* Even in read/modify/write mode, other commands aside from display data read/write commands can also be used.



Display Control

This bits D and E selects the display mode.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	D	0	E

Flag	Description		
D,E	D	E	The bits D and E select the display mode.
	0	0	Display off
	1	0	Normal display
	0	1	All display segments on
	1	1	Inverse video mode

Set Y address of RAM

Y [3:0] defines the Y address vector address of the display RAM.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	Y_3	Y_2	Y_1	Y_0

X/Y Address range

Y_3	Y_2	Y_1	Y_0	CONTENT	ALLOWED X-RANGE
0	0	0	0	Page0 (display RAM)	0 to 101
0	0	0	1	Page1 (display RAM)	0 to 101
0	0	1	0	Page2 (display RAM)	0 to 101
0	0	1	1	Page3 (display RAM)	0 to 101
0	1	0	0	Page4 (display RAM)	0 to 101
0	1	0	1	Page5 (display RAM)	0 to 101
0	1	1	0	Page6 (display RAM)	0 to 101
0	1	1	1	Page7 (display RAM)	0 to 101
1	0	0	0	Page8 (display RAM)	0 to 101
1	0	0	1	Page9 (display RAM)	0 to 101

Start line set

Sets the line address of display RAM to determine the initial display line instruction. The RAM display data is displayed at the top of row (COM0) of LCD panel.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	S_5	S_4	S_3	S_2	S_1	S_0

S_5	S_4	S_3	S_2	S_1	S_0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
:	:	:	:	:	:	:
1	1	1	1	0	0	61
1	1	1	1	0	1	62
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Set X address of RAM

The X address points to the columns. The range of X is 0…101.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	X_6	X_5	X_4	X_3	X_2	X_1	X_0

X_6	X_5	X_4	X_3	X_2	X_1	X_0	Column address
0	0	0	0	0		0	0
0	0	0	0	0		1	1
0	0	0	0	1		0	2
0	0	0	0	1		1	3
:	:	:	:	:		:	:
1	1	0	0	0	1	0	98
1	1	0	0	0	1	1	99
1	1	0	0	1	0	0	100
1	1	0	0	1	0	1	101

H=”1”

Booster stages

The ST7568 incorporates a software configurable voltage multiplier. After reset (RESB), the default voltage multiplier is set to 2*VDD2. Other voltage multiplier factors are set via the command “Set Booster stages”.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	0	PC_1	PC_0

Flag	Description		
	PC_1	PC_0	
PC_1, PC0	0	0	2*voltage multiplier
	0	1	3*voltage multiplier
	1	0	4*voltage multiplier
	1	1	5*voltage multiplier

Booster Efficiency

The ST7568 incorporates software configurable Booster Efficiency Command. It could be used with Voltage multiplier to get the suitable Vout and Power consumption. Default setting is Level 2

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	0	BE_1	BE_0

Flag	Description		
	BE_1	BE_2	
BE[1:0]	0	0	Booster Efficiency Level 1
	0	1	Booster Efficiency Level 2
	1	0	Booster Efficiency Level 3
	1	1	Booster Efficiency Level 4

Release N-line inversion

ST7568 returns to the frame inversion condition from the n-line inversion condition.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	1	0	0

Set N-line inversion

Sets the inverted line number within range of 3 to 33 to improve the display quality by controlling the phase of the internal LCD AC signal (M) by 2-byte instruction.

Note: The N-line inversion mode will be disabled when partial display mode enter. After the partial display mode end, the N-line inversion mode will return as it was.

The 1st Instruction

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	1	0	1

The 2nd Instruction

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	X	X	X	N_4	N_3	N_2	N_1	N_0

N_4	N_3	N_2	N_1	N_0	Selected n-line inversion
0	0	0	0	0	0-line inversion (frame inversion)
0	0	0	0	1	3-line inversion
0	0	0	1	0	4-line inversion
0	0	0	1	1	5-line inversion
:	:	:	:	:	:
1	1	1	0	1	31-line inversion
1	1	1	1	0	32-line inversion
1	1	1	1	1	33-line inversion

S/W initial Internal register

The 1st Instruction

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	1	1	0

The 2nd Instruction

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	0	1	0

Frame frequency adjusts and set FRC, PWM

This command is designed for frame frequency adjustment, which can provide about 50% variation of frame frequency to avoid the interference with the frequency of daylight lamp in different countries and set by double command instruction. Select 3/4 FRC and 9/12/15 PWM and set by double command instruction.

The 1st Instruction

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	1	1	1

The 2nd Instruction

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	X	FR_2	FR_1	FR_0	X	FRC	PWM_1	PWM_0

Frame frequency

This command is used to set the frame frequency.

FR_2	FR_1	FR_0	FR frequency
0	0	0	77 Hz ±5%
0	0	1	80 Hz ±20%
0	1	0	85 Hz ±20%
0	1	1	90 Hz ±20%
1	0	0	100 Hz ±20%
1	0	1	110 Hz ±20%
1	1	0	120 Hz ±20%
1	1	1	130 Hz ±20%

Select 3/4 FRC

FRC	Status of FRC
0	4 FRC
1	3 FRC

Select 9/12/15 PWM

PWM_1	PWM_0	Status of PWM
0	0	9 PWM
0	1	9 PWM
1	0	12 PWM
1	1	15 PWM

System Bias

Select LCD bias ratio of the voltage required for driving the LCD.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	BS_2	BS_1	BS_0

BS_2	BS_1	BS_0	Bias	Recommend Duty
0	0	0	11	1:100
0	0	1	10	1:80
0	1	0	9	1:65/1:68
0	1	1	8	1:48
1	0	0	7	1/40:1/34
1	0	1	6	1/24
1	1	0	5	1:18/1:16
1	1	1	4	1:10/1:9/1:8

Set Gray Scale Mode & Register

The first byte sets grayscale mode and the second byte updates the contents of gray scale register without issuing any other instruction.

--Set Gray Scale Mode

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	1	GM_2	GM_1	GM_0

GM_2	GM_1	GM_0	Description
0	0	0	In case of setting whit mode and 1^{st} / 2^{nd} frame
0	0	1	In case of setting whit mode and 3^{rd} / 4^{th} frame
0	1	0	In case of setting light gray mode and 1^{st} / 2^{nd} frame
0	1	1	In case of setting light gray mode and 3^{rd} / 4^{th} frame
1	0	0	In case of setting dark gray mode and 1^{st} / 2^{nd} frame
1	0	1	In case of setting dark gray mode and 3^{rd} / 4^{th} frame
1	1	0	In case of setting block mode and 1^{st} / 2^{nd} frame
1	1	1	In case of setting block mode and 3^{rd} / 4^{th} frame

--Set Gray Scale Register

GA3, GB3, GC3, GD3	GA2, GB2, GC2, GD2	GA1, GB1, GC1, GD1	GA0, GB0, GC0, GD0	Pulse width (9 PWM)	Pulse width (12 PWM)	Pulse width (15 PWM)
0	0	0	0	0/9	0/12	0/15
0	0	0	1	1/9	1/12	1/15
:	:	:	:	:	:	:
1	0	0	1	9/9	9/12	9/15
1	0	1	0	0/9	10/12	10/15
1	0	1	0	0/9	11/12	11/15
1	1	0	0	0/9	12/12	12/15
1	1	0	1	0/9	0/12	13/15
1	1	1	0	0/9	0/12	14/15
1	1	1	1	0/9	0/12	15/15

* GA3=WA3, LA3, DA3, BA3 GA2=WA2, LA2, DA2, BA2 GA1=WA1, LA1, DA1, BA1 GA0=WA0, LA0, DA0, BA0
GB3=WB3, LB3, DB3, BB3 GA2=WB2, LB2, DB2, BB2 GA1=WB1, LB1, DB1, BB1 GA0=WB0, LB0, DB0, BB0
GC3=WC3, LC3, DC3, BC3 GA2=WC2, LC2, DC2, BC2 GA1=WC1, LC1, DC1, BC1 GA0=WC0, LC0, DC0, BC0

GD3=WD3, LD3, DD3, BD3 GA2=WD2, LD2, DD2, BD2 GA1=WD1, LD1, DD1, BD1 GA0=WD0, LD0, DD0, BD0

LCD bias voltage

Symbol	Bias voltage for 1/8 bias	Symbol	Bias voltage for 1/8 bias
VLCDIN	VLCDIN	V3	2/8 X VLCDIN
V1	7/8 X VLCDIN	V4	1/8 X VLCDIN
V2	6/8 X VLCDIN	VSS	VSS

Set VOP value:

The operation voltage V_{LCD} can be set by software.

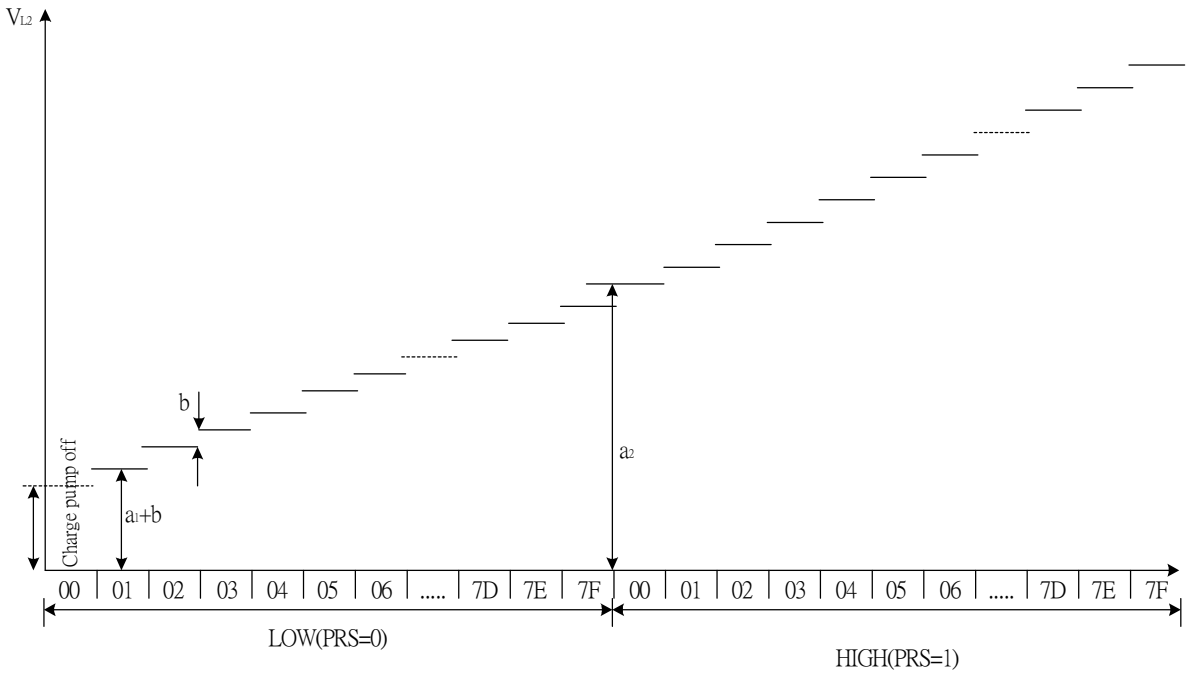
$$V_0=(a + V_{OP} \times b) \quad (1)$$

The parameters are explained in table 4.The maximum voltage that can be generated is depending on the VDD voltage and the display load current. Two overlapping VLCD ranges are selectable via the command "Booster control". For the LOW (PS=0) range a=a1 and for the HIGH (PRS=1) range a=a2 with steps equal to "b" in both ranges. Note that the charge pump is turned off if VOP [6;0] and the bit PRS are all set to zero.

The V0 Temperature Gradient is -0.05%/^{o}C

Table 4 Typical values for parameter for the HV-Generator programming

SYMBOL	VALUE	UNIT
a1	2.94(PRS=0)	V
a2	6.75(PRS=1)	V
b	0.03	V



VOP [6:0](programmed) {00 hex… 7F hex}

Fig.21 V_{OP} programming of ST7568

Caution

As the programming range for the internally generated VLCDIN allows values above the max allowed VLCDIN, the customer has to ensure while setting the VOP register that under all condition and including all tolerances the VLCD limit of max. 13V will never be exceeded. As VLCDIN increases with lower temperatures, care must be taken not to set a Vop generating a VLCDIN voltage that will exceed the maximum of 10.6V when operating at －30 ℃.

10. COMMAND DESCRIPTION

Referential Instruction Setup Flow: Initializing with the built-in Power Supply Circuits

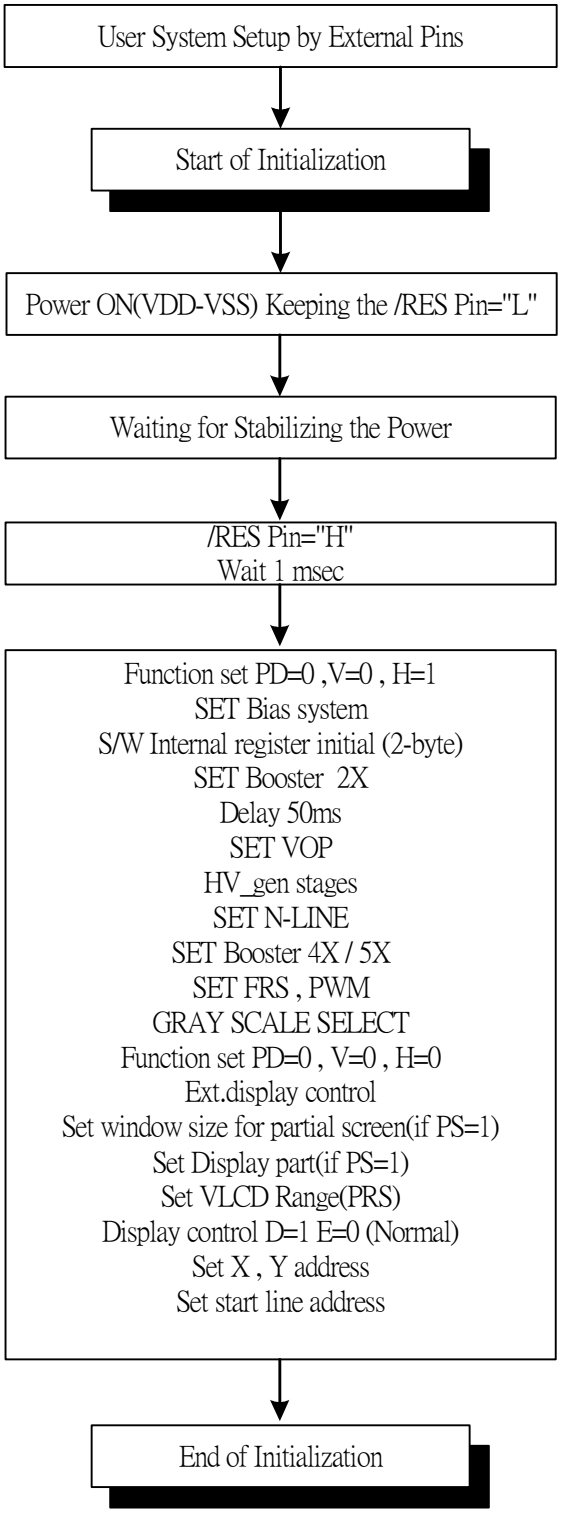


Figure 22. Initializing with the Built-in Power Supply Circuits

Referential Instruction Setup Flow: Initializing without the built-in Power Supply Circuits

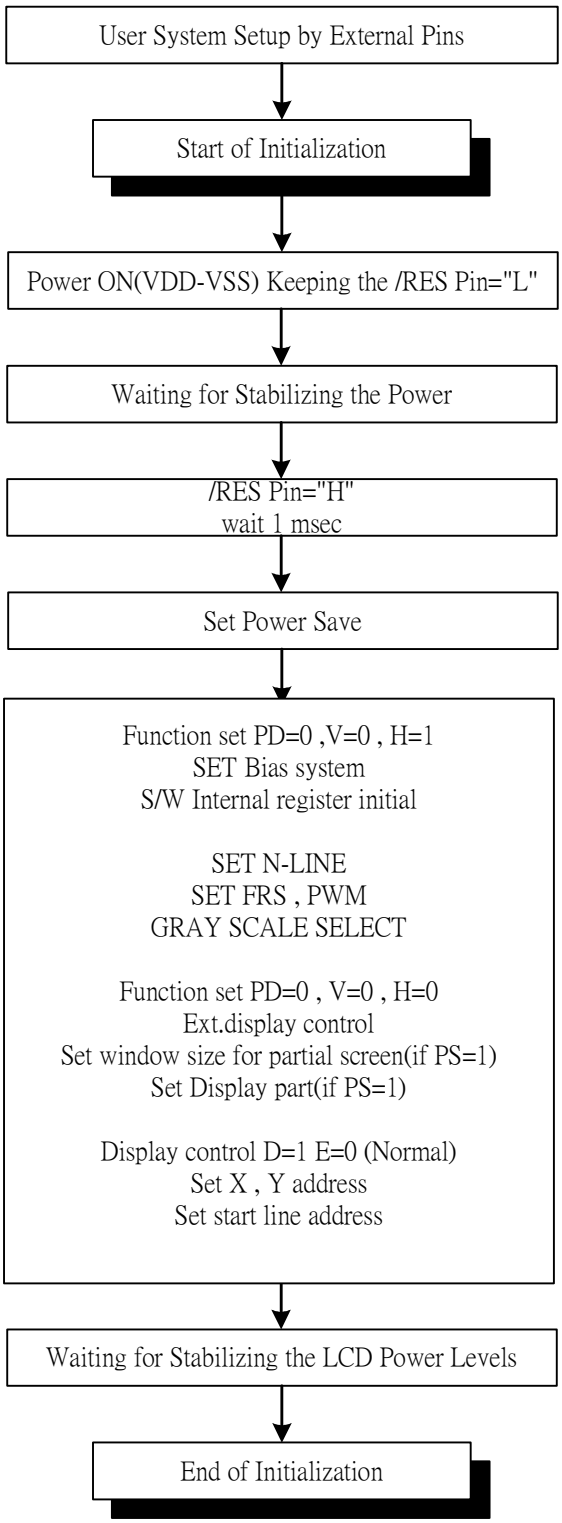


Fig 23. Initializing without Built-in Power Supply Circuits

Referential Instruction Setup Flow: Data Displaying

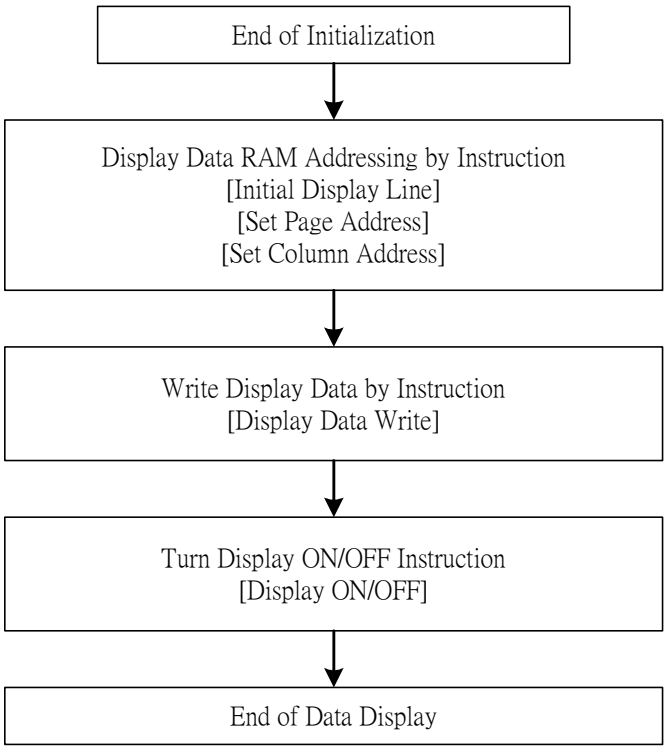


Figure 24.Data Displaying

Referential Instruction Setup Flow: Power OFF

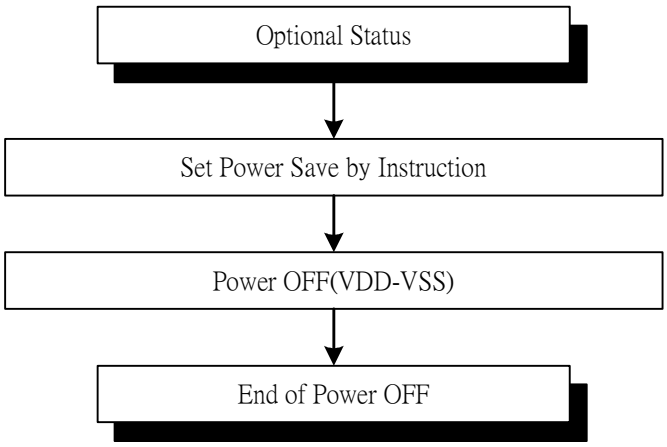
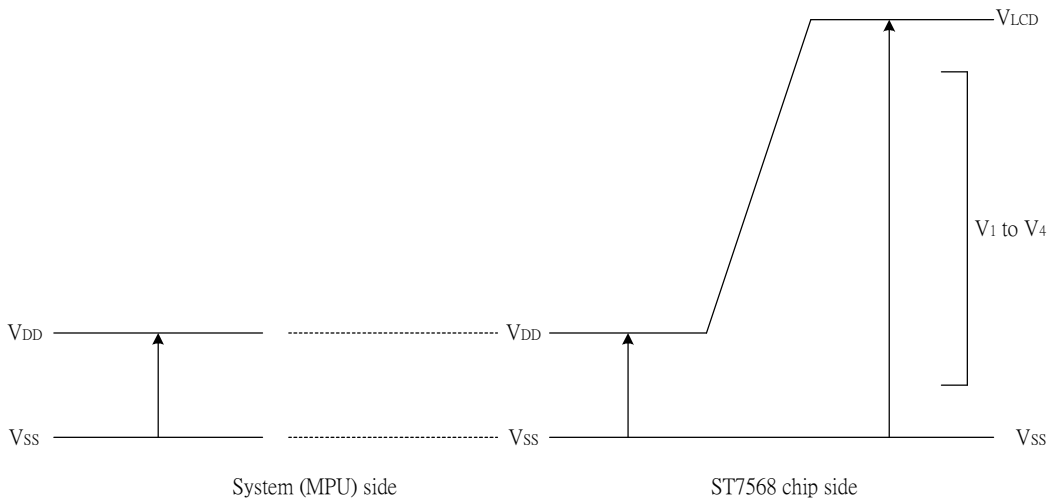


Figure 25. Power OFF

11. LIMITING VALUES

In accordance with the Absolute Maximum Rating System; see notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Power Supply Voltage	VDD	–0.3 ~ +3.6	V
Power supply voltage	V0	3.0 ~ 12	V
Power supply voltage	VLCDIN	–0.3 ~ +13.5	V
Power supply voltage	V1, V2, V3, V4	0.3 to VLCDIN	V
Input voltage	VIN	–0.5 to VDD+0.5	V
Output voltage	VO	–0.5 to VDD+0.5	V
Operating temperature	TOPR	–30 to +85	°C
Storage temperature	TSTR	–65 to +150	°C



Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
3. Insure that the voltage levels of V1, V2, V3, and V4 are always such that

   Vout ≧ V0 ≧ V1 ≧ V2 ≧ V3 ≧ V4 ≧ Vss

12. HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see “Handling MOS devices”).

13. DC CHARACTERISTICS

V_{DD} = 1.8 V to 3.3V; V_{SS} = 0 V; V_{LCD} = 3.0 to 13.0V; T_{amb} = -30℃ to +85℃; unless otherwise specified.

Item		Symbol	Condition		Rating			Units	Applicable Pin
					Min.	Typ.	Max.		
Operating Voltage (1)		VDD			1.8	—	3.3	V	Vss*1
Operating Voltage (2)		VDD2	(Relative to VSS)		1.8	—	3.3	V	VSS2
High-level Input Voltage		VIHC			0.7 x VDD	—	VDD	V	*2
Low-level Input Voltage		VILC			VSS	—	0.3 x VDD	V	*2
High-level Output Voltage		VOHC			0.7 x VDD	—	VDD	V	*3
Low-level Output Voltage		VOLC			VSS	—	0.3 x VDD	V	*3
Input leakage current		ILI	VIN = VDD or VSS		–1.0	—	1.0	μA	*4
Output leakage current		ILO	VIN = VDD or VSS		–3.0	—	3.0	μA	*5
Liquid Crystal Driver ON Resistance		RON	Ta = 25°C (Relative To VSS)	VLCDIN = 13.0 V	—	2.0	3.5	KΩ	SEGn COMn *6
				VLCDIN = 8.0 V	—	3.2	5.4		
Oscillator Frequency	Internal Oscillator	fOSC	1/68 duty	Ta = 25°C 15 PWM	—	80	84	kHz	*7
	External Input	fCL			—	80	84	kHz	OSC
	Frame frequency	fFRAME			—	77	80.3	Hz	

Item		Symbol	Condition	Rating			Units	Applicable Pin
				Min.	Typ.	Max.		
Internal Power	Input voltage	VDD	(Relative To VSS)	1.8	—	3.3	V	
	Supply Step-up output voltage Circuit	VLCDOUT	(Relative To VSS)	—	—	13.5	V	VLCDOUT
	Voltage regulator Circuit Operating Voltage	VLCDIN	(Relative To VSS)	—	—	13.5	V	VLCDIN

Bare Dice Consumption Current : During Display, with the Internal Power Supply, Current consumed by total ICs when an external power supply(VDD,VDD2) is used .

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern SNOW	ISS	VDD,VDD2 = 3.0 V, V0 – VSS = 9.0 V 4X Booster 1/9 Bias	—	300	400	μA	*8
Power Down	ISS	VDD=3.0V Ta = 25°C	—	0.01	2	μA	

Notes to the DC characteristics

1. The maximum possible V_{LCD} voltage that may be generated is dependent on voltage, temperature and (display) load.
2. Internal clock
3. Power-down mode. During power down all static currents are switched off.
4. If external V_{LCDIN}, the display load current is not transmitted to I_{DD}.
5. V_{OUT} external voltage applied to VLCDIN pin; VLCDIN disconnected from VLCDOUT (no connect)

References for items market with *

*1 While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.

*2 The A0, D0 to D5, D6 (SI), D7 (SCL), /RD (E), /WR ,/(R/W), CSB, IMS, OSC, P/S, /DOF, RESB ,and MODE terminals.

*3 The D0 to D7, and OSC terminals.

*4 The A0,/RD (E), /WR ,/(R/W), CSB, IMS, OSC, P/S, /DOF, RESB ,and MODE terminals.

*5 Applies when the D0 to D5, D6 (SI), D7 (SCL) terminals are in a high impedance state.

*6 These are the resistance values for when a 0.1 V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V1, V2, V3, and V4). These are specified for the operating voltage range.
RON = 0.1 V /ΔI (Where ΔI is the current that flows when 0.1 V is applied while the power supply is ON.)

*7 The relationship between the oscillator frequency and the frame rate frequency.

*8,9It indicates the current consumed on ICs alone when the internal oscillator circuit and display are turned on.

14. TIMING CHARACTERISTICS

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

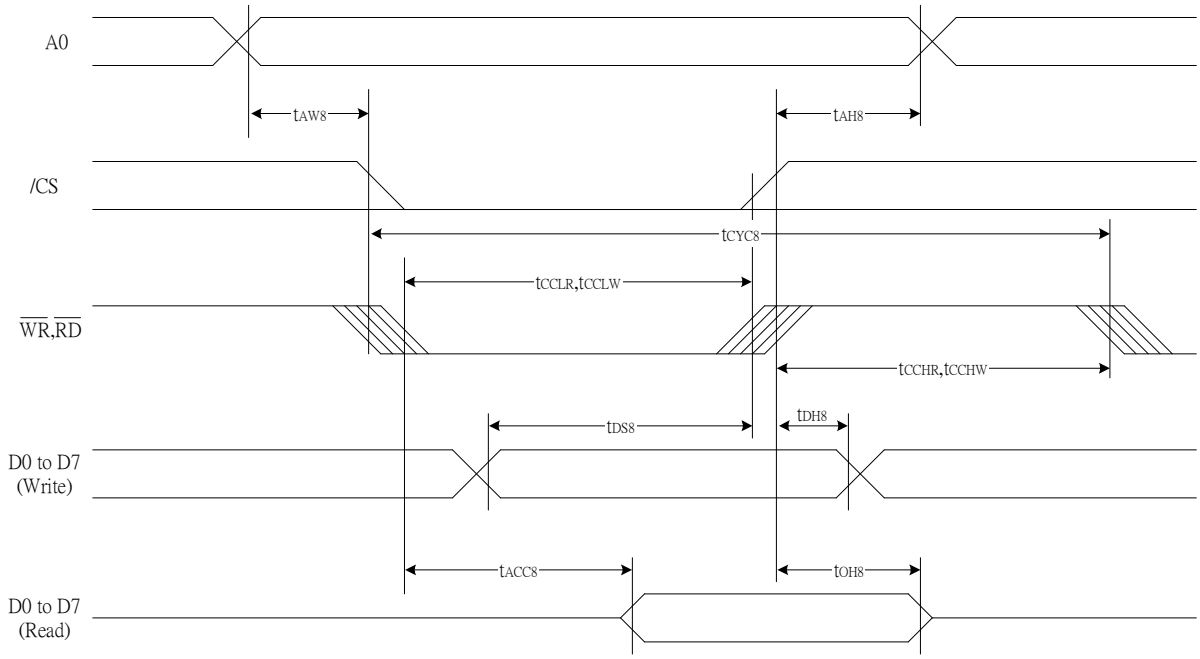


Figure 26.

(VDD = 3.3V , Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		240	—	
Enable L pulse width (WRITE)	WR	tCCLW		80	—	
Enable H pulse width (WRITE)		tCCHW		80	—	
Enable L pulse width (READ)	RD	tCCLR		140	—	
Enable H pulse width (READ)		tCCHR		80		
WRITE Data setup time	D0 to D7	tDS8		40	—	
WRITE Data hold time		tDH8		10	—	
READ access time		tACC8	CL = 100 pF	—	70	
READ Output disable time		tOH8	CL = 100 pF	5	50	

(VDD = 2.7 V , Ta = -30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		400	—	
Enable L pulse width (WRITE)	WR	tCCLW		220	—	
Enable H pulse width (WRITE)		tCCHW		180	—	
Enable L pulse width (READ)	RD	tCCLR		220	—	
Enable H pulse width (READ)		tCCHR		180	—	
WRITE Data setup time	D0 to D7	tDS8		40	—	
WRITE Data hold time		tDH8		15	—	
READ access time		tACC8	CL = 100 pF	—	140	
READ Output disable time		tOH8	CL = 100 pF	10	100	

(VDD = 1.8V , Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		640	—	
Enable L pulse width (WRITE)	WR	tCCLW		360	—	
Enable H pulse width (WRITE)		tCCHW		280	—	
Enable L pulse width (READ)	RD	tCCLR		360	—	
Enable H pulse width (READ)		tCCHR		280		
WRITE Data setup time	D0 to D7	tDS8		80	—	
WRITE Data hold time		tDH8		30	—	
READ access time		tACC8	CL = 100 pF	—	240	
READ Output disable time		tOH8	CL = 100 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) $\leqq$ (tCYC8 – tCCLW – tCCHW) for (tr + tf) $\leqq$ (tCYC8 – tCCLR – tCCHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tCCLW and tCCLR are specified as the overlap between CSB being “L” and WR and RD being at the “L” level.

System Bus Read/Write Characteristics 1 (For the 6800 Series MPU)

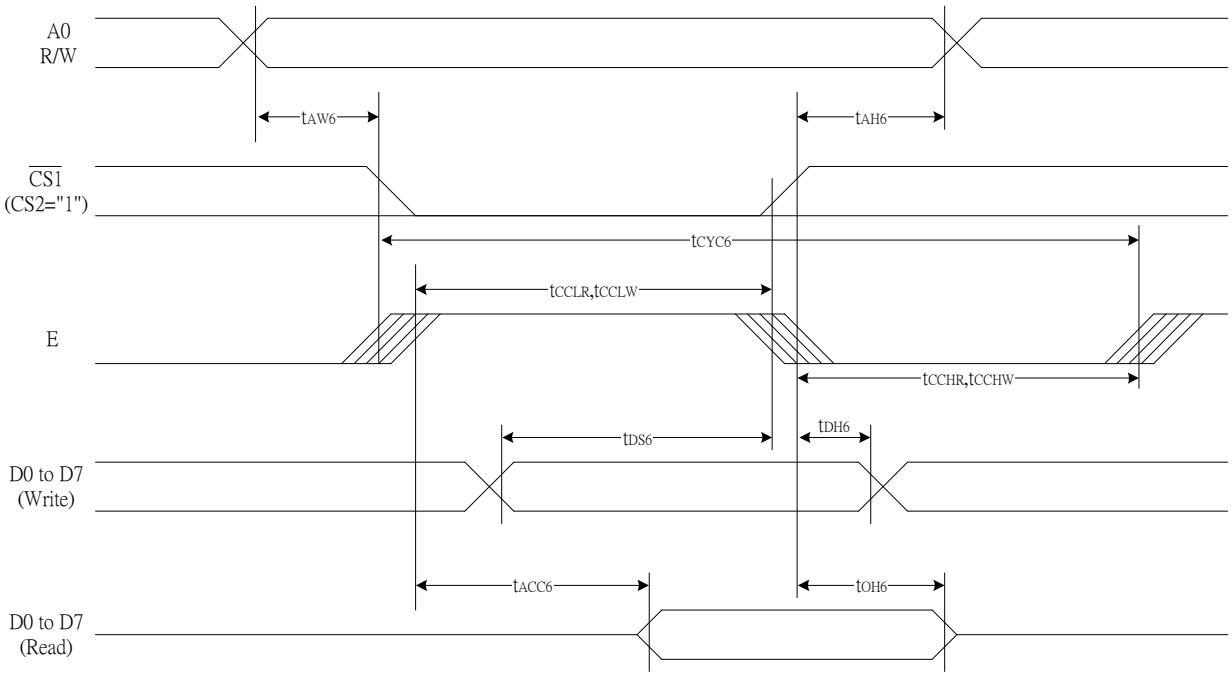


Figure 27.

(V_{DD} = 3.3 V , Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		240	—	
Enable L pulse width (WRITE)	WR	tEWLW		80	—	
Enable H pulse width (WRITE)		tEWHW		80	—	
Enable L pulse width (READ)	RD	tEWLR		80	—	
Enable H pulse width (READ)		tEWHR		140		
WRITE Data setup time	D0 to D7	tDS6		40	—	
WRITE Data hold time		tDH6		10	—	
READ access time		tACC6	CL = 100 pF	—	70	
READ Output disable time		tOH6	CL = 100 pF	5	50	

(VDD = 2.7V , Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		400	—	
Enable L pulse width (WRITE)	WR	tEWLW		220	—	
Enable H pulse width (WRITE)		tEWHW		180	—	
Enable L pulse width (READ)	RD	tEWLR		220	—	
Enable H pulse width (READ)		tEWHR		180	—	
WRITE Data setup time	D0 to D7	tDS6		40	—	
WRITE Data hold time		tDH6		15	—	
READ access time		tACC6	CL = 100 pF	—	140	
READ Output disable time		tOH6	CL = 100 pF	10	100	

(VDD =1.8V , Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		640	—	
Enable L pulse width (WRITE)	WR	tEWLW		360	—	
Enable H pulse width (WRITE)		tEWHW		280	—	
Enable L pulse width (READ)	RD	tEWLR		360	—	
Enable H pulse width (READ)		tEWHR		280	—	
WRITE Data setup time	D0 to D7	tDS6		80	—	
WRITE Data hold time		tDH6		30	—	
READ access time		tACC6	CL = 100 pF	—	240	
READ Output disable time		tOH6	CL = 100 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≦ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≦ (tCYC6 – tEWLR – tEWHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tEWLW and tEWLR are specified as the overlap between CSB being “L” and E.

SERIAL INTERFACE(4-Line Interface)

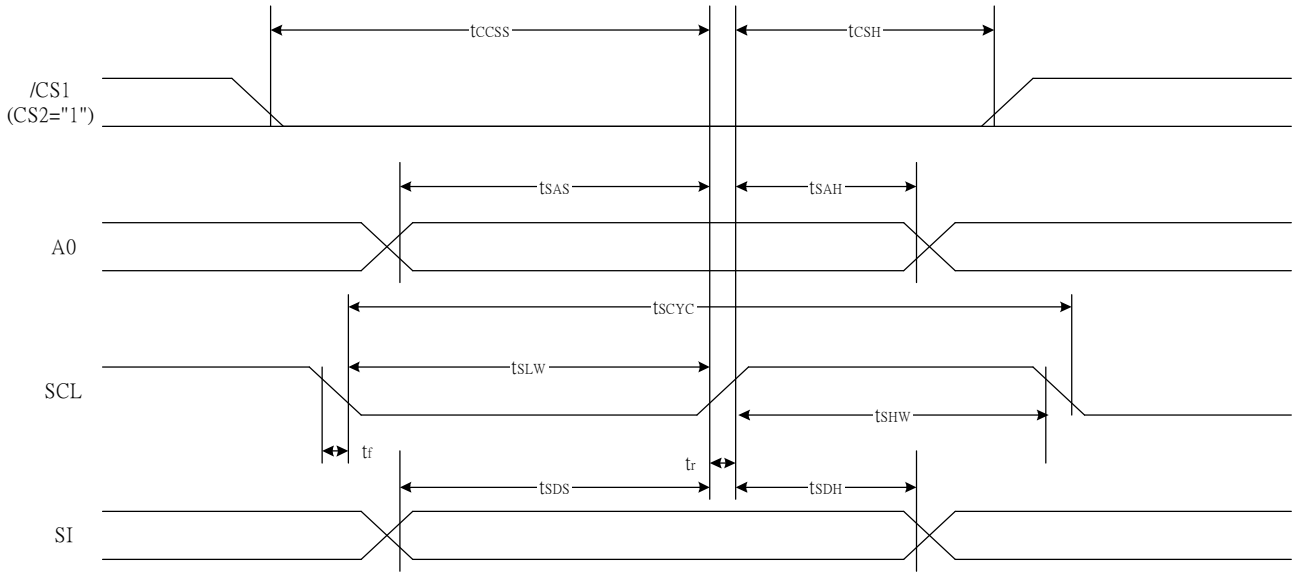


Fig 28.

(V_{DD}=3.3V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		50	—	ns
SCL “H” pulse width		tSHW		25	—	
SCL “L” pulse width		tSLW		25	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		10	—	
Data setup time	SI	tSDS		20	—	
Data hold time		tSDH		10	—	
CS-SCL time	CSB	tCSS		20	—	
CS-SCL time		tCSH		140	—	

(V_{DD}=2.7V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		100	—	ns
SCL “H” pulse width		tSHW		50	—	
SCL “L” pulse width		tSLW		50	—	
Address setup time	A0	tSAS		30	—	
Address hold time		tSAH		20	—	
Data setup time	SI	tSDS		30	—	
Data hold time		tSDH		20	—	
CS-SCL time	CSB	tCSS		30	—	
CS-SCL time		tCSH		160	—	

(V_{DD}=1.8V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		200	—	ns
SCL “H” pulse width		tSHW		80	—	
SCL “L” pulse width		tSLW		80	—	
Address setup time	A0	tSAS		60	—	
Address hold time		tSAH		30	—	
Data setup time	SI	tSDS		60	—	
Data hold time		tSDH		30	—	
CS-SCL time	CSB	tCSS		40	—	
CS-SCL time		tCSH		200	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

15. RESET TIMING

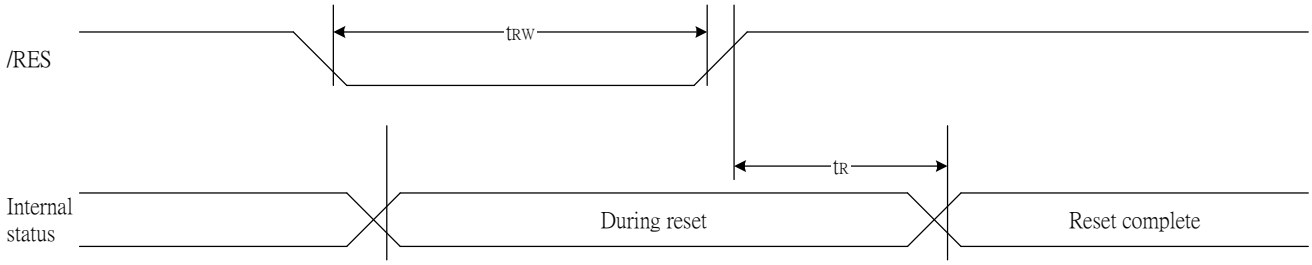


Fig 29.

(VDD = 3.3V , Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	1	us
Reset “L” pulse width	RESB	tRW		1	—	—	us

(VDD = 2.7V , Ta = –30 to 85°C)

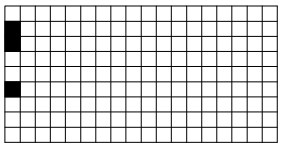
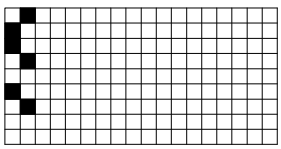
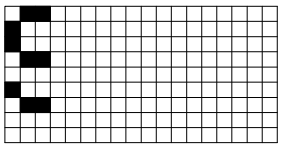
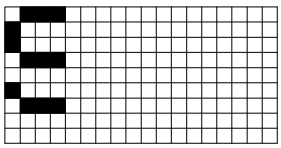
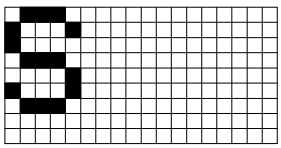
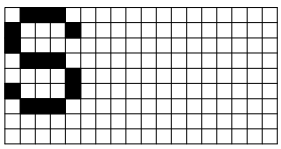
Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	1.5	us
Reset “L” pulse width	RESB	tRW		1.5	—	—	us

(VDD = 1.8V , Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	2.0	us
Reset “L” pulse width	RESB	tRW		2.0	—	—	us

16. APPLICATION INFORMATION

Table 5 programming example for ST7568

SETP	SERIAL BUS BYTE	DISPLAY	OPERATION
1	Start		CSB IS going low.
2	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 1 0 0 0 0 0		Function Set. PD=0,V=0,select extended Instruction set(H=0 mode)
3	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 1 0 0 0 0		Set V_{OP} V_{OP} is set to a+16*b[V]
4	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 1 0 0 0 0 0		Function Set. PD=0,V=0,select normal Instruction set(H=0 mode).
5	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 0 1 0 0		Display control. Set normal mode(D=1,E=0)
6	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1 1 0		Data Write. Y,X are initialized to 0 by default, so they aren't set here…
7	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1		Data Write.
8	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1		Data Write.
9	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1		Data Write.
10	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 1 1 0 0 1 0 1 0 0 1 1 0 0 1 0		Data Write.
11	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0		Data Write.

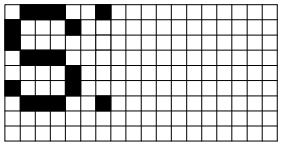
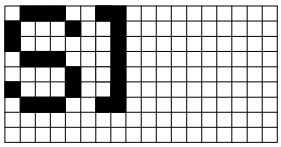
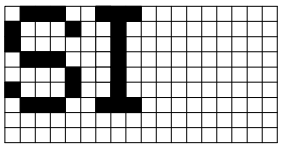
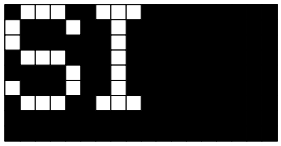
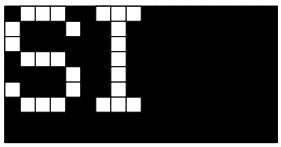
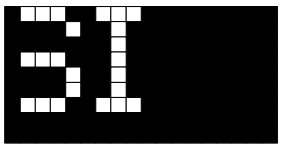
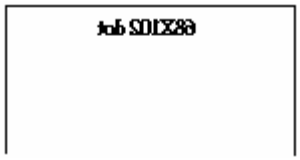
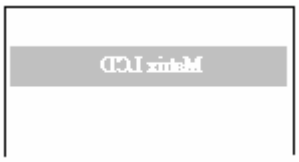
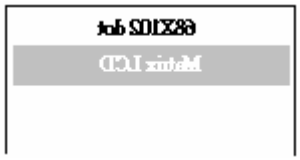
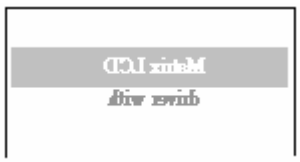
12	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 0 0 0 1 1 0 1 0 0 0 0 0 1		Data Write.
13	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1		Data Write.
14	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 0 0 0 1 1 0 1 0 0 0 0 0 1		Data Write.
15	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 1 1 0 1		Display Control. Set inverse video mode (D=1,E=1).
16	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 0 0 0 0 0		Set X address of RAM. Set address to “0000000”.
17	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0		Data Write.

Table 6 Display examples for ST7568 depending on PS,MX,MY and DP[2:0] bit setting

Example	WS	PS	DP_2	DP_1	DP_0	MX	MY	DISPLAY
1	0	0	X	X	X	0	0	
2	0	0	X	X	X	1	0	

3	0	0	X	X	X	0	1	
4	0	0	X	X	X	1	1	
5	0	1	0	0	0	0	0	
6	0	1	0	0	0	1	0	
7	0	1	0	0	0	0	1	
8	0	1	0	0	0	1	1	
9	0	1	0	0	1	0	0	
10	0	1	0	0	1	1	0	
11	0	1	0	0	1	0	1	

12	0	1	0	0	1	1	1	
13	1	1	0	0	0	0	0	
14	1	1	0	0	0	1	0	
15	1	1	0	0	0	0	1	
16	1	1	0	0	0	1	1	
17	1	1	0	0	1	0	0	
18	1	1	0	0	1	1	0	
19	1	1	0	0	1	0	1	
20	1	1	0	0	1	1	1	

Note: When you use 68 com mode and will use partial display to display , then you can control 0~64com to display , not control 65~67 com to display.

The pinning of the ST7568 is optimized for single plane wiring e.g. for chip-on-glass display modules. Display size: 65x102 pixels.

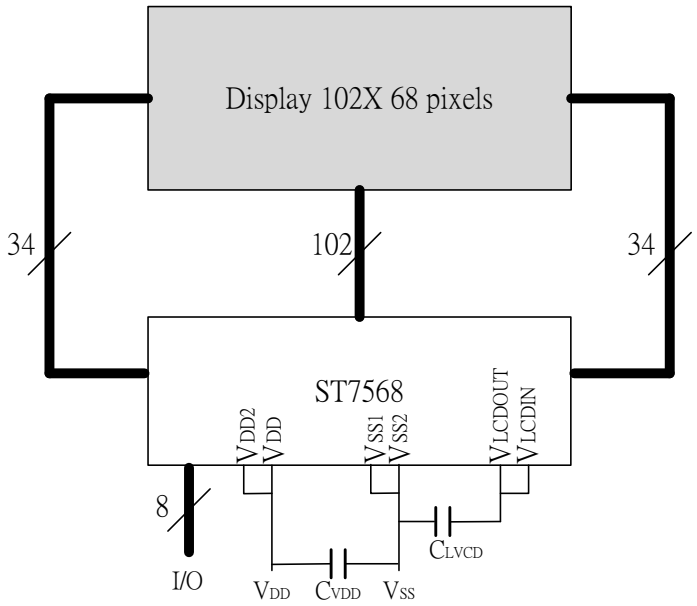


Fig 30. Application diagram: internal charge pump is used and single V_{DD}

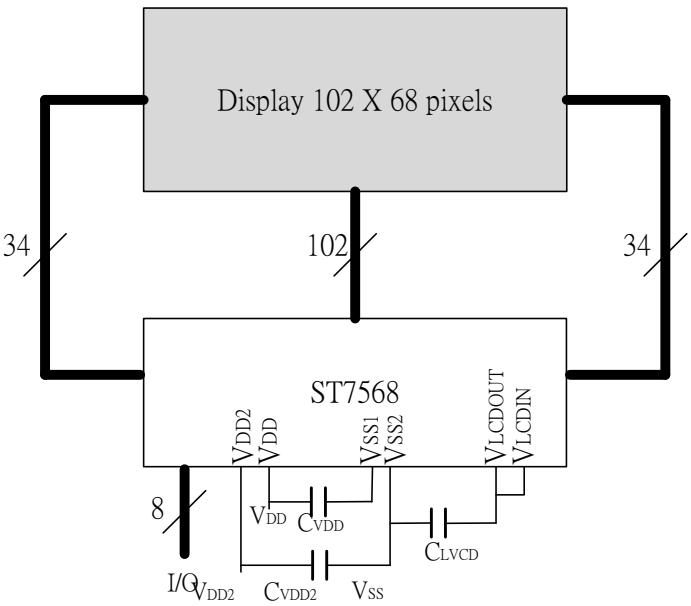


Fig 31. Application diagram: Internal charge pump is used and two separate VDD(V_{DD2})

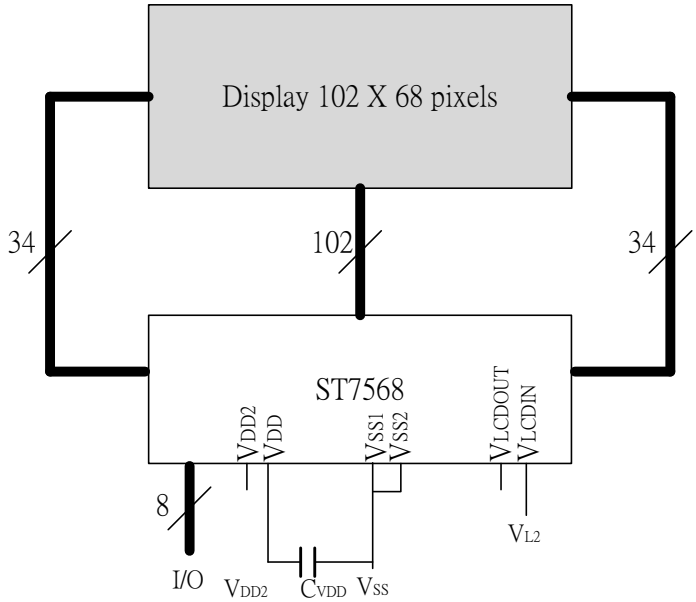


Fig 32. application diagram : External high voltage generation is used

The required minimum value for the external capacitors in an application with the ST7568 are:

C_{VLCD} = min. 100nF $C_{VDD,2}$= min. 1.0 μF

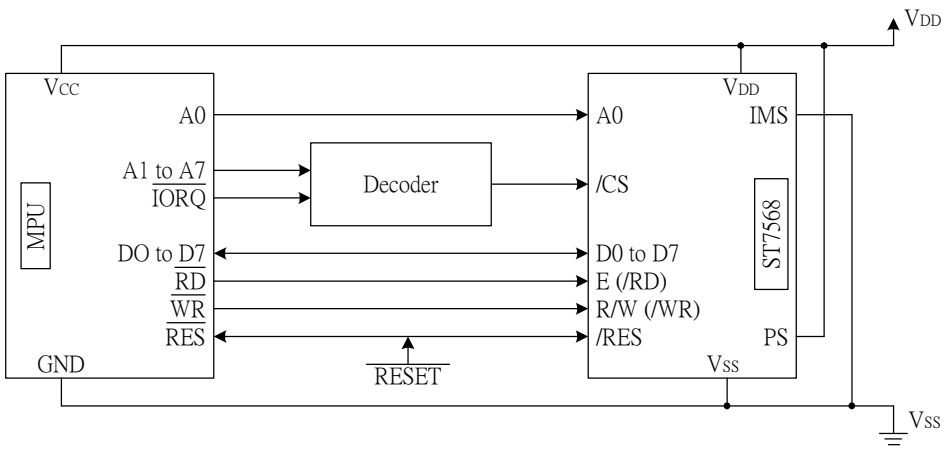
Higher capacitor values are recommended for ripple reduction.

17.THE MPU INTERFACE (REFERENCE EXAMPLES)

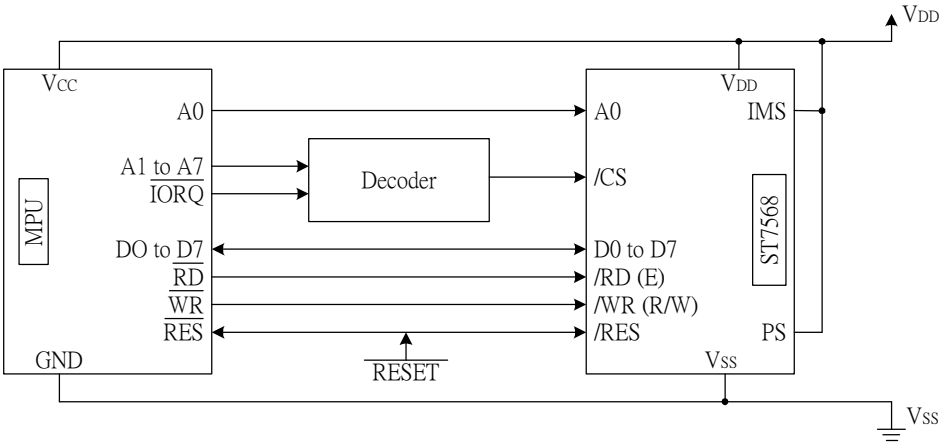
The ST7568 Series can be connected to either60X86 Series MPUs or to 6800Swries MPUs. Moreover, using the serial interface it is possible to operate the ST7568 series chips with fewer signal lines.

The display area can be enlarged by using multiple ST7568 Series chips. When this is done, the chip select signal can be used to select the individual Ics to access.

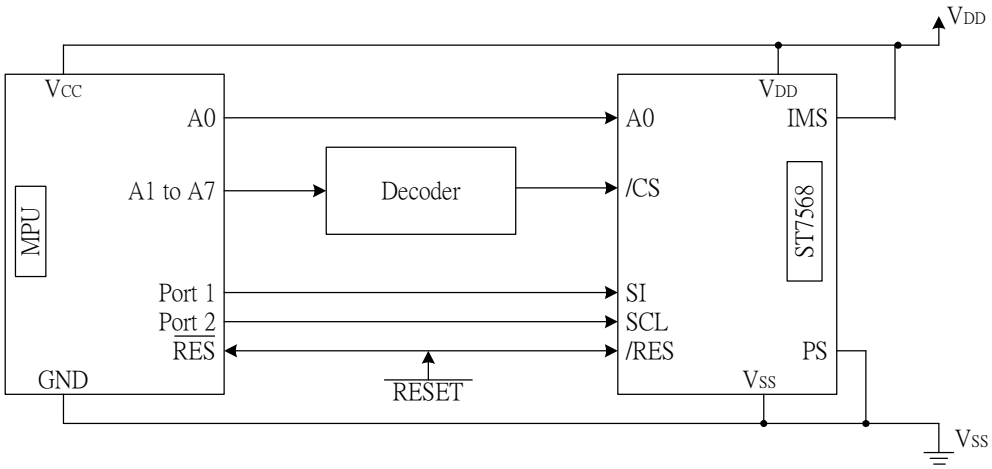
(1) 8080 Series MPUs



(2) 6800 Series MPUs



(3) Using the Serial Interface (4-line interface)



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Hardware Option set up & interfaces

Figure – 1: 68-duty/parallel-6800/VLCDIN-internal/VDD2=VDD/internal-OSC

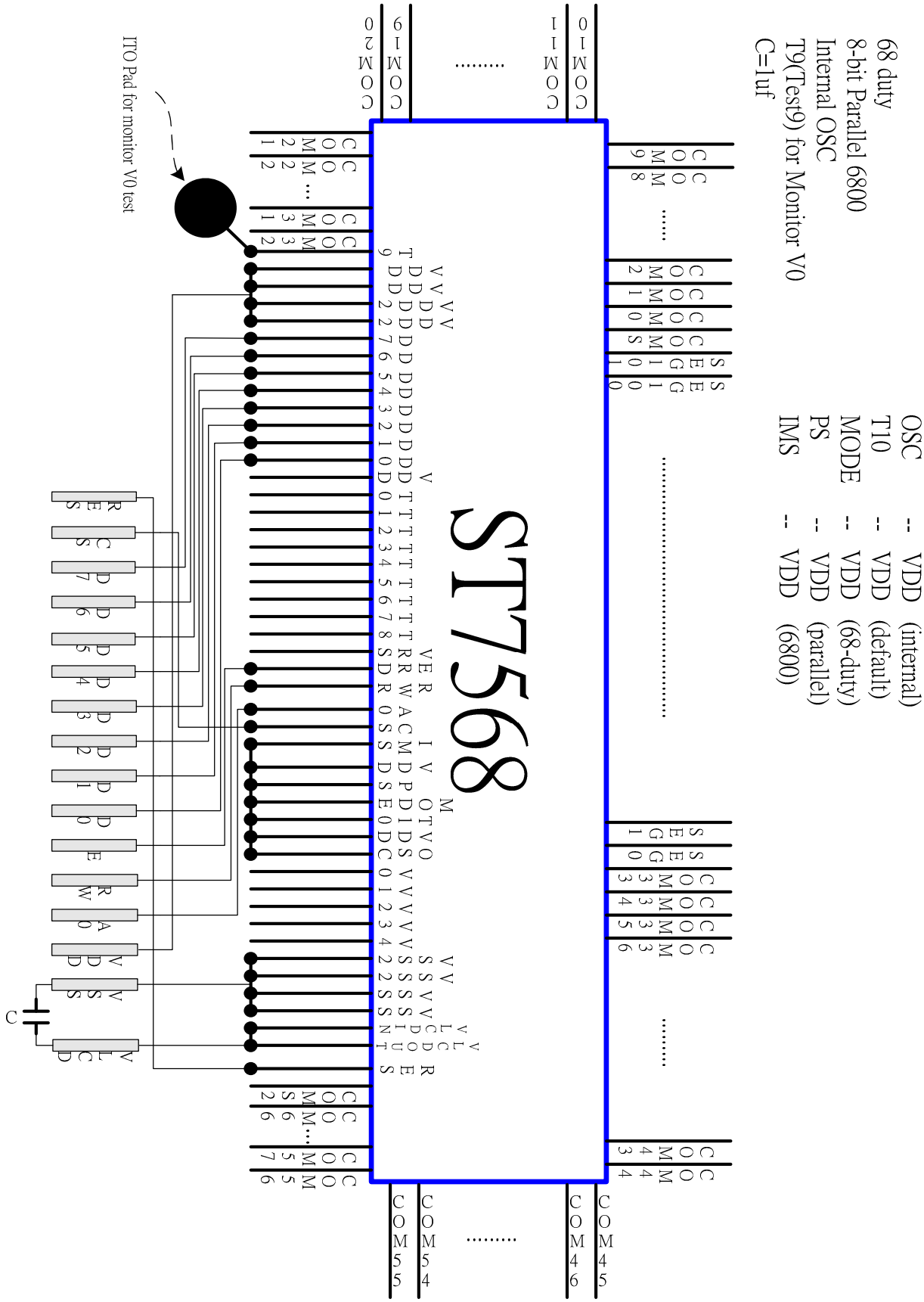


Figure - 2: 65-duty/parallel-6800/VLCDIN-internal/VDD2=VDD/internal-OSC

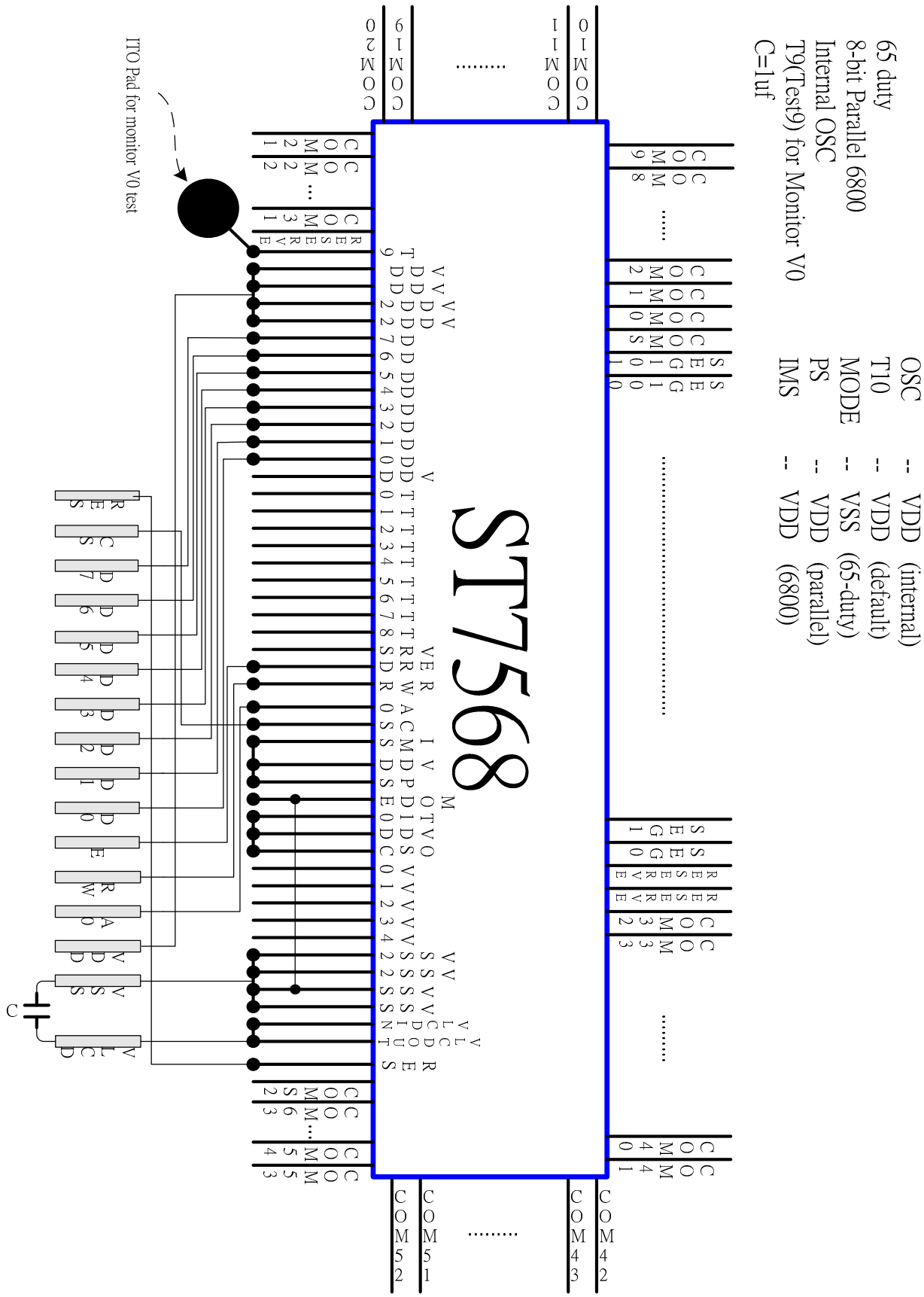


Figure - 3: 68-duty/parallel-8080/VLCDIN-internalVDD2=VDD/internal-OSC

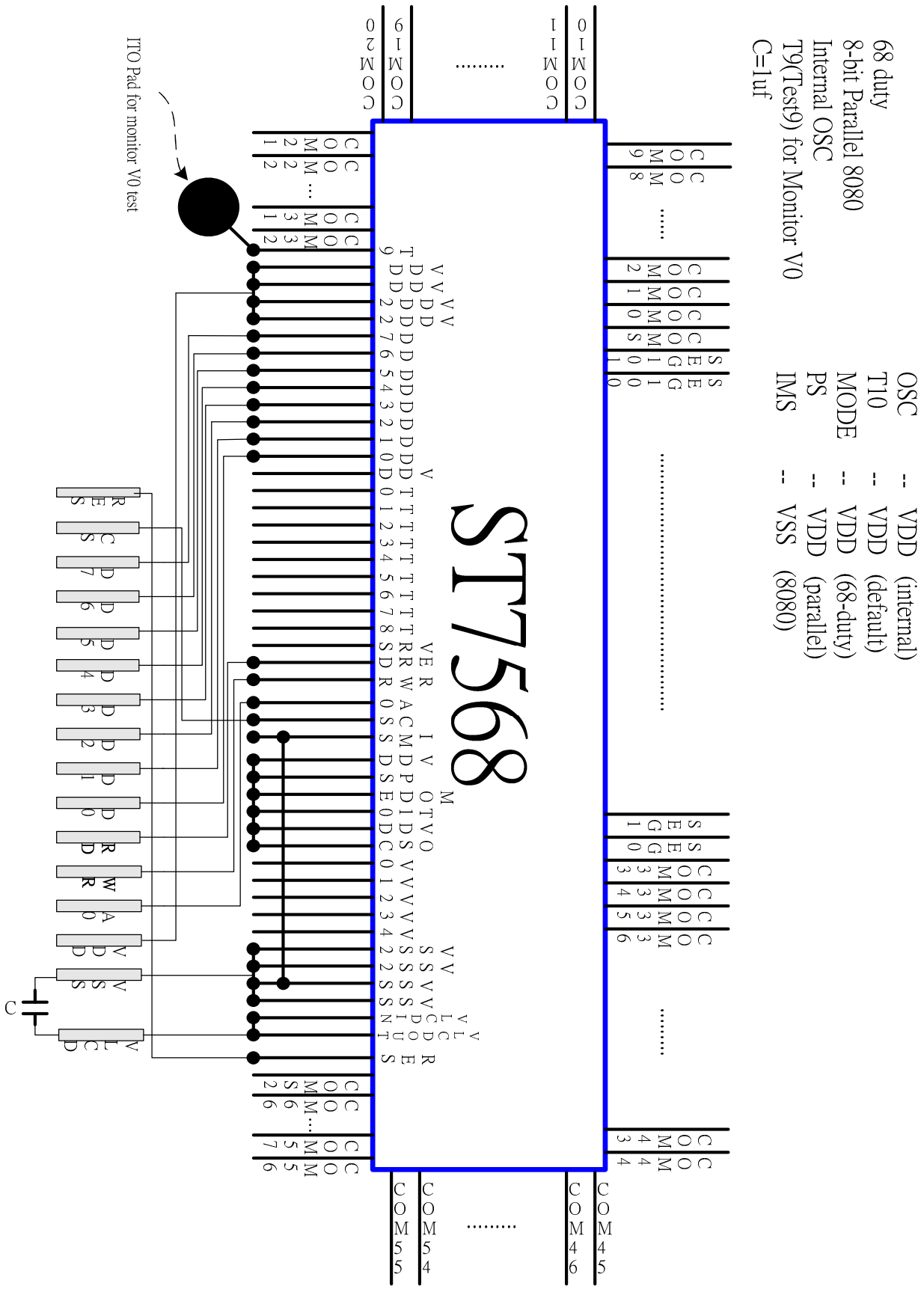


Figure - 4: 68-duty/serial-4Line/VLCDIN-internal/VDD2=VDD/internal-OSC

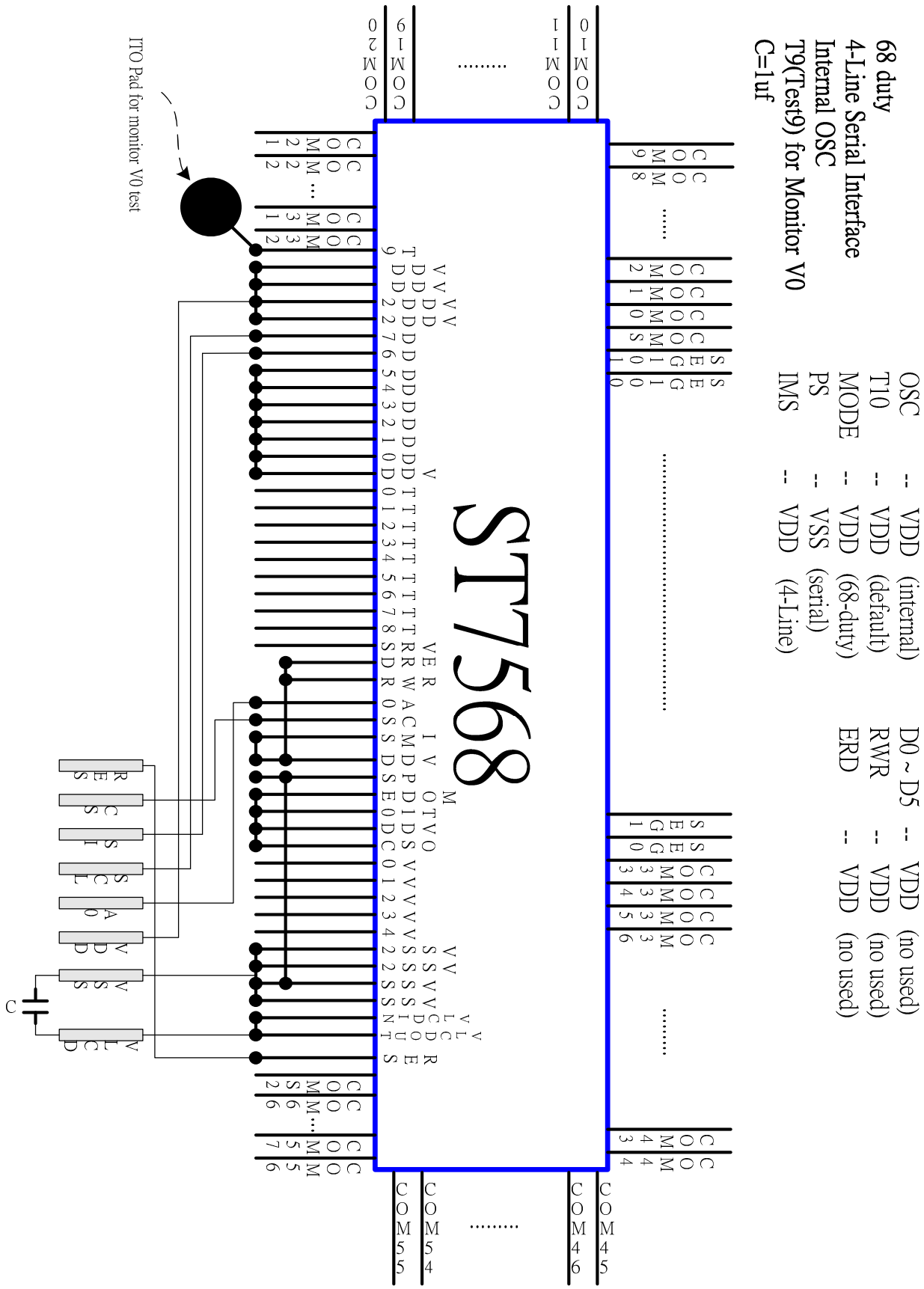


Figure - 5: 68-duty/parallel-6800 /VLCDIN-External/VDD2=VDD/internal-OSC

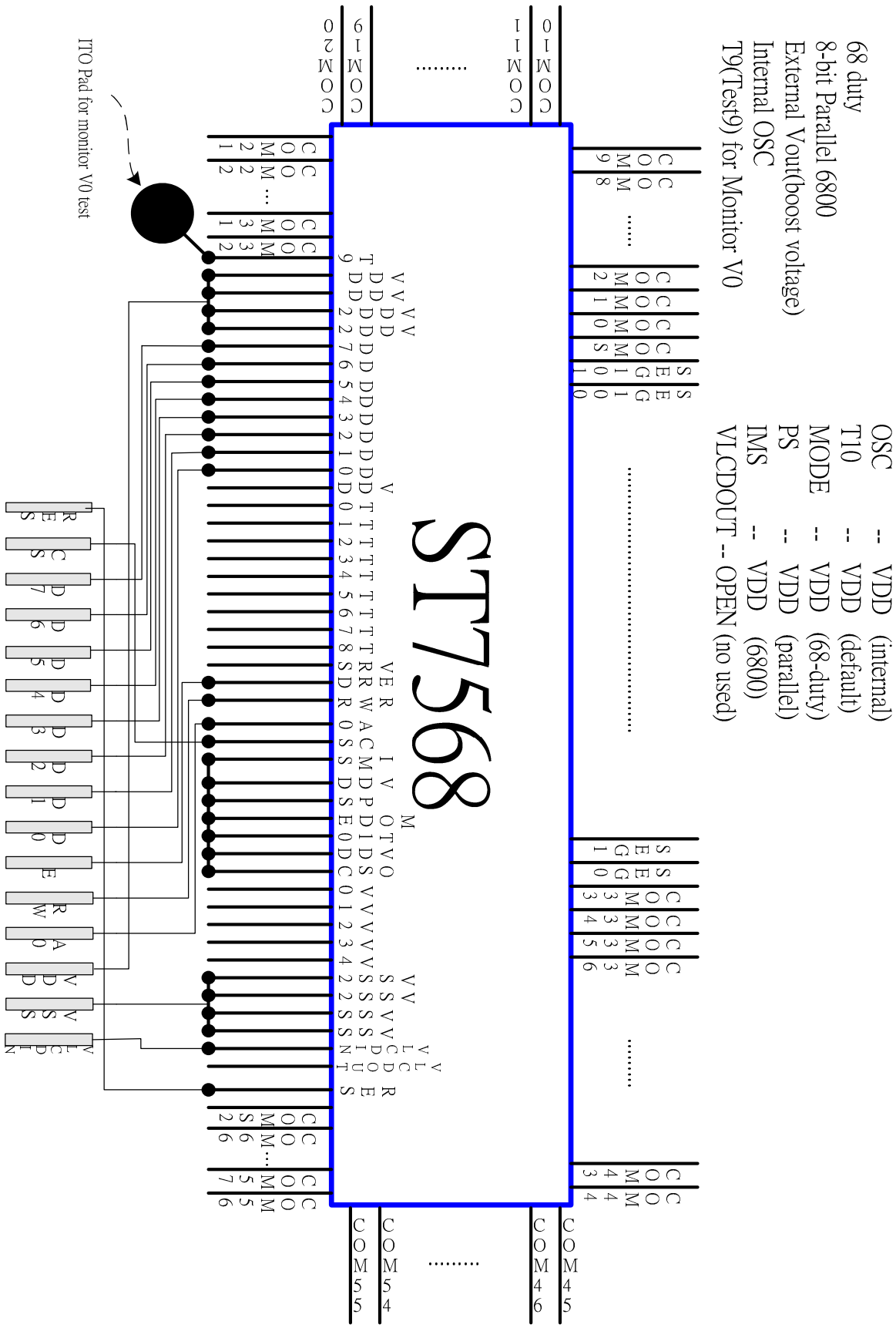


Figure - 6: 68-duty/parallel-6800 /VLCDIN-External/VDD2=Independent/internal-OSC

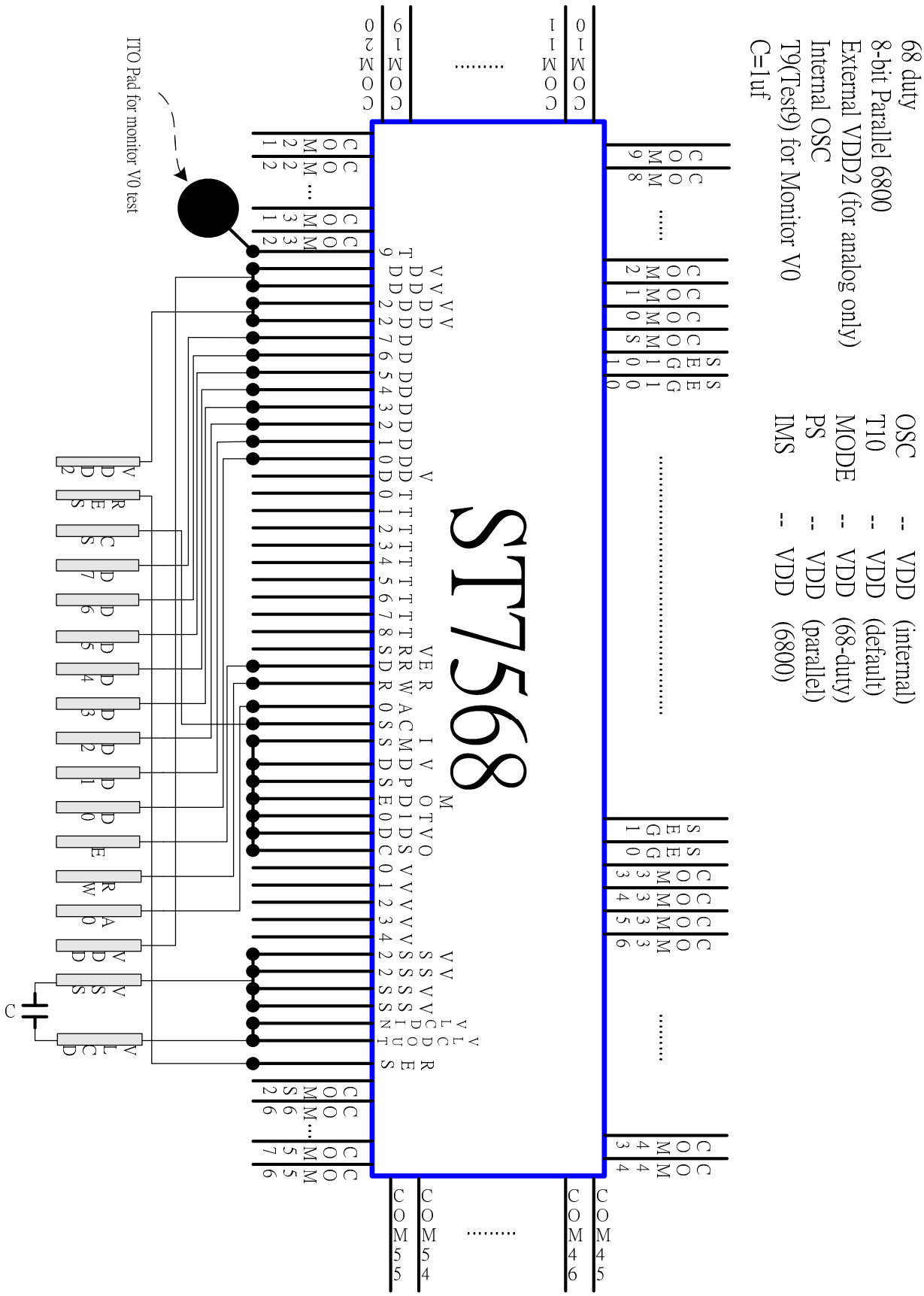


Figure - 7: 68-duty/parallel-6800 /VLCDIN-External/VDD2=VDD/External-OSC

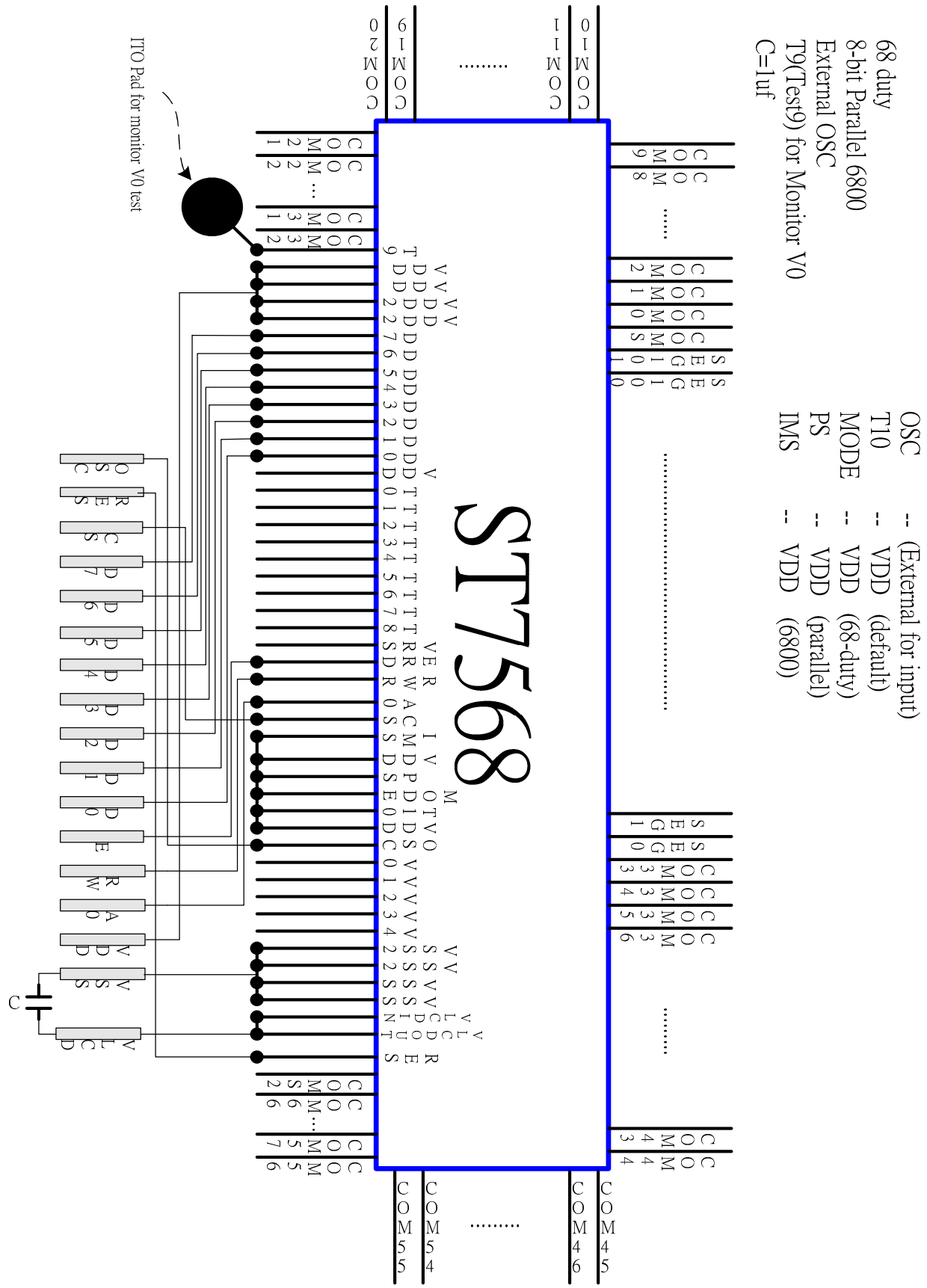
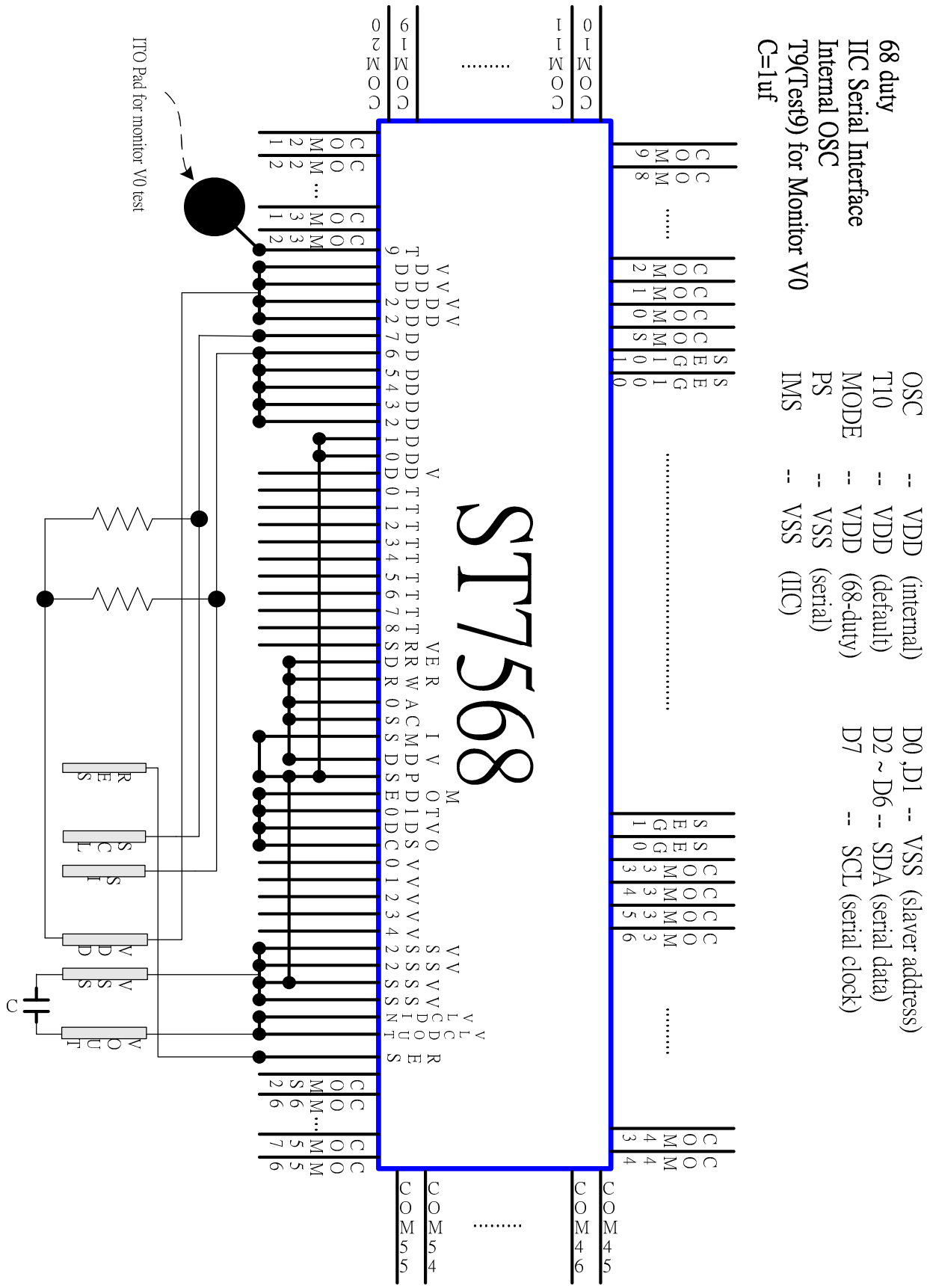


Figure - 8: 68-duty/IIC serial /VLCDIN-internal/VDD2=VDD/internal-OSC



Revision

Version 0.X - Preliminary

Version 1.0 – 2002/11/15 version 1.0

Version 1.0a – 2002/12/05 add application Note

Version 1.0b – 2003/01/02 Character Correction

Version 1.1 – 2003/04/11 modify application Note

Version 2.0 --- 2003/05/10 add ST7568i

Version 2.1 --- 2005/10/05 Gold Bump Height: 17um; voltage and temperature range.

Version 2.1a – 2007/07/24 Add ITO resistance; Fix serial application mistake: D7=SCL