Sitronix

ST7585

66 x 102 Dot Matrix LCD Controller/Driver

1. INTRODUCTION

ST7585 is a driver & controller LSI for graphic dot-matrix liquid crystal display systems. It contains 102-segment and 65-common with 1-icon-common driver circuits. This chip is connected directly to a microprocessor which accepts 3-line or 4-line serial peripheral interface (SPI) or 8-bit parallel interface. Display data stores in an on-chip display data RAM (DDRAM) of 66 x 102 bits. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

Single-chip LCD Controller & Driver

Driver Output Circuits

102-segment / 65-common+1-icon-common (1/66 duty)

On-chip Display Data RAM

- Capacity: 66X102= 6,732 bits

Microprocessor Interface

- 8-bit parallel bi-directional interface for 6800-series or 8080-series MPU
- 3-line & 4-line SPI (serial peripheral interface) are available (write only)
- Compatible with I^2C interface

External RESB (reset) Pin

Built-in Oscillation Circuit

- Oscillator requires no external component

Built-in OTP (One-Time Programmable) Function

Low Power Consumption Analog Circuit

- Voltage booster (X5)
- Voltage regulator generates LCD operating voltage (Temperature Gradient: -0.05%/°C)
- Electronic contrast control (32 steps)
- Voltage follower generates LCD bias voltages (1/7 and 1/9 bias)

Wide Supply Voltage Range

- VDD1 – VSS1 : 1.8V ~ 3.3V (covers 1.7V~3.4V)
- VDD2 – VSS2 : 2.7V ~ 3.3V (covers 2.6V~3.4V)

Recommend Display Supply Voltage

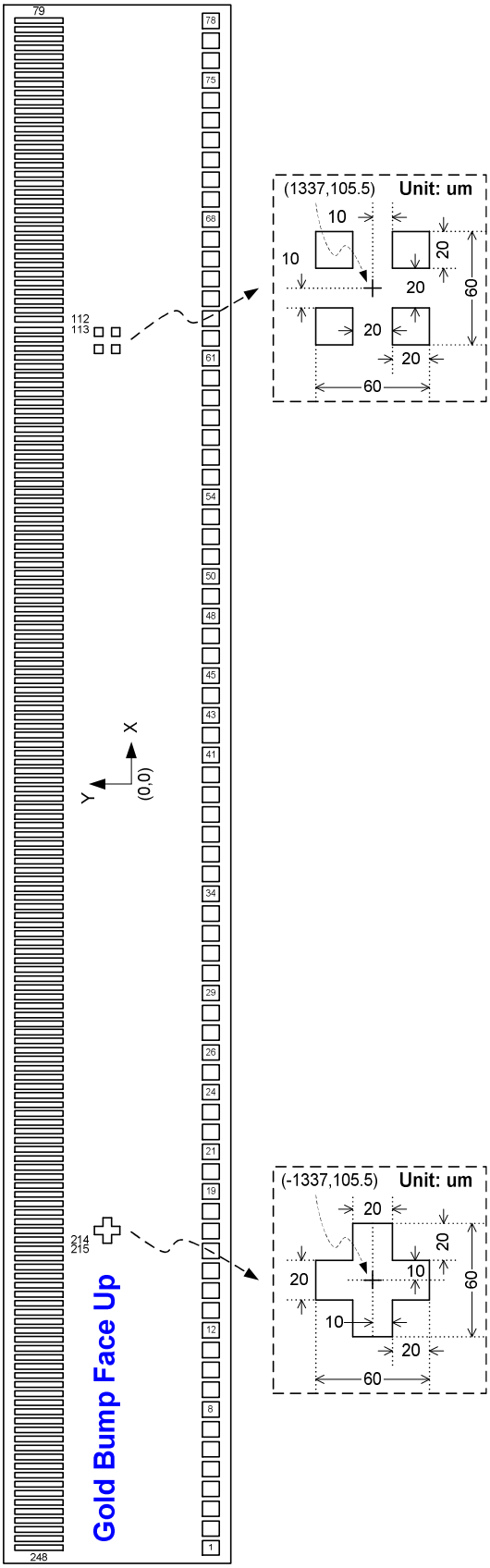
- Vop: 8.5V ~ 9.5V (1/9 bias)

LCD Module Size: 1.4" (up to 1.8")

Temperature Range: -30°C ~ +85°C

ST7585	**6800 , 8080 , 4-Line , 3-Line interface**	
ST7585i	**I^2C interface**	

3. ST7585 PAD ARRANGEMENT



Chip Size: 4720 X 650 **Unit: um**

Chip Thickness: 300 **Bump Height: 15**

PAD No.	Bump Size
5~11	35 X 57
1~4, 12~78	45 X 57
79~248	15 X 137.5
PAD No.	**Bump Pitch (min)**
5~11	50
1~4, 12~78	60
79~248	27

*** Refer "PAD CENTER COORDINATES" section for ITO layout.**

Fig 1.

4. PAD CENTER COORDINATES

66 Duty (TMX=TMY=0)

PAD#	Name	X	Y
1	VPP	-2298.50	-258.50
2	VPP	-2238.50	-258.50
3	VPP	-2178.50	-258.50
4	XEN	-2118.50	-258.50
5	VDD1	-2053.50	-258.50
6	MODE	-2003.50	-258.50
7	TA	-1953.50	-258.50
8	BR	-1903.50	-258.50
9	PS2	-1853.50	-258.50
10	PS1	-1803.50	-258.50
11	PS0	-1753.50	-258.50
12	TMX	-1698.50	-258.50
13	TMX	-1638.50	-258.50
14	TMY	-1578.50	-258.50
15	TMY	-1518.50	-258.50
16	Reserved	-1458.50	-258.50
17	Reserved	-1398.50	-258.50
18	Reserved	-1338.50	-258.50
19	Reserved	-1278.50	-258.50
20	Reserved	-1218.50	-258.50
21	Reserved	-1158.50	-258.50
22	Reserved	-1098.50	-258.50
23	VSS1	-1034.50	-258.50
24	VSS1	-966.50	-258.50
25	VSS2	-897.50	-258.50
26	VSS2	-837.50	-258.50
27	VSS2	-777.50	-258.50
28	VDD1	-717.50	-258.50
29	VDD1	-657.50	-258.50
30	VDD2	-597.50	-258.50
31	VDD2	-537.50	-258.50
32	VDD2	-477.50	-258.50
33	RESB	-417.50	-258.50
34	CSB	-357.50	-258.50
35	RWR	-297.50	-258.50
36	ERD	-237.50	-258.50
37	A0	-177.50	-258.50
38	D[7]	-117.50	-258.50
39	D[6]	-57.50	-258.50
40	D[5]	2.50	-258.50
41	D[4]	62.50	-258.50
42	D[3]	122.50	-258.50
43	D[2]	182.50	-258.50
44	D[1]	242.50	-258.50
45	D[0]	302.50	-258.50
46	OSC	362.50	-258.50
47	VDD1	426.50	-258.50
48	Reserved	494.50	-258.50
49	Reserved	558.50	-258.50
50	Reserved	618.50	-258.50
51	Reserved	678.50	-258.50
52	VSS1	738.50	-258.50
53	VSS1	798.50	-258.50
54	VSS2	858.50	-258.50
55	VSS2	918.50	-258.50
56	VSS2	978.50	-258.50
57	VMO	1038.50	-258.50
58	VGO	1098.50	-258.50
59	VGO	1158.50	-258.50
60	VGS	1218.50	-258.50
61	VGI	1278.50	-258.50
62	VGI	1338.50	-258.50
63	VGI	1398.50	-258.50
64	VGI	1458.50	-258.50
65	V0I	1518.50	-258.50
66	V0I	1578.50	-258.50
67	V0I	1638.50	-258.50
68	V0I	1698.50	-258.50
69	V0S	1758.50	-258.50
70	V0O	1818.50	-258.50
71	V0O	1878.50	-258.50
72	XV0O	1938.50	-258.50
73	XV0O	1998.50	-258.50
74	XV0S	2058.50	-258.50
75	XV0I	2118.50	-258.50
76	XV0I	2178.50	-258.50
77	XV0I	2238.50	-258.50
78	XV0I	2298.50	-258.50
79	Reserved	2305.50	217.75
80	COMS2	2278.50	217.75
81	COM[64]	2251.50	217.75
82	COM[63]	2224.50	217.75

PAD#	Name	X	Y
83	COM[62]	2197.50	217.75
84	COM[61]	2170.50	217.75
85	COM[60]	2143.50	217.75
86	COM[59]	2116.50	217.75
87	COM[58]	2089.50	217.75
88	COM[57]	2062.50	217.75
89	COM[56]	2035.50	217.75
90	COM[55]	2008.50	217.75
91	COM[54]	1981.50	217.75
92	COM[53]	1954.50	217.75
93	COM[52]	1927.50	217.75
94	COM[51]	1900.50	217.75
95	COM[50]	1873.50	217.75
96	COM[49]	1846.50	217.75
97	COM[48]	1819.50	217.75
98	COM[47]	1792.50	217.75
99	COM[46]	1765.50	217.75
100	COM[45]	1738.50	217.75
101	COM[44]	1711.50	217.75
102	COM[43]	1684.50	217.75
103	COM[42]	1657.50	217.75
104	COM[41]	1630.50	217.75
105	COM[40]	1603.50	217.75
106	COM[39]	1576.50	217.75
107	COM[38]	1549.50	217.75
108	COM[37]	1522.50	217.75
109	COM[36]	1495.50	217.75
110	COM[35]	1468.50	217.75
111	COM[34]	1441.50	217.75
112	COM[33]	1414.50	217.75
113	SEG[0]	1363.50	217.75
114	SEG[1]	1336.50	217.75
115	SEG[2]	1309.50	217.75
116	SEG[3]	1282.50	217.75
117	SEG[4]	1255.50	217.75
118	SEG[5]	1228.50	217.75
119	SEG[6]	1201.50	217.75
120	SEG[7]	1174.50	217.75
121	SEG[8]	1147.50	217.75
122	SEG[9]	1120.50	217.75
123	SEG[10]	1093.50	217.75
124	SEG[11]	1066.50	217.75
125	SEG[12]	1039.50	217.75
126	SEG[13]	1012.50	217.75

PAD#	Name	X	Y
127	SEG[14]	985.50	217.75
128	SEG[15]	958.50	217.75
129	SEG[16]	931.50	217.75
130	SEG[17]	904.50	217.75
131	SEG[18]	877.50	217.75
132	SEG[19]	850.50	217.75
133	SEG[20]	823.50	217.75
134	SEG[21]	796.50	217.75
135	SEG[22]	769.50	217.75
136	SEG[23]	742.50	217.75
137	SEG[24]	715.50	217.75
138	SEG[25]	688.50	217.75
139	SEG[26]	661.50	217.75
140	SEG[27]	634.50	217.75
141	SEG[28]	607.50	217.75
142	SEG[29]	580.50	217.75
143	SEG[30]	553.50	217.75
144	SEG[31]	526.50	217.75
145	SEG[32]	499.50	217.75
146	SEG[33]	472.50	217.75
147	SEG[34]	445.50	217.75
148	SEG[35]	418.50	217.75
149	SEG[36]	391.50	217.75
150	SEG[37]	364.50	217.75
151	SEG[38]	337.50	217.75
152	SEG[39]	310.50	217.75
153	SEG[40]	283.50	217.75
154	SEG[41]	256.50	217.75
155	SEG[42]	229.50	217.75
156	SEG[43]	202.50	217.75
157	SEG[44]	175.50	217.75
158	SEG[45]	148.50	217.75
159	SEG[46]	121.50	217.75
160	SEG[47]	94.50	217.75
161	SEG[48]	67.50	217.75
162	SEG[49]	40.50	217.75
163	SEG[50]	13.50	217.75
164	SEG[51]	-13.50	217.75
165	SEG[52]	-40.50	217.75
166	SEG[53]	-67.50	217.75
167	SEG[54]	-94.50	217.75
168	SEG[55]	-121.50	217.75
169	SEG[56]	-148.50	217.75
170	SEG[57]	-175.50	217.75

PAD#	Name	X	Y
171	SEG[58]	-202.50	217.75
172	SEG[59]	-229.50	217.75
173	SEG[60]	-256.50	217.75
174	SEG[61]	-283.50	217.75
175	SEG[62]	-310.50	217.75
176	SEG[63]	-337.50	217.75
177	SEG[64]	-364.50	217.75
178	SEG[65]	-391.50	217.75
179	SEG[66]	-418.50	217.75
180	SEG[67]	-445.50	217.75
181	SEG[68]	-472.50	217.75
182	SEG[69]	-499.50	217.75
183	SEG[70]	-526.50	217.75
184	SEG[71]	-553.50	217.75
185	SEG[72]	-580.50	217.75
186	SEG[73]	-607.50	217.75
187	SEG[74]	-634.50	217.75
188	SEG[75]	-661.50	217.75
189	SEG[76]	-688.50	217.75
190	SEG[77]	-715.50	217.75
191	SEG[78]	-742.50	217.75
192	SEG[79]	-769.50	217.75
193	SEG[80]	-796.50	217.75
194	SEG[81]	-823.50	217.75
195	SEG[82]	-850.50	217.75
196	SEG[83]	-877.50	217.75
197	SEG[84]	-904.50	217.75
198	SEG[85]	-931.50	217.75
199	SEG[86]	-958.50	217.75
200	SEG[87]	-985.50	217.75
201	SEG[88]	-1012.50	217.75
202	SEG[89]	-1039.50	217.75
203	SEG[90]	-1066.50	217.75
204	SEG[91]	-1093.50	217.75
205	SEG[92]	-1120.50	217.75
206	SEG[93]	-1147.50	217.75
207	SEG[94]	-1174.50	217.75
208	SEG[95]	-1201.50	217.75
209	SEG[96]	-1228.50	217.75
210	SEG[97]	-1255.50	217.75
211	SEG[98]	-1282.50	217.75
212	SEG[99]	-1309.50	217.75
213	SEG[100]	-1336.50	217.75

PAD#	Name	X	Y
214	SEG[101]	-1363.50	217.75
215	COMS1	-1414.50	217.75
216	COM[0]	-1441.50	217.75
217	COM[1]	-1468.50	217.75
218	COM[2]	-1495.50	217.75
219	COM[3]	-1522.50	217.75
220	COM[4]	-1549.50	217.75
221	COM[5]	-1576.50	217.75
222	COM[6]	-1603.50	217.75
223	COM[7]	-1630.50	217.75
224	COM[8]	-1657.50	217.75
225	COM[9]	-1684.50	217.75
226	COM[10]	-1711.50	217.75
227	COM[11]	-1738.50	217.75
228	COM[12]	-1765.50	217.75
229	COM[13]	-1792.50	217.75
230	COM[14]	-1819.50	217.75
231	COM[15]	-1846.50	217.75
232	COM[16]	-1873.50	217.75
233	COM[17]	-1900.50	217.75
234	COM[18]	-1927.50	217.75
235	COM[19]	-1954.50	217.75
236	COM[20]	-1981.50	217.75
237	COM[21]	-2008.50	217.75
238	COM[22]	-2035.50	217.75
239	COM[23]	-2062.50	217.75
240	COM[24]	-2089.50	217.75
241	COM[25]	-2116.50	217.75
242	COM[26]	-2143.50	217.75
243	COM[27]	-2170.50	217.75
244	COM[28]	-2197.50	217.75
245	COM[29]	-2224.50	217.75
246	COM[30]	-2251.50	217.75
247	COM[31]	-2278.50	217.75
248	COM[32]	-2305.50	217.75

Note:

- Tolerance: +/- 0.02um
- Please refer to “Fig 12” (Page 18) for detailed output map for TMX=1 or TMY=1.
- Please don’t use the “Reserved” pads.

5. BLOCK DIAGRAM

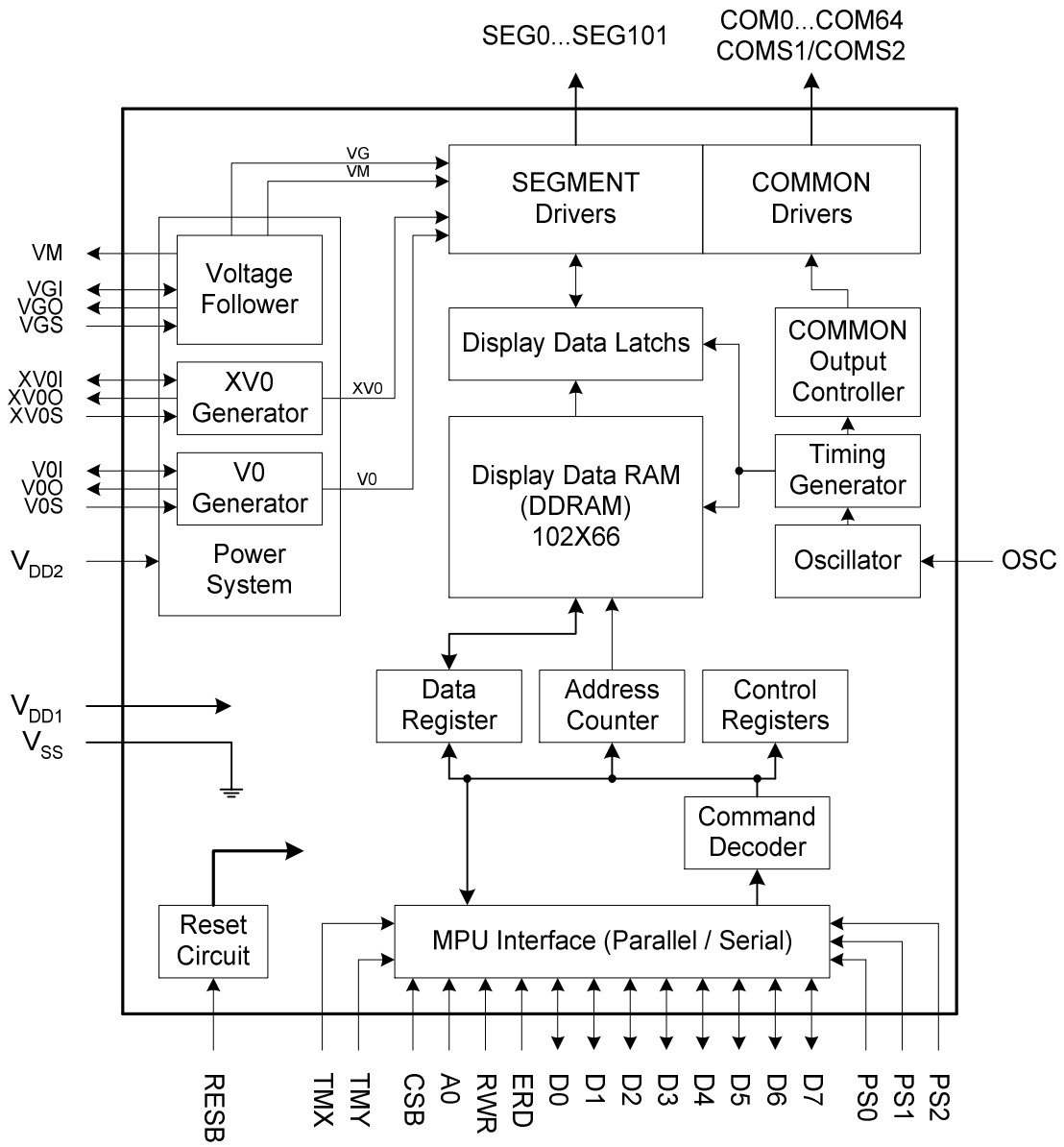


Fig 2. Block Diagram

6. PINNING DESCRIPTIONS

LCD Driver Output Pins

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td>SEG0 to SEG101</td><td>O</td><td>LCD segment driver outputs.
The display data and the frame control the output voltage.
<table>
<tr><th rowspan="2">Display data</th><th rowspan="2">Frame</th><th colspan="2">Segment driver output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>+</td><td>VG</td><td>VSS</td></tr>
<tr><td>H</td><td>-</td><td>VSS</td><td>VG</td></tr>
<tr><td>L</td><td>+</td><td>VSS</td><td>VG</td></tr>
<tr><td>L</td><td>-</td><td>VG</td><td>VSS</td></tr>
<tr><td colspan="2">Display OFF, Power Save</td><td>VSS</td><td>VSS</td></tr>
</table></td><td>102</td></tr>
<tr><td>COM0 to COM64</td><td>O</td><td>LCD common driver outputs.
The internal scanning signal and the frame control the output voltage.
<table>
<tr><th rowspan="2">Scan signal</th><th rowspan="2">Frame</th><th colspan="2">Common driver output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>+</td><td colspan="2">XV0</td></tr>
<tr><td>H</td><td>-</td><td colspan="2">V0</td></tr>
<tr><td>L</td><td>+</td><td colspan="2">VM</td></tr>
<tr><td>L</td><td>-</td><td colspan="2">VM</td></tr>
<tr><td colspan="2">Display OFF, Power Save</td><td colspan="2">VSS</td></tr>
</table></td><td>65</td></tr>
<tr><td>COMS1, COMS2
(COMS)</td><td>O</td><td>LCD common driver outputs for icons. These two pins are identical. Choose one of them if using icon. When icon is not used, left these pins open.</td><td>2</td></tr>
<tr><td>TMX</td><td>I</td><td>Select SEG output direction. Refer to “Fig 12”.
TMX=“L” : Normal direction (SEG0 ~ SEG101).
TMX=“H” : Reverse direction (SEG101 ~ SEG0).</td><td>2</td></tr>
<tr><td>TMY</td><td>I</td><td>Select COM output direction. Refer to “Fig 12”.
TMY=“L” : Normal direction (COM0 ~ COM64).
TMY=“H” : Reverse direction (COM64 ~ COM0).</td><td>2</td></tr>
</table>

Clock System Input

Pin Name	Type	Description	No. of Pins
OSC	**I**	OSC=“H” : Use built-in oscillator.	**1**

Power Supply Pins

Pin Name	Type	Description	No. of Pins
VSS1	**Power**	Digital ground. Connect to VSS2 by FPC. For pins that are set to be “L”, connect them to this power (use VSS1 for “L”).	**4**
VSS2	**Power**	Analog ground. Connect to VSS1 by FPC.	**6**
VDD1	**Power**	Digital power. If VDD1=VDD2, connect to VDD2 by FPC. For pins that are set to be “H”, connect them to this power (use VDD1 for “H”).	**4**
VDD2	**Power**	Analog power. If VDD1=VDD2, connect to VDD1 by FPC.	**3**

Built-in Power System Pins

Pin Name	Type	Description	No. of Pins
V0O V0I V0S	**Power**	LCD driving voltage for commons at negative frame. V0 ≥ VG > VM > VSS ≥ XV0 V0O, V0I & V0S should be separated in ITO layout. V0O, V0I & V0S should be connected together in FPC layout.	**2** **4** **1**
XV0O XV0I XV0S	**Power**	LCD driving voltage for commons at positive frame. XV0O, XV0I & XV0S should be separated in ITO layout. XV0O, XV0I & XV0S should be connected together in FPC layout.	**2** **4** **1**
VGO VGI VGS	**Power**	LCD driving voltage for segments. VGO, VGI & VGS should be separated in ITO layout. VGO, VGI & VGS should be connected together in FPC layout. 1.8 ≤ VG < VDD2.	**2** **4** **1**
BR	**I**	Bias circuit configuration pin for default setting : “L”=1/7; “H”=1/9. This pin sets the default bias ratio after reset.	**1**

Microprocessor Interface Pins

Pin Name	Type	Description	No. of Pins
PS[2:0]	**I**	Microprocessor interface select pins. **PS2** / **PS1** / **PS0** / **Selected Interface** “L” / “L” / “L” / 3-Line SPI interface “L” / “L” / “H” / 4-Line SPI interface “L” / “H” / “L” / 6800-series parallel interface “L” / “H” / “H” / 8080-series parallel interface “H” / “L” / “L” / I^2C Interface	**3**
CSB	**I**	Chip select input pin. Interface access is enabled when CSB is “L”. When CSB is non-active (CSB=“H”), D[7:0] pins are high impedance. CSB is not used in serial interfaces and should fix to “H” by VDD1.	**1**
RESB	**I**	Reset input pin. When RESB is “L”, internal initialization is executed.	**1**
A0	**I**	It determines whether the access is related to data or command. A0=“H” : Indicates that D[7:0] are display data. A0=“L” : Indicates that D[7:0] are control data. A0 is not used in serial interfaces and should fix to “H” by VDD1.	**1**
RWR	**I**	Read/Write execution control pin. When parallel interface is selected: **MPU Type** / **RWR** / **Description** 6800 series / R/W / Read/Write control input pin. R/W=“H”: read. R/W=“L”: write. 8080 series / /WR / Write enable input pin. Signals on D[7:0] will be latched at the rising edge of /WR signal. RWR is not used in serial interfaces and should fix to “H” by VDD1.	**1**

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td>ERD</td><td>I</td><td>Read/Write execution control pin. When parallel interface is selected:
<table>
<tr><th>MPU Type</th><th>ERD</th><th>Description</th></tr>
<tr><td>6800 series</td><td>E</td><td>Read/Write control input pin.
R/W=”H“: When E is “H”, D[7:0] are in an output status.
R/W=”L“: Signals on D[7:0] are latched at the falling edge of E signal.</td></tr>
<tr><td>8080 series</td><td>/RD</td><td>Read enable input pin.
When /RD is “L”, D[7:0] are in output status.</td></tr>
</table>
ERD is not used in serial interfaces and should fix to “H” by VDD1.</td><td>1</td></tr>
<tr><td rowspan="3">D[7:0]</td><td>I/O</td><td>When using 8-bit parallel interface: 6800 or 8080 mode
8-bit bi-directional data bus. Connect to the data bus of 8-bit microprocessor.
When CSB is non-active (CSB=“H”), D[7:0] pins are high impedance.</td><td rowspan="3">8</td></tr>
<tr><td>I</td><td>When using serial interface: 4-LINE or 3-LINE
D7=SCLK : Serial clock input.
D6=SDA : Serial data input.
D5=A0 : Command / Data selection (unused in 3-Line SPI; fix to H by VDD1).
D4=CSB : Chip select pin.
D[3:0] : Not used and should fix to “H” by VDD1.</td></tr>
<tr><td>I, O</td><td>When using I^{2}C interface
D7=SCLK : Serial clock input.
D6=SDA_IN [*1] : Serial data input.
D[5:3] : SDA_OUT [*1] : Outputs for acknowledge-bit of the I^{2}C protocol.
D[2]= Not used and should fix to “H” by VDD1.
D[1:0]=SA[1:0] : Slave address bits. Must set to “H” by VDD1 or “L” by VSS1.
<u>D[6:3] must connect together (SDA).</u> [*1]
CSB is not used in I^{2}C interface and should fix to “H” by VDD1.</td></tr>
</table>

Note:

1. By connecting SDA_IN and SDA_OUT externally, the SDA line becomes fully I^{2}C interface compatible. Separating acknowledge-output from serial data input is advantageous for chip-on-glass (COG) applications. In COG applications, the ITO resistance and the pull-up resistor will form a voltage divider which affects acknowledge-signal level. Larger ITO resistance will raise the acknowledge-signal level and system cannot recognize this level as a valid logic “0” level. By separating SDA_IN from SDA_OUT, the IC can be used in a mode which ignores the acknowledge-bit. For applications which check acknowledge-bit, it is necessary to minimize the ITO resistance of the SDA_OUT trace to guarantee a valid low level.
2. After VDD1 is turned ON, any MPU interface pins cannot be left floating.

OTP Pins

Pin Name	Type	Description	No. of Pins
VPP	**Power**	Programming voltage of OTP.	**3**
XEN	**I**	OTP programming control pin. This pin is pulled high internally. XEN="L", programming OPT is enabled. XEN="Floating", programming OPT is disabled.	**1**

Test Pins

Pin Name	Type	Description	No. of Pins
MODE	**Test**	Do NOT use. Reserved for testing. Must be "L". Connect to VSS1 for pull-low.	**1**
VMO	**Test**	Output VM for IC testing only.	**1**
TA	**Test**	Do NOT use. Reserved for testing. Must be "L". Connect to VSS1 for pull-low.	**1**

Recommend ITO Resistance

Pin Name	ITO Resistance
VMO, Reserved	Floating
VDD1, VDD2, VSS1, VSS2, VPP	< 100Ω
V0(V0I, V0O, V0S), VG(VGI, VGO, VGS), XV0(XV0I, XV0O, XV0S), SDA *1	< 300Ω
A0, RWR, ERD, CSB, D[7:0] *1	< 1KΩ
PS[2:0], OSC, BR, TMX, TMY, MODE, TA, XEN	< 5KΩ
RESB *2	< 10KΩ

Note:

1. If using I^2C interface mode, the resistance of SDA signal should be lower than 300Ω (if the system pull up resistor is 4.7KΩ).
   If using 3-Line or 4-Line SPI interface with VDD1 less than 2.4V, the SDA signal resistance should be less than 500Ω.
2. To prevent the ESD pulse resetting the internal register, applications should increase the resistance of RESB signal (add a series resistor or increase ITO resistance). The value is different from modules.
3. This table defines the actual ITO resistance. The actual ITO resistance should in these ranges, not the calculated ITO resistance value. The ITO tolerance should be considered.
4. The option setting to be "H" should connect to VDD1.
5. The option setting to be "L" should connect to VSS1.

7. FUNCTIONS DESCRIPTION

Microprocessor Interface

Chip Select Input

CSB pin is used for chip selection. ST7585 can interface with an MPU when CSB is "L". When CSB is “H”, the inputs of A0, ERD and RWR with any combination will be ignored and D[7:0] are high impedance. In 3-Line and 4-Line serial interface, the internal shift register and serial counter are reset when CSB is “H”.

Parallel / Serial Interface

ST7585 has types of interface for kinds of MPU. The MPU interface is selected by PS[2:0] pins as shown in table 1.

Table 1. Parallel/Serial Interface Mode

PS2	PS1	PS0	CSB	A0	ERD	RWR	D[7:0]	MPU Interface
“L”	“L”	“L”	---	---	---	---	Refer to serial interface.	3-Line SPI interface
“L”	“L”	“H”						4-Line SPI interface
“L”	“H”	“L”	CSB	A0	E	R/W	D[7:0]	6800-series parallel interface
“L”	“H”	“H”			/RD	/WR		8080-series parallel interface
“H”	“L”	“L”	---	---	---	---	Refer to serial interface.	I^2C Interface

* The un-used pins are marked as “---” and should be fixed to “H” by VDD1.

Parallel Interface

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by PS0 (fix PS2=L, PS1=H) as shown in table 2. The data transfer type is determined by signals of A0, ERD and RWR as shown in table 3.

Table 2. Microprocessor Selection for Parallel Interface

PS2	PS1	PS0	CSB	A0	ERD	RWR	D[7:0]	MPU Interface
“L”	“H”	“L”	CSB	A0	E	R/W	D[7:0]	6800-series
“L”	“H”	“H”			/RD	/WR		8080-series

Table 3. Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	E (ERD)	R/W (RWR)	/RD (ERD)	/WR (RWR)	
“H”	“H”	“H”	“L”	“H”	Display data read out
“H”	“H”	“L”	“H”	“L”	Display data write
“L”	“H”	“H”	“L”	“H”	Internal status read
“L”	“H”	“L”	“H”	“L”	Writes to internal register (instruction)

NOTE: In 6800-series interface mode, fixing E (ERD) pin at high can use CSB as enable signal instead. In this case, interface data is latched at the rising edge of CSB and the type of data transfer is determined by signals at A0 and R/W (RWR) pins as defined in 6800-series mode.

Setting Serial Interface

Interface	PS[2:0]	CSB, A0, ERD, RWR	D[7:0]
3-Line SPI	“L, L, L”	---	SCLK, SDA, ---, CSB, ---, ---, ---, ---
4-Line SPI	“L, L, H”		SCLK, SDA, A0, CSB, ---, ---, ---, ---
I^2C	“H, L, L”		SCLK, SDA_IN, SDA_OUT, SDA_OUT, SDA_OUT, ---, SA1, SA0

* The un-used pins are marked as “---” and should be fixed to “H” by VDD1.

Note:

1. The option setting to be “H” should connect to VDD1.
2. The option setting to be “L” should connect to VSS1.

4-Line & 3-Line Serial interface

In 4-Line and 3-Line interface, ST7585 is active when CSB is “L”, and serial data (SDA) and serial clock (SCLK) inputs are enabled. When CSB is “H”, ST7585 is not active, and the internal 8-bit shift register and 3-bit counter are reset. The read feature is not supported in this mode. The DDRAM column address pointer will be increased by one automatically after writing each byte of DDRAM.

4-Line Serial Interface

The display data/command indication is controlled by the register selection pin (A0). The signals transferred on data bus will be display data when A0 is high and will be instruction when A0 is low. Serial data (SDA) is latched at the rising edge of serial clock (SCLK). After the 8th serial clock, the serial data will be processed as 8-bit parallel data.

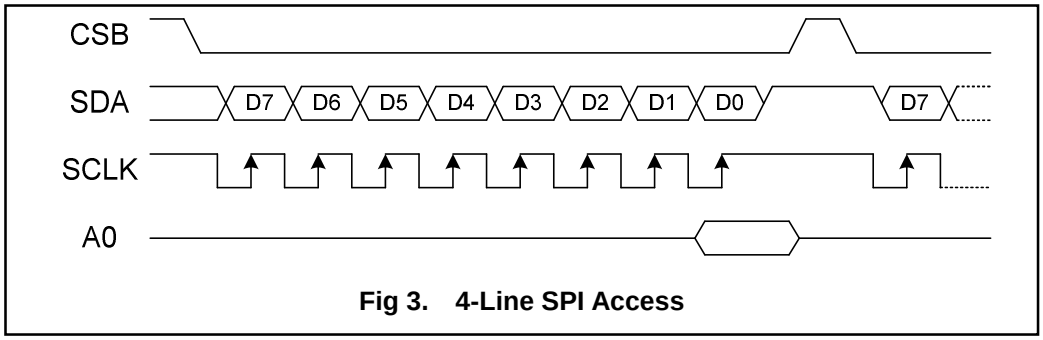


Fig 3. 4-Line SPI Access

3-Line Serial Interface

The A0 pin is not available in this mode. Before issuing serial data, an A0 bit is required to indicate the following 8-bit signals are data or instruction. Serial data (SDA) is latched at the rising edge of serial clock (SCLK). After the 9th serial clock, the serial data will be processed as 8-bit parallel data.

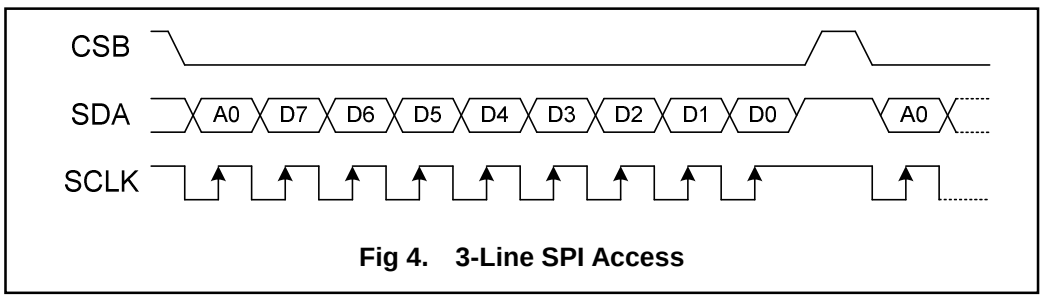


Fig 4. 3-Line SPI Access

I²C Interface

The I²C Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCLK). Both lines must be connected with a pull-up resistor which drives SDA and SCLK to high when the bus is not busy. Data transfer can be initiated only when the bus is not busy.

The I²C interface of ST7585 supports write access and read of acknowledge-bit. The I²C interface receives and executes the commands sent via the I²C Interface. It also receives RAM data and sends it to the Display RAM.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on SDA line must remain stable during the HIGH period of the clock pulse because changes of SDA line at this time will be interpreted as START or STOP condition. Refer to Fig 5.

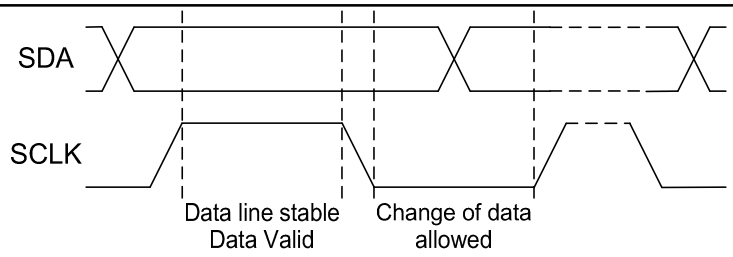


Fig 5. Bit transfer

START AND STOP CONDITIONS

Both SDA and SCLK lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of SDA, while SCLK is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCLK is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig 6.

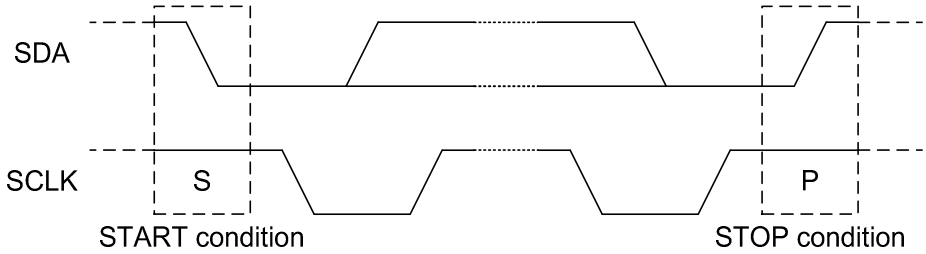


Fig 6. Definition of START and STOP conditions

SYSTEM CONFIGURATION

The system configuration is illustrated in Fig 7 and some word-definitions are explained below:

- Transmitter: the device which sends the data to the bus.
- Receiver: the device which receives the data from the bus.
- Master: the device, which initiates a transfer, generates clock signals and terminates a transfer.
- Slave: the device which is addressed by a master.
- Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: the procedure to ensure that, if more than one master tries to control the bus simultaneously, only one is allowed to do so and the message is not corrupted.
- Synchronization: procedure to synchronize the clock signals of two or more devices.

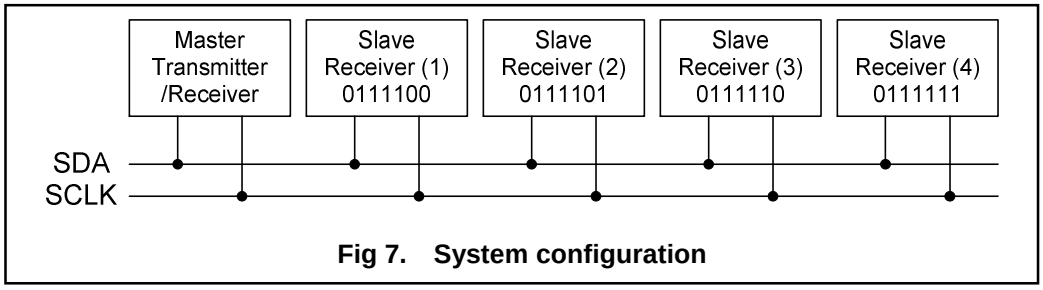


Fig 7. System configuration

ACKNOWLEDGEMENT

Each byte of eight bits is followed by an acknowledge-bit. The acknowledge-bit is a HIGH signal put on SDA by the transmitter during the time when the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge-bit after the reception of each byte. The device that acknowledges must pull-down the SDA line during the acknowledge-clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). Acknowledgement on the I^2C Interface is illustrated in Fig 8.

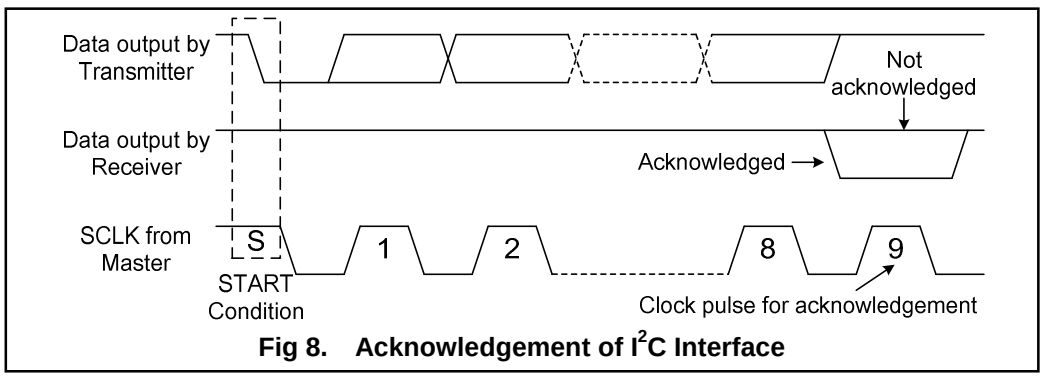


Fig 8. Acknowledgement of I^2C Interface

I^2C INTERFACE PROTOCOL

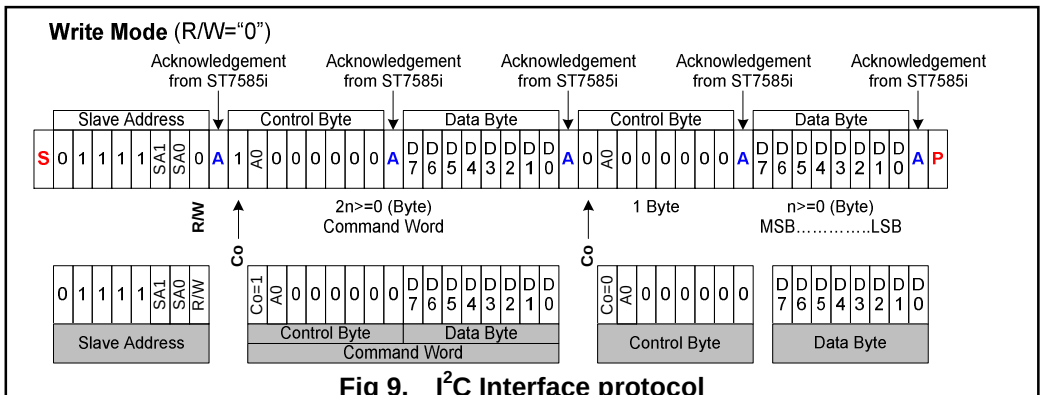


Fig 9. I^2C Interface protocol

Co	0	Last control byte. Only a stream of data bytes is allowed to follow. This stream may only be terminated by a STOP or RE-START condition.
	1	Another control byte will follow the data byte.

ST7585 supports command/data write to addressed slaves on the bus. The I^2C Interface protocol is illustrated in Fig 9.

Before any data is transmitted on the I^2C Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111**00**, 0111**01**, 0111**10** and 0111**11**) are reserved for ST7585. The least significant 2 bits of the slave address is set by connecting SA0 and SA1 to either logic 0 (VSS1) or logic 1 (VDD1).

The sequence is initiated with a START condition (S) from the I^2C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I^2C Interface transfer. After acknowledgement, one or more command words are followed and define the status of the addressed slaves. A command word consists of a control byte, which defines Co and A0, and a data byte.

The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data byte(s) will follow. The state of the A0 bit defines whether the following data bytes are interpreted as commands or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte either a series of display data bytes or command data bytes may follow (depending on the A0 bit setting).

If the A0 bit of the last control byte is set to logic 1, these data bytes (display data bytes) will be stored in the display RAM at the address specified by the internal data pointer. The data pointer is automatically updated and the data is directed to the intended ST7585 device.
If the A0 bit of the last control byte is set to logic 0, these data bytes (command data byte) will be decoded and the setting of ST7585 will be changed according to the received commands.

Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the bus master issues a STOP condition (P).

Data Transfer

ST7585 uses bus holder and internal data bus for data transfer with MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in Fig 10. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in Fig 11. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

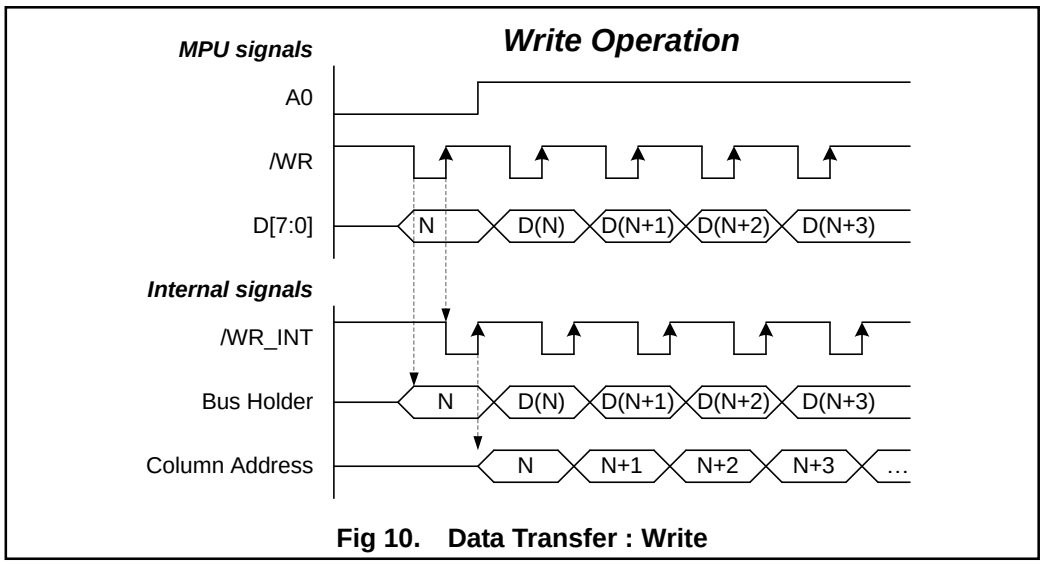


Fig 10. Data Transfer : Write

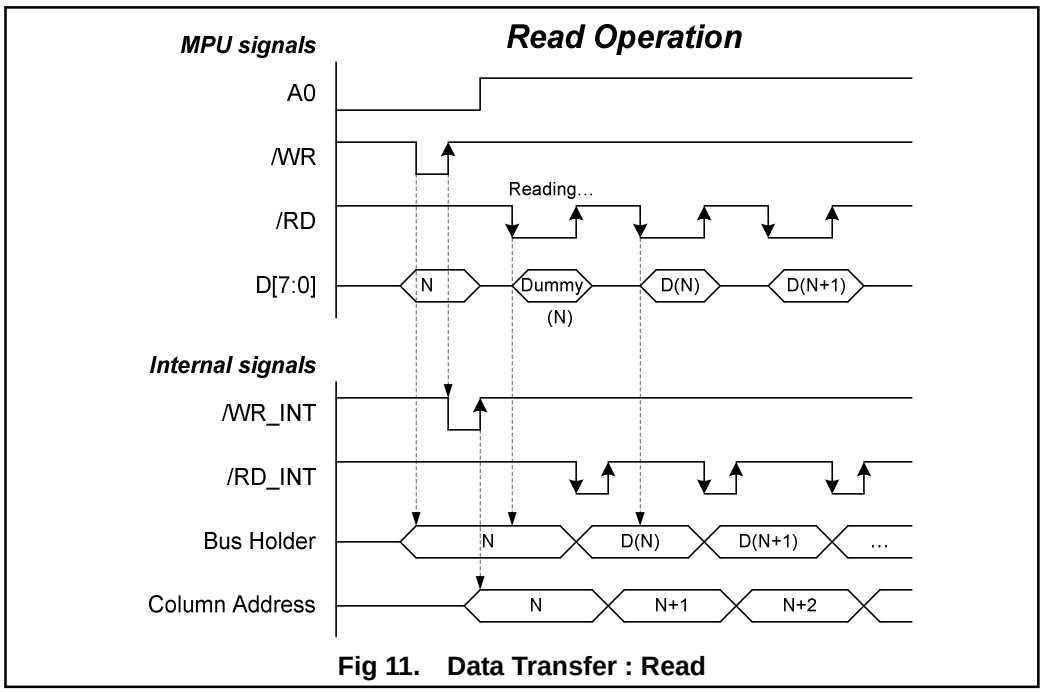


Fig 11. Data Transfer : Read

Display Data RAM (DDRAM)

ST7585 contains a 66X102 bit static RAM that stores the display data. The display data RAM (DDRAM) store the dot data for the LCD. It is an addressable array with 102 columns by 66 rows (8-page with 8-bit, 1-page with 1-bit and 1-page with 1-bit). The X-address is directly related to the column output number. Each pixel can be selected when the page and column addresses are specified. The rows are divided into: 8 pages (page 0~7) each with 8 lines (for COM0~63), the 8th page with only 1 line (for COM64) and the 9th page with only 1 line (the 65th row, COMS, for icon). The display data (D7~D0) corresponds to the LCD common-line direction (D7 at top). Those pages with 8 lines can be accessed through D[7:0] directly. When accessing those pages with fewer than 8 lines, the valid bit(s) in D[7:0] should be checked. Refer to Fig 13 for detailed illustration. The microprocessor can write to and read from (only Parallel interfaces) DDRAM by the I/O buffer. Since the LCD controller operates independently, data can be written into DDRAM at the same time as data is being displayed without causing the LCD flicker or data-conflict.

Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM. It incorporates 4-bit Page Address register changed by only the “Set Page” instruction. Page Address 9 is a special RAM area for the icons and display data is only 1-bit valid (D7).

Line Address Circuit

This circuit controls each line in DDRAM to transfer 102-bit line data to the display data latch circuit. Therefore, the content in DDRAM can be transferred to the segment drivers, and display the content on the LCD module as shown in Fig 12. At the beginning of each LCD frame, the 102-bit RAM data of Line-0 are transferred to the display data latch circuit. At the next line period, the Line Address is increased by one and the 102-bit RAM data at the next line are transferred to the display data latch circuit. The 102-bit icon data are transferred at the last line period during each frame.

Column Address Circuit

Column Address Circuit has an 8-bit preset counter that provides Column Address to the DDRAM. The display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously.

TMX and TMY make it possible to invert the relationship between the addresses (Line Address and Column Address) and the outputs (COM/SEG). It is necessary to rewrite the display data into built-in RAM after changing TMX setting. The relation between DDRAM and outputs with different TMX or TMY setting is shown below.

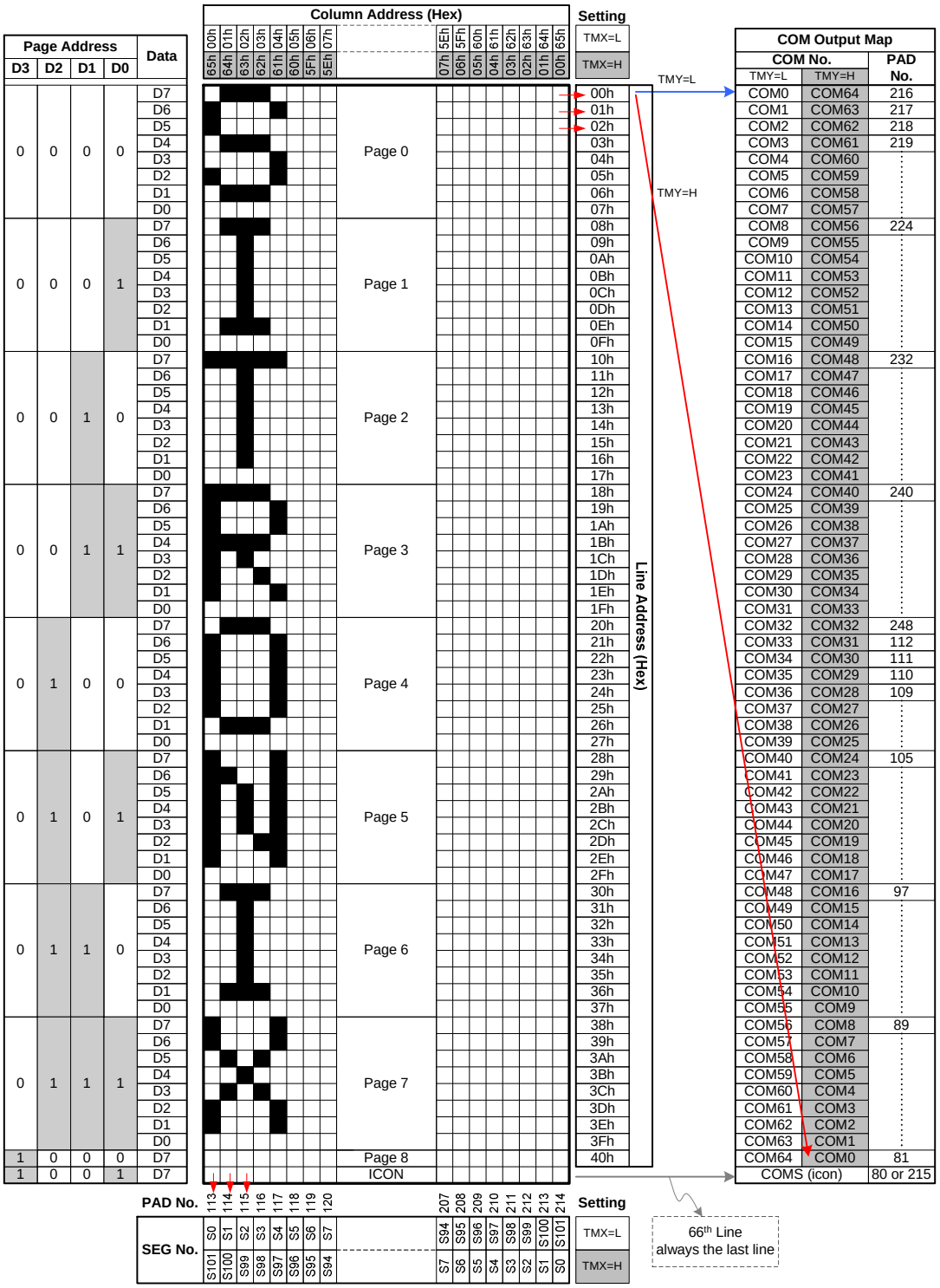


Fig 12. Relationship between DDRAM and Outputs

Addressing

Data is downloaded in bytes into the Display Data RAM matrix of ST7585 as shown below. The Display Data RAM has a matrix of 66 by 102 bits. The address pointer addresses the columns. The address ranges are: X 0 to 101 (1100101), Y 0 to 9 (1001) .Addresses outside these ranges are not allowed.

In horizontal addressing mode the X address increments after each byte (see Fig 15). After the last X address (X = 101), X wraps around to 0 and Y increments to address the next row.

After the very last address (X = 101, Y = 8) the address pointers wrap around to address (X = 0, Y =0)

Data Structure

Fig 13. RAM format

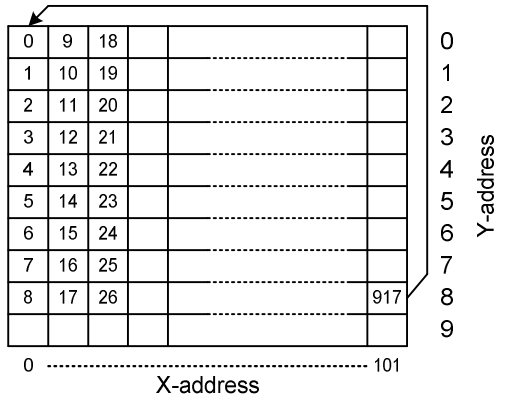


Fig 14. Addressing : Vertical Mode (V=1)

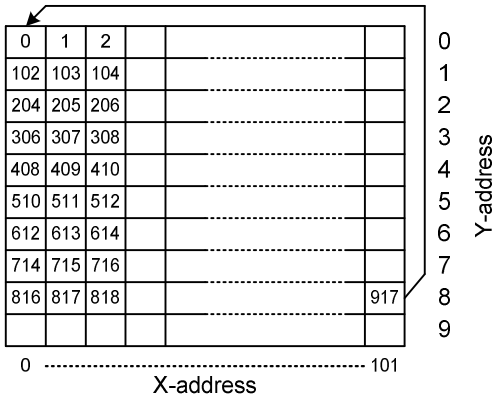


Fig 15. Addressing : Horizontal Mode (V=0)

Liquid Crystal Driver Power Circuit

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction.

External Power Components

The recommended external power components need only 2 capacitors. The detailed values of these two capacitors are determined by the panel size and loading.

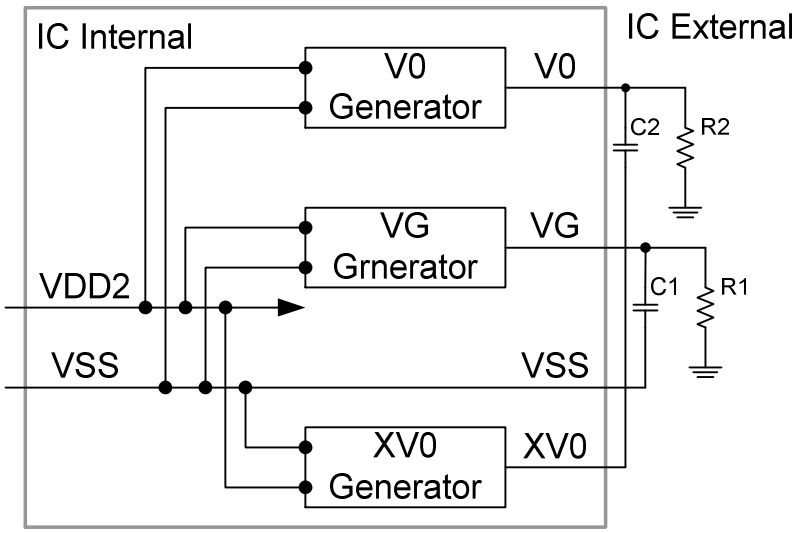


Fig 16. Power Circuit

The referential external component values are listed below (it is determined by the worse condition on 1.4” panel).

C1=0.1uF~1uF (Non-Polar/6V, default 1uF)

R1=47KΩ~100KΩ (default N.C.)

C2=0.1uF~1uF (Non-Polar/16V, default 0.1uF)

R2=600KΩ~1MΩ (default 750KΩ)

Customer applications are not necessary the same as the values listed above. The value can be determined by customer’s LCD module (panel loading and ITO resistance) and application (VDD, V0, bias and etc.).

8. RESET CIRCUIT

Setting RESB to “L” can initialize internal function. While RESB is “L”, no instruction can be accepted. RESB pin must connect to the reset pin of MPU and initialization by RESB pin is essential before operating.

When RESB becomes “L”, the following procedures will start.
Power Down Mode: PD=1 (Analog Power OFF, Oscillator OFF & COM/SEG output at VSS)
Page Address: Y[3:0]=0
Column Address: X[6:0]=0
COM Scan Direction: Depends on “TMY” setting
SEG Select Direction: Depends on “TMX” setting
Display Control: Display OFF: D=E=0
Basic Instruction Set: H=0
Initial V0 Setting: V0[4:0]=0
Bias: Depends on “BR” setting

After power-on, RAM data are undefined and the display status is “Display OFF”. It’s better to initialize whole DDRAM (ex: fill all 00h or write the display pattern) before turning the Display ON.

9-1. INSTRUCTION TABLE

H=0 or 1 (H-Flag Independent)											
INSTRUCTION	**A0**	**R/W (RWR)**	**COMMAND BYTE**								**DESCRIPTION**
			D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
NOP	0	0	0	0	0	0	0	0	0	0	No operation
Function Set	0	0	0	0	1	0	0	PD	V	H	Power down; entry mode; Select instruction table
Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data to RAM

H=0 (Basic Instruction)											
INSTRUCTION	**A0**	**R/W (RWR)**	**COMMAND BYTE**								**DESCRIPTION**
			D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Display Control	0	0	0	0	0	0	1	D	0	E	Sets display configuration
Set Y Address of RAM	0	0	0	1	0	0	Y3	Y2	Y1	Y0	Sets Y address of RAM 0≤Y≤9
Set X Address of RAM	0	0	1	X6	X5	X4	X3	X2	X1	X0	Sets X address of RAM 0≤X≤101

H=1 (Extended Instruction)											
INSTRUCTION	**A0**	**R/W (RWR)**	**COMMAND BYTE**								**DESCRIPTION**
			D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Set V0	0	0	1	V04	V03	V02	V01	V00	0	0	Set V_{OP} parameter to register
Set Test Mode	0	0	0	0	1	1	0	T1	T0	TEN	Select test mode

9-2. INSTRUCTION DESCRIPTION

H=0 or 1 (H-Flag Independent)

Function Set

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	PD	V	H

Flag	Description
PD	PD=0: chip is active PD=1: chip is in power down mode All LCD outputs at VSS (display off), bias generator and V0 generator off, VOUT can be disconnected, oscillator off (external clock possible), RAM contents not cleared; RAM data can be written.
V	Select addressing mode: V=0 for Horizontal Addressing; V=1 for Vertical Addressing.
H	H=0: Basic Instruction set; H=1: Extended instruction set. Data access can be used in both instruction blocks. Refer to the instruction table.

Read Data

By specify the column address and page address, the display data in DDRAM can be read by MPU (parallel interface).

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1	1	Read Data							

Write Data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1	0	Write Data							

H=0 (Basic Instruction)

Display Control

This bits D and E selects the display mode.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	D	0	E

Flag	Description
D,E	D E The bits D and E select the display mode. 0 0 Display OFF 0 1 All display segments on 1 0 Normal mode 1 1 Inverse video mode

Set Y Address of RAM

Y [3:0] defines the Y address vector address of the display RAM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	Y3	Y2	Y1	Y0

Y3	Y2	Y1	Y0	Content	Allowed X-Range	Valid Bit
0	0	0	0	Page0 (display RAM)	0 to 101	D7~ D0
0	0	0	1	Page1 (display RAM)	0 to 101	D7~ D0
0	0	1	0	Page2 (display RAM)	0 to 101	D7~ D0
0	0	1	1	Page3 (display RAM)	0 to 101	D7~ D0
0	1	0	0	Page4 (display RAM)	0 to 101	D7~ D0
0	1	0	1	Page5 (display RAM)	0 to 101	D7~ D0
0	1	1	0	Page6 (display RAM)	0 to 101	D7~ D0
0	1	1	1	Page7 (display RAM)	0 to 101	D7~ D0
1	0	0	0	Page8 (display RAM)	0 to 101	D7
1	0	0	1	Page9 (display RAM)	0 to 101	D7

Set X Address of RAM

The X address points to the columns. The range of X is 0…101.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	X6	X5	X4	X3	X2	X1	X0

X6	X5	X4	X3	X2	X1	X0	Column address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:
1	1	0	0	0	1	1	99
1	1	0	0	1	0	0	100
1	1	0	0	1	0	1	101

H=1 (Extended Instruction)

Set V0

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	V04	V03	V02	V01	V00	0	0

The operation voltage V0 can be set by software. The parameters are explained in table 4.

$$V0 = a + Vop[4:0] * b \quad (1)$$

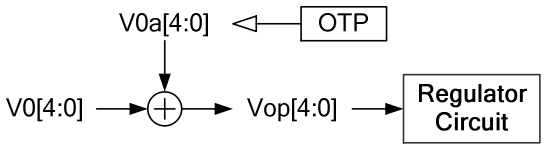
$$Vop[4:0] = V0[4:0] + V0a[4:0] \quad (2)$$

Note: The maximum V0 which can be generated depends on VDD2 and the loading of the display module.

Table 4 Parameters of V0 Generation Circuit

SYMBOL	VALUE	UNIT
a	8.232	V
b	0.049	V

V0a[4:0] provides an offset of V0[4:0] which is used to adjust V0 voltage to cover the process tolerance on LCD modules. It can be adjusted by OTP command “V0 Increase” or “V0 Decrease”.



*** Typically, it is recommended to set Vop[4:0] in 8.5V ~ 9.5V (including temperature effect). So that the application can have some range (<8.5V; >9.5V) for customer to adjust LCD contrast by themselves.**

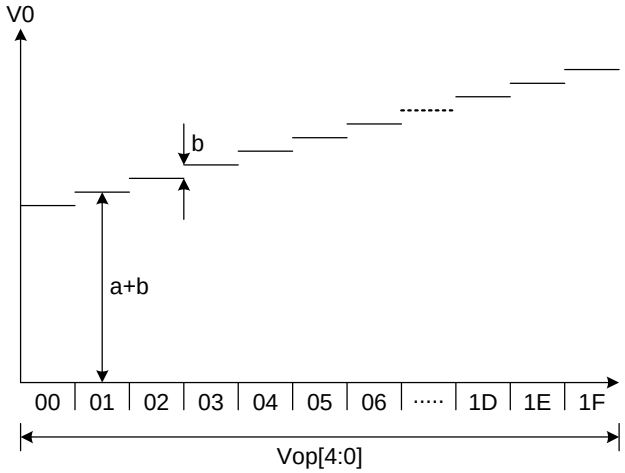


Fig 17. Setting V0 Voltage

The default V0 voltage is shown below (V0a[4:0] is not programmed into OTP by customer):

V04	V03	V02	V01	V00	V0a[4:0]	V0 (V)
0	0	0	0	0	0 (default) (without adjustment)	8.232
0	0	0	0	1		8.281
0	0	0	1	0		8.330
0	0	0	1	1		8.379
:	:	:	:	:		:
1	0	0	0	0		9.016
:	:	:	:	:		:
1	1	1	1	0		9.604
1	1	1	1	0		9.653
1	1	1	1	1		9.702
1	1	1	1	1		9.751

Please note that: V0a [4:0] is 2’s complement, so that V0a[4:0] can increase or decrease V0. If customer adjusts V0 by too many “V0 Increase” (or “V0 Decrease”) instructions, the purpose to increase V0 (or decrease V0) will become: “lower V0” (or “higher V0”).

Set Test Mode

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	T1	T0	TEN

Flag	Description
T[1:0]	Select test mode.
TEN	Enable test mode.

9-3. OTP INSTRUCTION TABLE

INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
H=1, T=0 or 1 (H-Flag Independent)											
Set Test Mode	0	0	0	0	1	1	0	T1	T0	TEN	Test Mode
T[1:0] = (0,0)											
OSC Enable	0	0	1	0	1	1	0	OSC	0	0	OSC enable/disable
T[1:0] = (0,1)											
V0 Increase	0	0	0	1	0	0	0	0	0	1	V0a[4:0] +1
V0 Decrease	0	0	0	1	0	0	0	0	1	0	V0a[4:0] -1
T[1:0] = (1,0)											
OTP Read Enable	0	0	0	1	0	0	XARD	0	0	0	Set OTP to be read mode
OTP Control In	0	0	0	1	1	1	0	0	0	1	Enable OTP Control
OTP Control Out	0	0	1	0	0	0	1	0	0	0	Disable OTP Control
OTP Write Enable	0	0	1	0	0	1	1	1	1	1	Enable OTP Write
OTP Write	0	0	1	0	1	0	0	0	0	1	OTP write
OTP V0 Address	0	0	1	1	0	0	0	0	1	0	OTP V0 address
T[1:0] = (1,1) Reserved Table Do Not Use											
Reserved			*	*	*	*	*	*	*	*	Do not use

9-4. OTP INSTRUCTION DESCRIPTION

Before using OTP instructions, the TEN flag in “Set Test Mode” must be enabled.

T[1:0]=(0,0)

OSC Enable

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	1	0	OSC	0	0

Flag	Description
OSC	OSC=1: Enable internal OSC. OSC=0: Disable internal OSC.

T[1:0]=(0,1)

V0 Increase

The V0 will be increased one step by every time executes this command. V0 OTP function include a 5 bits counter circuit V0a[4:0]. The range is (+1) to (+15) when set V0 Increase and the register of counter wil increase automatically.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0	0	0	1

V0 Decrease

The V0 will be decreased one step by every time executes this command. V0 OTP function include a 5 bits counter circuit V0a[4:0]. The range is (-1) to (-16) when set V0 Decrease and the register of counter will decrease automatically.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0	0	1	0

Software Overflow

It is recommended to add a software protection when customer burning OTP to adjust V0. The software protection should prevent the operator issuing too many “V0 Increase” or “V0 Decrease” instructions. The adjustment should be in the range of “+15~+1”, 0 and “-1~-16”. The adjustment over this range should not trigger any more adjustment.

T[1:0]=(1,0)

OTP Read Enable

This command sets OTP Auto-Read enable or disable. It should be set before issuing OTP Write.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	XARD	0	0	0

Flag	Description
XARD	0: Enable OTP Auto-Read. 1: Disable OTP Auto-Read.

OTP Control In

This command should be set before “OTP Write”.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	1	0	0	0	1

OTP Control Out

This command should be set after finishing OTP operation.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	1	0	0	0

OTP Write Enable

This command will enable OTP write operation. Set this command before OTP Write.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	1	1	1	1	1

OTP Write

This command will burn the data into OTP.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	0	1

OTP V0 Address

This command points OTP function to V0 address.

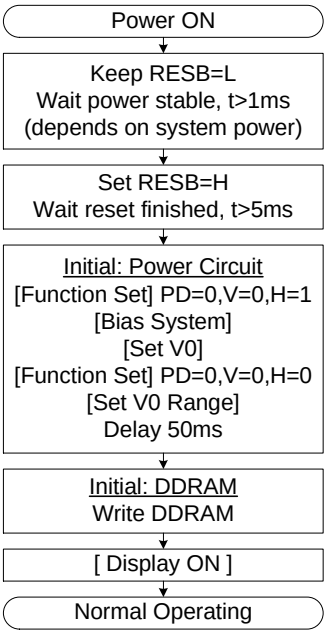
A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	0	0	1	0

10. COMMAND SEQUENCE

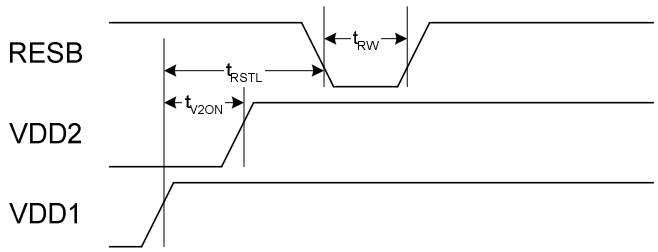
This section introduces some reference operation flows.

Power ON flow and instruction sequence:

Operating Flow



Power Sequence



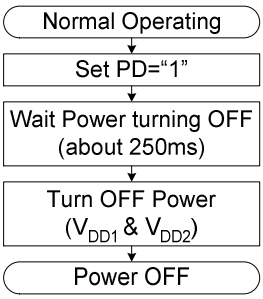
1. t_{V2ON}: VDD2 power ON delay.
   => $0 \le t_{V2ON} \le$ No Limitation.
2. t_{RSTL}: Reset Low time after VDD1 is stable.
   => $0 \le t_{RSTL} \le 50$ ms[*1].
3. t_{RW}: Reset low pulse width.
   Please refer to RESB timing specification.

Note:

1. IC will NOT be damaged if either VDD1 or VDD2 is OFF while another is ON. The specification listed here is to prevent abnormal display on LCD module.
2. Be sure the power is stable and the internal reset is finished (refer to RESB timing specification).

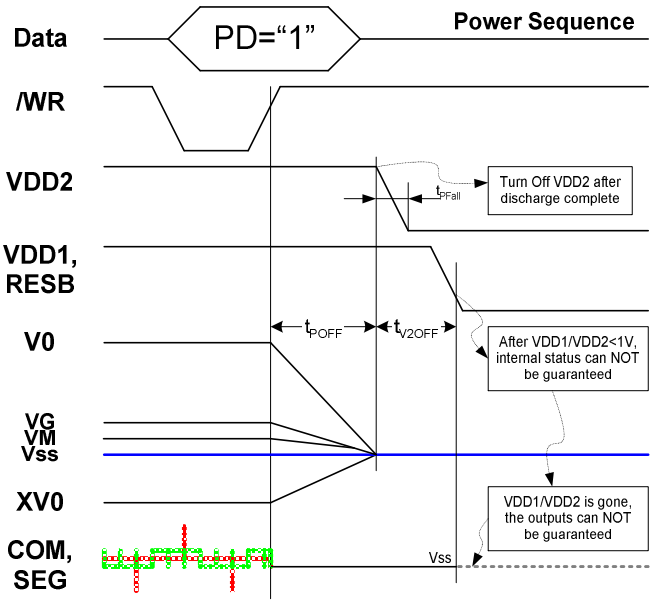
Power OFF Flow and Sequence

By setting PD="1", ST7585 will go into power save mode. The LCD driving outputs are fixed to VSS, built-in power circuits are turned OFF and a discharge process starts.

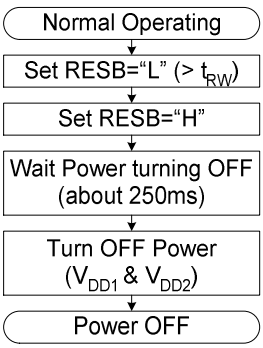


Instruction Flow

After the built-in power circuits are turned OFF and completely discharged, the power (VDD1 and VDD2) can be removed.

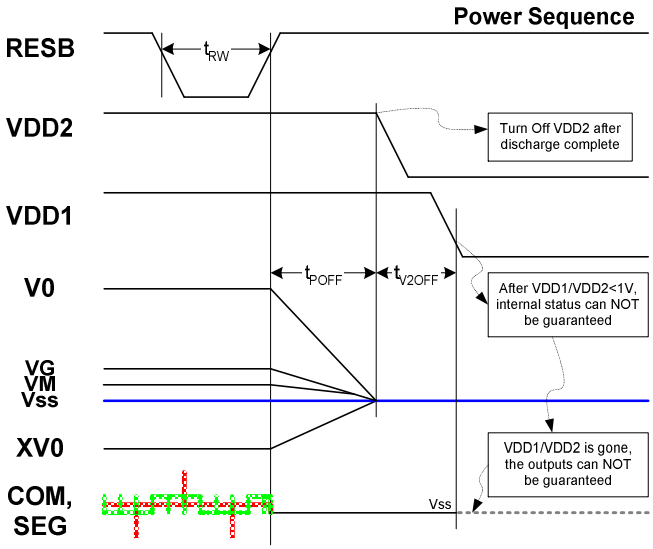


An alternate method is to use the RESB signal to set ST7585 into power save mode. After hardware reset, the PD flag is "1" and ST7585 is in power save mode (same as previous case).



Operating Flow

After the built-in power circuits are turned OFF and completely discharged, the power (VDD1 and VDD2) can be removed.



Note:

1. t_{IPOFF}: Internal Power discharge time. => 250ms (max).
2. t_{V2OFF}: Period between VDD1 and VDD2 OFF time. => 0 ms (min).
3. It is NOT recommended to turn VDD1 OFF before VDD2. Without VDD1, the internal status cannot be guaranteed and internal discharge-process maybe stopped. The un-discharged power maybe flows into COM/SEG output(s) and the liquid crystal in panel maybe polarized.
4. IC will NOT be damaged if either VDD1 or VDD2 is OFF while another is ON.
5. The timing is dependent on panel loading and the external capacitor(s).
6. The timing in these figures is base on the condition that: LCD Panel Size = 1.4" with C1=1uF, C2=1uF.

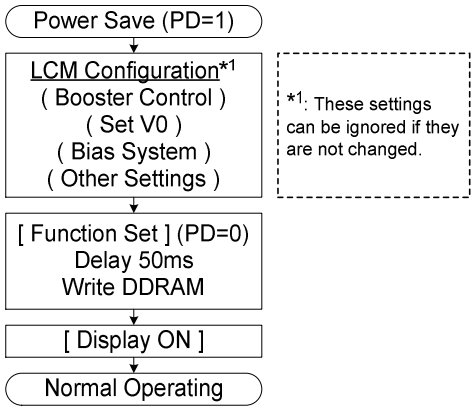
7. When turning VDD2 OFF, the falling time should follow the specification:
   300ms ≤ t_{PFall} ≤ 1sec
8. If the power OFF flow cannot meet this specification, it is recommended to use the discharge resistors (R1 & R2 in application circuits).

Power-Save Flow and Sequence

ENTERING THE POWER SAVE MODE

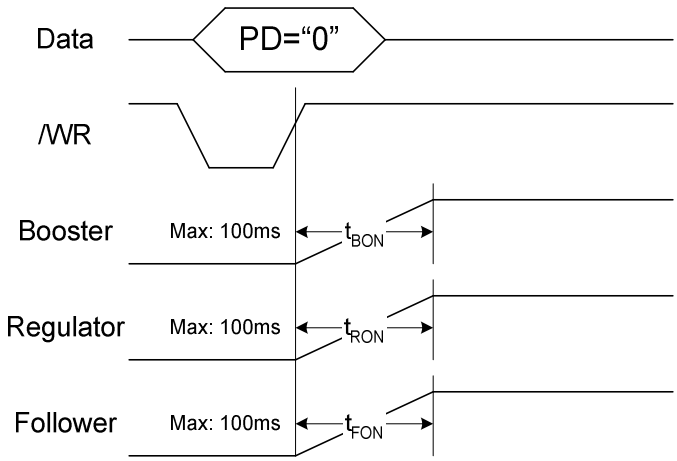
The power save mode is achieved by setting PD bit to be “1”. No specified instruction flow required.

EXITING THE POWER SAVE MODE



INTERNAL SEQUENCE of EXIT POWER SAVE MODE

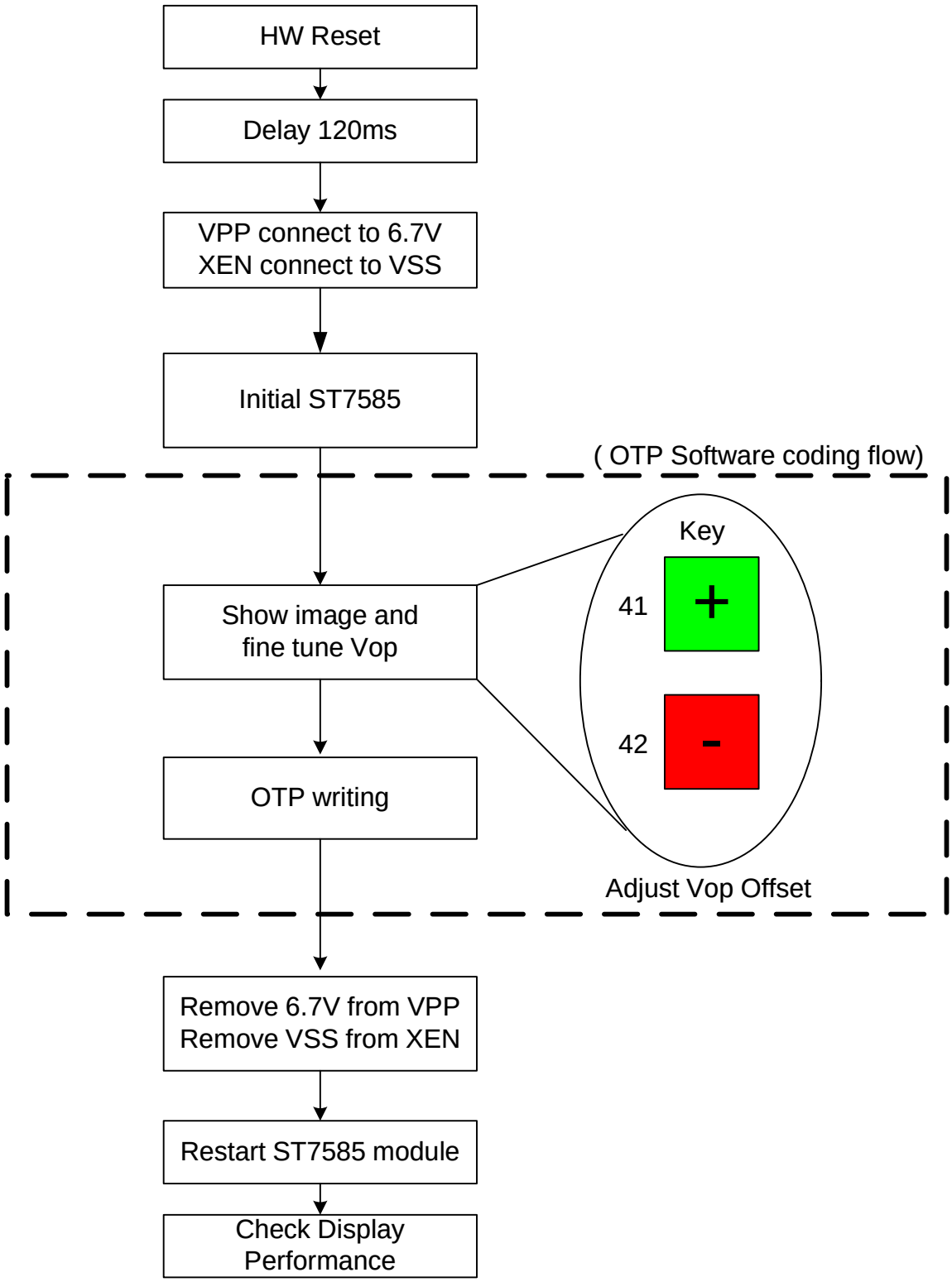
After receiving “PD=0”, the internal circuits (Power) will starts the following procedure.



Note:

1. The power stable time is determined by LCD panel loading.
2. The power stable time in this figure is base on: LCD Panel Size = 1.4” with C1=1uF, C2=1uF.

OTP Burning Flow



Note:

1. OTP can be written only 1 time and the written value can “NOT” be read out by MPU interface.
2. After writing OTP, a hardware reset (set RESB=“L”) will let ST7585 exit the “Test Mode”.

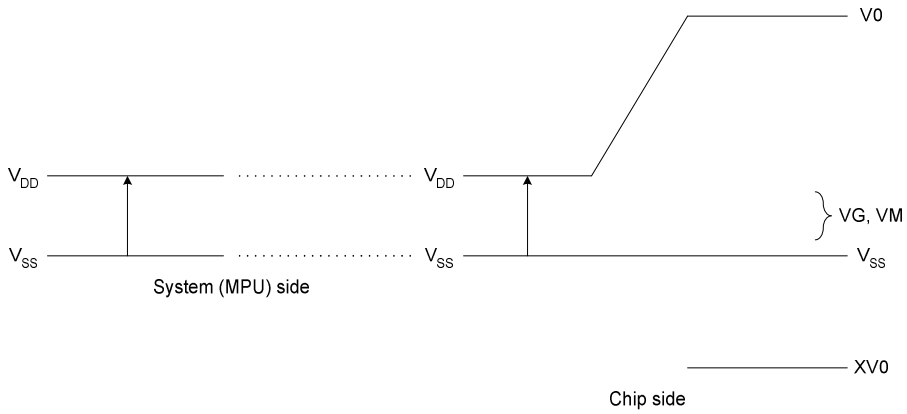
Referential OTP Related Codes

```
void Fine_Tune_VOP(void)
{
        Show_Image();                          // Display an image
        Write(COMMAND,0x20 );                  // Function Set PD=0,V=0, H=0
        Write(COMMAND,0x0C);                   //Normal Display On

        Write(COMMAND,0x21);                   // Function Set PD=0,V=0, H=1
        Write(COMMAND,0x35);                   //OTP Function Set T:10
        Write(COMMAND,0x48);                   //OTP auto read disable
        Write(COMMAND,0x31);                   // OTP Function Set T:00
        Write(COMMAND,0xB4);                   // OSC enable
        Write(COMMAND,0x33);                   // OTP Function Set T:01
        Write(COMMAND,0x41);                   // VOP offset increase 1 step
        Or
        Write(COMMAND,0x42);                   // VOP offset decrease 1 step
        Write(COMMAND,0x30);                   // Leave OTP Function mode
}
void OTP_Writing(void)
{
        Write(COMMAND,0x20 );                  // Function Set PD=0,V=0, H=0
        Write(COMMAND,0x08);                   // Display Off

        Write(COMMAND,0x21);                   // Function Set PD=1,V=0, H=1
        Write(COMMAND,0x35);                   // OTP Function Set T:10
        Write(COMMAND,0x71);                   // OTP control in

        Write(COMMAND,0xC2);                   // set OTP address VOP offset
        Write(COMMAND,0x9F);                   // OTP enable
        Delay (1500);                          // delay 1.5ms
        Write(COMMAND,0xA1);                   // OTP write
        Delay (750);                           //delay 750us
        Write(COMMAND,0x88);                   //OTP control out

        Write(COMMAND,0x30);                   // Leave OTP Function mode
}
```

11. LIMITING VALUES

In accordance with the Absolute Maximum Rating System; please refer to notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Digital Power Supply Voltage	VDD1	-0.3 ~ 3.6	V
Analog Power supply voltage	VDD2	-0.3 ~ 3.6	V
LCD Power supply voltage	V0-XV0	-0.3~15	V
LCD Power driving voltage	VG, VM	-0.3 ~ VDD2	V
Operating temperature	TOPR	–30 to +85	°C
Storage temperature	TSTR	–65 to +150	°C



Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.
3. Insure the voltage levels of V0, VDD2, VG, VM, VSS and XV0 always match the correct relation:
   V0 ≥ VDD2 > VG > VM > VSS ≥ XV0

12. HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

13. DC CHARACTERISTICS

VDD1=1.8V to 3.3V, VSS=0V; Tamb = -30°C to +85°C; unless otherwise specified.

Item	Symbol	Condition	Rating			Unit	Applicable Pin
			Min.	Typ.	Max.		
Operating Voltage (1)	VDD1		1.7	—	3.4	V	VDD1
Operating Voltage (2)	VDD2		2.6	—	3.4	V	VDD2
Input High-level Voltage	V_{IHC}		0.7 x VDD1	—	VDD1	V	MPU Interface
Input Low-level Voltage	V_{ILC}		VSS	—	0.3 x VDD1	V	MPU Interface
Output High-level Voltage	V_{OHC}	I_{OUT}=1mA, VDD1=1.8V	0.8 x VDD1	—	VDD1	V	D[7:0]
Output Low-level Voltage	V_{OLC}	I_{OUT}=-1mA, VDD1=1.8V	VSS	—	0.2 x VDD1	V	D[7:0]
Input Leakage Current	I_{LI}		-1.0	—	1.0	μA	MPU Interface
Output Leakage Current	I_{LO}		-3.0	—	3.0	μA	MPU Interface
Liquid Crystal Driver ON Resistance	R_{ON}	Ta=25°C, Vop=9V, △V=0.9V	—	0.5	—	KΩ	COMx
		Ta=25°C, VG=2V, △V=0.2V	—	1.0	—	KΩ	SEGx
Frame Frequency	FR	1/66 Duty, Ta = 25°C	68	72	77	Hz	

Note:

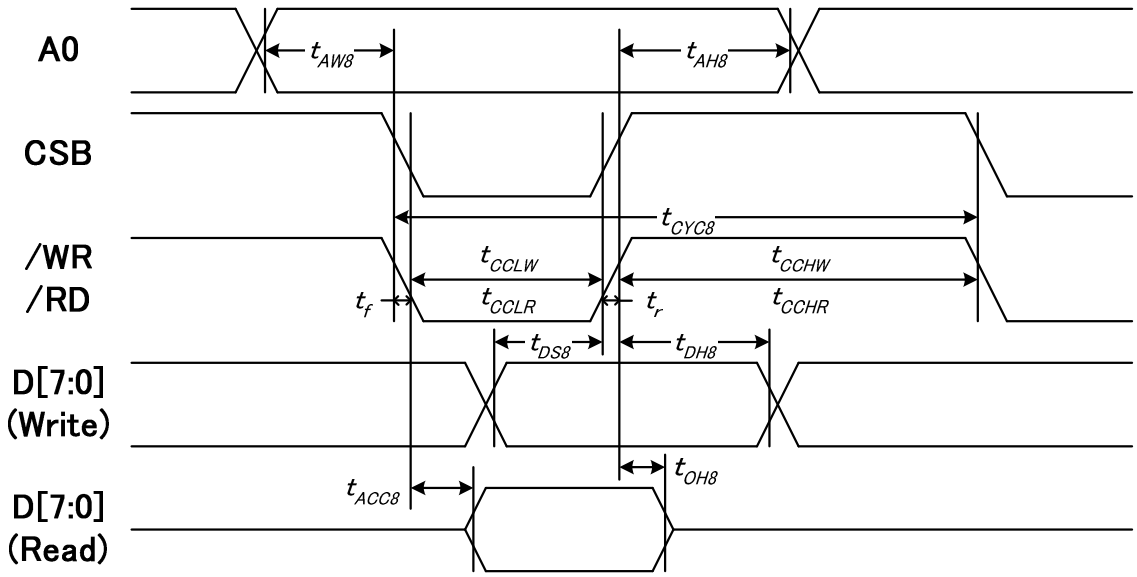
1. Please refer to the “Selection of Application Voltage” section for the recommend application Vop voltage level.

Current consumption: During Display, with internal power system, current consumed by whole IC (bare die).

Test Pattern	Symbol	Condition	Rating			Unit	Note
			Min.	Typ.	Max.		
Display Pattern: SNOW (Static)	ISS	VDD1=VDD2=3V, Booster X5 V0 = 9.0 V, Bias=1/9 Ta=25°C	—	150	220	μA	
Power Down	ISS	VDD1=VDD2=3V, Ta=25°C	—	3	15	μA	

14. TIMING CHARACTERISTICS

System Bus Read/Write Characteristics (For the 8080 Series MPU)



(VDD1 = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		80	—	ns
Address hold time		tAH8		10	—	
System cycle time	/WR	tCYC8		350	—	
Write L pulse width		tCCLW		70	—	
Write H pulse width		tCCHW		50	—	
Read L pulse width	/RD	tCCLR		120	—	
Read H pulse width		tCCHR		50		
Data setup time (Write)	D[7:0]	tDS8		60	—	
Write Data hold time (Write)		tDH8		10	—	
Data access time (Read)		tACC8	CL = 16 pF	—	70	
Output disable time (Read)		tOH8	CL = 16 pF	10	50	

(VDD1 = 2.8V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		120	—	ns
Address hold time		tAH8		15	—	
System cycle time	/WR	tCYC8		450	—	
Write L pulse width		tCCLW		120	—	
Write H pulse width		tCCHW		100	—	
Read L pulse width	/RD	tCCLR		120	—	
Read H pulse width		tCCHR		100	—	
Data setup time (Write)	D[7:0]	tDS8		90	—	
Write Data hold time (Write)		tDH8		15	—	
Data access time (Read)		tACC8	CL = 16 pF	—	140	
Output disable time (Read)		tOH8	CL = 16 pF	10	100	

(VDD1 = 1.8V , Ta =25°C)

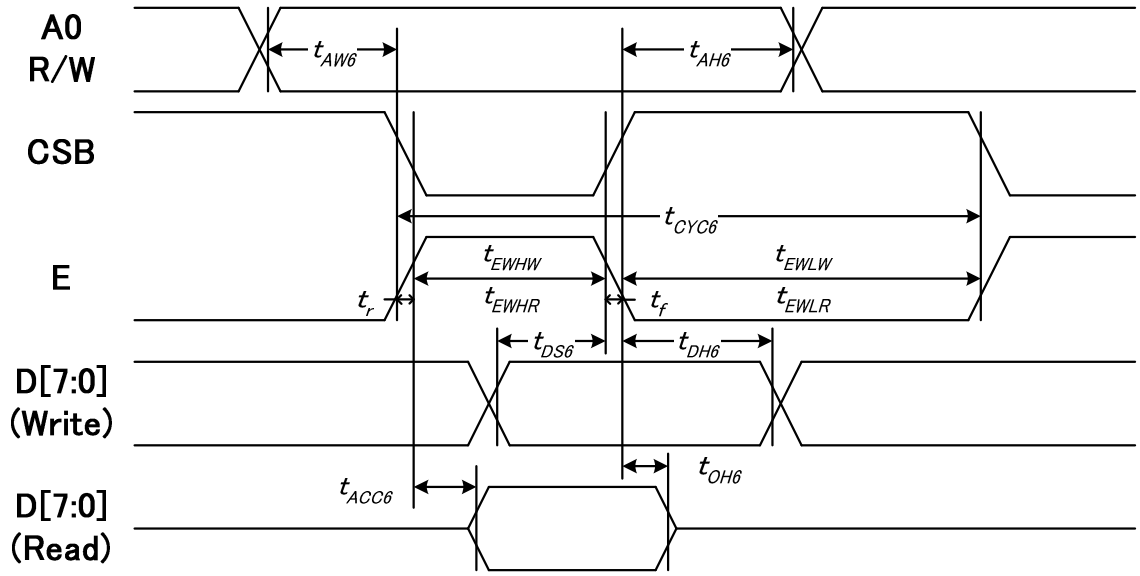
Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		150	—	ns
Address hold time		tAH8		30	—	
System cycle time	/WR	tCYC8		550	—	
Write L pulse width		tCCLW		170	—	
Write H pulse width		tCCHW		150	—	
Read L pulse width	/RD	tCCLR		170	—	
Read H pulse width		tCCHR		150		
Data setup time (Write)	D[7:0]	tDS8		120	—	
Write Data hold time (Write)		tDH8		30	—	
Data access time (Read)		tACC8	CL = 16 pF	—	240	
Output disable time (Read)		tOH8	CL = 16 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≦ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≦ (tCYC8 – tCCLR – tCCHR) are specified.

*2 All timing is specified using 20% and 80% of VDD1 as the reference.

*3 tCCLW and tCCLR are specified as the overlap between CSB being “L” and WR and RD being at the “L” level.

System Bus Read/Write Characteristics (For the 6800 Series MPU)



(VDD1 = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		80	—	ns
Address hold time		tAH6		10	—	
System cycle time	E	tCYC6		240	—	
Enable L pulse width (WRITE)		tEWLW		70	—	
Enable H pulse width (WRITE)		tEWHW		50	—	
Enable L pulse width (READ)		tEWLR		70	—	
Enable H pulse width (READ)		tEWHR		130		
Write data setup time	D[7:0]	tDS6		60	—	
Write data hold time		tDH6		10	—	
Read data access time		tACC6	CL = 16 pF	—	70	
Read data output disable time		tOH6	CL = 16 pF	10	50	

(VDD1 = 2.8V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		100	—	ns
Address hold time		tAH6		15	—	
System cycle time	E	tCYC6		340	—	
Enable L pulse width (WRITE)		tEWLW		120	—	
Enable H pulse width (WRITE)		tEWHW		100	—	
Enable L pulse width (READ)		tEWLR		120	—	
Enable H pulse width (READ)		tEWHR		100	—	
Write data setup time	D[7:0]	tDS6		120	—	
Write data hold time		tDH6		15	—	
Read data access time		tACC6	CL = 16 pF	—	140	
Read data output disable time		tOH6	CL = 16 pF	10	100	

(VDD1 = 1.8V , Ta =25°C)

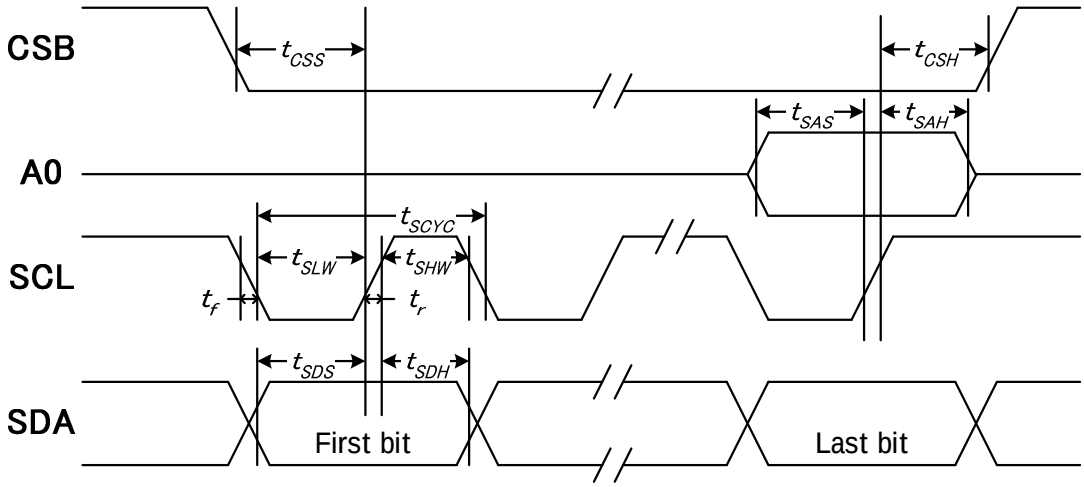
Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		150	—	ns
Address hold time		tAH6		30	—	
System cycle time	E	tCYC6		440	—	
Enable L pulse width (WRITE)		tEWLW		170	—	
Enable H pulse width (WRITE)		tEWHW		150	—	
Enable L pulse width (READ)		tEWLR		170	—	
Enable H pulse width (READ)		tEWHR		150	—	
Write data setup time	D[7:0]	tDS6		180	—	
Write data hold time		tDH6		30	—	
Read data access time		tACC6	CL = 16 pF	—	240	
Read data output disable time		tOH6	CL = 16 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≦ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≦ (tCYC6 – tEWLR – tEWHR) are specified.

*2 All timing is specified using 20% and 80% of VDD1 as the reference.

*3 tEWLW and tEWLR are specified as the overlap between CSB being “L” and E.

SERIAL INTERFACE (4-Line Interface)



(VDD1 = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		120	—	ns
SCLK “H” pulse width		tSHW		60	—	
SCLK “L” pulse width		tSLW		60	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		90	—	
Data setup time	SDA	tSDS		20	—	
Data hold time		tSDH		10	—	
CSB-SCLK time	CSB	tCSS		20	—	
CSB-SCLK time		tCSH		120	—	

(VDD1 = 2.8V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		200	—	ns
SCLK “H” pulse width		tSHW		100	—	
SCLK “L” pulse width		tSLW		100	—	
Address setup time	A0	tSAS		30	—	
Address hold time		tSAH		120	—	
Data setup time	SDA	tSDS		30	—	
Data hold time		tSDH		20	—	
CSB-SCLK time	CSB	tCSS		30	—	
CSB-SCLK time		tCSH		150	—	

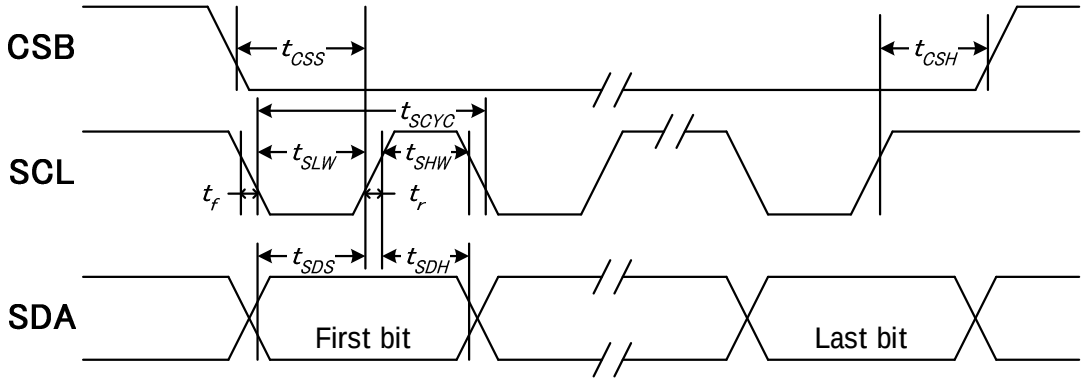
(VDD1 = 1.8V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		280	—	ns
SCLK “H” pulse width		tSHW		140	—	
SCLK “L” pulse width		tSLW		140	—	
Address setup time	A0	tSAS		50	—	
Address hold time		tSAH		150	—	
Data setup time	SDA	tSDS		50	—	
Data hold time		tSDH		50	—	
CSB-SCLK time	CSB	tCSS		40	—	
CSB-SCLK time		tCSH		180	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD1 as the standard.

SERIAL INTERFACE (3-Line Interface)



(VDD1 = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		120	—	ns
SCLK “H” pulse width		tSHW		60	—	
SCLK “L” pulse width		tSLW		60	—	
Data setup time	SDA	tSDS		20	—	
Data hold time		tSDH		10	—	
CSB-SCLK time	CSB	tCSS		20	—	
CSB-SCLK time		tCSH		130	—	

(VDD1 = 2.8V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		180	—	ns
SCLK “H” pulse width		tSHW		90	—	
SCLK “L” pulse width		tSLW		90	—	
Data setup time	SDA	tSDS		30	—	
Data hold time		tSDH		20	—	
CSB-SCLK time	CSB	tCSS		30	—	
CSB-SCLK time		tCSH		160	—	

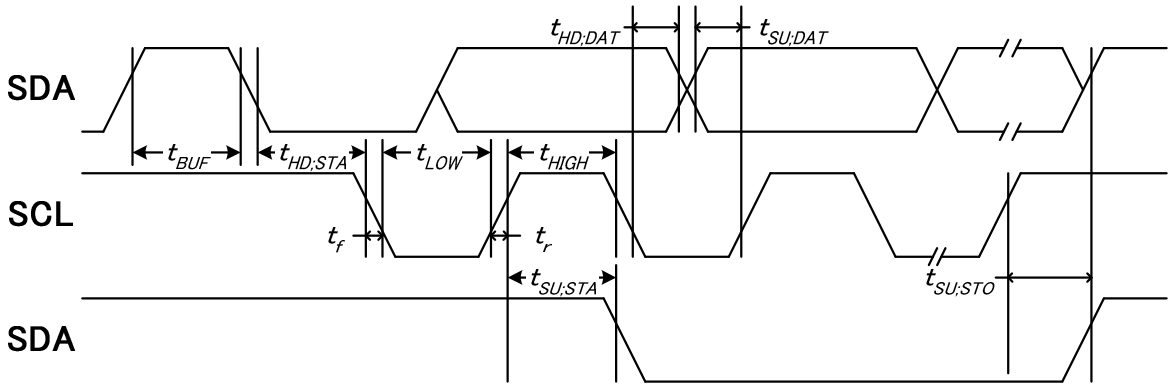
(VDD1 = 1.8V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		240	—	ns
SCLK “H” pulse width		tSHW		120	—	
SCLK “L” pulse width		tSLW		120	—	
Data setup time	SDA	tSDS		60	—	
Data hold time		tSDH		50	—	
CSB-SCLK time	CSB	tCSS		40	—	
CSB-SCLK time		tCSH		190	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD1 as the standard.

SERIAL INTERFACE (I²C Interface)



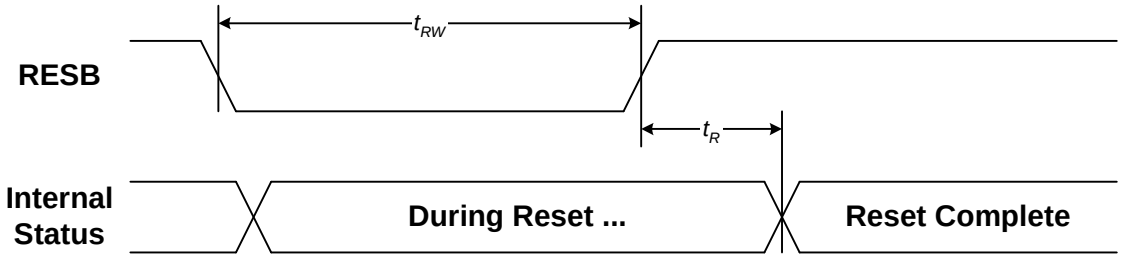
(VDD1 = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
SCL clock frequency	SCL	fSCLK		-	400	KHz
SCL clock low period		tLOW		1.3	-	us
SCL clock high period		tHIGH		0.6	-	us
Data set-up time	SDA	tSU;Data		100	-	ns
Data hold time		tHD;Data		0	0.9	us
Setup time for a repeated START condition	SDA	tSU;SUA		0.6	-	us
Start condition hold time		tHD;STA		0.6	-	us
Setup time for STOP condition		tSU;STO		0.6	-	us
SCL,SDA rise time	SCL SDA	tR		20+0.1Cb	300	ns
SCL,SDA fall time		tF		20+0.1Cb	300	ns
Capacitive load represented by each bus line		Cb		-	400	pF
Tolerable spike width on bus		tSW		-	50	ns
Bus free time between a STOP and START condition	SCL	tBUF		1.3		us

Note:

1. I²C timing will be affected by the external pull-up resistor and the ITO resistance of COG.

RESET TIMING



(VDD1 = 3.3V , Ta =25°C)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	1.5	us
Reset “L” pulse width	tRW		1.5	—	

(VDD1 = 2.8V , Ta =25°C)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	2.0	us
Reset “L” pulse width	tRW		2.0		

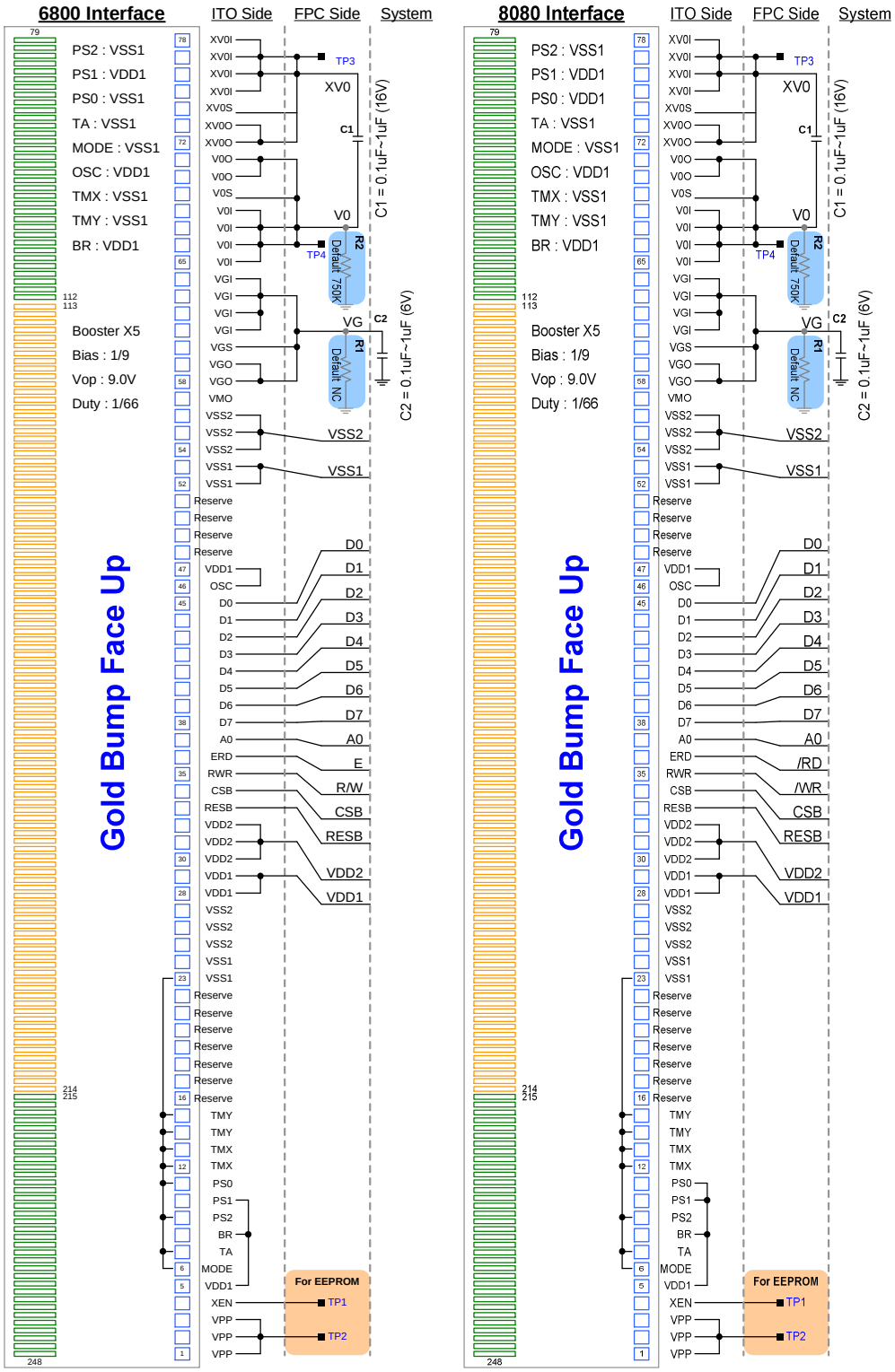
(VDD1 = 1.8V , Ta =25°C)

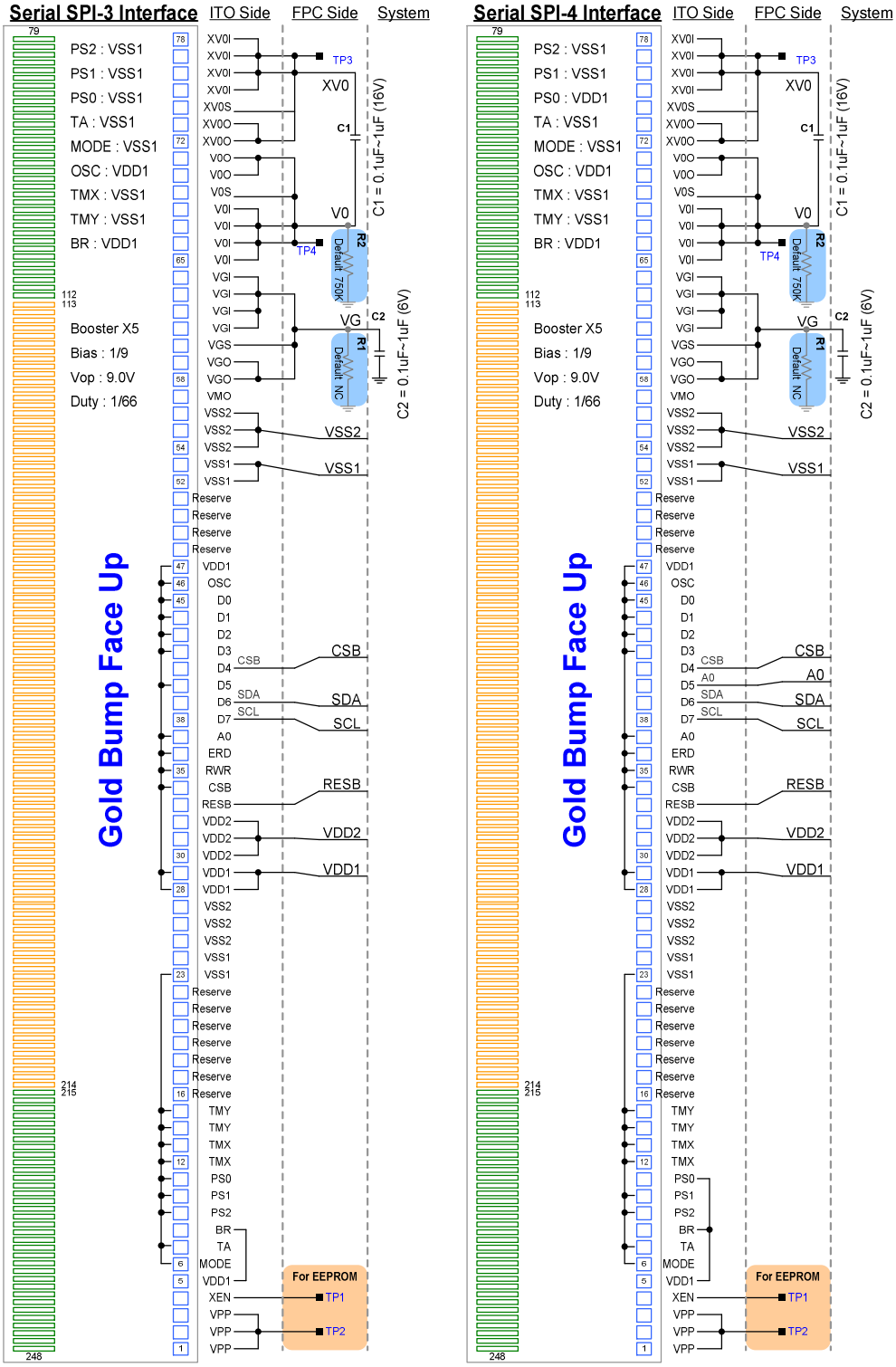
Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	3.0	us
Reset “L” pulse width	tRW		3.0	—	

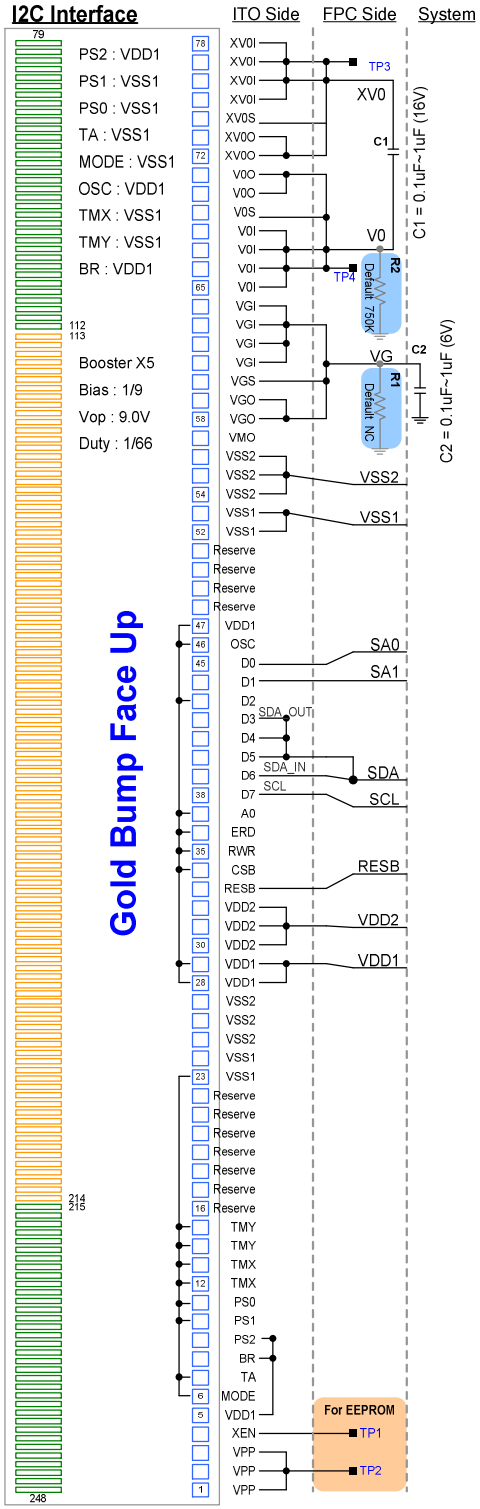
APPLICATION NOTE

Application Circuits

The application circuits are for reference only and actual settings are dependent on LCD module characteristics.




Serial SPI-3 Interface
ITO Side
FPC Side
System
PS2 : VSS1
PS1 : VSS1
PS0 : VSS1
TA : VSS1
MODE : VSS1
OSC : VDD1
TMX : VSS1
TMY : VSS1
BR : VDD1
Booster X5
Bias : 1/9
Vop : 9.0V
Duty : 1/66
Gold Bump Face Up
TP3
TP4
XV0
V0
VG
C1
C2
R1
R2
Default 750K
Default NC
C1 = 0.1uF~1uF (16V)
C2 = 0.1uF~1uF (6V)
VSS2
VSS1
CSB
SDA
SCL
RESB
VDD2
VDD1
For EEPROM
TP1
TP2
Serial SPI-4 Interface
ITO Side
FPC Side
System
PS2 : VSS1
PS1 : VSS1
PS0 : VDD1
TA : VSS1
MODE : VSS1
OSC : VDD1
TMX : VSS1
TMY : VSS1
BR : VDD1
Booster X5
Bias : 1/9
Vop : 9.0V
Duty : 1/66
Gold Bump Face Up
TP3
TP4
XV0
V0
VG
C1
C2
R1
R2
Default 750K
Default NC
C1 = 0.1uF~1uF (16V)
C2 = 0.1uF~1uF (6V)
VSS2
VSS1
CSB
A0
SDA
SCL
RESB
VDD2
VDD1
For EEPROM
TP1
TP2


I2C Interface
ITO Side
FPC Side
System
PS2 : VDD1
PS1 : VSS1
PS0 : VSS1
TA : VSS1
MODE : VSS1
OSC : VDD1
TMX : VSS1
TMY : VSS1
BR : VDD1
Booster X5
Bias : 1/9
Vop : 9.0V
Duty : 1/66
Gold Bump Face Up
TP3
XV0
C1
C1 = 0.1uF~1uF (16V)
V0
TP4
R2
Default 750K
VG
C2
R1
Default NC
C2 = 0.1uF~1uF (6V)
VSS2
VSS1
SA0
SA1
SDA_OUT
SDA_IN
SDA
SCL
RESB
VDD2
VDD1
For EEPROM
TP1
TP2

Selection of Application Voltage

Referential LCD Module Setting

VDD1=2.8V, VDD2 =2.8V, Panel Size=1.4”, Ta=25°C

Duty	Booster	Vop	Bias *1	Adjustment *2	Temperature Effect (-30°C) *3	Max. Vop *4
1/66	X5	8.8V	1/9	+/- 0.3V	+ 0.24V	9.34V
		8.6V	1/7	+/- 0.2V	+ 0.23V	8.93V

1. The Bias can be used to select suitable Liquid Crystal.
2. It is usually reserved some range for user adjustment (the reserved range depends on customer’s system).
   Be sure that: there is a suitable V0 level can be programmed into the V0 control register (V0[4:0]).
3. The internal Regulator has Temperature Gradient (-0.05%/°C).
4. Be sure that: the “Max. Vop” is still available by internal Booster (watch out the Booster Efficiency).
   Besides, the VG limitation should be followed.

- The display performance should be checked with customer’s LCD modules.

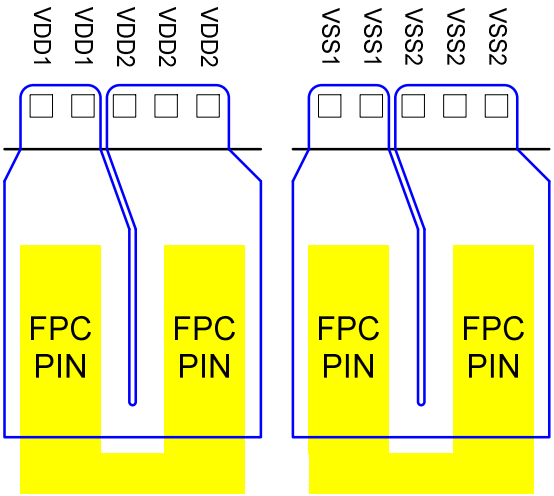
Note:

- Positive Booster: ***(VDD2 x 5 x BE) ≥ V0*** or ***(VDD2 x5 x BE) ≥ Vop***;
- Negative Booster: ***[–VDD2 x4 x BE] ≤ XV0*** or ***[VDD2 x4 x BE] ≥ (Vop - VG)***,
  where VG = Vop x 2 / N;
- Vop requirement: ***[VDD2 x4 x BE] ≥ [Vop x (N - 2) / N]*** or ***[Vop ≤ VDD2 x4 x BE x N / (N - 2)]***.
- BE is the booster efficiency. Referential values are listed below:
  (assume VDD2 =2.8V)
  Module Size ≤ 1.4”: BE=80% (Typical);
  Module Size = 1.5”~1.8”: BE=76% (Typical).
  Actual BE should be determined by module loading and ITO resistance value.
- 1.6V ≤ VG < VDD2. Recommend VG is: VDD2-VG around 0.5~0.8V.
- VM=VG/2 and 0.8V ≤ VM < VDD2.
- The worse condition should be considered:
  Low temperature effect and display on with snow pattern on panel (max: 1.8”).

ITO Layout Reference

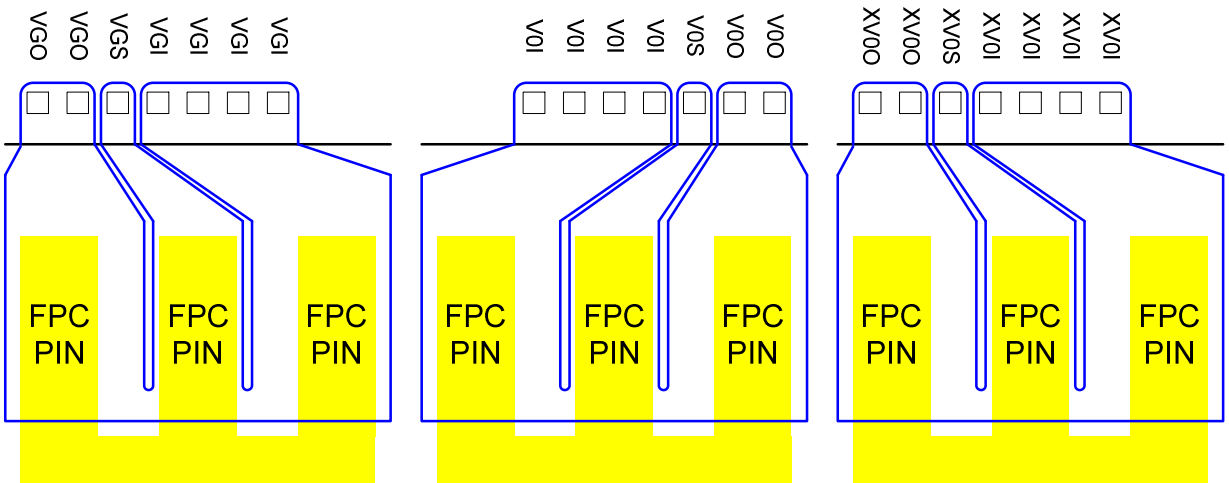
[VDD and VSS Layout]

1. The VDD and VSS of the internal digital and analog system should be separated on ITO and then short by FPC. This can isolate the operating noise.
2. Try to keep the ITO resistance as small as possible. The recommend resistance priority is:
   $R_{VSS2} \leq R_{VDD2} \leq R_{VDD1} \leq R_{VSS1}$



[LCD Power Layout]

1. In order to increase voltage accuracy, a layout topology shown below is required.
2. Try to keep the ITO resistance as small as possible. The recommend resistance priority is: (take VG as example)
   $R_{VGI} \leq R_{VGO} \leq R_{VGS}$



REVERSION HISTORY

Version	Date	Description
0.0	2007/10/17	Preliminary
0.1	2008/01/17	1. Add PAD information 2. Modify description
0.2	2008/01/22	Add application circuits: 6800, 8080, SPI-3 & SPI-4
0.3	2008/03/19	1. Update Chip Size. 2. Add OTP operation information. 3. Add 3 VSS2 pads for new version.
0.4	2008/08/04	1. Modify OTP command table 2. Add I^2C timing spec 3. modify power on flow reset wait time 4. modify DC characteristics
1.0	2008/12/10	1. Add I^2C application circuit. 2. Modify P18 typo. 3. Timing TBD remove 4. RON value modify 5. Add selection of V_{OP}
1.0b	2008/12/31	1. Update VDD2 Operation Range: Typical=2.7V~3.3V, Minimum=2.6V. 2. Add precautions to: OTP Burning Flow, I^2C interface timing. 3. Modify Vop range in “Selection of Application Voltage”.
1.0c	2009/04/14	1. Reserve Pin 48. 2. Fix Fig 11 and redraw Fig 10.