Sitronix

ST7636

65K Color Dot Matrix LCD Controller/Driver

1. INTRODUCTION

The ST7636 is a driver & controller LSI for 65K color graphic dot-matrix liquid crystal display systems. It generates 396 Segment and 132 Common driver circuits. This chip is connected directly to a microprocessor, accepts Serial Peripheral Interface (SPI) or 8-bit/16-bit parallel display data and stores in an on-chip display data RAM. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

Driver Output Circuits

- 396 segment outputs / 132 common outputs

Applicable Duty Ratios

- Various partial display
- Partial window moving & data scrolling

Gray-Scale Display

- 4FRC & 31 PWM function circuit to display
- 64 gray-scale display.

On-chip Display Data RAM

- Capacity: 132 · 132 · 16 =278,784bits
- 65K colors (RGB)=(565) mode
- Dithered 262K colors (RGB)=(666) mode
- Dithered 16M colors (RGB)=(888) mode

Microprocessor Interface

- 8/16-bit parallel bi-directional interface with 6800-series or 8080-series
- 4-line serial interface (4-line-SIF)
- 3-line serial interface (3-line-SIF)

On-chip Low Power Analog Circuit

- On-chip oscillator circuit
- Voltage converter (x2, x3, x4, x5, x6, x7, x8)
- Voltage regulator
- On-chip electronic contrast control function (406 steps)
- Voltage follower (LCD bias: 1/5 to 1/12)

Operating Voltage Range

- Supply voltage (VDD, VDD1): 2.4 to 3.3V
  (VDD2, VDD3, VDD4, VDD5): 2.4 to 3.3V
- LCD driving voltage (VOP = V0 - VSS): 3.76 to 18.0 V
- the suggested value of V0 is 12~15 V under bias =1/11.

LCD Driving Voltage (EEPROM)

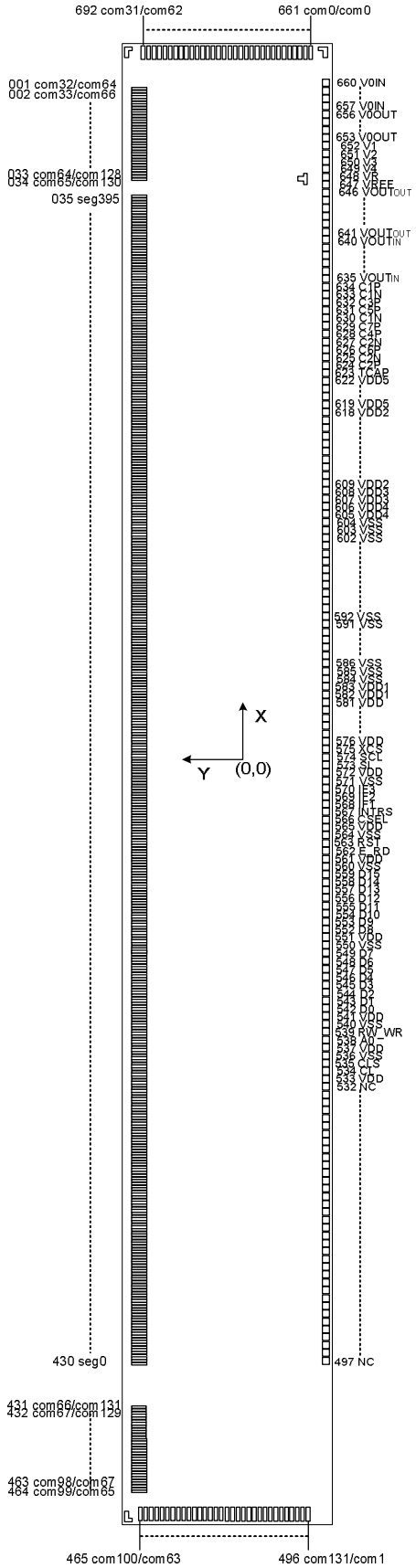
- To store contrast adjustment value for better display

Package Type

- Application for COG

ST7636	6800 , 8080 ,4-Line , 3-Line interface	ST

3. ST7636 Pad Arrangement (COG)



Chip Size: 20,050 um x1,650 um

Bump Pitch:

PAD NO 1 ~ 496, 661~692: 40 um (COM/SEG)

PAD NO 497 ~ 660: 110 um (O)

Bump size:

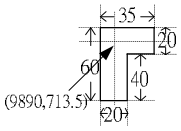
PAD NO.1~464: 25(x)um X 96(y)um

PAD No.465~ 496,661~692: 96(x)um X 25(y)um

PAD N0. 497~660: 90(x)um X 40(y)um

Bump Height: 17um

Chip Thickness: 635um



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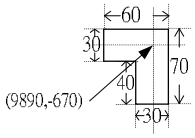

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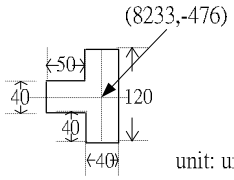

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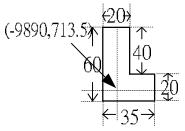
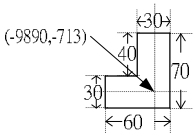
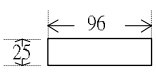


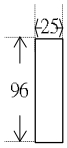
unit: um



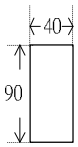
unit: um



Bump size of
PAD 1~464
unit: um



Bump size of
PAD 465~496
PAD 661~692
unit: um



Bump size of
PAD 497 ~ 660
unit: um

4. Pad Center Coordinates

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
001	COM[32]	COM[64]	9602.0	670.5
002	COM[33]	COM[66]	9562.0	670.5
003	COM[34]	COM[68]	9522.0	670.5
004	COM[35]	COM[70]	9482.0	670.5
005	COM[36]	COM[72]	9442.0	670.5
006	COM[37]	COM[74]	9402.0	670.5
007	COM[38]	COM[76]	9362.0	670.5
008	COM[39]	COM[78]	9322.0	670.5
009	COM[40]	COM[80]	9282.0	670.5
010	COM[41]	COM[82]	9242.0	670.5
011	COM[42]	COM[84]	9202.0	670.5
012	COM[43]	COM[86]	9162.0	670.5
013	COM[44]	COM[88]	9122.0	670.5
014	COM[45]	COM[90]	9082.0	670.5
015	COM[46]	COM[92]	9042.0	670.5
016	COM[47]	COM[94]	9002.0	670.5
017	COM[48]	COM[96]	8962.0	670.5
018	COM[49]	COM[98]	8922.0	670.5
019	COM[50]	COM[100]	8882.0	670.5
020	COM[51]	COM[102]	8842.0	670.5
021	COM[52]	COM[104]	8802.0	670.5
022	COM[53]	COM[106]	8762.0	670.5
023	COM[54]	COM[108]	8722.0	670.5
024	COM[55]	COM[110]	8682.0	670.5
025	COM[56]	COM[112]	8642.0	670.5
026	COM[57]	COM[114]	8602.0	670.5
027	COM[58]	COM[116]	8562.0	670.5
028	COM[59]	COM[118]	8522.0	670.5
029	COM[60]	COM[120]	8482.0	670.5
030	COM[61]	COM[122]	8442.0	670.5
031	COM[62]	COM[124]	8402.0	670.5
032	COM[63]	COM[126]	8362.0	670.5
033	COM[64]	COM[128]	8322.0	670.5
034	COM[65]	COM[130]	8282.0	670.5

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
035	SEG[395]		8141.0	670.5
036	SEG[394]		8101.0	670.5
037	SEG[393]		8061.0	670.5
038	SEG[392]		8021.0	670.5
039	SEG[391]		7981.0	670.5
040	SEG[390]		7941.0	670.5
041	SEG[389]		7901.0	670.5
042	SEG[388]		7861.0	670.5
043	SEG[387]		7821.0	670.5
044	SEG[386]		7781.0	670.5
045	SEG[385]		7741.0	670.5
046	SEG[384]		7701.0	670.5
047	SEG[383]		7661.0	670.5
048	SEG[382]		7621.0	670.5
049	SEG[381]		7581.0	670.5
050	SEG[380]		7541.0	670.5
051	SEG[379]		7501.0	670.5
052	SEG[378]		7461.0	670.5
053	SEG[377]		7421.0	670.5
054	SEG[376]		7381.0	670.5
055	SEG[375]		7341.0	670.5
056	SEG[374]		7301.0	670.5
057	SEG[373]		7261.0	670.5
058	SEG[372]		7221.0	670.5
059	SEG[371]		7181.0	670.5
060	SEG[370]		7141.0	670.5
061	SEG[369]		7101.0	670.5
062	SEG[368]		7061.0	670.5
063	SEG[367]		7021.0	670.5
064	SEG[366]		6981.0	670.5
065	SEG[365]		6941.0	670.5
066	SEG[364]		6901.0	670.5
067	SEG[363]		6861.0	670.5
068	SEG[362]		6821.0	670.5

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
069	SEG[361]		6781.0	670.5
070	SEG[360]		6741.0	670.5
071	SEG[359]		6701.0	670.5
072	SEG[358]		6661.0	670.5
073	SEG[357]		6621.0	670.5
074	SEG[356]		6581.0	670.5
075	SEG[355]		6541.0	670.5
076	SEG[354]		6501.0	670.5
077	SEG[353]		6461.0	670.5
078	SEG[352]		6421.0	670.5
079	SEG[351]		6381.0	670.5
080	SEG[350]		6341.0	670.5
081	SEG[349]		6301.0	670.5
082	SEG[348]		6261.0	670.5
083	SEG[347]		6221.0	670.5
084	SEG[346]		6181.0	670.5
085	SEG[345]		6141.0	670.5
086	SEG[344]		6101.0	670.5
087	SEG[343]		6061.0	670.5
088	SEG[342]		6021.0	670.5
089	SEG[341]		5981.0	670.5
090	SEG[340]		5941.0	670.5
091	SEG[339]		5901.0	670.5
092	SEG[338]		5861.0	670.5
093	SEG[337]		5821.0	670.5
094	SEG[336]		5781.0	670.5
095	SEG[335]		5741.0	670.5
096	SEG[334]		5701.0	670.5
097	SEG[333]		5661.0	670.5
098	SEG[332]		5621.0	670.5
099	SEG[331]		5581.0	670.5
100	SEG[330]		5541.0	670.5
101	SEG[329]		5501.0	670.5
102	SEG[328]		5461.0	670.5
103	SEG[327]		5421.0	670.5

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
104	SEG[326]		5381.0	670.5
105	SEG[325]		5341.0	670.5
106	SEG[324]		5301.0	670.5
107	SEG[323]		5261.0	670.5
108	SEG[322]		5221.0	670.5
109	SEG[321]		5181.0	670.5
110	SEG[320]		5141.0	670.5
111	SEG[319]		5101.0	670.5
112	SEG[318]		5061.0	670.5
113	SEG[317]		5021.0	670.5
114	SEG[316]		4981.0	670.5
115	SEG[315]		4941.0	670.5
116	SEG[314]		4901.0	670.5
117	SEG[313]		4861.0	670.5
118	SEG[312]		4821.0	670.5
119	SEG[311]		4781.0	670.5
120	SEG[310]		4741.0	670.5
121	SEG[309]		4701.0	670.5
122	SEG[308]		4661.0	670.5
123	SEG[307]		4621.0	670.5
124	SEG[306]		4581.0	670.5
125	SEG[305]		4541.0	670.5
126	SEG[304]		4501.0	670.5
127	SEG[303]		4461.0	670.5
128	SEG[302]		4421.0	670.5
129	SEG[301]		4381.0	670.5
130	SEG[300]		4341.0	670.5
131	SEG[299]		4301.0	670.5
132	SEG[298]		4261.0	670.5
133	SEG[297]		4221.0	670.5
134	SEG[296]		4181.0	670.5
135	SEG[295]		4141.0	670.5
136	SEG[294]		4101.0	670.5
137	SEG[293]		4061.0	670.5
138	SEG[292]		4021.0	670.5

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
139	SEG[291]		3981.0	670.5
140	SEG[290]		3941.0	670.5
141	SEG[289]		3901.0	670.5
142	SEG[288]		3861.0	670.5
143	SEG[287]		3821.0	670.5
144	SEG[286]		3781.0	670.5
145	SEG[285]		3741.0	670.5
146	SEG[284]		3701.0	670.5
147	SEG[283]		3661.0	670.5
148	SEG[282]		3621.0	670.5
149	SEG[281]		3581.0	670.5
150	SEG[280]		3541.0	670.5
151	SEG[279]		3501.0	670.5
152	SEG[278]		3461.0	670.5
153	SEG[277]		3421.0	670.5
154	SEG[276]		3381.0	670.5
155	SEG[275]		3341.0	670.5
156	SEG[274]		3301.0	670.5
157	SEG[273]		3261.0	670.5
158	SEG[272]		3221.0	670.5
159	SEG[271]		3181.0	670.5
160	SEG[270]		3141.0	670.5
161	SEG[269]		3101.0	670.5
162	SEG[268]		3061.0	670.5
163	SEG[267]		3021.0	670.5
164	SEG[266]		2981.0	670.5
165	SEG[265]		2941.0	670.5
166	SEG[264]		2901.0	670.5
167	SEG[263]		2861.0	670.5
168	SEG[262]		2821.0	670.5
169	SEG[261]		2781.0	670.5
170	SEG[260]		2741.0	670.5
171	SEG[259]		2701.0	670.5
172	SEG[258]		2661.0	670.5
173	SEG[257]		2621.0	670.5

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
174	SEG[256]		2581.0	670.5
175	SEG[255]		2541.0	670.5
176	SEG[254]		2501.0	670.5
177	SEG[253]		2461.0	670.5
178	SEG[252]		2421.0	670.5
179	SEG[251]		2381.0	670.5
180	SEG[250]		2341.0	670.5
181	SEG[249]		2301.0	670.5
182	SEG[248]		2261.0	670.5
183	SEG[247]		2221.0	670.5
184	SEG[246]		2181.0	670.5
185	SEG[245]		2141.0	670.5
186	SEG[244]		2101.0	670.5
187	SEG[243]		2061.0	670.5
188	SEG[242]		2021.0	670.5
189	SEG[241]		1981.0	670.5
190	SEG[240]		1941.0	670.5
191	SEG[239]		1901.0	670.5
192	SEG[238]		1861.0	670.5
193	SEG[237]		1821.0	670.5
194	SEG[236]		1781.0	670.5
195	SEG[235]		1741.0	670.5
196	SEG[234]		1701.0	670.5
197	SEG[233]		1661.0	670.5
198	SEG[232]		1621.0	670.5
199	SEG[231]		1581.0	670.5
200	SEG[230]		1541.0	670.5
201	SEG[229]		1501.0	670.5
202	SEG[228]		1461.0	670.5
203	SEG[227]		1421.0	670.5
204	SEG[226]		1381.0	670.5
205	SEG[225]		1341.0	670.5
206	SEG[224]		1301.0	670.5
207	SEG[223]		1261.0	670.5
208	SEG[222]		1221.0	670.5

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
209	SEG[221]		1181.0	670.5
210	SEG[220]		1141.0	670.5
211	SEG[219]		1101.0	670.5
212	SEG[218]		1061.0	670.5
213	SEG[217]		1021.0	670.5
214	SEG[216]		981.0	670.5
215	SEG[215]		941.0	670.5
216	SEG[214]		901.0	670.5
217	SEG[213]		861.0	670.5
218	SEG[212]		821.0	670.5
219	SEG[211]		781.0	670.5
220	SEG[210]		741.0	670.5
221	SEG[209]		701.0	670.5
222	SEG[208]		661.0	670.5
223	SEG[207]		621.0	670.5
224	SEG[206]		581.0	670.5
225	SEG[205]		541.0	670.5
226	SEG[204]		501.0	670.5
227	SEG[203]		461.0	670.5
228	SEG[202]		421.0	670.5
229	SEG[201]		381.0	670.5
230	SEG[200]		341.0	670.5
231	SEG[199]		301.0	670.5
232	SEG[198]		261.0	670.5
233	SEG[197]		221.0	670.5
234	SEG[196]		181.0	670.5
235	SEG[195]		141.0	670.5
236	SEG[194]		101.0	670.5
237	SEG[193]		61.0	670.5
238	SEG[192]		21.0	670.5
239	SEG[191]		-19.0	670.5
240	SEG[190]		-59.0	670.5
241	SEG[189]		-99.0	670.5
242	SEG[188]		-139.0	670.5
243	SEG[187]		-179.0	670.5

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
244	SEG[186]		-219.0	670.5
245	SEG[185]		-259.0	670.5
246	SEG[184]		-299.0	670.5
247	SEG[183]		-339.0	670.5
248	SEG[182]		-379.0	670.5
249	SEG[181]		-419.0	670.5
250	SEG[180]		-459.0	670.5
251	SEG[179]		-499.0	670.5
252	SEG[178]		-539.0	670.5
253	SEG[177]		-579.0	670.5
254	SEG[176]		-619.0	670.5
255	SEG[175]		-659.0	670.5
256	SEG[174]		-699.0	670.5
257	SEG[173]		-739.0	670.5
258	SEG[172]		-779.0	670.5
259	SEG[171]		-819.0	670.5
260	SEG[170]		-859.0	670.5
261	SEG[169]		-899.0	670.5
262	SEG[168]		-939.0	670.5
263	SEG[167]		-979.0	670.5
264	SEG[166]		-1019.0	670.5
265	SEG[165]		-1059.0	670.5
266	SEG[164]		-1099.0	670.5
267	SEG[163]		-1139.0	670.5
268	SEG[162]		-1179.0	670.5
269	SEG[161]		-1219.0	670.5
270	SEG[160]		-1259.0	670.5
271	SEG[159]		-1299.0	670.5
272	SEG[158]		-1339.0	670.5
273	SEG[157]		-1379.0	670.5
274	SEG[156]		-1419.0	670.5
275	SEG[155]		-1459.0	670.5
276	SEG[154]		-1499.0	670.5
277	SEG[153]		-1539.0	670.5
278	SEG[152]		-1579.0	670.5

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
279	SEG[151]		-1619.0	670.5
280	SEG[150]		-1659.0	670.5
281	SEG[149]		-1699.0	670.5
282	SEG[148]		-1739.0	670.5
283	SEG[147]		-1779.0	670.5
284	SEG[146]		-1819.0	670.5
285	SEG[145]		-1859.0	670.5
286	SEG[144]		-1899.0	670.5
287	SEG[143]		-1939.0	670.5
288	SEG[142]		-1979.0	670.5
289	SEG[141]		-2019.0	670.5
290	SEG[140]		-2059.0	670.5
291	SEG[139]		-2099.0	670.5
292	SEG[138]		-2139.0	670.5
293	SEG[137]		-2179.0	670.5
294	SEG[136]		-2219.0	670.5
295	SEG[135]		-2259.0	670.5
296	SEG[134]		-2299.0	670.5
297	SEG[133]		-2339.0	670.5
298	SEG[132]		-2379.0	670.5
299	SEG[131]		-2419.0	670.5
300	SEG[130]		-2459.0	670.5
301	SEG[129]		-2499.0	670.5
302	SEG[128]		-2539.0	670.5
303	SEG[127]		-2579.0	670.5
304	SEG[126]		-2619.0	670.5
305	SEG[125]		-2659.0	670.5
306	SEG[124]		-2699.0	670.5
307	SEG[123]		-2739.0	670.5
308	SEG[122]		-2779.0	670.5
309	SEG[121]		-2819.0	670.5
310	SEG[120]		-2859.0	670.5
311	SEG[119]		-2899.0	670.5
312	SEG[118]		-2939.0	670.5
313	SEG[117]		-2979.0	670.5

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
314	SEG[116]		-3019.0	670.5
315	SEG[115]		-3059.0	670.5
316	SEG[114]		-3099.0	670.5
317	SEG[113]		-3139.0	670.5
318	SEG[112]		-3179.0	670.5
319	SEG[111]		-3219.0	670.5
320	SEG[110]		-3259.0	670.5
321	SEG[109]		-3299.0	670.5
322	SEG[108]		-3339.0	670.5
323	SEG[107]		-3379.0	670.5
324	SEG[106]		-3419.0	670.5
325	SEG[105]		-3459.0	670.5
326	SEG[104]		-3499.0	670.5
327	SEG[103]		-3539.0	670.5
328	SEG[102]		-3579.0	670.5
329	SEG[101]		-3619.0	670.5
330	SEG[100]		-3659.0	670.5
331	SEG[99]		-3699.0	670.5
332	SEG[98]		-3739.0	670.5
333	SEG[97]		-3779.0	670.5
334	SEG[96]		-3819.0	670.5
335	SEG[95]		-3859.0	670.5
336	SEG[94]		-3899.0	670.5
337	SEG[93]		-3939.0	670.5
338	SEG[92]		-3979.0	670.5
339	SEG[91]		-4019.0	670.5
340	SEG[90]		-4059.0	670.5
341	SEG[89]		-4099.0	670.5
342	SEG[88]		-4139.0	670.5
343	SEG[87]		-4179.0	670.5
344	SEG[86]		-4219.0	670.5
345	SEG[85]		-4259.0	670.5
346	SEG[84]		-4299.0	670.5
347	SEG[83]		-4339.0	670.5
348	SEG[82]		-4379.0	670.5

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
349	SEG[81]		-4419.0	670.5
350	SEG[80]		-4459.0	670.5
351	SEG[79]		-4499.0	670.5
352	SEG[78]		-4539.0	670.5
353	SEG[77]		-4579.0	670.5
354	SEG[76]		-4619.0	670.5
355	SEG[75]		-4659.0	670.5
356	SEG[74]		-4699.0	670.5
357	SEG[73]		-4739.0	670.5
358	SEG[72]		-4779.0	670.5
359	SEG[71]		-4819.0	670.5
360	SEG[70]		-4859.0	670.5
361	SEG[69]		-4899.0	670.5
362	SEG[68]		-4939.0	670.5
363	SEG[67]		-4979.0	670.5
364	SEG[66]		-5019.0	670.5
365	SEG[65]		-5059.0	670.5
366	SEG[64]		-5099.0	670.5
367	SEG[63]		-5139.0	670.5
368	SEG[62]		-5179.0	670.5
369	SEG[61]		-5219.0	670.5
370	SEG[60]		-5259.0	670.5
371	SEG[59]		-5299.0	670.5
372	SEG[58]		-5339.0	670.5
373	SEG[57]		-5379.0	670.5
374	SEG[56]		-5419.0	670.5
375	SEG[55]		-5459.0	670.5
376	SEG[54]		-5499.0	670.5
377	SEG[53]		-5539.0	670.5
378	SEG[52]		-5579.0	670.5
379	SEG[51]		-5619.0	670.5
380	SEG[50]		-5659.0	670.5
381	SEG[49]		-5699.0	670.5
382	SEG[48]		-5739.0	670.5
383	SEG[47]		-5779.0	670.5

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
384	SEG[46]		-5819.0	670.5
385	SEG[45]		-5859.0	670.5
386	SEG[44]		-5899.0	670.5
387	SEG[43]		-5939.0	670.5
388	SEG[42]		-5979.0	670.5
389	SEG[41]		-6019.0	670.5
390	SEG[40]		-6059.0	670.5
391	SEG[39]		-6099.0	670.5
392	SEG[38]		-6139.0	670.5
393	SEG[37]		-6179.0	670.5
394	SEG[36]		-6219.0	670.5
395	SEG[35]		-6259.0	670.5
396	SEG[34]		-6299.0	670.5
397	SEG[33]		-6339.0	670.5
398	SEG[32]		-6379.0	670.5
399	SEG[31]		-6419.0	670.5
400	SEG[30]		-6459.0	670.5
401	SEG[29]		-6499.0	670.5
402	SEG[28]		-6539.0	670.5
403	SEG[27]		-6579.0	670.5
404	SEG[26]		-6619.0	670.5
405	SEG[25]		-6659.0	670.5
406	SEG[24]		-6699.0	670.5
407	SEG[23]		-6739.0	670.5
408	SEG[22]		-6779.0	670.5
409	SEG[21]		-6819.0	670.5
410	SEG[20]		-6859.0	670.5
411	SEG[19]		-6899.0	670.5
412	SEG[18]		-6939.0	670.5
413	SEG[17]		-6979.0	670.5
414	SEG[16]		-7019.0	670.5
415	SEG[15]		-7059.0	670.5
416	SEG[14]		-7099.0	670.5
417	SEG[13]		-7139.0	670.5
418	SEG[12]		-7179.0	670.5

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
419	SEG[11]		-7219.0	670.5
420	SEG[10]		-7259.0	670.5
421	SEG[9]		-7299.0	670.5
422	SEG[8]		-7339.0	670.5
423	SEG[7]		-7379.0	670.5
424	SEG[6]		-7419.0	670.5
425	SEG[5]		-7459.0	670.5
426	SEG[4]		-7499.0	670.5
427	SEG[3]		-7539.0	670.5
428	SEG[2]		-7579.0	670.5
429	SEG[1]		-7619.0	670.5
430	SEG[0]		-7659.0	670.5
431	COM[66]	COM[131]	-8282.0	670.5
432	COM[67]	COM[129]	-8322.0	670.5
433	COM[68]	COM[127]	-8362.0	670.5
434	COM[69]	COM[125]	-8402.0	670.5
435	COM[70]	COM[123]	-8442.0	670.5
436	COM[71]	COM[121]	-8482.0	670.5
437	COM[72]	COM[119]	-8522.0	670.5
438	COM[73]	COM[117]	-8562.0	670.5
439	COM[74]	COM[115]	-8602.0	670.5
440	COM[75]	COM[113]	-8642.0	670.5
441	COM[76]	COM[111]	-8682.0	670.5
442	COM[77]	COM[109]	-8722.0	670.5
443	COM[78]	COM[107]	-8762.0	670.5
444	COM[79]	COM[105]	-8802.0	670.5
445	COM[80]	COM[103]	-8842.0	670.5
446	COM[81]	COM[101]	-8882.0	670.5
447	COM[82]	COM[99]	-8922.0	670.5
448	COM[83]	COM[97]	-8962.0	670.5
449	COM[84]	COM[95]	-9002.0	670.5
450	COM[85]	COM[93]	-9042.0	670.5
451	COM[86]	COM[91]	-9082.0	670.5
452	COM[87]	COM[89]	-9122.0	670.5
453	COM[88]	COM[87]	-9162.0	670.5

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
454	COM[89]	COM[85]	-9202.0	670.5
455	COM[90]	COM[83]	-9242.0	670.5
456	COM[91]	COM[81]	-9282.0	670.5
457	COM[92]	COM[79]	-9322.0	670.5
458	COM[93]	COM[77]	-9362.0	670.5
459	COM[94]	COM[75]	-9402.0	670.5
460	COM[95]	COM[73]	-9442.0	670.5
461	COM[96]	COM[71]	-9482.0	670.5
462	COM[97]	COM[69]	-9522.0	670.5
463	COM[98]	COM[67]	-9562.0	670.5
464	COM[99]	COM[65]	-9602.0	670.5
465	COM[100]	COM[63]	-9870.5	650.0
466	COM[101]	COM[61]	-9870.5	610.0
467	COM[102]	COM[59]	-9870.5	570.0
468	COM[103]	COM[57]	-9870.5	530.0
469	COM[104]	COM[55]	-9870.5	490.0
470	COM[105]	COM[53]	-9870.5	450.0
471	COM[106]	COM[51]	-9870.5	410.0
472	COM[107]	COM[49]	-9870.5	370.0
473	COM[108]	COM[47]	-9870.5	330.0
474	COM[109]	COM[45]	-9870.5	290.0
475	COM[110]	COM[43]	-9870.5	250.0
476	COM[111]	COM[41]	-9870.5	210.0
477	COM[112]	COM[39]	-9870.5	170.0
478	COM[113]	COM[37]	-9870.5	130.0
479	COM[114]	COM[35]	-9870.5	90.0
480	COM[115]	COM[33]	-9870.5	50.0
481	COM[116]	COM[31]	-9870.5	10.0
482	COM[117]	COM[29]	-9870.5	-30.0
483	COM[118]	COM[27]	-9870.5	-70.0
484	COM[119]	COM[25]	-9870.5	-110.0
485	COM[120]	COM[23]	-9870.5	-150.0
486	COM[121]	COM[21]	-9870.5	-190.0
487	COM[122]	COM[19]	-9870.5	-230.0
488	COM[123]	COM[17]	-9870.5	-270.0

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
489	COM[124]	COM[15]	-9870.5	-310.0
490	COM[125]	COM[13]	-9870.5	-350.0
491	COM[126]	COM[11]	-9870.5	-390.0
492	COM[127]	COM[9]	-9870.5	-430.0
493	COM[128]	COM[7]	-9870.5	-470.0
494	COM[129]	COM[5]	-9870.5	-510.0
495	COM[130]	COM[3]	-9870.5	-550.0
496	COM[131]	COM[1]	-9870.5	-590.0
497	NC		-8355.0	-699.0
498	NC		-8245.0	-699.0
499	NC		-8135.0	-699.0
500	NC		-8025.0	-699.0
501	NC		-7915.0	-699.0
502	NC		-7805.0	-699.0
503	NC		-7695.0	-699.0
504	NC		-7585.0	-699.0
505	NC		-7475.0	-699.0
506	NC		-7365.0	-699.0
507	NC		-7255.0	-699.0
508	NC		-7145.0	-699.0
509	NC		-7035.0	-699.0
510	NC		-6925.0	-699.0
511	NC		-6815.0	-699.0
512	NC		-6705.0	-699.0
513	NC		-6595.0	-699.0
514	NC		-6485.0	-699.0
515	NC		-6375.0	-699.0
516	NC		-6265.0	-699.0
517	NC		-6155.0	-699.0
518	NC		-6045.0	-699.0
519	NC		-5935.0	-699.0
520	NC		-5825.0	-699.0
521	NC		-5715.0	-699.0
522	NC		-5605.0	-699.0
523	NC		-5495.0	-699.0

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
524	NC		-5385.0	-699.0
525	NC		-5275.0	-699.0
526	NC		-5165.0	-699.0
527	NC		-5055.0	-699.0
528	NC		-4945.0	-699.0
529	NC		-4835.0	-699.0
530	NC		-4725.0	-699.0
531	NC		-4615.0	-699.0
532	NC		-4505.0	-699.0
533	VDD		-4395.0	-699.0
534	CL		-4285.0	-699.0
535	CLS		-4175.0	-699.0
536	VSS		-4065.0	-699.0
537	VDD		-3955.0	-699.0
538	A0		-3845.0	-699.0
539	RW_WR		-3735.0	-699.0
540	VSS		-3625.0	-699.0
541	VDD		-3515.0	-699.0
542	D0		-3405.0	-699.0
543	D1		-3295.0	-699.0
544	D2		-3185.0	-699.0
545	D3		-3075.0	-699.0
546	D4		-2965.0	-699.0
547	D5		-2855.0	-699.0
548	D6		-2745.0	-699.0
549	D7		-2635.0	-699.0
550	VSS		-2525.0	-699.0
551	VDD		-2415.0	-699.0
552	D8		-2305.0	-699.0
553	D9		-2195.0	-699.0
554	D10		-2085.0	-699.0
555	D11		-1975.0	-699.0
556	D12		-1865.0	-699.0
557	D13		-1755.0	-699.0
558	D14		-1645.0	-699.0

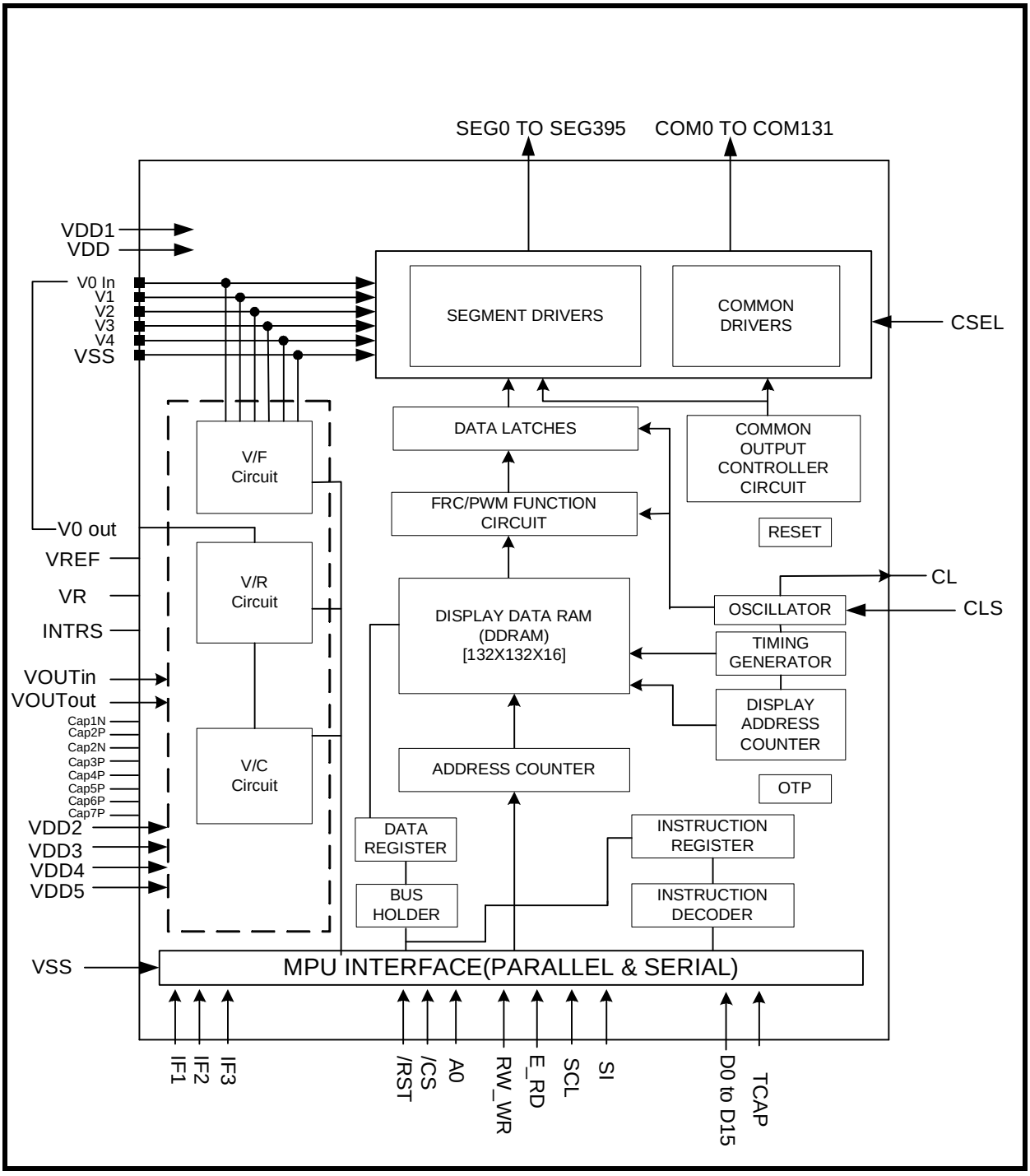
PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
559	D15		-1535.0	-699.0
560	VSS		-1425.0	-699.0
561	VDD		-1315.0	-699.0
562	E_RD		-1205.0	-699.0
563	RST		-1095.0	-699.0
564	VSS		-985.0	-699.0
565	VDD		-875.0	-699.0
566	CSEL		-765.0	-699.0
567	INTRS		-655.0	-699.0
568	IF1		-545.0	-699.0
569	IF2		-435.0	-699.0
570	IF3		-325.0	-699.0
571	VSS		-215.0	-699.0
572	VDD		-105.0	-699.0
573	SI		5.0	-699.0
574	SCL		115.0	-699.0
575	/CS		225.0	-699.0
576	VDD		335.0	-699.0
577	VDD		445.0	-699.0
578	VDD		555.0	-699.0
579	VDD		665.0	-699.0
580	VDD		775.0	-699.0
581	VDD		885.0	-699.0
582	VDD1		995.0	-699.0
583	VDD1		1105.0	-699.0
584	VSS		1215.0	-699.0
585	VSS		1325.0	-699.0
586	VSS		1435.0	-699.0
587	VSS		1545.0	-699.0
588	VSS		1655.0	-699.0
589	VSS		1765.0	-699.0
590	VSS		1875.0	-699.0
591	VSS		1985.0	-699.0
592	VSS		2095.0	-699.0
593	VSS		2205.0	-699.0

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
594	VSS		2315.0	-699.0
595	VSS		2425.0	-699.0
596	VSS		2535.0	-699.0
597	VSS		2645.0	-699.0
598	VSS		2755.0	-699.0
599	VSS		2865.0	-699.0
600	VSS		2975.0	-699.0
601	VSS		3085.0	-699.0
602	VSS		3195.0	-699.0
603	VSS		3305.0	-699.0
604	VSS		3415.0	-699.0
605	VDD4		3525.0	-699.0
606	VDD4		3635.0	-699.0
607	VDD3		3745.0	-699.0
608	VDD3		3855.0	-699.0
609	VDD2		3965.0	-699.0
610	VDD2		4075.0	-699.0
611	VDD2		4185.0	-699.0
612	VDD2		4295.0	-699.0
613	VDD2		4405.0	-699.0
614	VDD2		4515.0	-699.0
615	VDD2		4625.0	-699.0
616	VDD2		4735.0	-699.0
617	VDD2		4845.0	-699.0
618	VDD2		4955.0	-699.0
619	VDD5		5065.0	-699.0
620	VDD5		5175.0	-699.0
621	VDD5		5285.0	-699.0
622	VDD5		5395.0	-699.0
623	TCAP		5505.0	-699.0
624	CAP2P		5615.0	-699.0
625	CAP2N		5725.0	-699.0
626	CAP6P		5835.0	-699.0
627	CAP2N		5945.0	-699.0
628	CAP4P		6055.0	-699.0

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
629	CAP7P		6165.0	-699.0
630	CAP1N		6275.0	-699.0
631	CAP5P		6385.0	-699.0
632	CAP3P		6495.0	-699.0
633	CAP1N		6605.0	-699.0
634	CAP1P		6715.0	-699.0
635	$VOUT_{IN}$		6825.0	-699.0
636	$VOUT_{IN}$		6935.0	-699.0
637	$VOUT_{IN}$		7045.0	-699.0
638	$VOUT_{IN}$		7155.0	-699.0
639	$VOUT_{IN}$		7265.0	-699.0
640	$VOUT_{IN}$		7375.0	-699.0
641	$VOUT_{OUT}$		7485.0	-699.0
642	$VOUT_{OUT}$		7595.0	-699.0
643	$VOUT_{OUT}$		7705.0	-699.0
644	$VOUT_{OUT}$		7815.0	-699.0
645	$VOUT_{OUT}$		7925.0	-699.0
646	$VOUT_{OUT}$		8035.0	-699.0
647	VREF		8145.0	-699.0
648	VR		8255.0	-699.0
649	V4		8365.0	-699.0
650	V3		8475.0	-699.0
651	V2		8585.0	-699.0
652	V1		8695.0	-699.0
653	V0OUT		8805.0	-699.0
654	V0OUT		8915.0	-699.0
655	V0OUT		9025.0	-699.0
656	V0OUT		9135.0	-699.0
657	V0IN		9245.0	-699.0
658	V0IN		9355.0	-699.0
659	V0IN		9465.0	-699.0
660	V0IN		9575.0	-699.0

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
661	COM[0]	COM[0]	9870.5	-590.0
662	COM[1]	COM[2]	9870.5	-550.0
663	COM[2]	COM[4]	9870.5	-510.0
664	COM[3]	COM[6]	9870.5	-470.0
665	COM[4]	COM[8]	9870.5	-430.0
666	COM[5]	COM[10]	9870.5	-390.0
667	COM[6]	COM[12]	9870.5	-350.0
668	COM[7]	COM[14]	9870.5	-310.0
669	COM[8]	COM[16]	9870.5	-270.0
670	COM[9]	COM[18]	9870.5	-230.0
671	COM[10]	COM[20]	9870.5	-190.0
672	COM[11]	COM[22]	9870.5	-150.0
673	COM[12]	COM[24]	9870.5	-110.0
674	COM[13]	COM[26]	9870.5	-70.0
675	COM[14]	COM[28]	9870.5	-30.0
676	COM[15]	COM[30]	9870.5	10.0
677	COM[16]	COM[32]	9870.5	50.0
678	COM[17]	COM[34]	9870.5	90.0
679	COM[18]	COM[36]	9870.5	130.0
680	COM[19]	COM[38]	9870.5	170.0
681	COM[20]	COM[40]	9870.5	210.0
682	COM[21]	COM[42]	9870.5	250.0
683	COM[22]	COM[44]	9870.5	290.0
684	COM[23]	COM[46]	9870.5	330.0
685	COM[24]	COM[48]	9870.5	370.0
686	COM[25]	COM[50]	9870.5	410.0
687	COM[26]	COM[52]	9870.5	450.0
688	COM[27]	COM[54]	9870.5	490.0
689	COM[28]	COM[56]	9870.5	530.0
690	COM[29]	COM[58]	9870.5	570.0
691	COM[30]	COM[60]	9870.5	610.0
692	COM[31]	COM[62]	9870.5	650.0

5. BLOCK DIAGRAM



6. PIN DESCRIPTION

6.1 POWER SUPPLY

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>VDD</td><td>Supply</td><td>Power supply for logic circuit</td></tr>
<tr><td>VDD1</td><td>Supply</td><td>Power supply for OSC circuit</td></tr>
<tr><td>VDD2</td><td>Supply</td><td>Power supply for Booster Circuit</td></tr>
<tr><td>VDD3</td><td>Supply</td><td>Power supply for LCD.</td></tr>
<tr><td>VDD4</td><td>Supply</td><td>Power supply for LCD.</td></tr>
<tr><td>VDD5</td><td>Supply</td><td>Power supply for LCD.</td></tr>
<tr><td>VSS</td><td>Supply</td><td>Ground. Ground system should be connected together.</td></tr>
<tr><td>$VOUT_{OUT}$</td><td>Supply</td><td>If the internal voltage generator is used, the VOUTIN & $VOUT_{OUT}$ must be connected together.
If an external supply is used, this pin must be left open.</td></tr>
<tr><td>$VOUT_{IN}$</td><td>Supply</td><td>An external LCD supply voltage can be supplied using the $VOUT_{IN}$ pad. In this case, $VOUT_{OUT}$ has to be left open, and the internal voltage generator has to be programmed to zero. (SET register VC=0)</td></tr>
<tr><td>V0in
V0out
V1
V2
V3
V4</td><td>I/O</td><td>LCD driver supply voltages
V0in & V0out should be connected together.
Voltages should have the following relationship;
V0 (V0in) ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS.
When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias.
<table>
<tr><th>LCD bias</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr>
<tr><td>1/N bias</td><td>(N-1) / N x V0</td><td>(N-2) / N x V0</td><td>(2/N) x V0</td><td>(1/N) x V0</td></tr>
</table>
NOTE: N = 5 to 12</td></tr>
</table>

6.2 LCD Power Supply Pins

Pin Name	I/O	Function
CAP1N	O	DC/DC voltage converter. Connect capacitors between this terminal and the CAP1P, CAP3P, CAP5P, CAP7P terminal.
CAP2N	O	DC/DC voltage converter. Connect capacitors between this terminal and the CAP2P, CAP4P, CAP6P terminal.
CAP1P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
CAP2P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.
CAP3P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
CAP4P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.
CAP5P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
CAP6P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.

CAP7P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
VREF	O	Reference voltage output for monitor only. Left it opened.
VR	I	Reference voltage output for monitor only. Left it opened.

6.3 SYSTEM CONTROL

Name	I/O	Description
CLS	I	When using internal clock oscillator, connect CLS to VDD. When using external clock oscillator, connect CLS to VSS.
CL	I/O	When using internal clock oscillator, it's oscillator output. When using external clock oscillator, it's clock input.
INTRS	I	This terminal selects the resistors for the V0 voltage level adjustment. This pin should be fixed to High.
CSEL	I	Select Common output direction. CSEL="L", COM0~COM65 is in one side, COM66~COM131 is in the opposite side. CSEL="H", COM2n(even number) is in the one side, COM2n+1 (odd number) is in the opposite side.
TCAP	I/O	Test pin. Left it opened.

6.4 MICROPROCESSOR INTERFACE

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RST</td><td>I</td><td>Reset input pin
When RESETB is “L”, initialization is executed.</td></tr>
<tr><td>IF[3:1]</td><td>I</td><td>Parallel / Serial data input select input
<table>
<tr><th>IF1</th><th>IF2</th><th>IF3</th><th>MPU interface type</th></tr>
<tr><td>H</td><td>H</td><td>H</td><td>80 series 16-bit parallel</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>80 series 8-bit parallel</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>68 series 16-bit parallel</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>68 series 8-bit parallel</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>9-bit serial (3 line)</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>8-bit serial (4 line)</td></tr>
</table></td></tr>
<tr><td>/CS</td><td>I</td><td>Chip select input pins
Data / Instruction I/O is enabled only when /CS is "L". When chip select is non-active, D0 to D15 become high impedance.</td></tr>
</table>

<table>
<tr><td>A0</td><td>I</td><td>Register select input pin
A0 = "H": D0 to D15 or SI are display data
A0 = "L": D0 to D15 or SI are control data
In 3-line interface not let it floating, contact it to VSS or VDD.</td></tr>
<tr><td>RW_WR</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>MPU type</th><th>RW_WR</th><th>Description</th></tr>
<tr><td>6800-series</td><td>RW</td><td>Read / Write control input pin
RW = “H” : read
RW = “L” : write</td></tr>
<tr><td>8080-series</td><td>/WR</td><td>Write enable clock input pin
The data on D0 to D15 are latched at the rising edge of the /WR signal.</td></tr>
</table>
When in the serial interface, contact it to VSS or VDD.</td></tr>
<tr><td>E_RD</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>MPU Type</th><th>E_RD</th><th>Description</th></tr>
<tr><td>6800-series</td><td>E</td><td>Read / Write control input pin
RW = “H”: When E is “H”, D0 to D15 are in an output status.
RW = “L”: The data on D0 to D15 are latched at the falling edge of the E signal.</td></tr>
<tr><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is “L”, D0 to D15 are in an output status.</td></tr>
</table>
When in the serial interface, contact it to VSS or VDD.</td></tr>
<tr><td>D15 to D0</td><td>I/O</td><td>They connect to the standard 8-bit or 16 bit MPU bus via the 8/16 –bit bi-directional bus.
When the following interface is selected and the /CS pin is high, the following pins become high impedance.
1. In 8-bit parallel: D15-D8 are in the state of high impedance, should contact to “H” level or “L” level.
2. In Serial interface: D15-D0 are in the state of high impedance, should contact to “H” level or “L” level.</td></tr>
<tr><td>SI</td><td>I</td><td>This pin is used to input serial data when the serial interface is selected.(3 line and 4 line)
When not use contact it to VSS.</td></tr>
<tr><td>SCL</td><td>I</td><td>This pin is used to input serial clock when the serial interface is selected.
The data is converted in the rising edge. (3 line and 4 line)
When not use contact it to VSS.</td></tr>
</table>

NOTE: Microprocessor interface pins should not be floating in any operation mode.

6.5 LCD DRIVER OUTPUTS

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>SEG0
to
SEG395</td><td>O</td><td>LCD segment driver outputs
The display data and the M signal control the output voltage of segment driver.
<table>
<tr><th rowspan="2">Display data</th><th rowspan="2">M (Internal)</th><th colspan="2">Segment driver output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>VSS</td></tr>
<tr><td colspan="2">Sleep in mode</td><td>VSS</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COM0
to
COM131</td><td>O</td><td>LCD common driver outputs
The internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><th>Scan data</th><th>M (Internal)</th><th>Common driver output voltage</th></tr>
<tr><td>H</td><td>H</td><td>VSS</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
<tr><td colspan="2">Sleep in mode</td><td>VSS</td></tr>
</table></td></tr>
</table>

ST7636 I/O PIN ITO Resister Limitation

Pin Name	ITO Resister
VREF, TCAP, CL, VR	Floating
IF[3:1],CLS,CSEL,INTRS	No Limitation
VDD, VDD1~VDD5, VSS, CAP1N, CAP2N, $VOUT_{IN}$, $VOUT_{OUT}$	<100Ω
V0in, V0out, V1, V2, V3, V4, CAP1P~7P	<100Ω
A0, E_RD, RW_WR, /CS, D0 …D15, SCL, SI	<1KΩ
RST	<10KΩ

NOTE:

Make sure the ITO resistance of COM0 ~ COM131 is equal, and so is it of SEG0 ~ SEG395.

7. FUNCTIONAL DESCRIPTION

7.1 MICROPROCESSOR INTERFACE

Chip Select Input

/CS pin is for chip selection. The ST7636 can function with an MPU when /CS is "L". In case of serial interface, the internal shift register and the counter are reset.

7.1.1 Selecting Parallel / Serial Interface

ST7636 has six types of interface with an MPU, which are two serial and four parallel interfaces. This parallel or serial interface is determined by IF pin as shown in table 7.1.1**.**

Table 7.1.1 Parallel / Serial Interface Mode

I/F Mode			I/F Description	Pin Assignment							
IF1	IF2	IF3		/CS	A0	E_RD	RW_WR	D15 to D8	D7 to D0	SI	SCL
H	H	H	80 serial 16-bit parallel	/CS	A0	/RD	/WR	D15 ~ D8	D7 ~ D0	--	--
H	H	L	80 serial 8-bit parallel	/CS	A0	/RD	/WR	--	D7 ~ D0	--	--
H	L	L	68 serial 16-bit parallel	/CS	A0	E	R/W	D15 ~ D8	D7 ~ D0	--	--
L	H	H	68 serial 8-bit parallel	/CS	A0	E	R/W	--	D7 ~ D0	--	--
L	L	L	8-bit SPI mode (4 line)	/CS	A0	--	--	--	--	SI	SCL
L	L	H	9-bit SPI mode (3 line)	/CS	--	--	--	--	--	SI	SCL

NOTE: When these pins are set to any other combination, A0, E_RD and RW_WR inputs are disabled and D0 to D15 are to be high impedance.

7.1.2 8-bit or 16-bit Parallel Interface

The ST7636 identifies the type of the data bus signals according to the combination of A0, /RD (E) and /WR (W/R) signals, as shown in table 7.1.2.

Table 7.1.2 Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	R/W	E	/RD	/WR	
H	H	H	L	H	Display data read out
H	L	H	H	L	Display data write
L	H	H	L	H	Register status read
L	L	H	H	L	Writes to internal register (instruction)

Relation between Data Bus and Gradation Data

ST7636 offers the 65K color display, dithered 262K color, and dithered 16M color.

When using 65K, 262K, and 16M color, you can specify color for each of R, G, B using the palette function.

Use the command for switching between these modes.

(1) 65K color input mode

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: RRRRRGGG 1st write

D7, D6, D5, D4, D3, D2, D1, D0: GGGBBBBB 2nd write

A single pixel of data is read after the second write operation as shown, and it is written in the display RAM.

2. 16-bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRRGGGGGGBBBBB (16 bits)

Data is acquired through signal write operation and then written to the display RAM.

(2) 262K color input mode

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRXX 1st write

D7, D6, D5, D4, D3, D2, D1, D0: GGGGGGXX 2nd write

D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBXX 3rd write

A single pixel of data is read after the third write operation as shown, and it is written in the display RAM.

"X" is dummy bit, and it is ignored for display.

2. 16 bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRXXGGGGGGXX 1st write

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBXXXXXXXXXX 2nd write

A single pixel of data is read after the second write operation as shown, and it is written in the display RAM.

(3) 16M color input mode

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRRR 1st write

D7, D6, D5, D4, D3, D2, D1, D0: GGGGGGGG 2nd write

D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBBB 3rd write

A single pixel of data is read after the third write operation as shown, and it is written in the display RAM.

2. 16 bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRRRGGGGGGGG 1st write

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBBBXXXXXXXX 2nd write

A single pixel of data is read after the second write operation as shown, and it is written in the display RAM.

7.1.3 8- and 9-bit Serial Interface

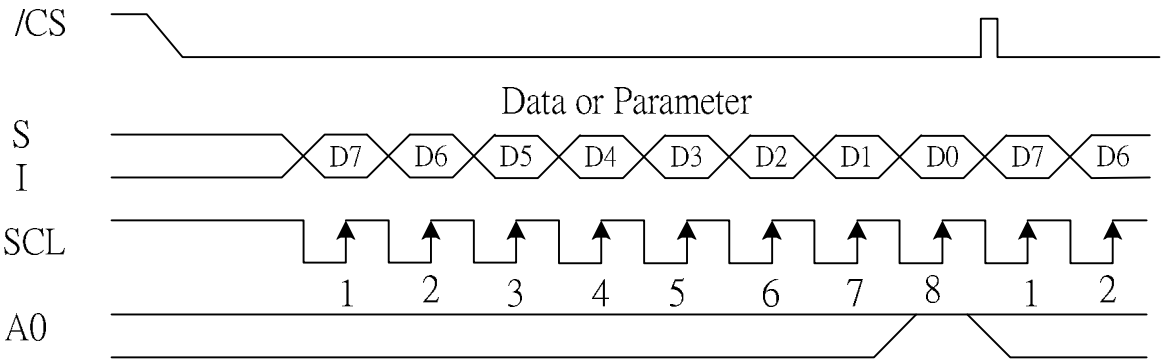
The 8-bit serial interface uses four pins /CS, SI, SCL, and A0 to enter commands and data. Meanwhile, the 9-bit serial interface uses three pins /CS, SI and SCL for the same purpose.

Data read is not available in the serial interface. Data entered must be 8 bits. Refer to the following chart for entering commands, parameters or gray-scale data.

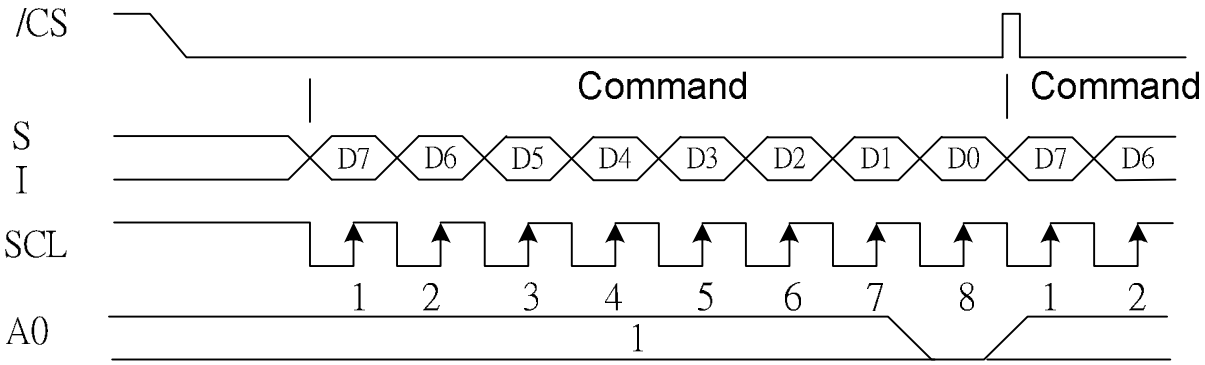
The relation between gray-scale data and data bus in the serial input is the same as that in the 8-bit parallel interface mode at every gradation.

(1) 8-bit serial interface (4 line)

When entering data (parameters): A0= HIGH at the rising edge of the 8th SCL.

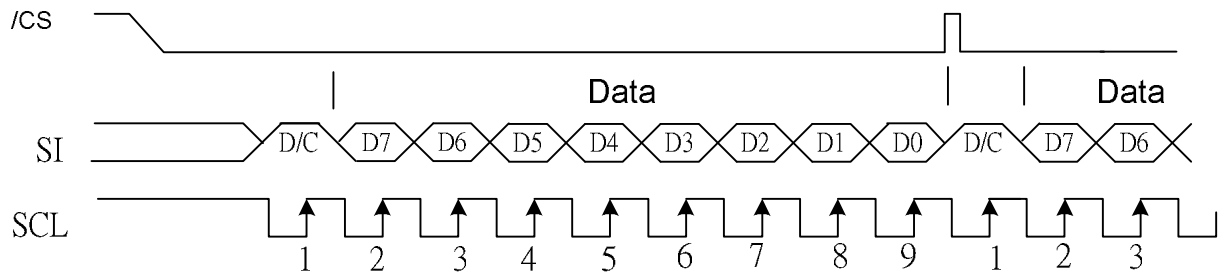


When entering command: A0= LOW at the rising edge of the 8th SCL

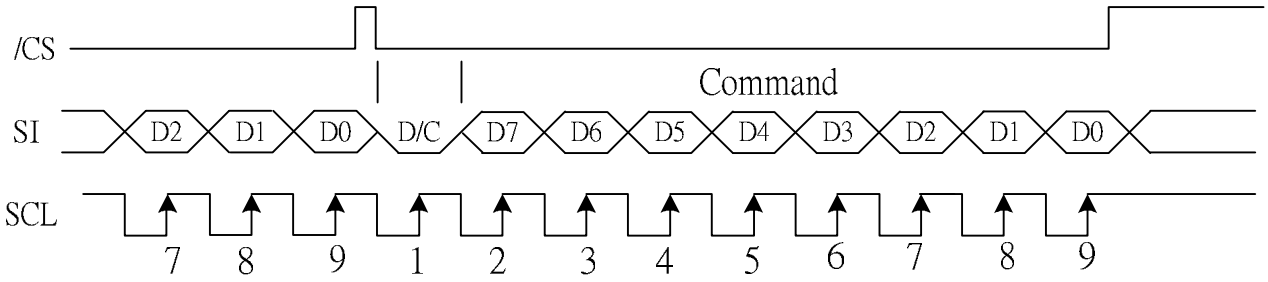


(2) 9-bit serial interface (3 line)

When entering data (parameters): SI= HIGH at the rising edge of the 1st SCL.



When entering command: SI= LOW at the rising edge of the 1st SCL.



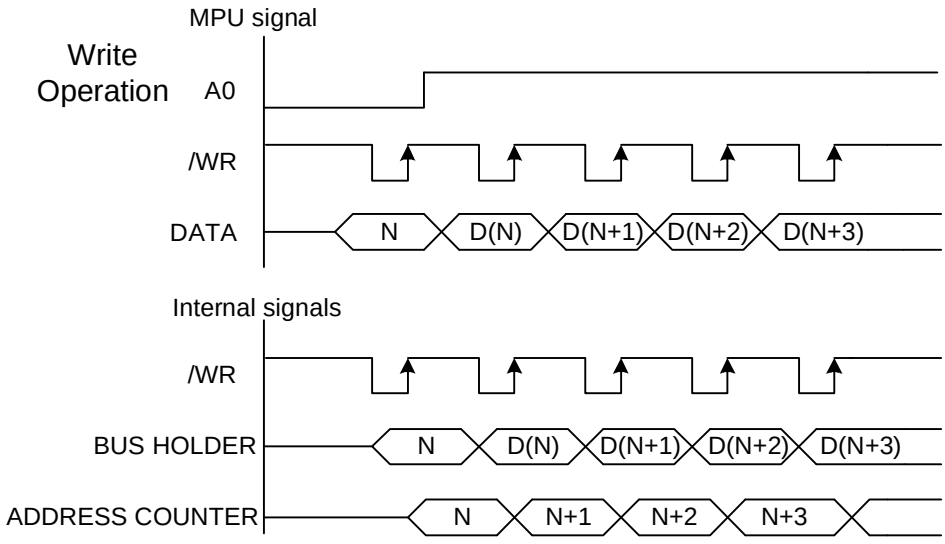
- If /CS is set to HIGH while the 8 bits from D7 to D0 are entered, the data concerned is invalidated. Before entering succeeding sets of data, you must correctly input the data concerned again.
- In order to avoid data transfer error due to incoming noise, it is recommended to set /CS at HIGH on byte basis to initialize the serial-to-parallel conversion counter and the register.
- When executing the command RAMWR, set /CS to HIGH after writing the last address (after starting the 9th pulse in case of 9-bit serial input or after starting the 8th pulse in case of 8-bit serial input).

7.2 ACCESS TO DDRAM AND INTERNAL REGISTERS

ST7636 realizes high-speed data transfer because the access from MPU is a sort of pipeline processing done via the bus holder attached to the internal, requiring the cycle time alone without needing the wait time.

For example, when MPU writes data to the DDRAM, the data is once held by the bus holder and then written to the DDRAM before the succeeding write cycle is started. When MPU reads data from the DDRAM, the first read cycle is dummy and the bus holder holds the data read in the dummy cycle, and then it read from the bus holder to the system bus in the succeeding read cycle. Figure 7.2.1 illustrates these relations.

In 80-series interface mode:



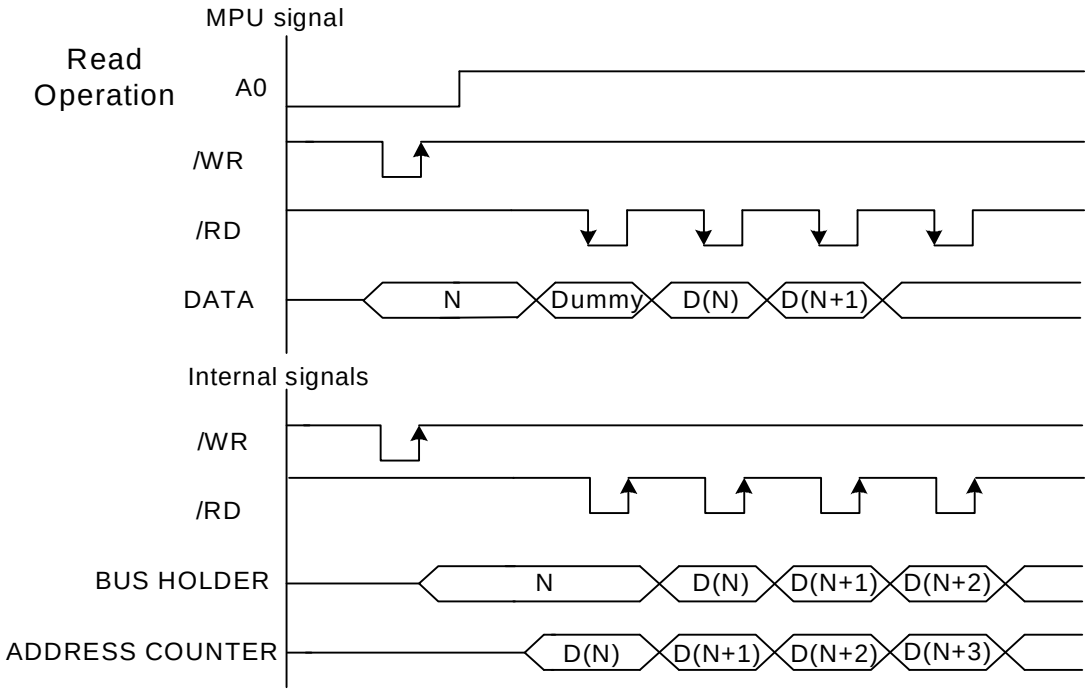


Figure 7.2.1

7.3 DISPLAY DATA RAM (DDRAM)

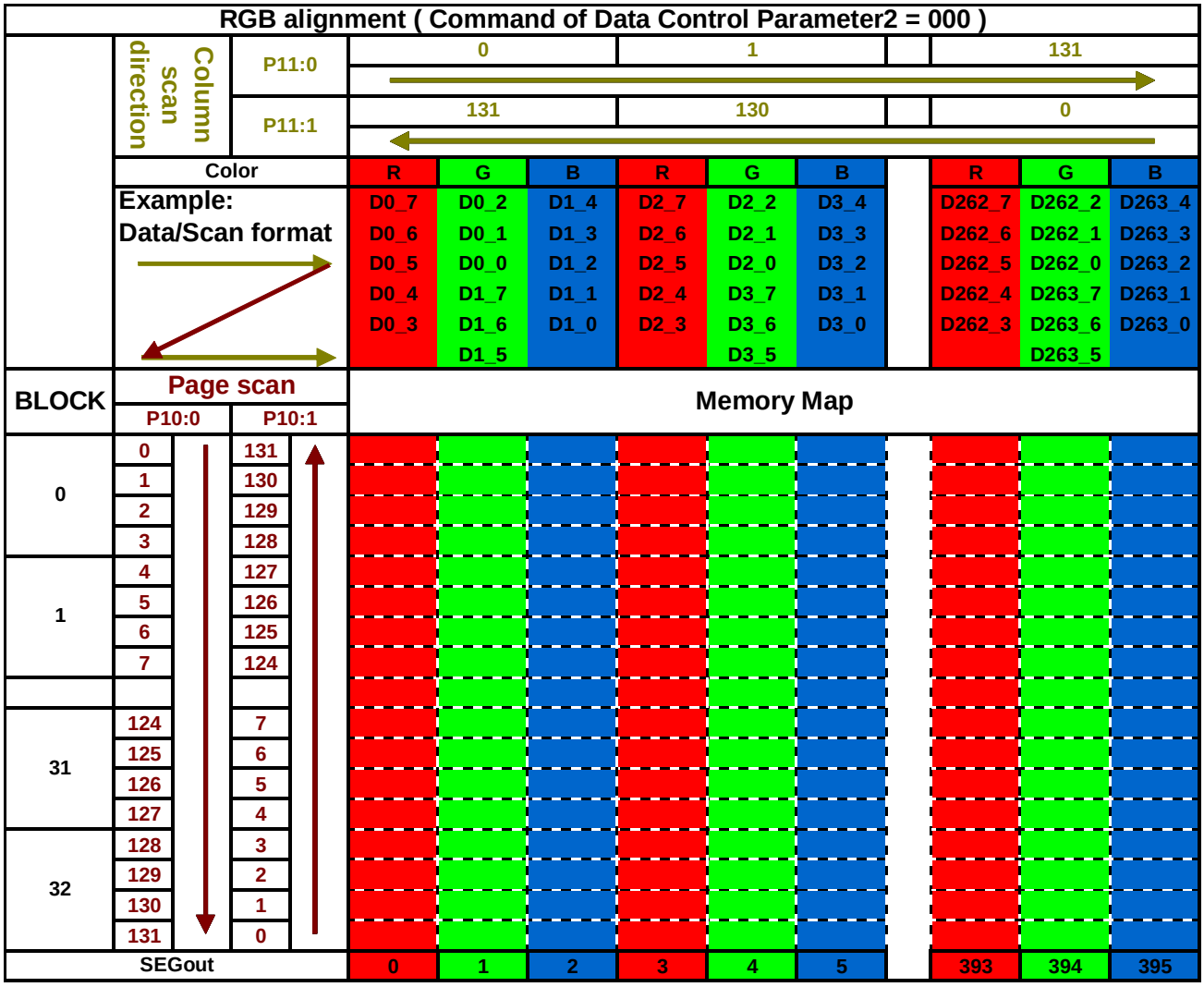
7.3.1 DDRAM

It is 132 X 132 X 16 bits capacity RAM prepared for storing dot data. You can access a desired bit by specifying the page address and column address. Since display data from MCU D7 to D0 and D15 to D8 correspond to one or two pixels of RGB, data transfer related restrictions are reduced, realizing the display flexing.

The RAM on ST7636 is separated to a block per 4 lines to allow the display system to process data on the block basis.

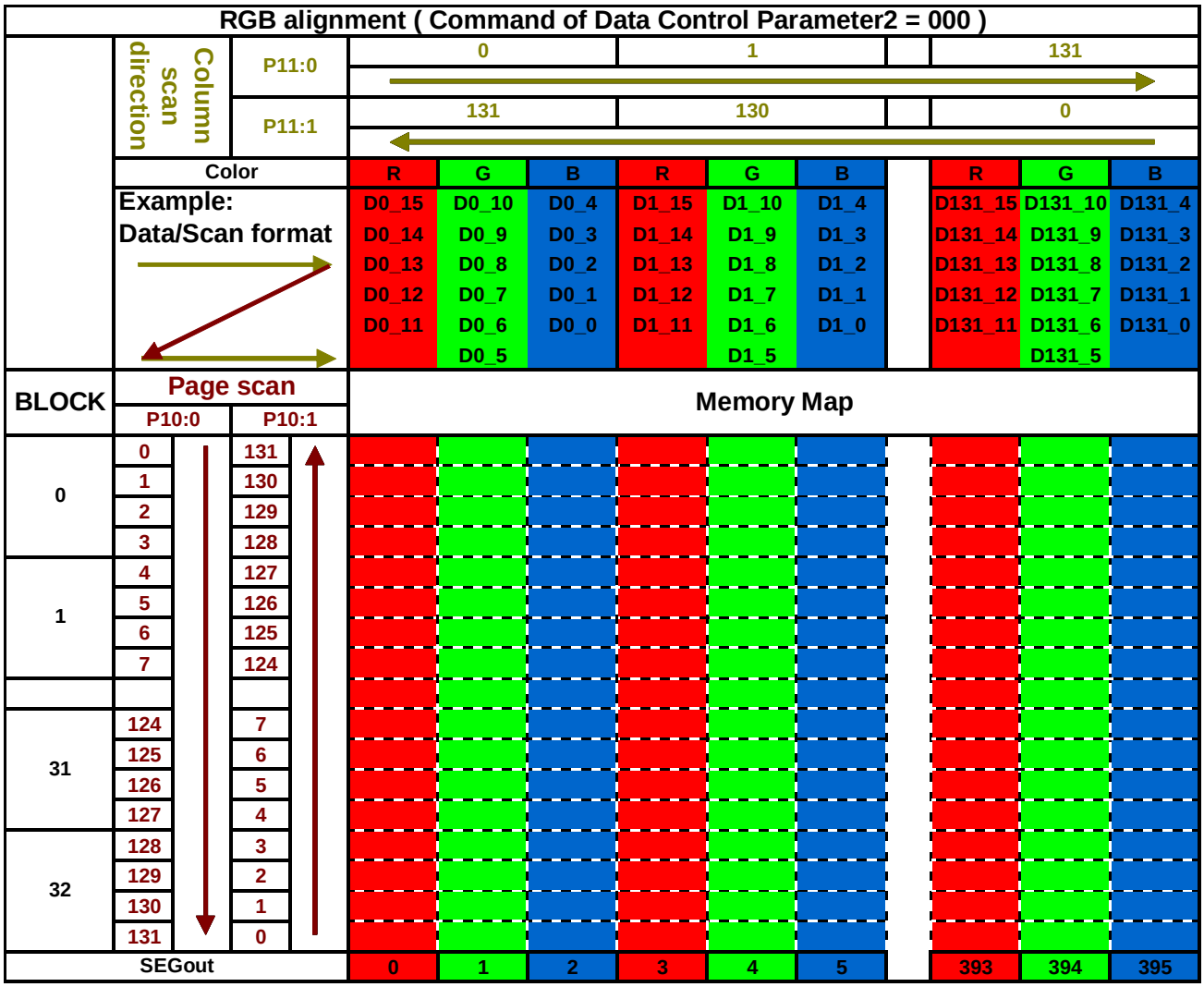
MPU's read and write operations to and from the RAM are performed via the I/O buffer circuit; Reading of the RAM for the liquid crystal drive is controlled from another separate circuit. Refer to the following memory map for the RAM configuration.

Memory Map (When using the 65Kcolor. 8-bit mode,)



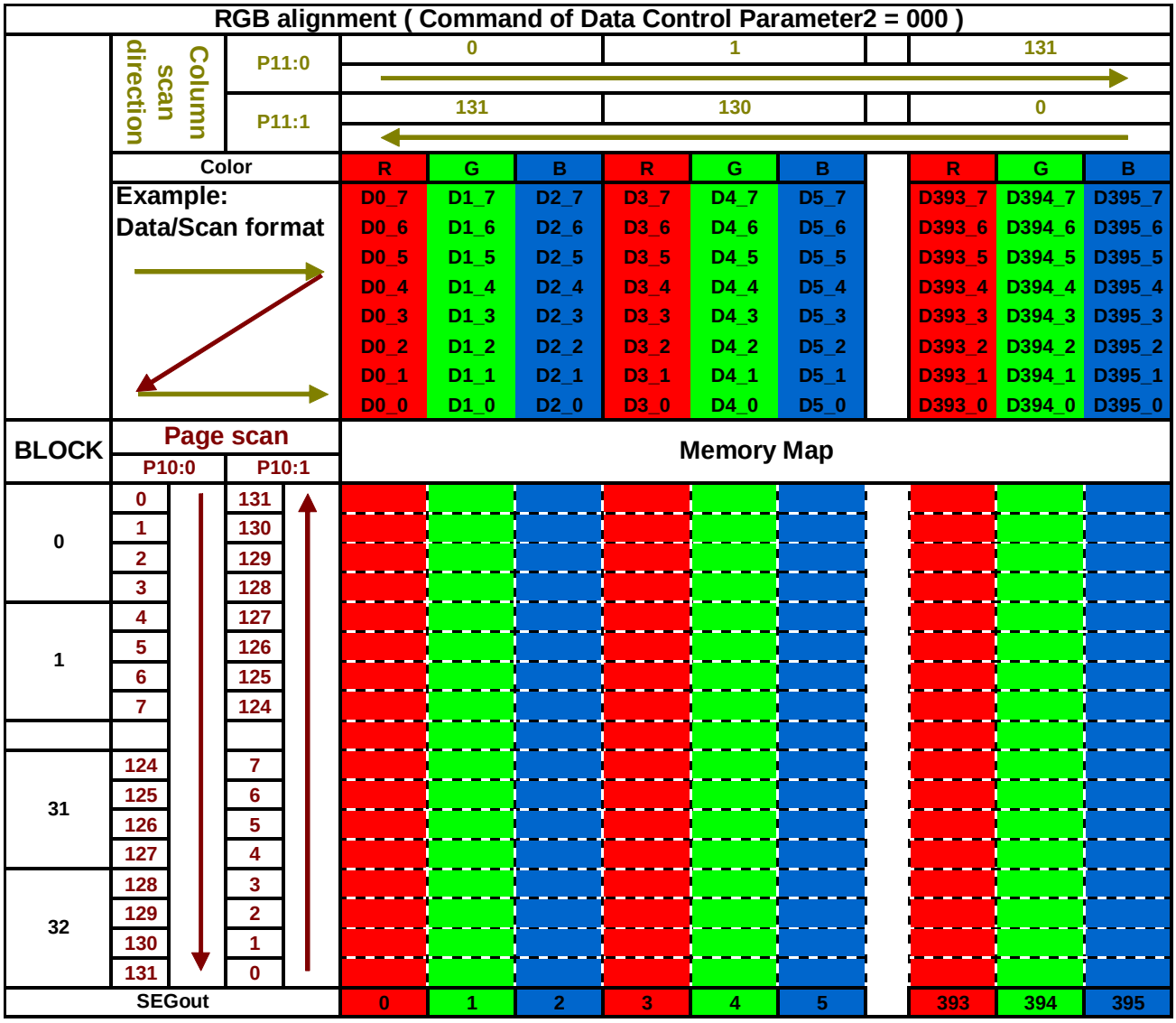
You can change position of R and B with DATACTL command.

Memory Map (When using the 65K color. 16-bit mode)



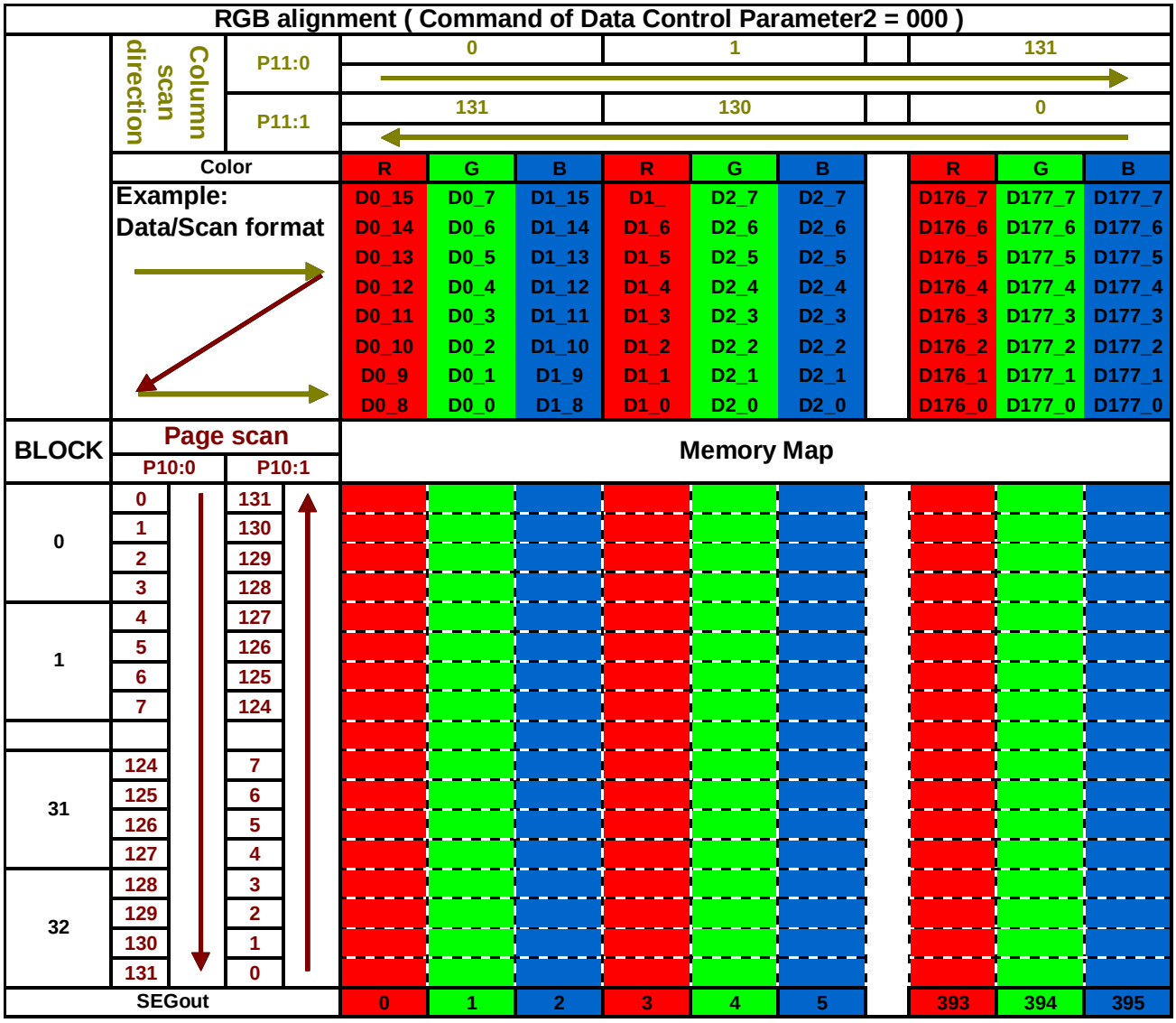
You can change position of R and B with DATACTL command.

Memory Map (When using the 262K/16Mcolor. 8-bit mode,)



You can change position of R and B with DATACTL command.

Memory Map (When using the 16 gray-scale, 262K/16M color. 16-bit mode)



You can change position of R and B with DATACTL command.

7.3.2 Page Address Control Circuit

This circuit is used to control the address in the page direction when MPU accesses the DDRAM or when reading the DDRAM to display image on the LCD.

You can specify a scope of the page address with page address set command. When the page-direction scan is specified with DATACTL command and the address are incremented from the start up to the end page, the column address is incremented by 1 and the page address returns to start page.

The DDRAM supports up to 132 lines, and thus the total page becomes 132.

In the read operation, as the end page is reached, the column address is automatically incremented by 1 and the page address is returned to start page.

Using the address normal/inverse parameter of DATACTL command allows you to inverse the correspondence between the DDRAM address and command output.

7.3.3 Column Address Control Circuit

This circuit is used to control the address in the column direction when MPU accesses the DDRAM. You can specify a scope of the column address using column address set command. When the column-direction scan is specified with DATACTL command and the address are incremented from the start up to the end page, the page address is incremented by 1 and the column address returns to start column.

In the read operation, too, the column address is automatically incremented by 1 and returned to start page as the end column is reached.

Just like the page address control circuit, using the column address normal/inverse parameter of DATACTL command enables to inverse the correspondence between the DDRAM column address and segment output. This arrangement relaxes restrictions in the chip layout on the LCD module.

7.3.4 I/O Buffer Circuit

It is the bi-directional buffer used when MPU reads or writes the DDRAM. Since MPU's read or write of DDRAM is performed independently from data output to the display data latch circuit, asynchronous access to the DDRAM when the LCD is turned on does not cause troubles such as flicking of the display images.

7.3.5 Block Address Circuit

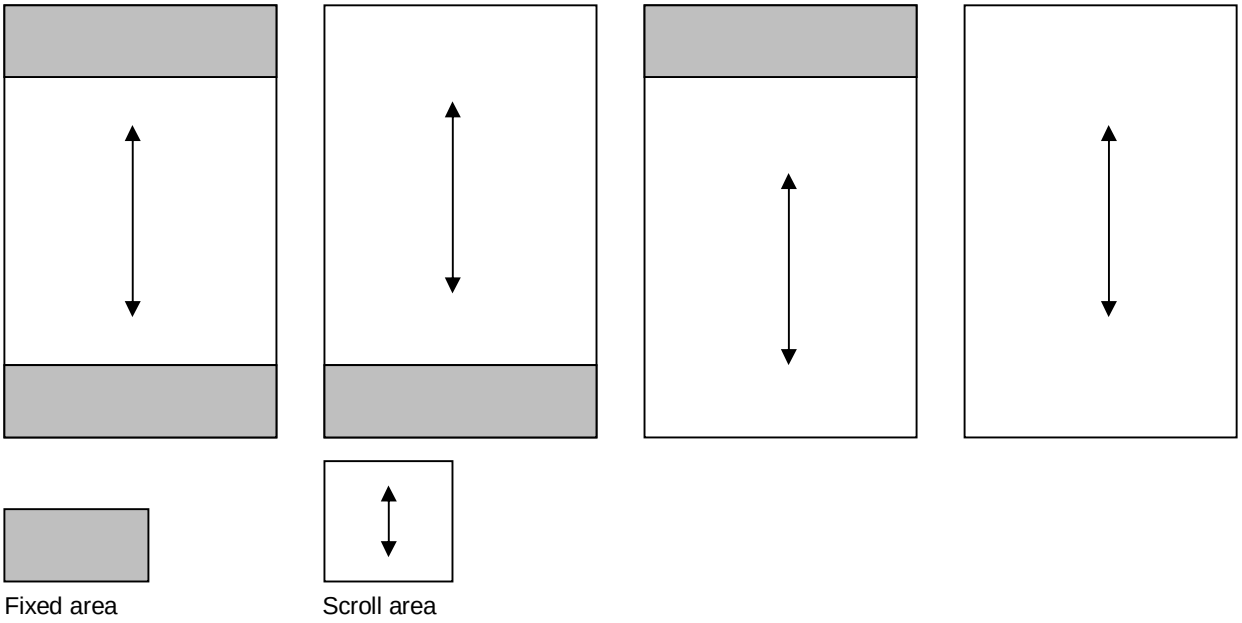
The circuit associates pages on DDRAM with COM output. ST7636 processes signals for the liquid crystal display on 4-page basis. Thus, when specifying a specific area in the area scroll display or partial display, you must designate it in block.

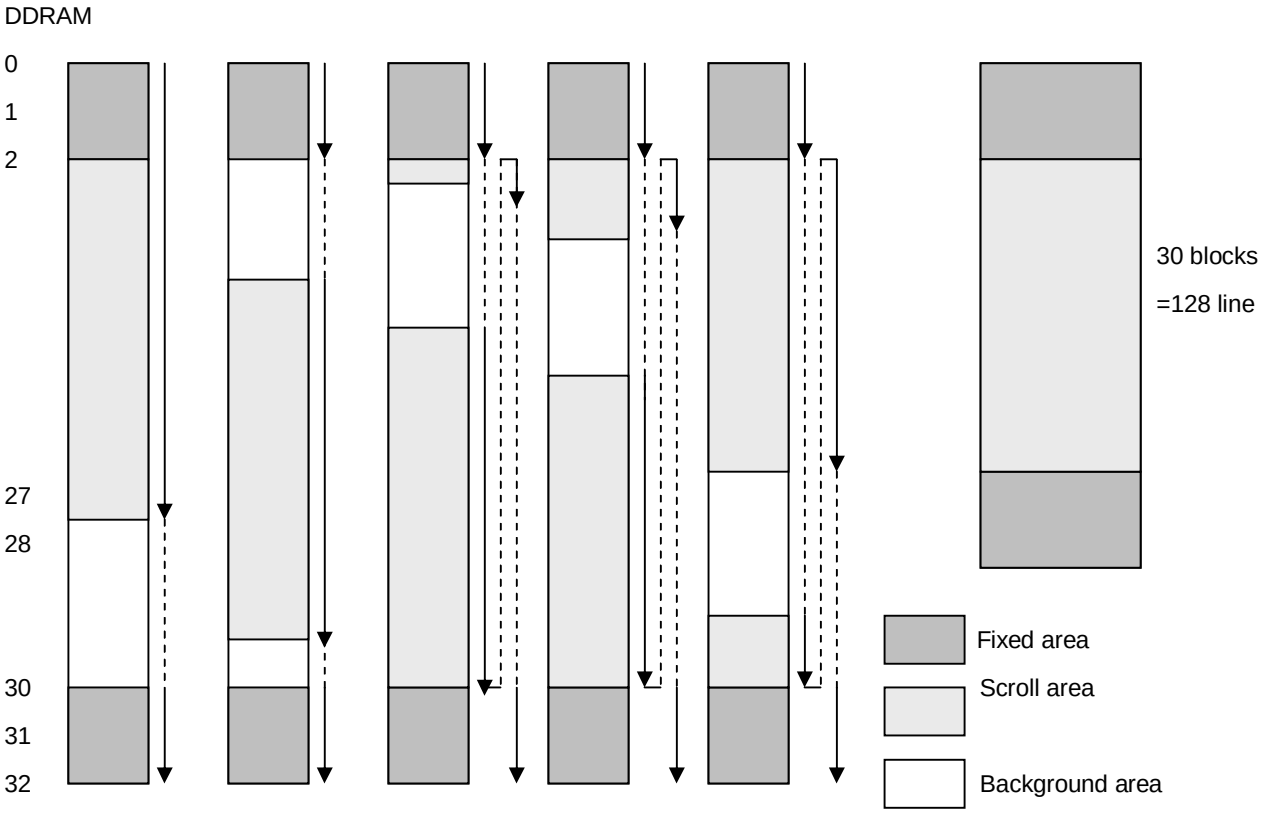
7.3.6 Display data Latch Circuit

This circuit is used to temporarily hold display data to be output from the DDRAM to the SEG decoder circuit. Since display normal/inverse and display on/off commands are used to control data in the latch circuit alone, they do not modify data in the DDRAM.

7.4 Area Scroll Display

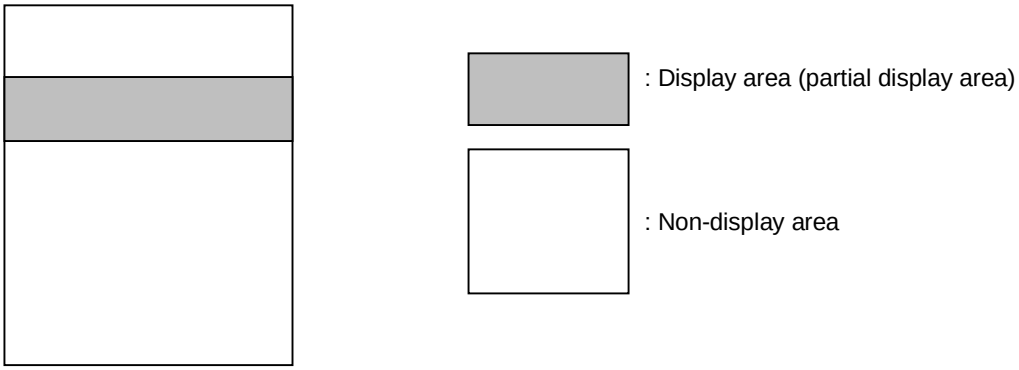
Using area scroll set and scroll start set commands allows you to scroll the display screen partially. You can select any one of the following four scroll patterns.





7.5 Partial Display

Using partial in command allows you turn on the partial display (division by line) of the screen. This mode requires less current consumption than the whole screen display, making it suitable for the equipment in the standby state.



If the partial display region is out of the Max. Display range, it would be no operation

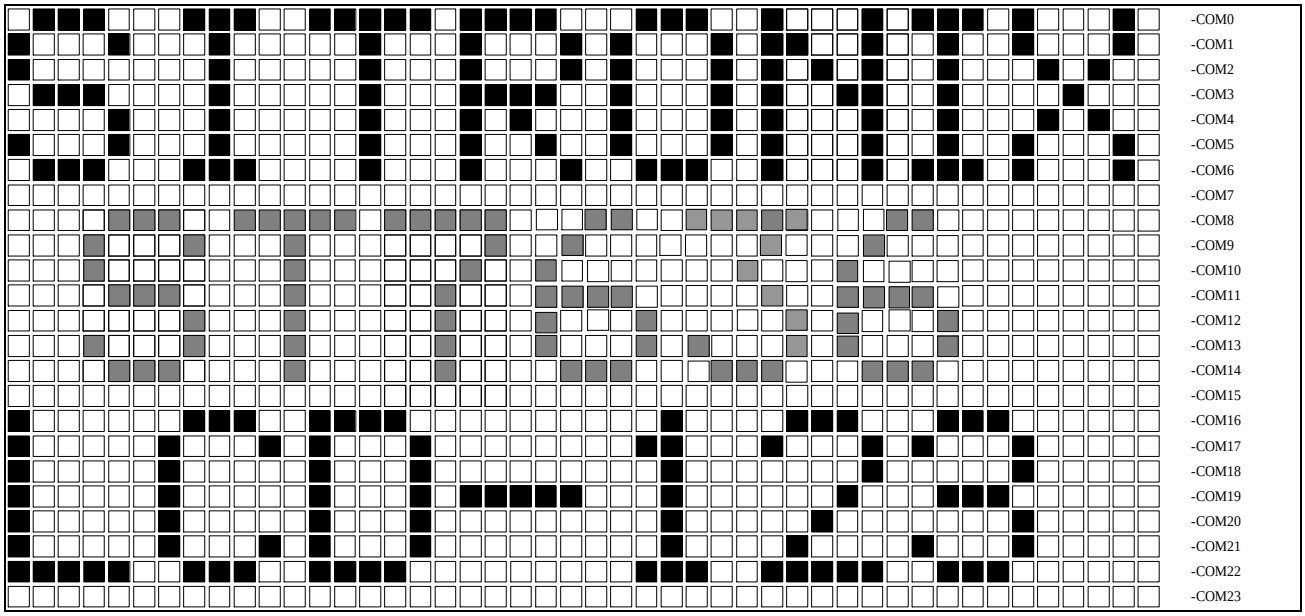


Figure 7.5.1 Reference Example for Partial Display

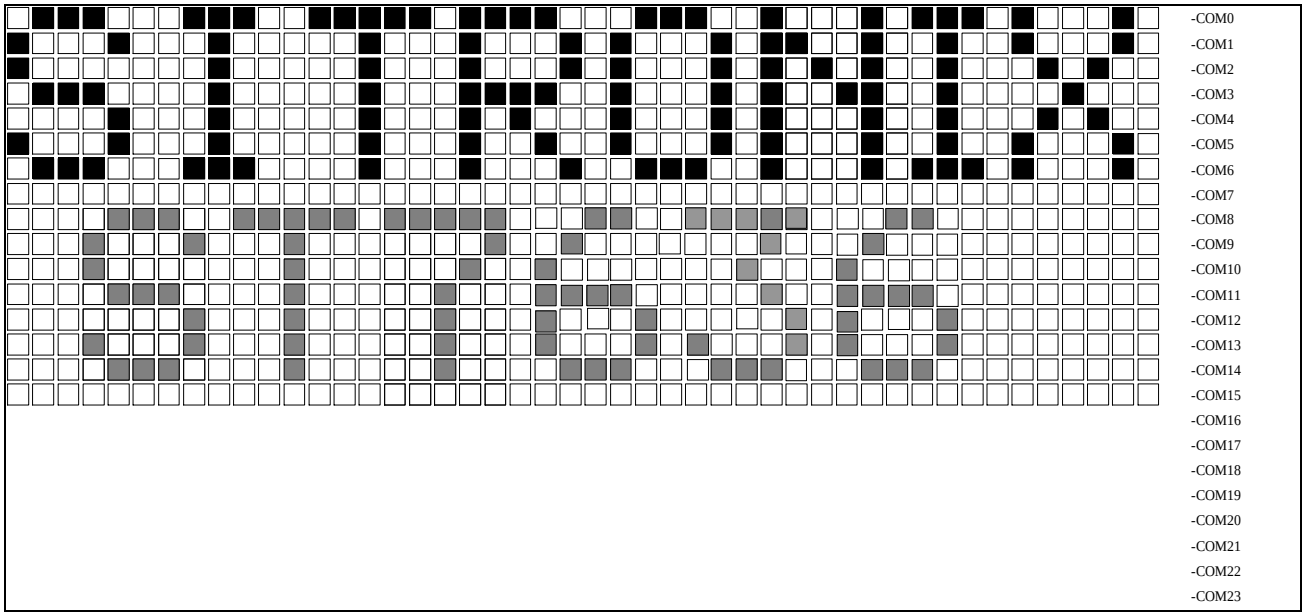


Figure 7.5.2 Partial Display (Partial Display Duty=16,initial COM0=0)

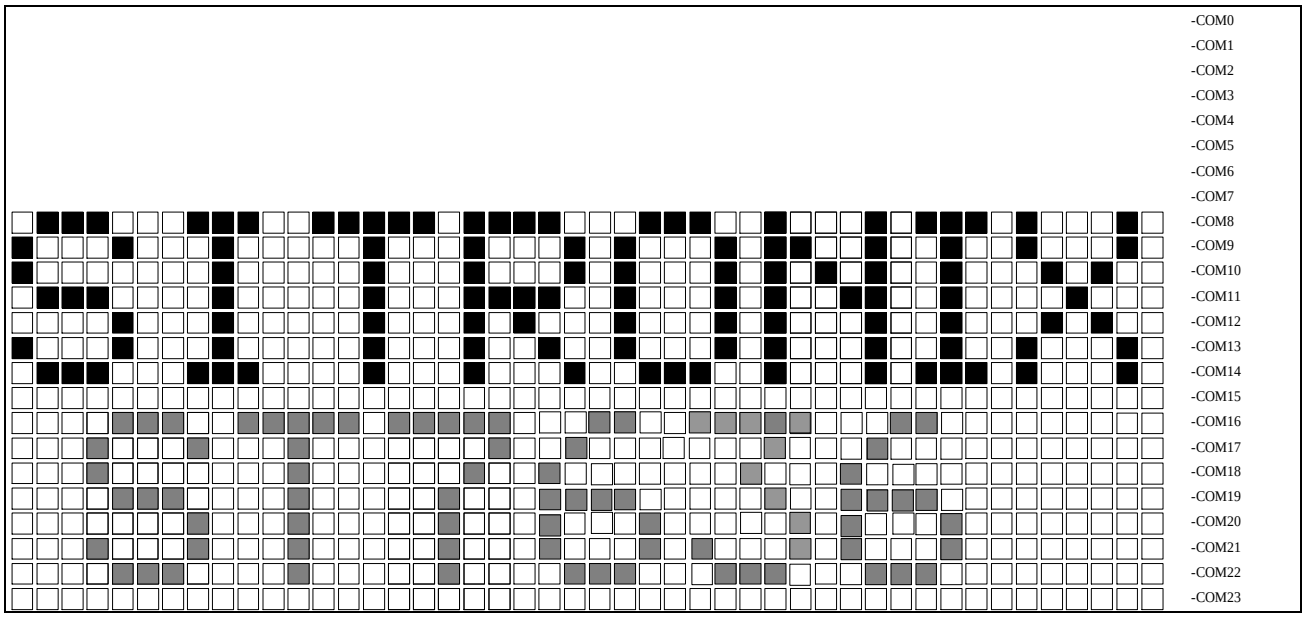


Figure 7.5.3 Moving Display (Partial Display Duty=16,Initial COM0=8)

7.6 Gary-Scale Display

ST7636 incorporates a 4FRC & 31 PWM function circuit to display a 64 gray-scale display.

7.7 Oscillation circuit

This is on-chip Oscillator without external resistor. When the internal oscillator is used, CLS must connect to VDD; when the external oscillator is used, CL could be input pin. This oscillator signal is used in the voltage converter and display timing generation circuit.

7.8 Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL (internal), generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 132-bit display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M), which enables the LCD driver to make an AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Figure 7.8.1.

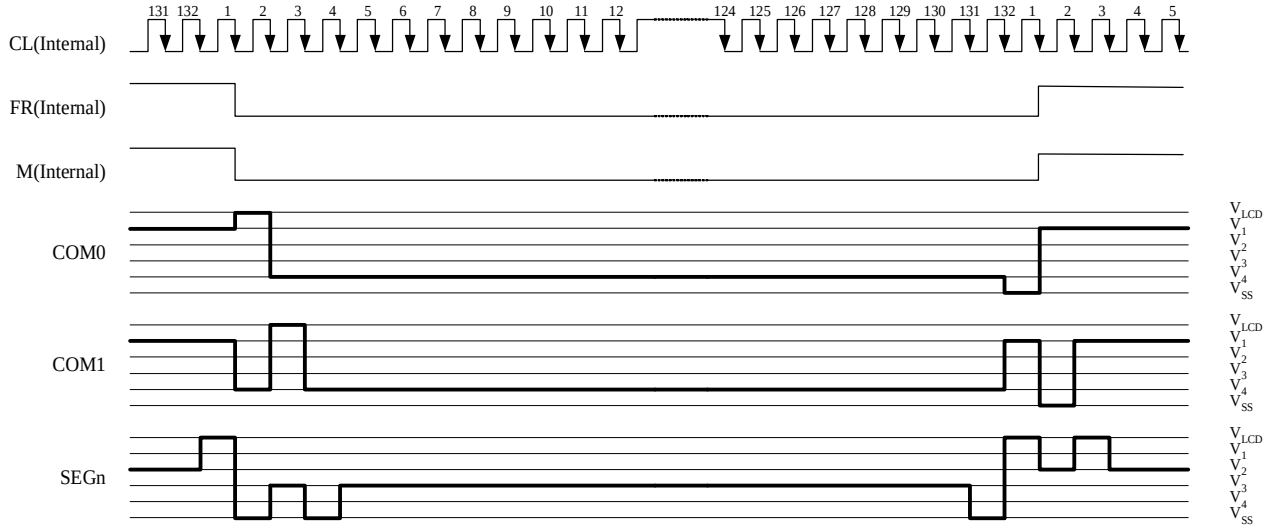


Figure 7.8.1 2-frame AC Driving Waveform (Duty Ratio: 1/132)

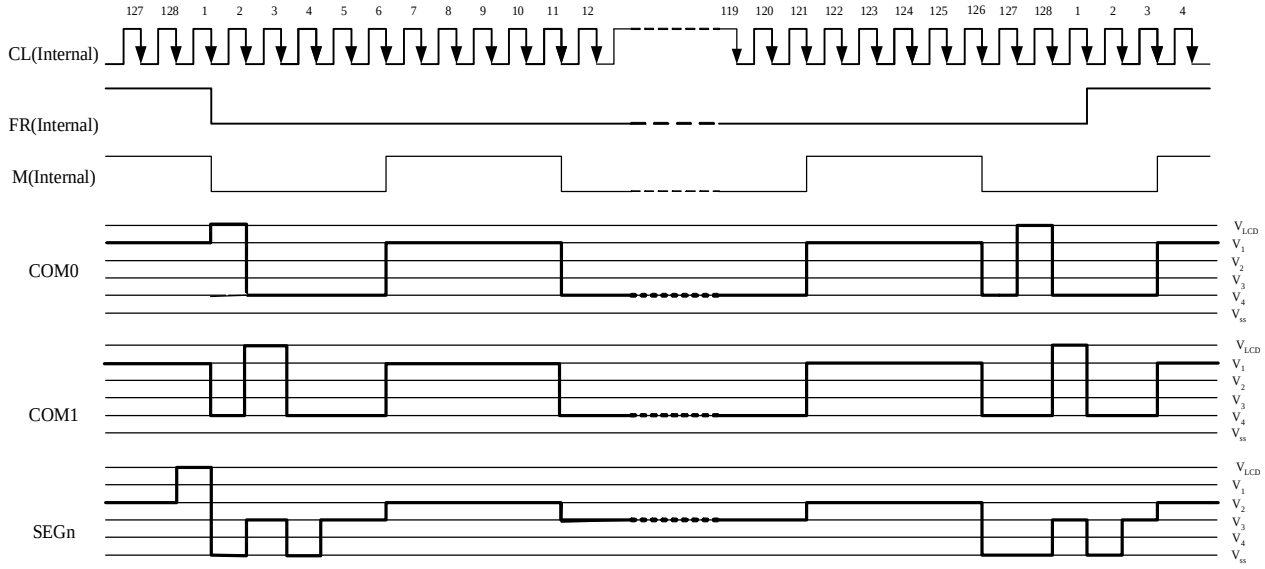
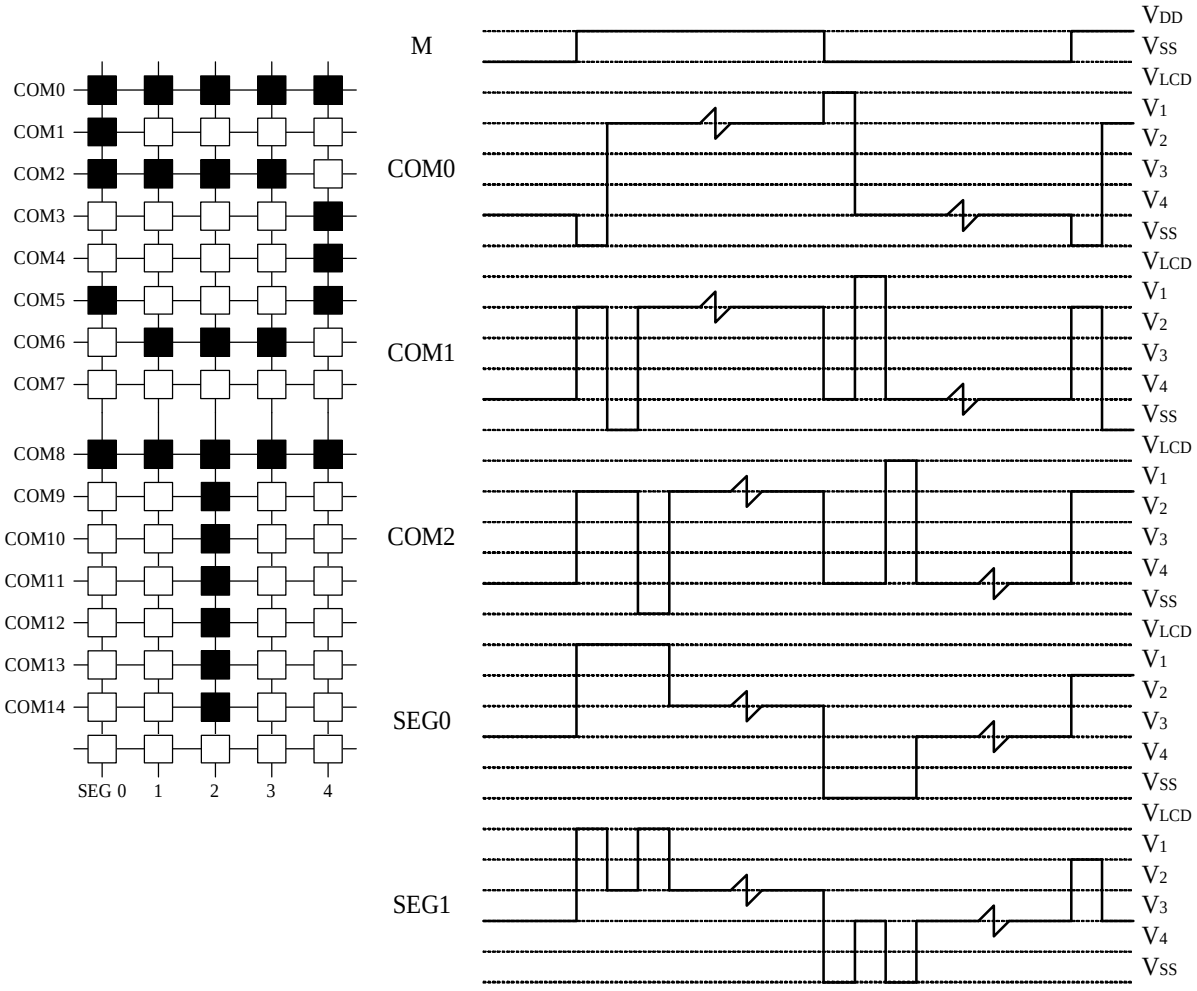


Figure 7.8.2 N-Line Inversion Driving Waveform (N=5,Duty Ratio=1/128)

7.9 Liquid Crystal drive Circuit

This driver circuit is configured by 132-channel common drivers and 396-channel segment drivers. This LCD panel driver voltage depends on the combination of display data and M signal.



7.10 Liquid Crystal Driver Power Circuit

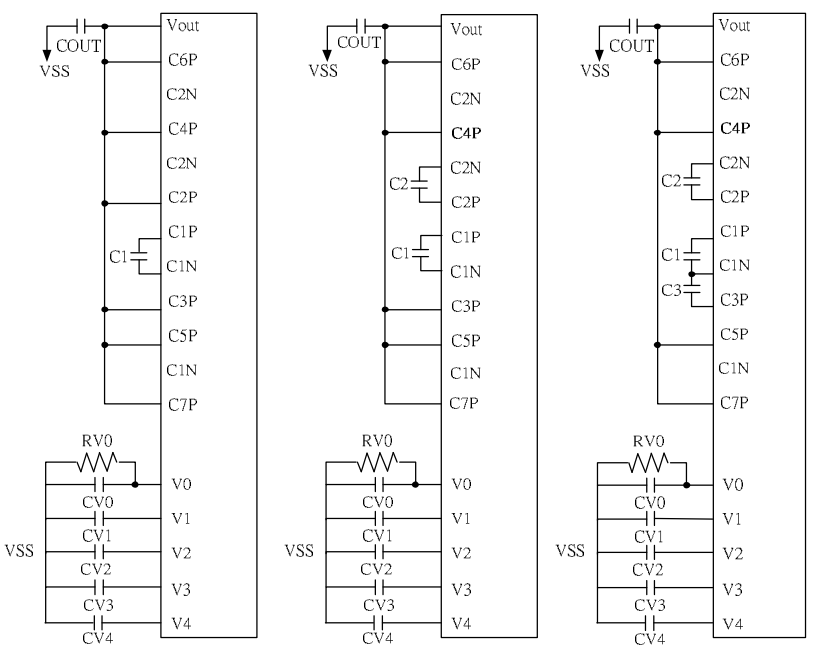
The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction. For details, refers to "Instruction Description". Table 7.10.1 shows the referenced combinations in using Power Supply circuits.

Table 7.10.1 Recommended Power Supply Combinations

User setup	Power control (VC VR VF)	V/C circuits	V/R circuits	V/F circuits	VOUT	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	ON	ON	ON	To series a capacitor to GND	To series a capacitor and a resister in parallel to GND	To series a capacitor to GND
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	OFF	ON	ON	External input	To series a capacitor and a resister in parallel to GND	To series a capacitor to GND
Only the voltage follower circuits are used	0 0 1	OFF	OFF	ON	Open	External input	To series a capacitor to GND
Only the external power supply circuits are used	0 0 0	OFF	OFF	OFF	Open	External input	External input

7.10.1 Voltage Converter Circuits

The Step-up Voltage Circuits

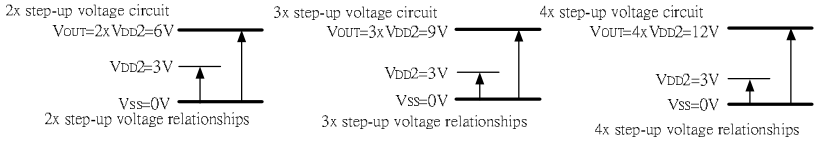


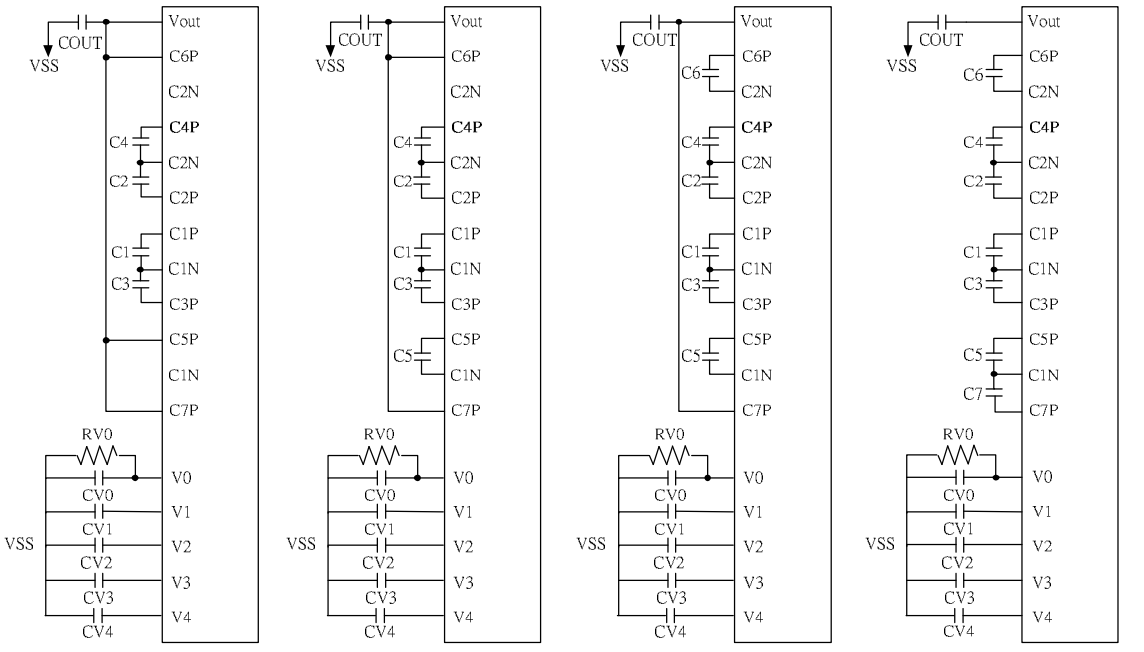
The critical operating voltage of capacitor is determined by following calculations.

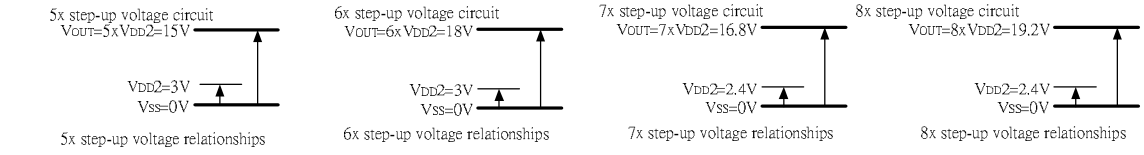
Booster capacitors:
C1 > VDD2 X 1
C2 > VDD2 X 2
C3 > VDD2 X 3
C4 > VDD2 X 4
C5 > VDD2 X 5
C6 > VDD2 X 6
C7 > VDD2 X 7
COUT > VDD2 X Booster Step

Follower output capacitors:
CV0 > V0
CV1 > V0 X [(N-1)/N]
CV2 > V0 X [(N-2)/N]
CV3 > V0 X [2/N]
CV4 > V0 X [1/N]
note: N = VLCD Bias

RV0=1~3M Ohm







7.10.2 Voltage Regulator Circuits

SET VOP (SETVOP)

The set VOP function is used to program the optimum LCD supply voltage V0.

SETVOP

Reset state of Vop[8:0] is 257DEC = 13.88V.

The VOP value is programmed via the Vop[8:0] register.

V0=a+(Vop[8:6]Vop[5:0]) · b

Ex:Vop[5:0]=000001, Vop[8:6]=100

→ Vop [8:0]=100000001

→ 3.6+257x0.04=13.88

- a is a fixed constant value (see table 7.10.2).
- b is a fixed constant value (see table 7.10.2).
- Vop[8:0] is the programmed VOP value. The programming range for Vop[8:0] is 5 to 410 (19Ahex).
- Vop[5:0] is the set contrast value which can be set via the interface and is in two's complement format.(See command VOLUP & VOLDOWN)
-

Table 7.10.2

SYMBOL	VALUE	UNIT
a	3.6	V
b	0.04	V

The Vop[8:0] value must be in the VLCD programming range as given in Figure 7.10.2. Evaluating equation (1), values outside the programming range indicated in Figure 7.10.2 may result. Calculated values below 4 will be mapped to VOP[8:0] = 4, resulting VOP[8:0] values higher than 410 will be mapped to VOP[8:0] = 410.

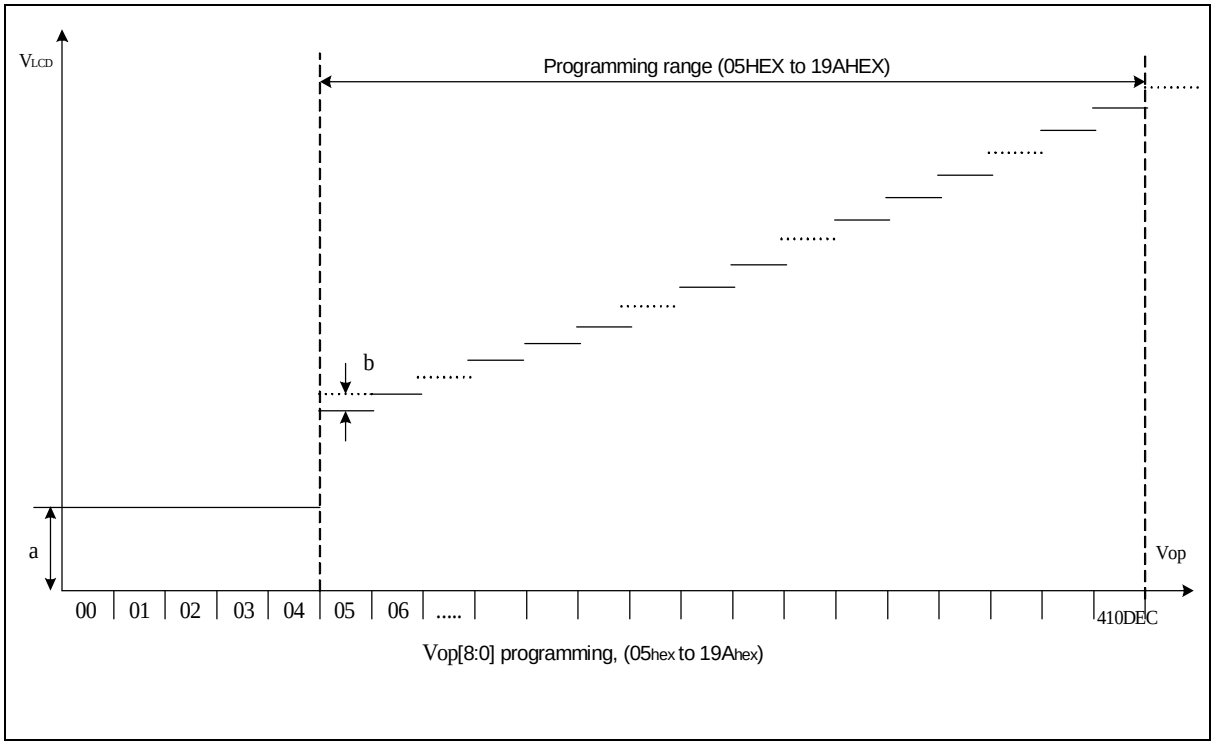


Figure 7.10.2 VLCD programming range

As the programming range for the internally generated V0 allows values above the max (18V). Allowed V0 (18V) the user has to ensure while setting the VPR register and selecting the temperature compensation, that under all conditions and including all tolerances the V0 remains below 18V.

Par no.	Equipment Type	Thermal Gradient
ST7636	Internal Power Supply	-0.136%(tolerance +/-10%)/^{0}C@ V0=14V, 25^{0}C or -19.6 mV/^{0}C

$$\textbf{Temperature Gradient Coefficient} = \frac{Vop(90^0C) - Vop(-30^0C)}{Vop(25^0C) * [90^0C - (-30^0C)]} \ (\%/^0C)$$

$$\textbf{Or} = \frac{Vop(90^0C) - Vop(-30^0C)}{[90^0C - (-30^0C)]} \ (mV/^0C)$$

7.10.3 EEPROM Setting Flow

EEPROM Setting Flow

The ST7636 provide the Write and Read function to write the Electronic Control value and Built-in resistance ratio into and read them from the built-in EEPROM. Using the Write and Read functions, you can store these values appropriate to each LCD panel. This function is very convenient for user in setting from some different panel's voltage. But using this function must attention the setting procedure. Please see the following diagram.

Note1: This setting flow is used for LCM assembler.

Note2: When writing value to EEPROM, the voltage of $VOUT_{IN}$ must be more than 17V.

Note3: To avoid some errors during IC operation, EEPROM shouldn't be written without preceding loading correctly from EEPROM.

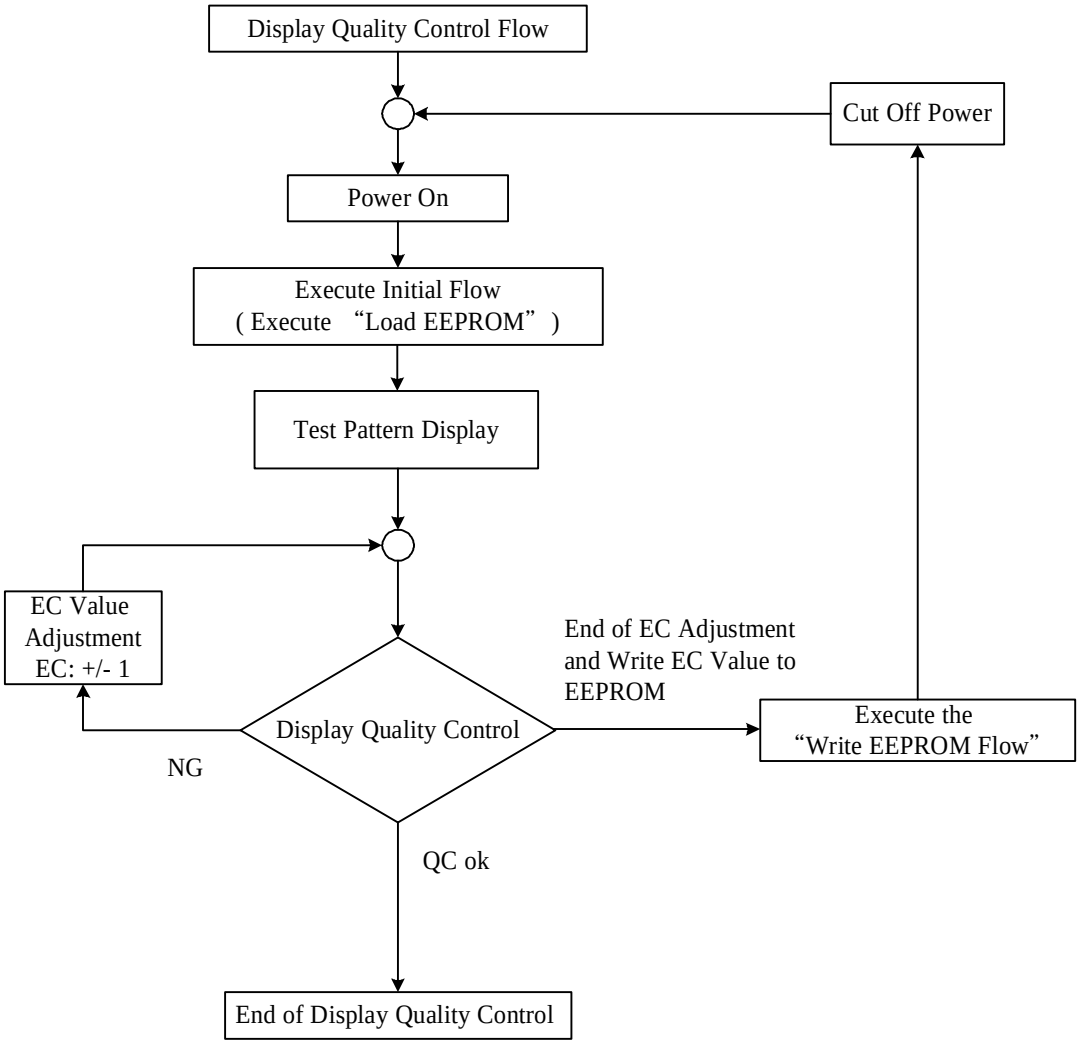


Figure 7.10.3.1 Flow of EC value adjustment for display quality control by writing EEPROM offset

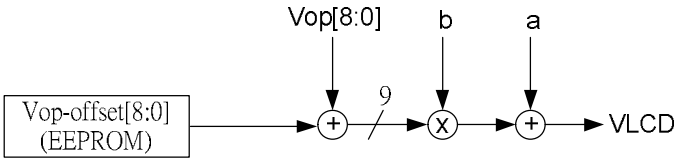


Figure 7.10.3.2 EC value control for different modules by loading EEPROM offset

Example：EEPROM Read Operation

```
void ReadEEPROM( void )
{
        Write( COMMAND, 0x0030 );           // Ext = 0
        Write( COMMAND, 0x0007 );           // EEPROM Function Start ( EEOK )
        Write( DATA, 0x0019 );              // EEPROM Function Parameter

        Write( COMMAND, 0x0030 );           // Ext = 0
        Write( COMMAND, 0x00d1 );           // Internal OSC on
        Write( COMMAND, 0x0020 );           // Power Control
        Write( DATA, 0x000b );              // B/F/R = On/On/On

        Write( COMMAND, 0x0031 );           // Ext = 1
        Write( COMMAND, 0x00cd );           // EEPROM ON
        Write( DATA, 0x0000 );              // Entry "Read Mode"
        Delay( 100ms );                     // Waite for EEPROM Operation ( 100ms )
        Write( COMMAND, 0x00fd );           // Start EEPROM Reading Operation
        Delay( 100ms );                     // Waite for EEPROM Operation ( 100ms )
        Write( COMMAND, 0x00cc );           // Exist EEPORM Mode step.1
        Write( COMMAND, 0x0030 );           // Exist EEPORM Mode step.2
}
```

Example：EEPROM Write Operation

```
void WriteEEPROM( void )
{
        Write( COMMAND, 0x0030 );           // Ext = 0
        Write( COMMAND, 0x00AE );           // Display off
        Write( COMMAND, 0x0007 );           // EEPROM Function Start ( EEOK )
        Write( DATA, 0x0019 );              // EEPROM Function Parameter

        Write( COMMAND, 0x0030 );           // Ext = 0
        Write( COMMAND, 0x00d1 );           // Internal OSC on
        Write( COMMAND, 0x0020 );           // Power Control
        Write( DATA, 0x000b );              // B/F/R = On/On/On

        Write( COMMAND, 0x0031 );           // Ext = 1
        Write( COMMAND, 0x00cd );           // EEPROM ON
        Write( DATA, 0x0020 );              // Entry "Write Mode"
        Delay( 100ms );                     // Waite for EEPROM Operation ( 100ms )
        Write( COMMAND, 0x00fc );           // Start EEPROM Writing Operation
        Delay( 100ms );                     // Waite for EEPROM Operation ( 100ms )
        Write( COMMAND, 0x00cc );           // Exist EEPORM Mode step.1
        Write( COMMAND, 0x0030 );           // Exist EEPORM Mode step.2

        Write( COMMAND, 0x0030 );           // Ext = 0
        Write( COMMAND, 0x00AF );           // Display on
}
```

Example：EEPROM Load Operation

```
void LoadEEPROM( void )
{
        Write( COMMAND, 0x0030 );           // Ext = 0
        Write( COMMAND, 0x0007 );           // EEPROM Function Start ( EEOK )
        Write( DATA, 0x0019 );              // EEPROM Function Parameter

        Write( COMMAND, 0x0031 );           // Ext = 1
        Write( COMMAND, 0x00cd );           // EEPROM ON
        Write( DATA, 0x0000 );              // Entry "Read Mode"
        Delay( 100ms );                     // Waite for EEPROM Operation ( 100ms )
        Write( COMMAND, 0x00fd );           // Start EEPROM Reading Operation
        Delay( 100ms );                     // Waite for EEPROM Operation ( 100ms )
        Write( COMMAND, 0x00cc );           // Exit EEPORM Mode step.1
        Write( COMMAND, 0x0030 );           // Exit EEPORM Mode step.2
```

}

RESET CIRCUIT

When Power is Turned On

Input power (VDD1~VDD5)

↓

Be sure to apply POWER-ON RESET (RESET=LOW)

↓

< Display Setting 1 >

Display control (DISCTL)

Setting clock dividing ratio : **<< State after reset >>**

Duty setting :

Setting reverse rotation number of line : **2 divisions**

Common scan direction (COMSCN) **1/4**

Setting scan direction : **11H reverse rotations**

Oscillation on (OSCON) :

↓ **COM0 à COM65, COM66 à COM131**

Sleep-out (SLIPOUT) : **Oscillation off**

↓

< Power Supply Setting > **Sleep-in**

Electronic volume control (VOLCTR)

Setting volume value : **<< State after reset >>**

Setting built-in resistance value :

Power control (PWRCTR) **0**

Setting operation of power supply circuit : **0 (3.76)**

↓

< Display Setting 2 > **ALL OFF**

Normal rotation of display (DISNOR) / inversion of display (DISINV) :

Partial-in (PTLIN) / Partial-out (PLOUT) **<< State after reset >>**

Setting fix area : **Normal rotation of display**

Area scroll set (ASCSET)

Setting area scroll region : **Partial-out**

Setting area scroll type :

Scroll start set (SCSTART) **0**

Setting scroll start address : **Full-screen scroll**

↓

< Display Setting 3 > **0**

Data control (DATCTL)

Setting normal radiation / inversion of page address : **<< State after reset >>**

Setting normal radiation / inversion of column address :

Normal rotation	
Normal rotation	**Column direction**
Setting direction of address scanner :	**RGB**
Setting RGB arrangement :	**65K**
Setting gradation :	
65K-color position set (RGBSET8)	**All 0**
Setting color position at 65K-color :	
↓	**<< State after reset >>**
< RAM Setting >	
Page address set (PASET)	**0**
Setting start page address :	**0**
Setting end page address :	
Column address set (PASET)	**0**
Setting start column address :	**0**
Setting end column address :	
↓	**<< State after reset >>**
< RAM Write >	
Memory write command (RAMWR)	
Writing displayed data : repeat as many as the number needed and exit by entering other command.	
↓	
< Waiting (approximately 100ms) >	
Wait until the power supply voltage has stabilized. Enter the power supply control command first, then wait at least 100ms before entering the Display ON command when the built-in power supply circuit operates. If you do not wait, an unwanted display may appear on the liquid crystal panel.	
↓	**Display off**
Display on (DISON) :	

(Note) If changes are unnecessary after reset, command input is unnecessary.

8. COMMANDS

8.1 Command table

Ext=0															
Command	***A0***	***RD***	***WR***	***D7***	***D6***	***D5***	***D4***	***D3***	***D2***	***D1***	***D0***	***Function***	***Hex***	***Parameter***	***Index***
DISON	0	1	0	1	0	1	0	1	1	1	1	Display On	AF	None	1
DISOFF	0	1	0	1	0	1	0	1	1	1	0	Display Off	AE	None	2
DISNOR	0	1	0	1	0	1	0	0	1	1	0	Normal Display	A6	None	3
DISINV	0	1	0	1	0	1	0	0	1	1	1	Inverse Display	A7	None	4
COMSCN	0	1	0	1	0	1	1	1	0	1	1	Com Scan Direction	BB	1 byte	5
DISCTR	0	1	0	1	1	0	0	1	0	1	0	Display Control	CA	3 byte	6
SLPP	0	1	0	0	0	0	0	0	1	0	0	Sleep In/Out Preparation	04	1 byte	7
SLPIN	0	1	0	1	0	0	1	0	1	0	1	Sleep In	95	None	8
SLPOUT	0	1	0	1	0	0	1	0	1	0	0	Sleep Out	94	None	9
PASET	0	1	0	0	1	1	1	0	1	0	1	Page Address Set	75	2 byte	10
CASET	0	1	0	0	0	0	1	0	1	0	1	Column Address Set	15	2 byte	11
DATCTL	0	1	0	1	0	1	1	1	1	0	0	Data Scan Direction	BC	3 byte	12
RAMWR	0	1	0	0	1	0	1	1	1	0	0	Writing to Memory	5C	Data	13
RAMRD	0	1	0	0	1	0	1	1	1	0	1	Reading from Memory	5D	Data	14
PLTIN	0	1	0	1	0	1	0	1	0	0	0	Partial display in	A8	2 byte	15
PLTOUT	0	1	0	1	0	1	0	1	0	0	1	Partial display out	A9	None	16
RMWIN	0	1	0	1	1	1	0	0	0	0	0	Read Modify Write In	E0	None	17
RMWOUT	0	1	0	1	1	1	0	1	1	1	0	Read Modify Write Out	EE	None	18
ASCSET	0	1	0	1	0	1	0	1	0	1	0	Area Scroll Set	AA	4 byte	19
SCSTART	0	1	0	1	0	1	0	1	0	1	1	Scroll Start Set	AB	1 byte	20
OSCON	0	1	0	1	1	0	1	0	0	0	1	Internal OSC on	D1	None	21
OSCOFF	0	1	0	1	1	0	1	0	0	1	0	Internal OSC off	D2	None	22
PWRCTL	0	1	0	0	0	1	0	0	0	0	0	Power Control	20	1 byte	23
VOLCTR	0	1	0	1	0	0	0	0	0	0	1	EC control	81	2 byte	24
VOLUP	0	1	0	1	1	0	1	0	1	1	0	EC increase 1	D6	None	25
VOLDOWN	0	1	0	1	1	0	1	0	1	1	1	EC decrease 1	D7	None	26
STREAD	0	0	1	Status Read								Status Read			27
EPSRRD1	0	1	0	0	1	1	1	1	1	0	0	READ Register1	7C	None	28
EPSRRD2	0	1	0	0	1	1	1	1	1	0	1	READ Register2	7D	None	29
NOP	0	1	0	0	0	1	0	0	1	0	1	NOP Instruction	25	None	30
EEOK	0	1	0	0	0	0	0	0	1	1	1	EEPROM Function Start	07	1 byte	31
RESERVED	0	1	0	1	0	0	0	0	0	1	0	Not Use	82		32

Ext=1															
Command	***A0***	***RD***	***WR***	***D7***	***D6***	***D5***	***D4***	***D3***	***D2***	***D1***	***D0***	***Function***	***Hex***	***Parameter***	***Index***
Red1 Set	0	1	0	0	0	1	0	0	0	0	0	FRAME 1 Red PWM Set	20	16 byte	1
Red2 Set	0	1	0	0	0	1	0	0	0	0	1	FRAME 2 Red PWM Set	21	16 byte	2
Red3 Set	0	1	0	0	0	1	0	0	0	1	0	FRAME 3 Red PWM Set	22	16 byte	3
Red4 Set	0	1	0	0	0	1	0	0	0	1	1	FRAME 4 Red PWM Set	23	16 byte	4
Grn1 Set	0	1	0	0	0	1	0	0	1	0	0	FRAME 1 Green PWM Set	24	16 byte	5
Grn2 Set	0	1	0	0	0	1	0	0	1	0	1	FRAME 2 Green PWM Set	25	16 byte	6
Grn3 Set	0	1	0	0	0	1	0	0	1	1	0	FRAME 3 Green PWM Set	26	16 byte	7
Grn4 Set	0	1	0	0	0	1	0	0	1	1	1	FRAME 4 Green PWM Set	27	16 byte	8
Blu1 Set	0	1	0	0	0	1	0	1	0	0	0	FRAME 1 Blue PWM Set	28	16 byte	9
Blu2 Set	0	1	0	0	0	1	0	1	0	0	1	FRAME 2 Blue PWM Set	29	16 byte	10
Blu3 Set	0	1	0	0	0	1	0	1	0	1	0	FRAME 3 Blue PWM Set	2A	16 byte	11
Blu4 Set	0	1	0	0	0	1	0	1	0	1	1	FRAME 4 Blue PWM Set	2B	16 byte	12
ANASET	0	1	0	0	0	1	1	0	0	1	0	Analog	32	3 byte	13
DITHOFF	0	1	0	0	0	1	1	0	1	0	0	Dithering Circuit Off	34	None	14
DITHON	0	1	0	0	0	1	1	0	1	0	1	Dithering Circuit On	35	None	15
EPCTIN	0	1	0	1	1	0	0	1	1	0	1	Control EEPROM	CD	1 byte	16
EPCOUT	0	1	0	1	1	0	0	1	1	0	0	Cancel EEPROM	CC	None	17
EPMWR	0	1	0	1	1	1	1	1	1	0	0	Write to EEPROM	FC	None	18
EPMRD	0	1	0	1	1	1	1	1	1	0	1	Read from EEPROM	FD	None	19

Ext=1 or Ext=0															
Command	***A0***	***RD***	***WR***	***D7***	***D6***	***D5***	***D4***	***D3***	***D2***	***D1***	***D0***	***Function***	***Hex***	***Parameter***	***Index***
Ext In	0	1	0	0	0	1	1	0	0	0	0	Ext=0 Set	30	None	--
Ext Out	0	1	0	0	0	1	1	0	0	0	1	Ext=1 Set	31	None	--

8.2 EXT="0" Function Description

(1) Display ON (DISON) Command: 1; Parameter: None (AFH)

It is used to turn the display on. When the display is turned on, segment outputs and common outputs are generated at the level corresponding to the display data and display timing. You can't turn on the display as long as the sleep mode is selected. Thus, whenever using this command, you must cancel the sleep mode first.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	1	1	1	1

(2) Display OFF (DISOFF) Command: 1; Parameter: None (AEH)

It is used to forcibly turn the display off. As long as the display is turned off, every on segment and common outputs are forced to VSS level.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	1	1	1	0

(3) Normal display (DISNOR) Command: 1; Parameter: None (A6H)

It is used to normally highlight the display area without modifying contents of the display data RAM.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	0	1	1	0

(4) Inverse display (DISINV) Command: 1; Parameter: None (A7)

It is used to inversely highlight the display area without modifying contents of the display data RAM. This command does not invert non-display areas in case of using partial display.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	0	1	1	1

(5) Common scan (COMSCAN) Command: 1; Parameter: 1 (BBH)

It is used to specify the common output direction in the pin of CSEL = L. This command helps increasing degrees of freedom of wiring on the LCD panel.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	1	1	0	1	1	–
Parameter1 (P1)	1	1	0	*	*	*	*	*	P12	P11	P10	Command Scan direction

When CSEL=0 configuration is selected, pins and common outputs are scanned in the order shown below.

P12	P11	P10	Common scan direction				
			COM0 pin		COM65 pin	COM66 pin	COM131 pin
0	0	0	0	**à**	65	66 **à**	131
0	0	1	0	**à**	65	131 **à**	66
0	1	0	65	**à**	0	66 **à**	131
0	1	1	65	**à**	0	131 **à**	66

Common scan direction

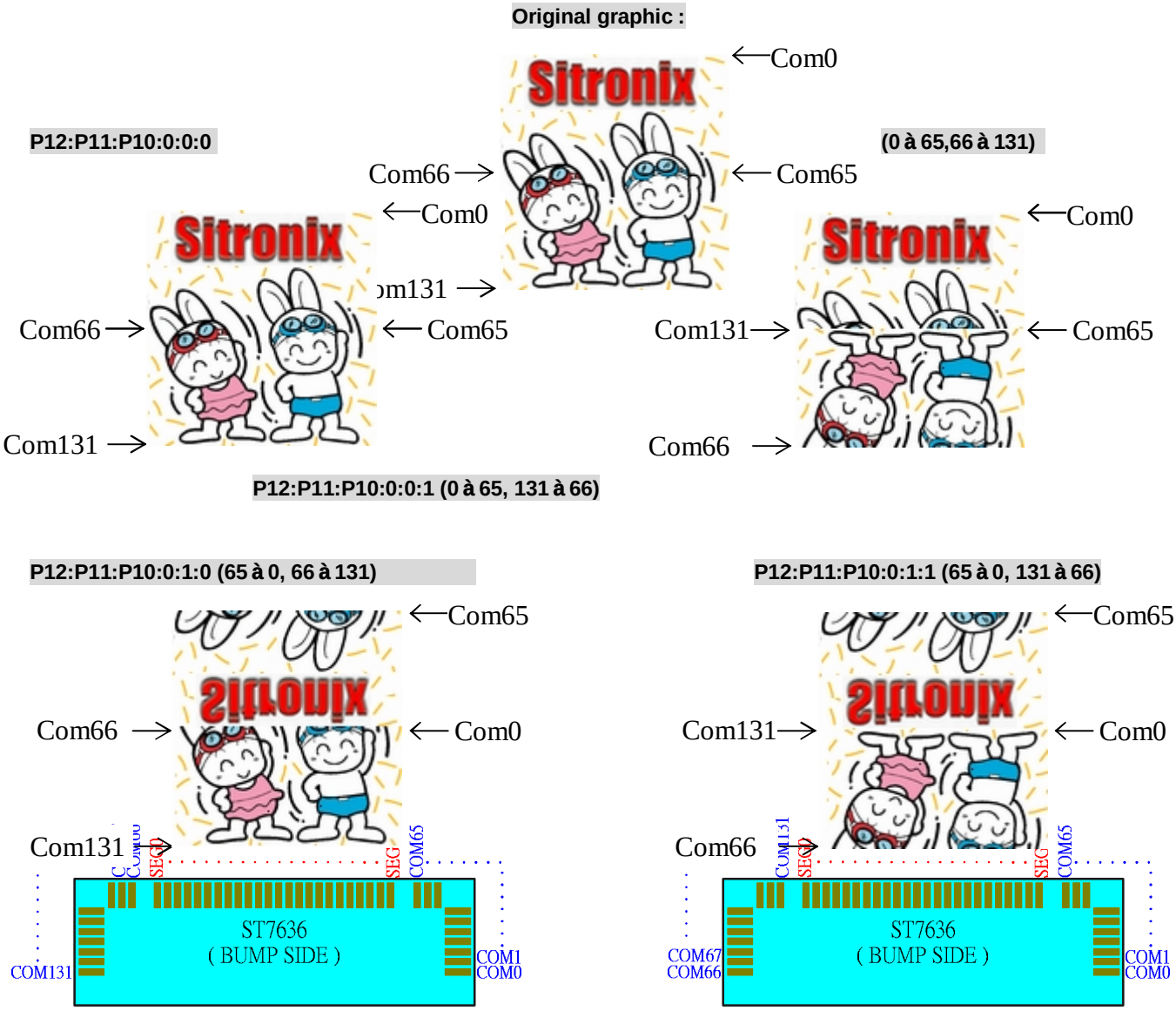


Figure 8.2.1 Common scan direction configuration when CSEL=0

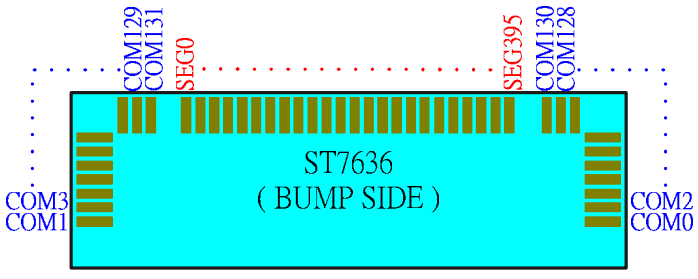


Figure 8.2.2 Common scan direction configuration when CSEL=1
Note : under CSEL=1 configuration, command #BBH will have no effect upon IC operation.

The common scan direction is fixed.

(6) Display control (DISCTL) Command: 1; Parameter: 3 (CAH)

This command and succeeding parameters are used to perform the display timing-related setups. This command must be selected before using SLPOUT. Don't change this command while the display is turned on.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	1	0	0	1	0	1	0	–
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	*	*	CL dividing ratio, F1 and F2 drive pattern.
Parameter2(P2)	1	1	0	*	*	P25	P24	P23	P22	P21	P20	Drive duty
Parameter3(P3)	1	1	0	*	*	*	P34	P33	P32	P31	P30	FR inverse-set value

P1: it is used to specify the CL dividing ratio.

P14, P13, P12: CL dividing ratio. They are used to change number of dividing stages of external or internal clock.

P14	P13	P12	CL dividing ratio
0	0	0	Not divide
0	0	1	2 divisions
0	1	0	4 divisions
0	1	1	8 divisions

P2: It is used to specify the duty of the module on block basis.

Duty	*	*	P25	P24	P23	P22	P21	P20	(Numbers of display lines)/4-1
Example: 1/128 duty	0	0	0	1	1	1	1	1	128/4-1=31
This will output driving voltage waveforms from com0 to com127.									

.

P3: It is used to specify number of lines to be inversely highlighted on LCD panel from P33 to P30 (lines can be inversely highlighted in the range of 2 to 16)

Inversely highlighted line	*	*	*	P34	P33	P32	P31	P30	Inversely highlighted lines-1
Example: 0AH	0	0	0	0	1	0	1	0	11-1=10
Example: 1CH	0	0	0	1	1	1	0	0	13-1=12

In the default, 0 inverse highlight lines is selected.

P34="0": Inversion occurs every frame. P34="1": Independent from frames.

(7) Sleep In/Out Preparation (SLPP) Command: 1; Parameter: 1

Using this command to setup ready status for sleep-in or sleep out.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	0	0	0	1	0	0	–
Parameter(P1)	1	1	0	0	0	1	1	1	1	1	P10	Sleep in/out ready

P10 =" 1": Ready for sleep in. P10 = "0": Ready for sleep out.

Parameter 3FH is used to initialize sleep-in sequencing, and parameter 3EH is used to initialize sleep-out sequencing.

(8) Sleep in (SPLIN) Command: 1; Parameter: None (95H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	0	1	0	1	0	1

(9) Sleep out (SLPOUT) Command: 1;Parameter: None (94H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	0	1	0	1	0	0

(10) Page address set (PASET) Command: 1; Parameter: 2 (75H)

When MPU makes access to the display data RAM, this command and succeeding parameters are used to specify the page address area. As the addresses are incremented from the start to the end page in the page-direction scan, the column address is incremented by 1 and the page address is returned to the start page.

Note: that the start and end page must be specified as a pair. Also, the relation “start page < end page” must be maintained.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	1	1	1	0	1	0	1	–
Parameter1(P1)	1	1	0	P17	P16	P15	P14	P13	P12	P11	P10	Start page
Parameter2(P2)	1	1	0	P27	P26	P25	P24	P23	P22	P21	P20	End page

(11) Column address set (CASET) Command: 1; Parameter: 2 (15H)

When MPU makes access to the display data RAM, this command and succeeding parameters are used to specify the column address area. As the addresses are incremented from the start to the end column in the column-direction scan, the page address is incremented by 1 and the column address is returned to the start column.

Note: that the start and end column must be specified as a pair. Also, the relation “start column < end column” must be maintained.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	0	1	0	1	0	1	–
Parameter1(P1)	1	1	0	P17	P16	P15	P14	P13	P12	P11	P10	Start address
Parameter2(P2)	1	1	0	P27	P26	P25	P24	P23	P22	P21	P20	End address

(12) Data control (DATCTL) Command: 1;Parameter: 3 (BCH)

This command and succeeding parameters are used to perform various setups needed when MPU operates display data stored on the built-in RAM.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	1	1	1	0	0	–
Parameter1(P1)	1	1	0	*	*	*	*	*	P12	P11	P10	Normal/inverse display of page / column address and

												address scan direction.
Parameter2(P2)	1	1	0	*	*	*	*	*	*	*	P20	RGB arrangement
Parameter3(P3)	1	1	0	*	*	*	*	*	P32	P31	P30	Gray-scale setup

P1: It is used to specify the normal or inverse display of the page / column address and also to specify the address scanning direction.

P10: Normal/inverse display of the page address. P10=0: Normal and P10=1: Inverse

P11: Normal/reverse turn of column address. P11=0: Normal rotation and P11=1: Reverse rotation.

P12: Address-scan direction. P12=0: In the column direction and P12=1: In the page direction.

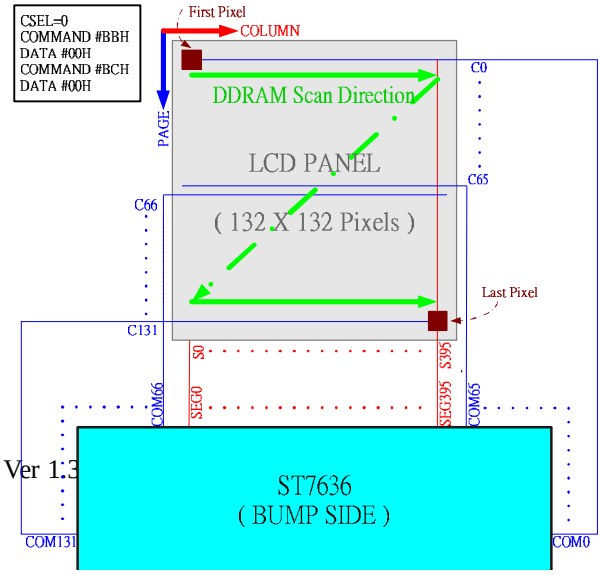
Page address and page-address scan direction

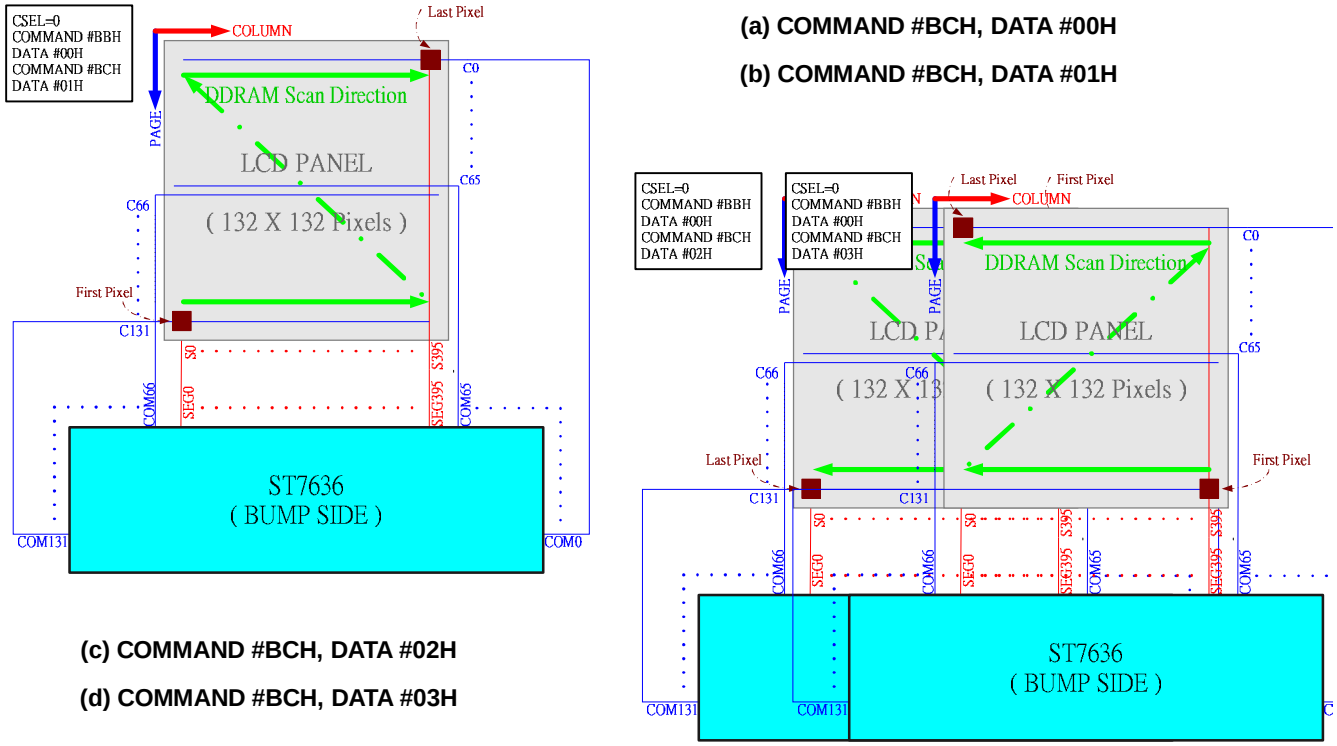
P12=0 Column direction

P11=0		0	1	2		129	130	131
P11=1		131	130	129		2	1	0
P10=0	P10=1							
0	131							
1	130							
2	129							
129	2							
130	1							
131	0							

P12=1 Page direction

P11=0		0	1	2		129	130	131
P11=1		131	130	129		2	1	0
P10=0	P10=1							
0	131							
1	130							
2	129							
129	2							
130	1							
131	0							





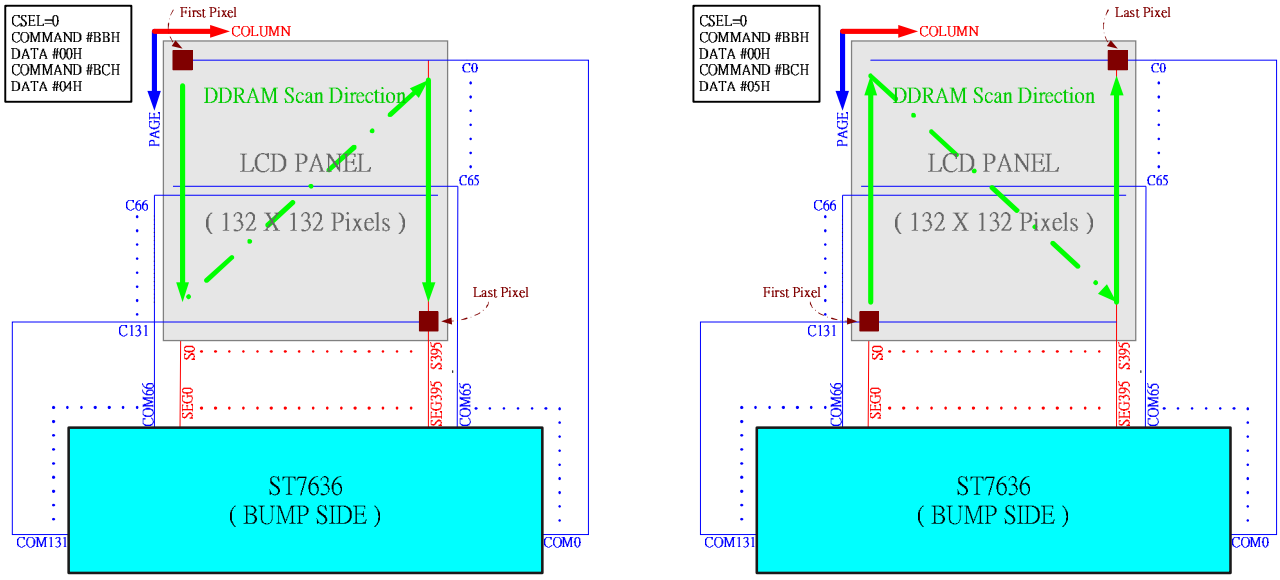
(a) COMMAND #BCH, DATA #00H

(b) COMMAND #BCH, DATA #01H

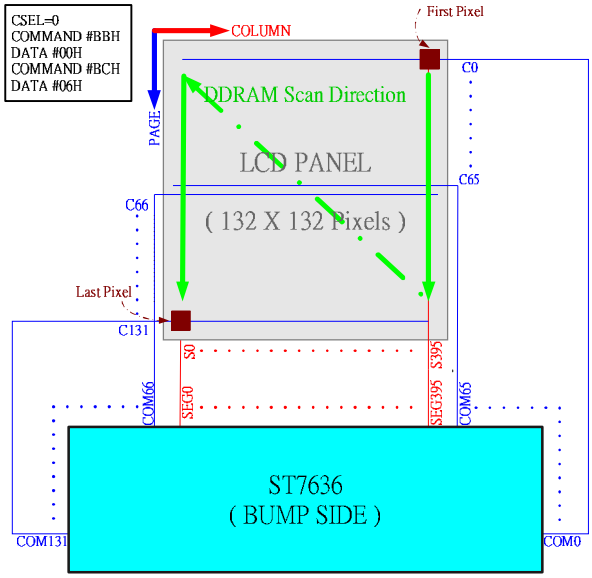
(c) COMMAND #BCH, DATA #02H

(d) COMMAND #BCH, DATA #03H

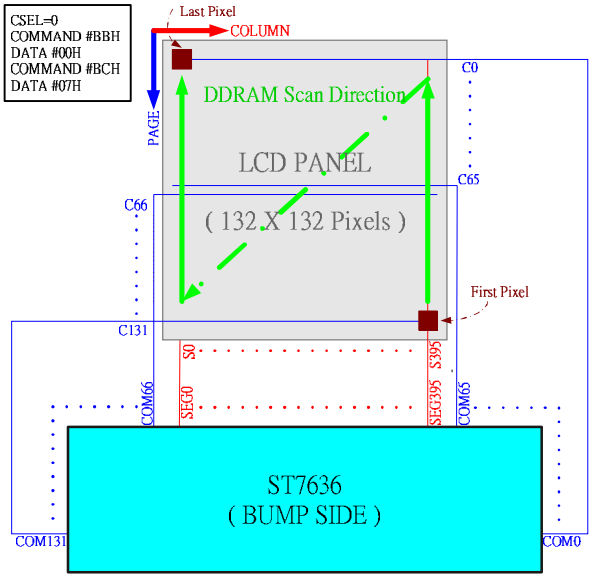
Figure 8.2.3 Different RAM accessing setup when CSEL=0 under COMMAND #BBH, DATA #00H
(a) COMMAND #BCH, DATA #00H
(b) COMMAND #BCH, DATA #01H
(c) COMMAND #BCH, DATA #02H
(d) COMMAND #BCH, DATA #03H



(e) COMMAND #BCH, DATA #04H



(f) COMMAND #BCH, DATA #05H



(g) COMMAND #BCH, DATA #06H

(h) COMMAND #BCH, DATA #07H

Figure 8.2.3 Different RAM accessing setup when CSEL=0 under COMMAND #BBH, DATA #00H (continue)
(e) COMMAND #BCH, DATA #04H
(f) COMMAND #BCH, DATA #05H
(g) COMMAND #BCH, DATA #06H
(h) COMMAND #BCH, DATA #07H

P2: RGB arrangement. This parameter allows you to change RGB arrangement of data which is going to be written into RAM, and therefore causes the inverse RGB rotation of the segment output of ST7636. You can fit RGB arrangement on the LCD panel according to this parameter setting.

P20	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	…	SEG395
0	R	G	B	R	G	B	R	G	…	B
1	B	G	R	B	G	R	B	G	…	R

P3: Gray scale setup. Using this parameter, 64 gray-scale display, you can select the 65K, 262K, and 16M display mode depending on the difference in RGB data arrangement.

P32	P31	P30	Numbers of gray-scale
0	0	1	64-gray 65K
0	1	0	64-gray 262K
1	0	0	64-gray 16M

(13) Memory write (RAMWR) Command: 1; Parameter: Numbers of data written (5CH)

When MPU writes data to the display memory, this command turns on the data entry mode. Entering this command always sets the page and column address at the start address. You can rewrite contents of the display data RAM by entering data succeeding to this command. At the same time, this operation increments the page or column address as applicable. The write mode is automatically cancelled if any other command is entered.

1. 8-bit bus

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	1	0	1	1	1	0	0	–
Parameter	1	1	0	Data to be written								Data to be written

2. 16-bit bus

	A0	RD	RW	D15	D14	…	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	*	*	…	*	*	0	1	0	1	1	1	0	0	Memory write
parameter	1	1	0	Data to be written													Write data

(14) Memory read (RAMRD) Command: 1; Parameter: Numbers of data read (5DH)

When MPU read data from the display memory, this command turns on the data read mode. Entering this command always sets the page and column address at the start address. After entering this command, you can read contents of the display data RAM. At the same time, this operation increments the page or column address as applicable. The data read mode is automatically cancelled if any other command is entered.

1. 8-bit bus

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	1	0	1	1	1	0	1	–
Parameter	1	0	1	Data to be read								Data to be read

2. 16-bit bus

	A0	RD	RW	D15	D14	….	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	*	*	*	*	*	0	1	0	1	1	1	0	1	Memory read
parameter	1	0	1	Data to be read													Read data

(15) Partial in (PTLIN) Command: 1; Parameter: 2 (A8H)

This command and succeeding parameters specify the partial display area. This command is used to turn on partial display of the screen (dividing screen by lines) in order to save power. Since ST7636 processes the liquid crystal display signal on 4-line basis (block basis), the display and non-display areas are also specified on 4-bit line (block basis).

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	0	1	0	0	0	–
Parameter(P1)	1	1	0	*	*	P15	P14	P13	P12	P11	P10	Start block address
Parameter(P2)	1	1	0	*	*	P25	P24	P23	P22	P21	P20	End block address

A block address that can be specified for the partial display must be the display one (don't try to specify an address not to be displayed when scrolled).

(16) Partial out (PTLOUT) Command: 1; Parameter: 0 (A9H)

This command is used to exit from the partial display mode.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	1	0	0	1

(17) Read modify write in (RMWIN) Command: 1; Parameter: 0 (E0H)

This command is used along with the column address set command, page address set command and read modify write out command. This function is used when frequently modifying data to specify a specific display area such as blinking cursor. First set a specific display area using the column and page address commands. Then, enter this command to set the column and page addresses at the start address of the specific area. When this operation is complete, the column (page) address won't be modified by the display data read command. It is incremented only when the display data write command is used. You can cancel this mode by entering the read modify write out or any other command.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	0	0	0	0	0

(18) Read modify write out (RMWOUT) Command: 1; Parameter: 0 (EEH)

Enter this command cancels the read modify write mode

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	0	1	1	1	0

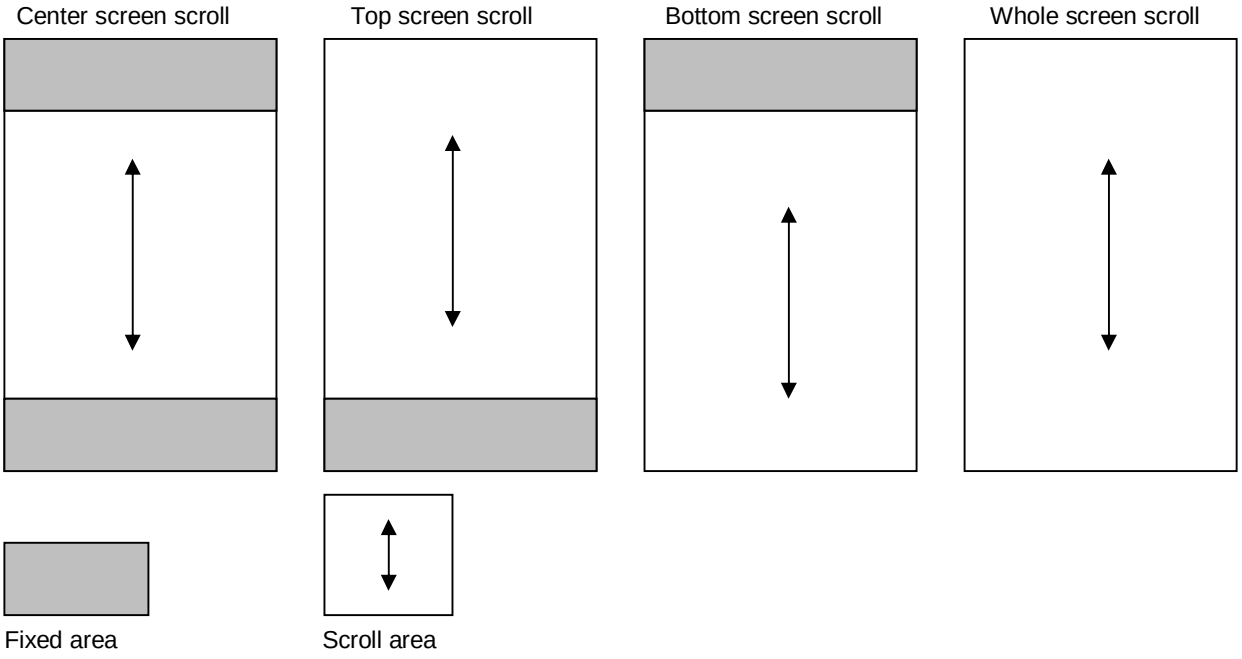
(19) Area scroll set (ASCSET) Command: 1; Parameter: 4 (AAH)

It is used when scrolling only the specified portion of the screen (dividing the screen by lines). This command and succeeding parameters specify the type of area scroll, fix area and scroll area.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	0	1	0	1	0	–
Parameter(P1)	1	1	0	*	*	P15	P14	P13	P12	P11	P10	Top block address
Parameter(P2)	1	1	0	*	*	P25	P24	P23	P22	P21	P20	Bottom block address
Parameter(P3)	1	1	0	*	*	P35	P34	P33	P32	P31	P30	Number of specified blocks
Parameter(P4)	1	1	0	*	*	*	*	*	*	P41	P40	Area scroll mode

P4: It is used to specify an area scroll mode.

P41	P40	Type of area scroll
0	0	Center screen scroll
0	1	Top screen scroll
1	0	Bottom screen scroll
1	1	Whole screen scroll



Since ST7636 processes the liquid crystal display signals on the four-line basis (block basis), FIX and scroll areas are also specified on the four-line basis (block basis).

DDRAM address corresponding to the top FIX area is set in the block address incrementing direction starting with 0 block. DDRAM address corresponding to the bottom FIX area is set in the block address decreasing direction starting with 32st block. Other DDRAM blocks excluding the top and bottom FIX areas are assigned to the scroll + background areas.

P1: It is used to specify the top block address of the scroll + background areas. Specify the 0th block for the top screen scroll or whole screen scroll.

P2: It specifies the bottom address of the scroll+ background areas. Specify the 32th block for the bottom or whole screen scroll.

Required relation between the start and end blocks (top block address<bottom block address) must be maintained.

P3: It specifies a specific number of blocks {Numbers of (Top FIX area +Scroll area) block-1}. When the bottom scroll or whole screen scroll, the value is identical with P2.

You can turn on the area scroll function by executing the area scroll set command first and then specifying the display start block of the scroll area with the scroll start set command.

[Area Scroll Setup Example]

In the center screen scroll of 1/120 duty (display range: 120 lines=30 blocks), if 8 lines=2 blocks and 8 lines=2 blocks are specified for the top and bottom FIX areas, 104 lines =26 blocks is specified for the scroll areas, respectively, 12 lines = 3 blocks on the DDRAM are usable as the background area. Value of each parameter at this time is as shown below.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	
P1	1	1	0	*	*	0	0	0	0	1	0	Top block address = 2
P2	1	1	0	*	*	0	1	1	1	1	0	Bottom block address = 30
P3	1	1	0	*	*	0	1	1	1	1	0	Number of specific blocks = 30
P4	1	1	0	*	*	*	*	*	*	0	0	Area scroll mode = center

(20) Scroll start address set (SCSTART) Command:1 Parameter: 1 (ABH)

This command and succeeding parameters are used to specify the start block address of the scroll area.

Note: that you must execute this command after executing the area scroll set command. Scroll becomes available by dynamically changing the start block address.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	0	1	0	1	1	–
Parameter(P1)	1	1	0	*	*	P15	P14	P13	P12	P11	P10	Start block address

(21) Internal oscillation on (OSCON) Command: 1; Parameter: 0 (D1H)

This command turns on the internal oscillation circuit. It is valid only when the internal oscillation circuit of CLS = HIGH is used.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	0	0	1

(22) Internal oscillation off (OSOFF) Command: 1; Parameter: 0 (D2H)

It turns off the internal oscillation circuit. This circuit is turned off in the reset mode.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	0	1	0

(23) Power control set (PWRCTR) Command: 1; Parameter: 1 (20H)

This command is used to turn on or off the Booster circuit, follower voltage, and voltage regulator circuit.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	1	0	0	0	1	0	0	0	0	–
Parameter(P1)	1	1	0	*	*	*	0	P13	0	P11	P10	LCD drive power

P10: It turns on or off the voltage regulator voltage.

P10 = “1”: ON. P10 =” 0”: OFF

P11: It turns on or off the follower circuit.

P11 = “1”: ON. P11 =” 0”: OFF

P13:It turns on or off the Booster.

P13 = “1”: ON. P13 =” 0”: OFF

(24) Electronic volume control (VOLCTR) Command: 1; Parameter: 2 (81H)

The command is used to program the optimum LCD supply voltage V_{LCD}. Reference to 7.10.2

	A0	**RD**	**RW**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Function**
Command	0	1	0	1	0	0	0	0	0	0	1	–
Parameter(P1)	1	1	0	*	*	P15	P14	P13	P12	P11	P10	Set Vop[5:0]
Parameter(P2)	1	1	0	*	*	*	*	*	P18	P17	P16	Set Vop[8:6]

(25) Increment electronic control (VOLUP) Command: 1; Parameter: 0 (D6H)

With the VOLUP and VOLDOWN command the V_{LCD} voltage and therewith the contrast of the LCD can be adjusted.

This command increments electronic control value Vop[5:0] of voltage regulator circuit by 1.

	A0	**RD**	**RW**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	0	1	0	1	1	0	1	0	1	1	0

If you set the electronic control value to 111111, the control value is set to 000000 after this command has been executed.

(26) Decrement electronic control (VOLDOWN) Command: 1; Parameter: 0 (D7H)

With the VOLUP and VOLDOWN command the V_{LCD} voltage and therewith the contrast of the LCD can be adjusted.

This command decrements electronic control value Vop[5:0] of voltage regulator circuit by 1.

	A0	**RD**	**RW**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	0	1	0	1	1	0	1	0	1	1	1

If you set the electronic control value to 000000, the control value is set to 111111 after this command has been executed.

Table 8.1.1 Possible Vop[5:0] values

Electronic Control Value	Decimal Equivalent	VLCD Offset
111111	31	+1240 mV
111110	30	+1200 mV
111101	29	+1160 mV
…	…	…
000010	2	+80 mV
000001	1	+40 mV
000000	0	0 mV
111111	-1	-40 mV
111110	-2	-80 mV
…	…	…
100010	-30	-1200 mV
100001	-31	-1240 mV
100000	-32	-1280mV

(27) Status read (STREAD) Command: 1; Parameter: None

It is the command for reading the internal condition of the IC.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	0	1	(8) Status data							

Issue STREAD (Status Read) command only to read the internal condition of the IC. One status data can be displayed depending on the setting. Issue the NOP command after the STREAD (Status Read) command.

The Status data will be composed of 8 bits below:

D7: Area scroll mode	Refer to P41 (ASCSET)	
D6: Area scroll mode	Refer to P40 (ASCSET)	
D5: RMW on/off	0 : Out	1 : In
D4: Scan direction	0 : Column	1 : Page
D3: Display ON/OFF	0 : OFF	1 : ON
D2: EEPROM access	0: OutAccess	1: InAccess
D1: Display normal/inverse	0 : Normal	1 : Inverse
D0: Partial display	0 : OFF	1 : ON

(28) Read Register 1 (EPSRRD1) Command: 1; Parameter: 0 (7CH)

It is the command for reading the Electronic Control values.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	1	1	1	1	1	0	0

Issue the EPSRRD1 and then STREAD (Status Read) commands in succession to read the Electronic Control values. One

status data can be displayed depending on the setting. Also, always issue the NOP command after the STREAD (Status Read) command.

The Status data will be composed of 8 bits below:

D7: 0

D6: 0

D[5:0]: Vop[5:0] Refer to electronic volume control values Vop[5:0]

(29) Read Register 2 (EPSRRD2) Command: 1 ;Parameter: 0 (7DH)

It is the command for reading ID codes of the ST7636 and the built-in resistance ratio.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	1	1	1	1	1	0	1

Issue the EPSRRD2 and then STREAD (Status Read) commands in succession to read IC's ID and the built-in resistance ratio. One status data can be displayed depending on the setting. Also, always issue the NOP command after the STREAD (Status Read) command.

The Status data will be composed of 8 bits below:

D[7:3]: ST7636 ID codes 00001

D[2:0]: Vop[8:6] Refer to the built-in resistance ratio Vop[8:6]

(30) Non-operating (NOP) Command: 1; Parameter: 0 (25H)

This command does not affect the operation.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	0	0	1	0	1

This command, however, has the function of canceling the IC test mode. Thus, it is recommended to enter it periodically to prevent malfunctioning due to noise and such.

(31) EEPROM Function Start (EEOK) Command:1;Parameter:1(07H)

In the OTP read/write flow, EEPROM is ready after issuing this command. Its parameter is set to 19H.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	0	0	0	1	1	1	–
Parameter(P1)	1	1	0	0	0	0	1	1	0	0	1	19H

(32) Reserved (82H)

Do not use this command

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	0	0	0	0	1	0

8.3 EXT="1" Function Description

(1) Set Red1 value (Red1 set) Command: 1; Parameter: 16 (20H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Red1 Set	0	1	0	0	0	1	0	0	0	0	0	FRAME 1 Red PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	–
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set red level 0 and 1st frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set red level 1 and 1st frame
Parameter14(P14)	1	1	0	*	*	*	P144	P143	P142	P141	P140	Set red level 13 and 1st frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set red level 15 and 1st frame

(2)Set Red2 value (Red2 set) Command: 1; Parameter: 16 (21H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Red2 Set	0	1	0	0	0	1	0	0	0	0	1	FRAME 2 Red PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	–
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set red level 0 and 2nd frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set red level 1 and 2nd frame
Parameter14(P14)	1	1	0	*	*	*	P144	P143	P142	P141	P140	Set red level 13 and 2nd frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set red level 15 and 2nd frame

(3) Set Red3 value (Red3 set) Command: 1; Parameter: 16 (22H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Red3 Set	0	1	0	0	0	1	0	0	0	1	0	FRAME 3 Red PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	–
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set red level 0 and 3rd frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set red level 1 and 3rdframe
Parameter14(P14)	1	1	0	*	*	*	P144	P143	P142	P141	P140	Set red level 13 and 3rd frame

Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set red level 15 and 3rd frame

(4) Set Red4 value (Red4 set) Command: 1; Parameter: 16 (23H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Red4 Set	0	1	0	0	0	1	0	0	0	1	1	FRAME 4 Red PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	—
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set red level 0 and 4th frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set red level 1 and 4thframe
Parameter14(P14)	1	1	0	*	*	*	P144	P143	P142	P141	P140	Set red level 13 and 4th frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set red level 15 and 4th frame

The default value of Red level set

	Red1 SET	Red2 SET	Red3 SET	Red4 SET
	FRAM1	FRAM2	FRAM3	FRAME4
red level0	00	00	00	00
red level1	02	02	02	02
red level2	05	05	05	05
red level3	07	07	07	08
red level4	0A	0A	0A	0B
red level5	0D	0D	0D	0C
red level6	0F	10	0F	10
red level7	11	12	11	12
red level8	13	14	13	14
red level9	16	16	16	15
red level10	18	18	18	17
red level11	19	19	19	1A
red level12	1B	1B	1B	1A
red level13	1C	1C	1C	1D
red level14	1D	1D	1D	1E
red level15	1E	1E	1E	1E

The modulation range of Red level set

	Red1 SET	Red2 SET	Red3 SET	Red4 SET
	FRAM1	FRAM2	FRAM3	FRAME4
red level0	0	0	0	0
red level1	0-7	0-7	0-7	0-7
red level2	0-F	0-F	0-F	0-F
red level3	0-F	0-F	0-F	0-F
red level4	8-F	8-F	8-F	8-F
red level5	0-1F	0-1F	0-1F	0-1F
red level6	0-1F	0-1F	0-1F	0-1F
red level7	0-1F	0-1F	0-1F	0-1F
red level8	10-17	10-17	10-17	10-17
red level9	10-1F	10-1F	10-1F	10-1F
red level10	10-1F	10-1F	10-1F	10-1F
red level11	10-1F	10-1F	10-1F	10-1F
red level12	10-1F	10-1F	10-1F	10-1F
red level13	10-1F	10-1F	10-1F	10-1F
red level14	10-1F	10-1F	10-1F	10-1F
red level15	18-1F	18-1F	18-1F	18-1F

(5) Set Green1 value (Green1 set) Command: 1; Parameter: 16 (24H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Green1 Set	0	1	0	0	0	1	0	0	1	0	0	FRAME 1 Green PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	–
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set green level 0 and 1st frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set green level 1 and 1st frame
Parameter14(P14)	1	1	0	*	*	*	P144	P143	P142	P141	P140	Set green level 13 and 1st frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set green level 15 and 1st frame

(6) Set Green2 value (Green1 set) Command: 1; Parameter: 16 (25H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Green2 Set	0	1	0	0	0	1	0	0	1	0	1	FRAME 2 Green PWM Set
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function

Command	0	1	0	0	0	1	0	0	0	0	0	–
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set green level 0 and 1st frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set green level 1 and 1st frame
Parameter14(P14)	1	1	0	*	*	*	P144	P143	P142	P141	P140	Set green level 13 and 1st frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set green level 15 and 1st frame

(7) Set Green3 value (Green1 set) Command: 1; Parameter: 16 (26H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Green3 Set	0	1	0	0	0	1	0	0	1	1	0	FRAME 3 Green PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	–
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set green level 0 and 1st frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set green level 1 and 1st frame
Parameter14(P14)	1	1	0	*	*	*	P144	P143	P142	P141	P140	Set green level 13 and 1st frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set green level 15 and 1st frame

(8) Set Green4 value (Green1 set) Command: 1; Parameter: 16 (27H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Green4 Set	0	1	0	0	0	1	0	0	1	1	1	FRAME 4 Green PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	–
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set green level 0 and 1st frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set green level 1 and 1st frame
Parameter14(P14)	1	1	0	*	*	*	P144	P143	P142	P141	P140	Set green level 13 and 1st frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set green level 15 and 1st frame

The default value of Green level set

	Green1 SET	Green2 SET	Green3 SET	Green4 SET
	FRAM1	FRAM2	FRAM3	FRAME4

green level0	00	00	00	00
green level1	02	02	02	02
green level2	05	05	05	05
green level3	07	07	07	08
green level4	0A	0A	0A	0B
green level5	0D	0D	0D	0C
green level6	0F	10	0F	10
green level7	11	12	11	12
green level8	13	14	13	14
green level9	16	16	16	15
green level10	18	18	18	17
green level11	19	19	19	1A
green level12	1B	1B	1B	1A
green level13	1C	1C	1C	1D
green level14	1D	1D	1D	1E
green level15	1E	1E	1E	1E

The modulation range of Green level set

	Green1 SET	**Green2 SET**	**Green3 SET**	**Green4 SET**
	FRAM1	**FRAM2**	**FRAM3**	**FRAME4**
green level0	0	0	0	0
green level1	0-7	0-7	0-7	0-7
green level2	0-F	0-F	0-F	0-F
green level3	0-F	0-F	0-F	0-F
green level4	8-F	8-F	8-F	8-F
green level5	0-1F	0-1F	0-1F	0-1F
green level6	0-1F	0-1F	0-1F	0-1F
green level7	0-1F	0-1F	0-1F	0-1F
green level8	10-17	10-17	10-17	10-17
green level9	10-1F	10-1F	10-1F	10-1F
green level10	10-1F	10-1F	10-1F	10-1F
green level11	10-1F	10-1F	10-1F	10-1F
green level12	10-1F	10-1F	10-1F	10-1F
green level13	10-1F	10-1F	10-1F	10-1F
green level14	10-1F	10-1F	10-1F	10-1F
green level15	18-1F	18-1F	18-1F	18-1F

(9) Set Blue1 value (Blue1 set) Command: 1; Parameter: 16 (28H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Blue1 Set	0	1	0	0	0	1	0	1	0	0	0	FRAME 1 Blue PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	–
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set blue level 0 and 1st frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set blue level 1 and 1st frame
Parameter14(P14)	1	1	0	*	*	*	P144	P143	P142	P141	P140	Set blue level 13 and 1st frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set blue level 15 and 1st frame

(10) Set Blue2 value (Blue2 set) Command: 1; Parameter: 16 (29H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Blue2 Set	0	1	0	0	0	1	0	1	0	0	1	FRAME 2 Blue PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	–
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set blue level 0 and 1st frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set blue level 1 and 1st frame
Parameter14(P14)	1	1	0	*	*	*	P144	P143	P142	P141	P140	Set blue level 13 and 1st frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set blue level 15 and 1st frame

(11) Set Blue3 value (Blue3 set) Command: 1; Parameter: 16 (2AH)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Blue3 Set	0	1	0	0	0	1	0	1	0	1	0	FRAME 3 Blue PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	–
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set blue level 0 and 1st frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set blue level 1 and 1st frame
Parameter14(P14)	1	1	0	*	*	*	P144	P143	P142	P141	P140	Set blue level 13 and 1st frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set blue level 15 and 1st frame

(12) Set Blue4 value (Blue4 set) Command: 1; Parameter: 16 (2BH)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Blue4 Set	0	1	0	0	0	1	0	1	0	1	1	FRAME 4 Blue PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	—
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set blue level 0 and 1st frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set blue level 1 and 1st frame
Parameter14(P14)	1	1	0	*	*	*	P144	P143	P142	P141	P140	Set blue level 13 and 1st frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set blue level 15 and 1st frame

The default value of Blue level set

	Blue1 SET	Blue2 SET	Blue3 SET	Blue4 SET
	FRAM1	FRAM2	FRAM3	FRAME4
blue level0	00	00	00	00
blue level1	02	02	02	02
blue level2	05	05	05	05
blue level3	07	07	07	08
blue level4	0A	0A	0A	0B
blue level5	0D	0D	0D	0C
blue level6	0F	10	0F	10
blue level7	11	12	11	12
blue level8	13	14	13	14
blue level9	16	16	16	15
blue level10	18	18	18	17
blue level11	19	19	19	1A
blue level12	1B	1B	1B	1A
blue level13	1C	1C	1C	1D
blue level14	1D	1D	1D	1E
blue level15	1E	1E	1E	1E

The modulation range of Blue level set

	Blue1 SET	Blue2 SET	Blue3 SET	Blue4 SET
	FRAM1	FRAM2	FRAM3	FRAME4
blue level0	0	0	0	0
blue level1	0-7	0-7	0-7	0-7
blue level2	0-F	0-F	0-F	0-F
blue level3	0-F	0-F	0-F	0-F
blue level4	8-F	8-F	8-F	8-F
blue level5	0-1F	0-1F	0-1F	0-1F
blue level6	0-1F	0-1F	0-1F	0-1F
blue level7	0-1F	0-1F	0-1F	0-1F
blue level8	10-17	10-17	10-17	10-17
blue level9	10-1F	10-1F	10-1F	10-1F
blue level10	10-1F	10-1F	10-1F	10-1F
blue level11	10-1F	10-1F	10-1F	10-1F
blue level12	10-1F	10-1F	10-1F	10-1F
blue level13	10-1F	10-1F	10-1F	10-1F
blue level14	10-1F	10-1F	10-1F	10-1F
blue level15	18-1F	18-1F	18-1F	18-1F

Example：Paint setup

```
void LoadPaint( void )
{
        Write( COMMAND, 0x0031 );           // Ext = 1

        Write( COMMAND, 0x0020 );           // Red Palette FRC1 Setup
        Write( DATA, 0x0000 );              // Red1 Level0 Setup
        Write( DATA, 0x0002 );              // Red1 Level1 Setup
        Write( DATA, 0x0005 );              // Red1 Level2 Setup
        …….                                 …….
        …….                                 …….
        Write( DATA, 0x001E );              // Red1 Level15 Setup

        Write( COMMAND, 0x0021 );           // Red Palette FRC2 Setup
        Write( DATA, 0x0000 );              // Red2 Level0 Setup
        Write( DATA, 0x0002 );              // Red2 Level1 Setup
        Write( DATA, 0x0005 );              // Red2 Level2 Setup
        …….                                 …….
        …….                                 …….
        Write( DATA, 0x001E );              // Red2 Level15 Setup

        Write( COMMAND, 0x0022 );           // Red Palette FRC3 Setup
        Write( DATA, 0x0000 );              // Red3 Level0 Setup
        Write( DATA, 0x0002 );              // Red3 Level1 Setup
        Write( DATA, 0x0005 );              // Red3 Level2 Setup
        …….                                 …….
        …….                                 …….
```

```
Write( DATA, 0x001E );              // Red3 Level15 Setup

Write( COMMAND, 0x0023 );           // R Palette FRC4 Setup
Write( DATA, 0x0000 );              // Red4 Level0 Setup
Write( DATA, 0x0002 );              // Red4 Level1 Setup
Write( DATA, 0x0005 );              // Red4 Level2 Setup
…….                                 …….
…….                                 …….
Write( DATA, 0x001E );              // Red4 Level15 Setup

Write( COMMAND, 0x0024 );           // Green Palette FRC1 Setup
Write( DATA, 0x0000 );              // Green 1 Level0 Setup
Write( DATA, 0x0002 );              // Green 1 Level1 Setup
Write( DATA, 0x0005 );              // Green 1 Level2 Setup
…….                                 …….
…….                                 …….
Write( DATA, 0x001E );              // Green 1 Level15 Setup

Write( COMMAND, 0x0025 );           // Green Palette FRC2 Setup
Write( DATA, 0x0000 );              // Green 2 Level0 Setup
Write( DATA, 0x0002 );              // Green 2 Level1 Setup
Write( DATA, 0x0005 );              // Green 2 Level2 Setup
…….                                 …….
…….                                 …….
Write( DATA, 0x001E );              // Green 2 Level15 Setup

Write( COMMAND, 0x0026 );           // Green Palette FRC3 Setup
Write( DATA, 0x0000 );              // Green 3 Level0 Setup
Write( DATA, 0x0002 );              // Green 3 Level1 Setup
Write( DATA, 0x0005 );              // Green 3 Level2 Setup
…….                                 …….
…….                                 …….
Write( DATA, 0x001E );              // Green 3 Level15 Setup

Write( COMMAND, 0x0027 );           // Green Palette FRC4 Setup
Write( DATA, 0x0000 );              // Green 4 Level0 Setup
Write( DATA, 0x0002 );              // Green 4 Level1 Setup
Write( DATA, 0x0005 );              // Green 4 Level2 Setup
…….                                 …….
…….                                 …….
Write( DATA, 0x001E );              // Green 4 Level15 Setup

Write( COMMAND, 0x0028 );           // Green Palette FRC1 Setup
Write( DATA, 0x0000 );              // Green 1 Level0 Setup
Write( DATA, 0x0002 );              // Green 1 Level1 Setup
Write( DATA, 0x0005 );              // Green 1 Level2 Setup
…….                                 …….
…….                                 …….
Write( DATA, 0x001E );              // Green 1 Level15 Setup

Write( COMMAND, 0x0029 );           // Green Palette FRC2 Setup
Write( DATA, 0x0000 );              // Green 2 Level0 Setup
Write( DATA, 0x0002 );              // Green 2 Level1 Setup
Write( DATA, 0x0005 );              // Green 2 Level2 Setup
…….                                 …….
…….                                 …….
Write( DATA, 0x001E );              // Green 2 Level15 Setup
```

```
        Write( COMMAND, 0x002A );          // Green Palette FRC3 Setup
        Write( DATA, 0x0000 );             // Green 3 Level0 Setup
        Write( DATA, 0x0002 );             // Green 3 Level1 Setup
        Write( DATA, 0x0005 );             // Green 3 Level2 Setup
        …….                                ……..
        …….                                ……..
        Write( DATA, 0x001E );             // Green 3 Level15 Setup

        Write( COMMAND, 0x002B );          // Green Palette FRC4 Setup
        Write( DATA, 0x0000 );             // Green 4 Level0 Setup
        Write( DATA, 0x0002 );             // Green 4 Level1 Setup
        Write( DATA, 0x0005 );             // Green 4 Level2 Setup
        …….                                ……..
        …….                                ……..
        Write( DATA, 0x001E );             // Green 4 Level15 Setup
}
```

(13) ANASET Command 1; Parameter: 3 (32H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	1	0	0	1	0	–
Parameter1(P1)	1	1	0	*	*	*	*	*	P12	P11	P10	OSC frequency Adjustment
Parameter2(P2)	1	1	0	*	*	*	*	*	*	P21	P20	Booster Efficiency Set
Parameter3(P3)	1	1	0	*	*	*	*	*	P32	P31	P30	Bias setting

P1: OSC frequency adjustment

P10	P11	P12	CL pin frequency (KHz) : CL dividing ratio setting = 00H (No division)	CL pin frequency (KHz) : CL dividing ratio setting = 04H (Divided by 2)
0	0	0	10.46	5.23
0	0	1	10.82	5.41
0	1	0	11.67	5.84
0	1	1	12.74	6.37
1	0	0	14.03	7.02
1	0	1	15.63	7.82
1	1	0	17.61	8.81
1	1	1	20.32	10.16

OSC frequency can be adjusted by P1 setting and command CAH, see page 49.

The default OSC frequency (CL pin frequency) is 10.46KHz.

And the frame frequency is from OSC frequency and duty setting, as the formula shown below:

Frame frequency = OSC frequency/(Duty+1)

Example:

1. duty=132, P1 setting=[000], frame frequency=10.46KHz/133~78.64Hz
2. duty=128, P1 setting=[101], frame frequency=15.63KHz/129~121.16Hz

P2: Booster Efficiency set

P21	P20	Frequency (Hz)
0	0	Level 1
0	1	Level 2
1	0	Level 3
1	1	Level 4

By Booster Stages (2X, 3X, 4X, 5X, 6X, 7X, 8X) and Booster Efficiency (Level1~4) commands, we could easily set the best Booster performance with suitable current consumption. If the Booster Efficiency is set to higher level (level4 is higher than level1). The Boost Efficiency is better than lower level, and it just need few more power consumption current.

P3: Select LCD bias ratio of the voltage required for driving the LCD.

P32	P31	P30	LCD bias
0	0	0	1/12
0	0	1	1/11
0	1	0	1/10
0	1	1	1/9
1	0	0	1/8
1	0	1	1/7
1	1	0	1/6
1	1	1	1/5

(14) Color Dither OFF (DITHOFF) Command: 1; Parameter: None (34H)

Turn off the dithering circuit.

	A0	**RD**	**RW**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	0	1	0	0	0	1	1	0	1	0	0

(15) Color Dither ON (DITHON) Command: 1; Parameter: None (35H)

Turn on the dithering circuit.

	A0	**RD**	**RW**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	0	1	0	0	0	1	1	0	1	0	1

(16) Control EEPROM: 1; Parameter: 1 (CDH)

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	0	1	1	0	1
Parameter (P1)	1	1	0	*	*	P15	*	*	*	*	*

P15: when setting “1” **è** The Write Enable of EEPROM will be opened.

P15: when setting “0” **è** The Read Enable of EEPROM will be opened.

(17) Cancel EEPROM Command: 1;Parameter: None (CCH)

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	0	1	1	0	0

(18) Write data to EEPROM (EPMWR) Command: 1; Parameter: None (FCH)

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	1	1	1	0	0

(19) Read data from EEPROM (EPMWR) Command: 1; Parameter: None (FDH)

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	1	1	1	0	1

8.4 EXT=”0” or ”1” Function Description

(1) Extension instruction disable (EXT IN) Command:1 Parameter: None (30H)

Use the “Ext=0” command table

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	1	0	0	0	0

(2) Extension instruction enable (EXT OUT) Command:1 Parameter: None (31H)

Use the extended command table (EXT=”1”)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	1	0	0	0	1

8.5 Referential Instruction Setup Flow

8.5.1 Initializing with the Built-in Power Supply Circuits

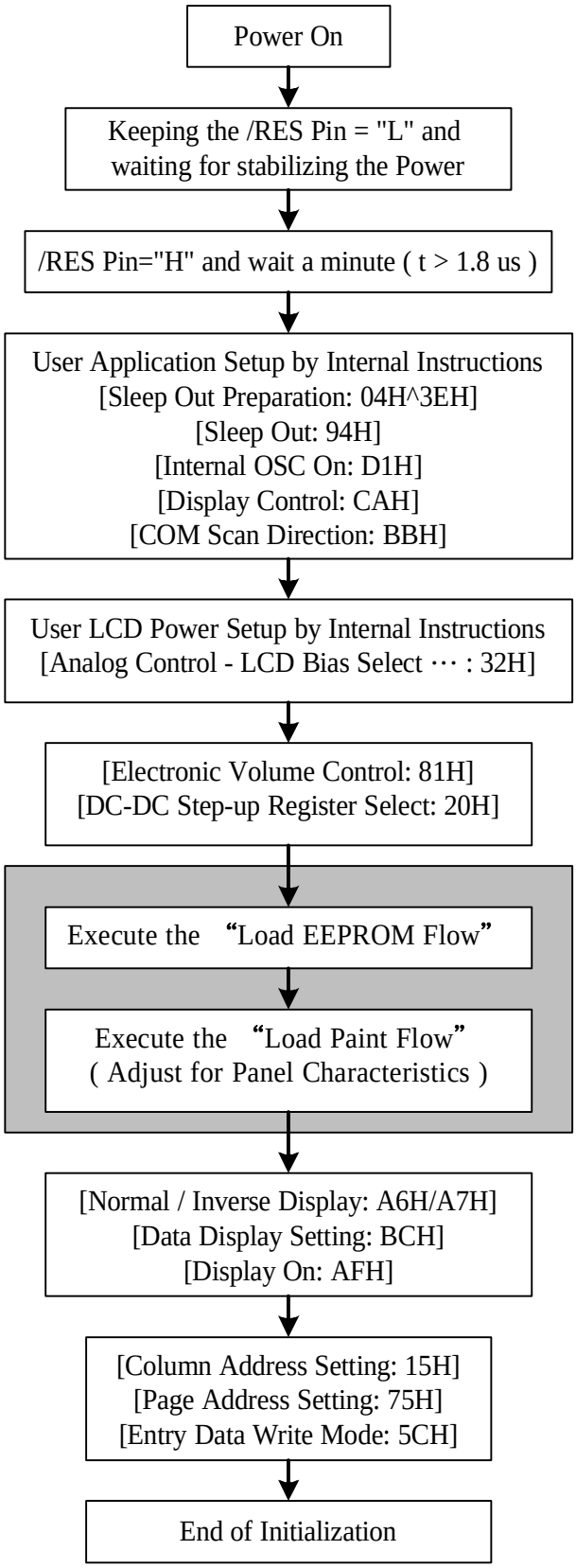


Figure 8.5.1.1 Initializing with the Built-in Power Supply Circuits

Example：Initial code for 128X128

```
void ST7636_Init( void )
{
        Write( COMMAND, 0x0030 );           // Ext = 0
        Write( COMMAND, 0x0004 );           // Sleep Preparation
        Write( DATA, 0x003e );              // Sleep Out Ready
        Write( COMMAND, 0x0094 );           // Sleep Out

        Write( COMMAND, 0x00d1 );           // Internal OSC on
        Write( COMMAND, 0x00ca );           // Display Control
        Write( DATA, 0x0000 );              // CL divisions
        Write( DATA, 0x001f );              // Duty Setting = 128
        Write( DATA, 0x0000 );              // Fr Inverse-set value
        Write( COMMAND, 0x00bb );           // Com Scan Direct.
        Write( DATA, 0x0001 );

        Write( COMMAND, 0x0031 );           // Ext = 1
        Write( COMMAND, 0x0032 );           // Analog Setting
        Write( DATA, 0x0000 );              // OSC adjustment
        Write( DATA, 0x0001 );              // Booster Efficiency Setting
        Write( DATA, 0x0000 );              // Bias Setting

        Write( COMMAND, 0x0030 );           // Ext = 0
        Write( COMMAND, 0x0081 );           // Electronic Volume Control
        Write( DATA, 0x003f );              // EV:Vop[5:0]_6bit
        Write( DATA, 0x0004 );              // EV:Vop[8:6]_3bit
        Write( COMMAND, 0x0020 );           // Power Control
        Write( DATA, 0x00b );               // B/F/R = On/On/On

        LoadEEPROM();                       // Load EEPROM, see page 42
        LoadPaint();                        // Load Paint Setup, see page 68

        Write( COMMAND, 0x0030 );           // Ext = 0
        Write( COMMAND, 0x00a6 );           // Normal Display
        Write( COMMAND, 0x00bc );           // Data Scan Direction
        Write( DATA, 0x0000 );              // Page / Column Address Setting
        Write( DATA, 0x0000 );              // RGB arrangement
        Write( DATA, 0x0001 );              // Gray-scale setup ( 64-gray: 01H)
        Write( COMMAND, 0x00af );           // Display On

        Write( COMMAND, 0x0015 );           // Column address set
        Write( DATA, 0 );                   // From column address 0 to 127
        Write( DATA, 127 );
        Write( COMMAND, 0x0075 );           // Page address set
        Write( DATA, 0 );                   // From page address 0 to 127
        Write( DATA, 127 );

}
```

8.5.2 Sleep In/Out

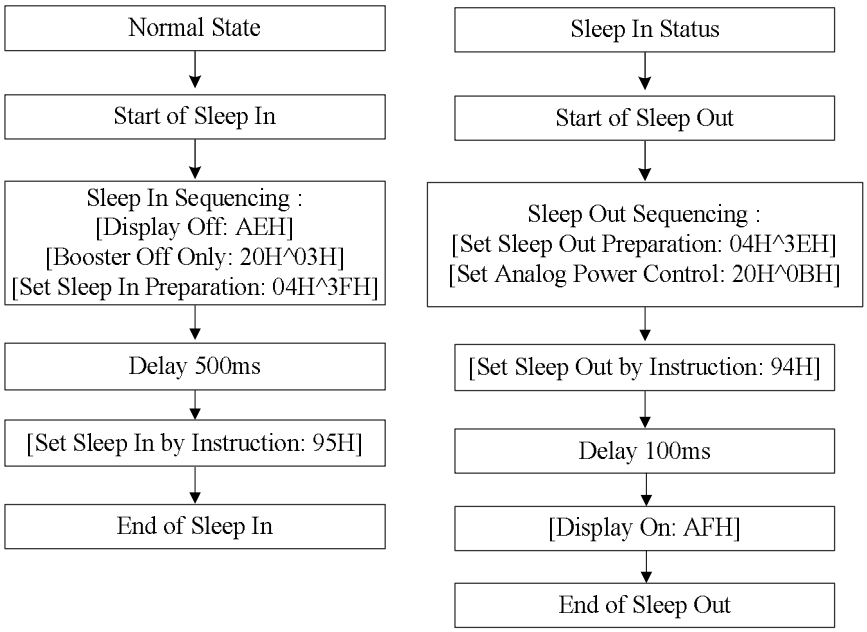


Fig 8.5.2.1 Sleep In/Out

Example：Sleep In Operation

```
void SleepIn( void )
{

        Write( COMMAND, 0x0030 );          // Ext = 0
        Write( COMMAND, 0x00ae );          // Display Off
        Write( COMMAND, 0x0020);           // Power Control
        Write( DATA, 0x0003 );             // B/F/R = Off/On/On
        Write( COMMAND, 0x0004 );          // Sleep Preparation
        Write( DATA, 0x003f );             // Sleep In Ready
        Delay( 500ms);
        Write( COMMAND, 0x0095 );          // Sleep In

}
```

Example：Sleep Out Operation

```
void SleepOut( void )
{

        Write( COMMAND, 0x0030 );          // Ext = 0
        Write( COMMAND, 0x0004 );          // Sleep Preparation
        Write( DATA, 0x003e );             // Sleep Out Ready
        Write( COMMAND, 0x0020 );          // Power Control
        Write( DATA, 0x000b );             // B/F/R = On/On/On
        Write( COMMAND, 0x0094 );          // Sleep Out
        Delay( 100ms );
        Write( COMMAND, 0x00af );          // Display On

}
```

8.5.3 Data Displaying

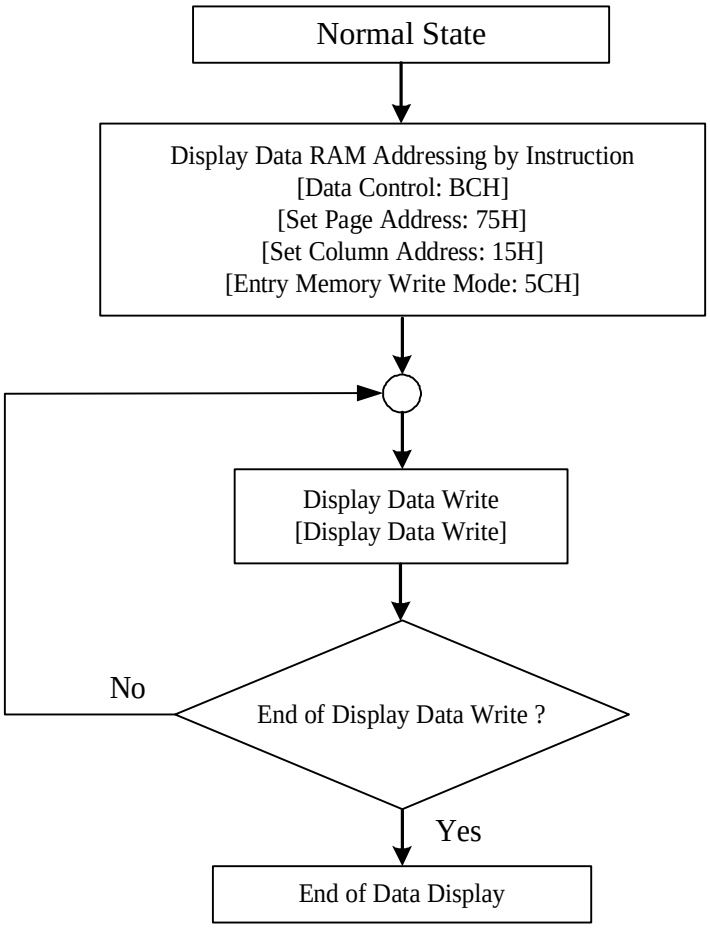


Figure 8.5.3.1 Data Displaying

Example：Display for 128X128

```
void Display( char *pattern )
{
        unsigned char i, j;

        Write( COMMAND, 0x0030 );                   // Ext = 0
        Write( COMMAND, 0x0015 );                   // Column address set
        Write( DATA, 0 );                           // From column address 0 to 127
        Write( DATA, 127 );
        Write( COMMAND, 0x0075 );                   // Page address set
        Write( DATA, 0 );                           // From page address 0 to 127
        Write( DATA, 127 );
        Write( COMMAND, 0x005c )                    // Entry Memory Write Mode
        for( j = 0; j < 127 ; j++ )
            for( i = 0 ; i < 127 ; i++ )
                Write( DATA, pattern[j*128+i] );    // Display Data Write


}
```

8.5.4 Partial Display In/Out

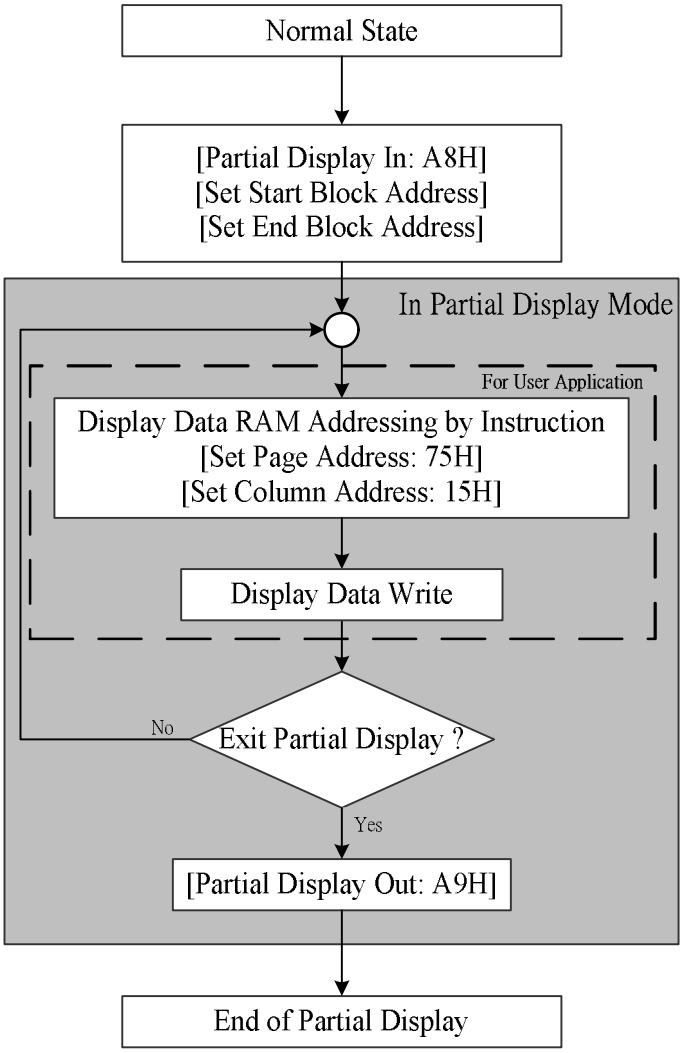


Figure 8.5.4.1 Partial Display In/Out

Example：Partial Display In Operation

```
void PartailIn( unsigned char start_block, unsigned char end_block )
{
        Write( COMMAND, 0x0030 );           // Ext = 0
        Write( COMMAND, 0x00A8);            // Partial Display In Function
        Write( DATA, start_block );         // Start Block
        Write( DATA, end_block );           // End Block

}

void PartailOut( void )
     {
        Write( COMMAND, 0x0030 );           // Ext = 0
        Write( COMMAND, 0x00A9 );           // Partial Display Out Function

}
```

```
extern unsigned char *display_pattern;
void main()
{
        PartialIn( 11, 18 );                    // entry partial display mode

        Windowing( 0, 11*4, 131, 18*4 );        // set the page and column range
        PartialDisplay( display_pattern );      // Fill the data into partial display area
            .
            .
            .
        PartialOut();                           // Out of partial display mode

}
```

8.5.5 Scroll Display

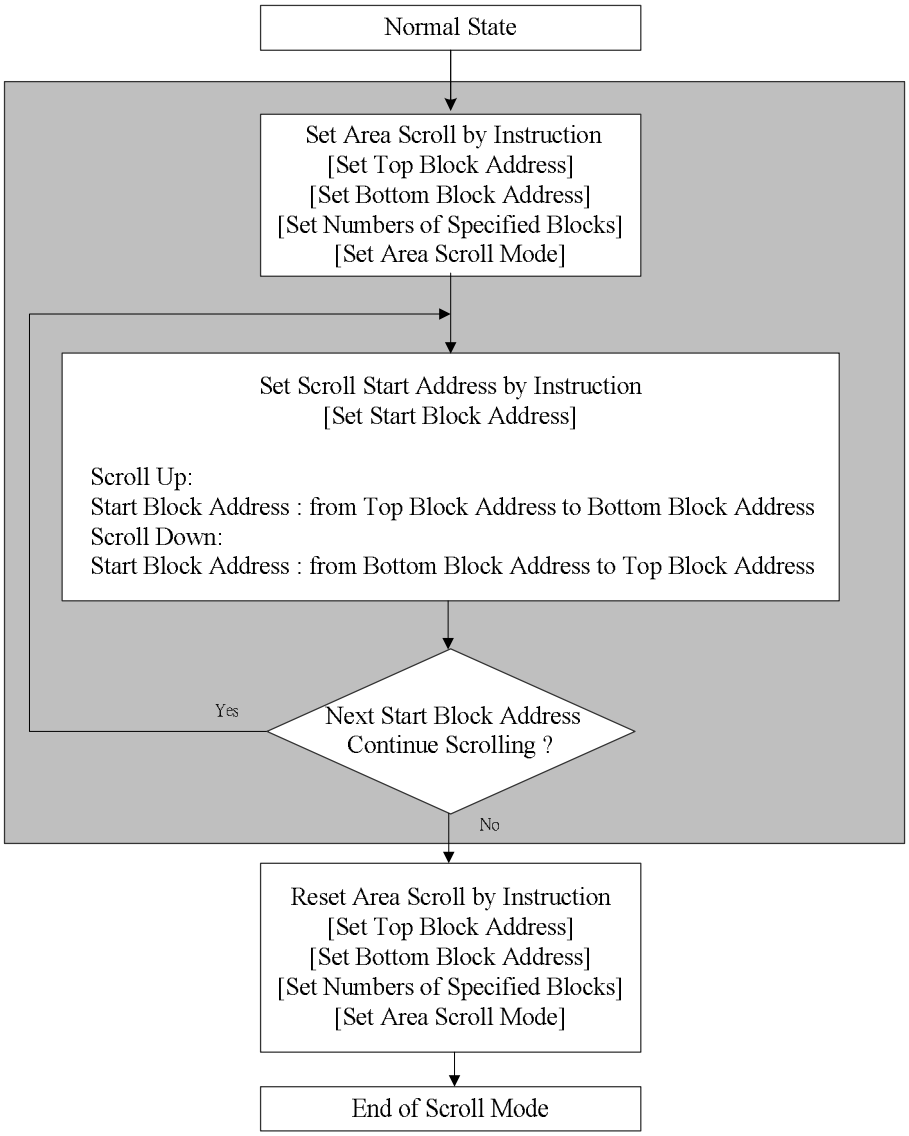


Figure 8.5.5.1 Scroll Display

Example：Screen Scroll Operation

```
void CenterScreenScroll( void )
{

        Write( COMMAND, 0x0030 );           // Ext = 0
        Write( COMMAND, 0x00AA);            // Partial Display In Function
        Write( DATA, 0x000a );              // Top_Block=10
        Write( DATA, 0x0014 );              // Bottom_Block=20
        Write( DATA, 0x0014 );              // Number of Specified Blocks=Bottom_Block=20
        Write( DATA, 0x0000 );              // Area Scroll Type=Center Screen Scroll

        ScrollUp() or ScrollDown();         // Scroll Up or Scroll Down

}

void TopScreenScroll( void )
{

        Write( COMMAND, 0x0030 );           // Ext = 0
        Write( COMMAND, 0x00AA);            // Partial Display In Function
        Write( DATA, 0x0000 );              // Top_Block=0
        Write( DATA, 0x0014 );              // Bottom_Block=20
        Write( DATA, 0x0014 );              // Number of Specified Blocks=Bottom_Block=20
        Write( DATA, 0x0001 );              // Area Scroll Type=Top Screen Scroll

        ScrollUp() or ScrollDown();         // Scroll Up or Scroll Down

}

void BottomScreenScroll( void )
{

        Write( COMMAND, 0x0030 );           // Ext = 0
        Write( COMMAND, 0x00AA);            // Partial Display In Function
        Write( DATA, 0x000a );              // Top_Block=10
        Write( DATA, 0x0020 );              // Bottom_Block=32
        Write( DATA, 0x0020 );              // Number of Specified Blocks=Bottom_Block=32
        Write( DATA, 0x0002 );              // Area Scroll Type=Bottom Screen Scroll

        ScrollUp() or ScrollDown();         // Scroll Up or Scroll Down

}

void WholeScreenScroll( void )
{

        Write( COMMAND, 0x0030 );           // Ext = 0
        Write( COMMAND, 0x00AA);            // Partial Display In Function
        Write( DATA, 0x0000 );              // Top_Block=0
        Write( DATA, 0x0020 );              // Bottom_Block=32
        Write( DATA, 0x0020 );              // Number of Specified Blocks=Bottom_Block=32
        Write( DATA, 0x0003 );              // Area Scroll Type=Whole Screen Scroll

        ScrollUp() or ScrollDown();         // Scroll Up or Scroll Down

}
```

```
void ScrollUp( void )
{

        Write( COMMAND, 0x0030 );           // Ext = 0
        Write( COMMAND, 0x00AB);            // Scroll Start Set
        Write( DATA, Top_Block);            // Start Block Address=Top_Block
        Delay();                            // Delay

        Write( COMMAND, 0x00AB);            // Scroll Start Set
        Write( DATA, Top_Block +1 );        // Start Block Address= Top_Block+1
        Delay();                            // Delay

        Write( COMMAND, 0x00AB);            // Scroll Start Set
        Write( DATA, Top_Block +2 );        // Start Block Address= Top_Block +2
        Delay();                            // Delay
        ……
        ……
        Write( COMMAND, 0x00AB);            // Scroll Start Set
        Write( DATA, Bottom_Block );        // Start Block Address= Bottom_Block
        Delay();                            // Delay

}

void ScrollDown( void )
{

        Write( COMMAND, 0x0030 );           // Ext = 0
        Write( COMMAND, 0x00AB);            // Scroll Start Set
        Write( DATA, Bottom_Block);         // Start Block Address= Bottom_Block
        Delay();                            // Delay

        Write( COMMAND, 0x00AB);            // Scroll Start Set
        Write( DATA, Bottom_Block -1 );     // Start Block Address= Bottom_Block -1
        Delay();                            // Delay

        Write( COMMAND, 0x00AB);            // Scroll Start Set
        Write( DATA, Bottom_Block -2 );     // Start Block Address= Bottom_Block -2
        Delay();                            // Delay
        ……
        ……
        Write( COMMAND, 0x00AB);            // Scroll Start Set
        Write( DATA, Top _Block );          // Start Block Address= Top_Block
        Delay();                            // Delay

}
```

8.5.6 Read-Modify-Write Cycle

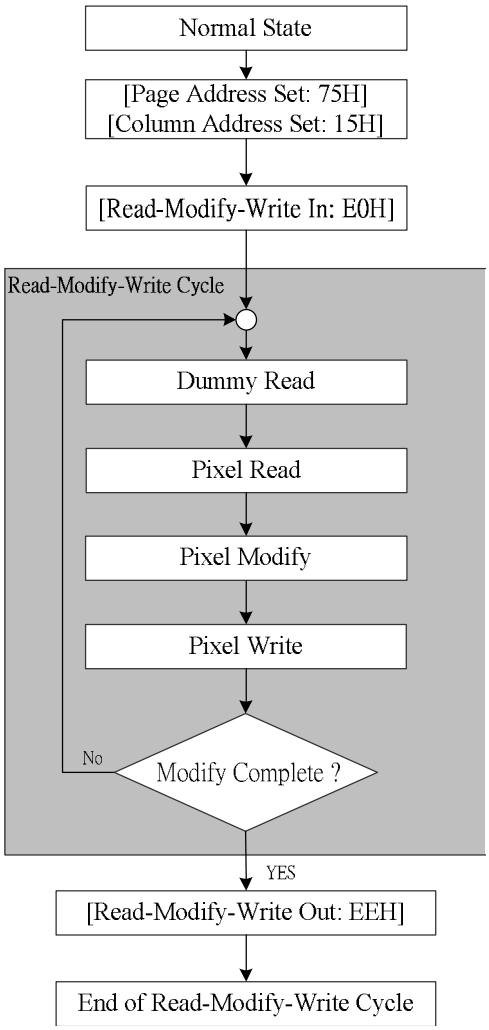


Figure 8.5.6.1 Read-Write-Modify Cycle

Example：Read-Write-Modify Cycle

```
void ReadModifyWriteIn( void )
{
        Write( COMMAND, 0x0030 );       // Ext = 0
        Write( COMMAND, 0x00E0 );       // Entry the Read-Modify-Write mode
}

void ReadModifyWriteOut( void )
{
        Write( COMMAND, 0x0030 );       // Ext = 0
        Write( COMMAND, 0x00EE );       // Out of partial display mode
}

extern unsigned char *display_pattern;
void main()
{
    unsigned pixel, i;

    Windowing( 11, 31, 80, 50 );            // set the page and column range
```

```
        ReadModifyWriteIn();                    // entry the Read-Modify-Write mode

        for( i = 0 ; i < 1400 ; i++ )
          {
            Read( DATA );                       // For dummy read
            pixel = Read( DATA );               // Pixel read
            pixel = pixel & 0x07ff;             // Pixel modify: red filter
            Write( DATA, pixel );
          }

        ReadModifyWriteOut();                   // Out of Read-Modify-Write mode

}
```

8.5.7 Power OFF

Power OFF

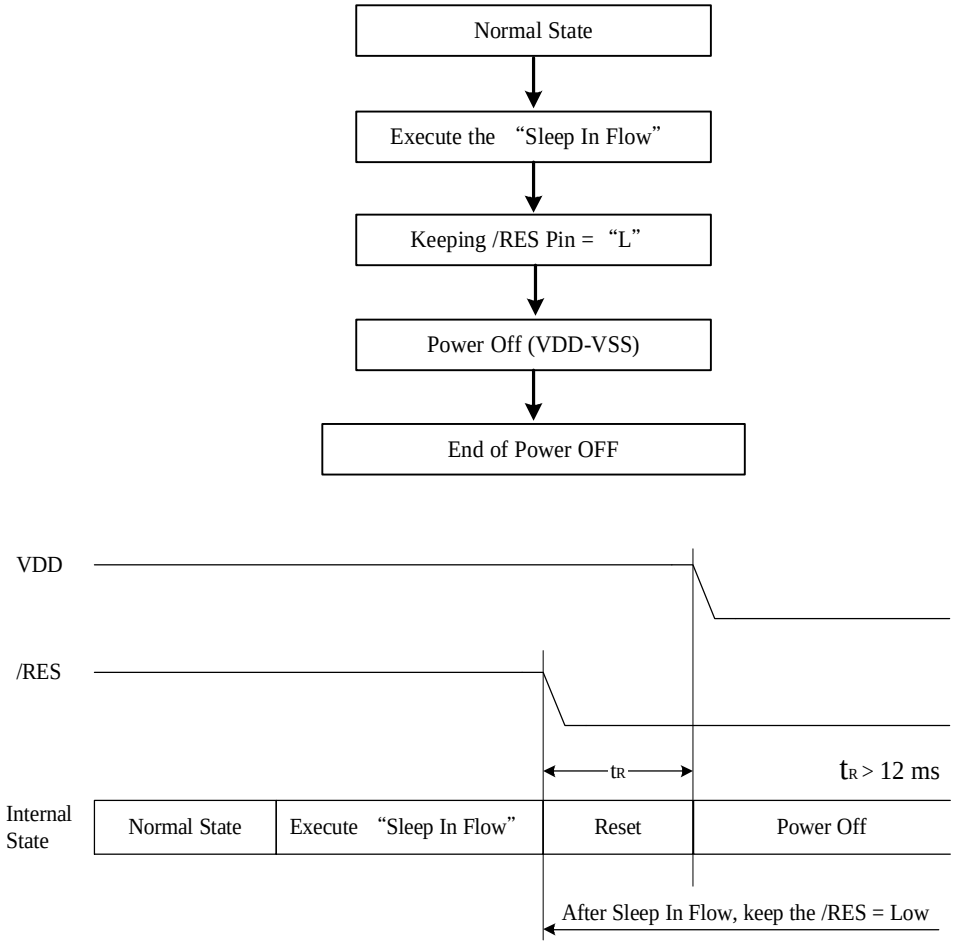
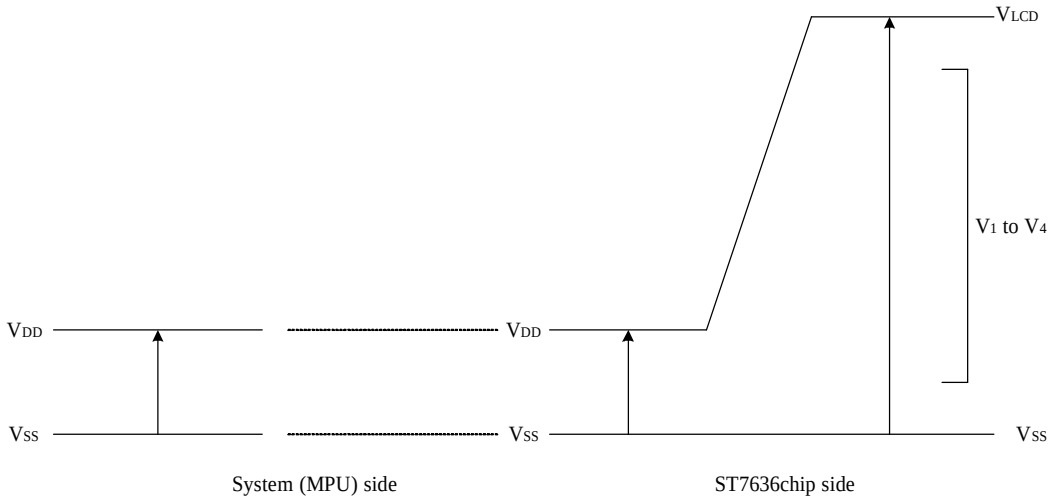


Figure 8.5.7.1 Power off

9. LIMITING VALUES

In accordance with the Absolute Maximum Rating System; see notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Power supply voltage	VDD, VDD1~VDD5	–0.5 ~ +4.0	V
Power supply voltage (VDD standard)	$VOUT_{IN}$	–0.5 ~ +20	V
Power supply voltage (VDD standard)	V1, V2, V3, V4	0.3 to $VOUT_{IN}$	V
Input voltage	VIN	–0.5 to VDD+0.5	V
Output voltage	VO	–0.5 to VDD+0.5	V
Operating temperature(Die)	TOPR	–30 to +85	°C
Storage temperature(Die)	TSTR	–40 to +125	°C



Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
3. Insure that the voltage levels of V1, V2, V3, and V4 are always such that

   $VOUT_{IN} \geqq V0 \geqq V1 \geqq V2 \geqq V3 \geqq V4 \geqq VSS$

10. HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see “Handling MOS devices”).

11. DC CHARACTERISTICS

V_{DD} = 2.4 V to 3.3V; V_{SS} = 0 V; V_{LCD} = 3.76 to 18.0V; T_{amb} = -30℃ to +85℃; unless otherwise specified.

Item		Symbol	Condition		Rating			Units	Applicable Pin
					Min.	Typ.	Max.		
High-level Input Voltage		VIHC			0.8 x VDD	—	VDD	V	*1
Low-level Input Voltage		VILC			VSS	—	0.2 x VDD	V	*1
High-level Output Voltage		VOHC			0.8 x VDD	—	VDD	V	*2
Low-level Output Voltage		VOLC			VSS	—	0.2 x VDD	V	*2
Input leakage current		ILI	VIN = VDD or VSS		–1.0	—	1.0	μA	*3
Output leakage current		ILO	VIN = VDD or VSS		–3.0	—	3.0	μA	*4
Liquid Crystal Driver ON Resistance		RON	Ta = 25°C (Relative To VSS)	$VOUT_{IN}$ = 15.0 V	—	1	10	KΩ	SEGn COMn *5
				$VOUT_{IN}$ = 8.0 V	—	2	15		
Oscillator Frequency	Internal Oscillator	fOSC	1/132 duty	Ta = 25°C 31 PWM	—	10.46	20.32	kHz	*6
	External Input	fCL			—	324.26	629.92	kHz	OSC
	Frame frequency	fFRAME			Internal OSC: fFRAME = fOSC /(Duty+1) External OSC: fFRAME = fCL /[31*(Duty+1)]			Hz	

Item		Symbol	Condition	Rating			Units	Applicable Pin
				Min.	Typ.	Max.		
Internal Power	Operating Voltage (1)	VDD VDD1	(Relative to VSS)	2.4	—	3.3	V	VSS*7
	Operating Voltage (2)	VDD2 VDD3 VDD4 VDD5	(Relative to VSS)	2.4	—	3.3	V	VSS
	Supply Step-up output voltage Circuit	$VOUT_{OUT}$	(Relative To VSS)	—	—	20	V	$VOUT_{OUT}$

	Voltage regulator Circuit Operating Voltage	$VOUT_{IN}$	(Relative To VSS)	—	—	20	V	$VOUT_{IN}$

Dynamic Consumption Current : During Display, with the Internal Power Supply OFF Current consumed by total ICs when an external power supply is used .

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern Normal	ISS	VDD = 2.8 V, Booster x 6 V0 – VSS = 13.8 V @ 1/12 bias,1/128 duty	—	500(Die)	—	μA	*8
Power Down	ISS	Ta = 25°C	—	—	10	μA	die

Notes to the DC characteristics

1. The maximum possible V_{LCD} voltage that may be generated is dependent on voltage, temperature and (display) load Internal clock.
2. Power-down mode. During power down all static currents are switched off.
3. If external V_{LCD}, the display load current is not transmitted to I_{DD}.
4. V_{LCD} external voltage applied to $VOUT_{IN}$ pin; $VOUT_{IN}$ disconnected from $VOUT_{OUT}$

References for items market with *

*1 The A0, D0 to D5, D6 (SI), D7 (SCL), /RD (E), /WR ,/(R/W), /CS, IMS, OSC, P/S, /DOF, RESB terminals.

*2 The D0 to D7.

*3 The A0,/RD (E), /WR ,/(R/W), /CS, and RES terminals.

*4 Applies when the D0 to D5, D6 (SI), D7 (SCL) terminals are in a high impedance state.

*5 These are the resistance values for when a 0.1 V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V1, V2, V3, and V4). These are specified for the operating voltage range.
RON = 0.1 V /ΔI (Where ΔI is the current that flows when 0.1 V is applied while the power supply is ON.)

*6 The relationship between the oscillator frequency and the frame rate frequency under CL dividing ratio setting = 00H.

*7 While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.

*8 It indicates the current consumed on ICs alone when the internal oscillator circuit and display are turned on.

12. TIMING CHARACTERISTICS

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

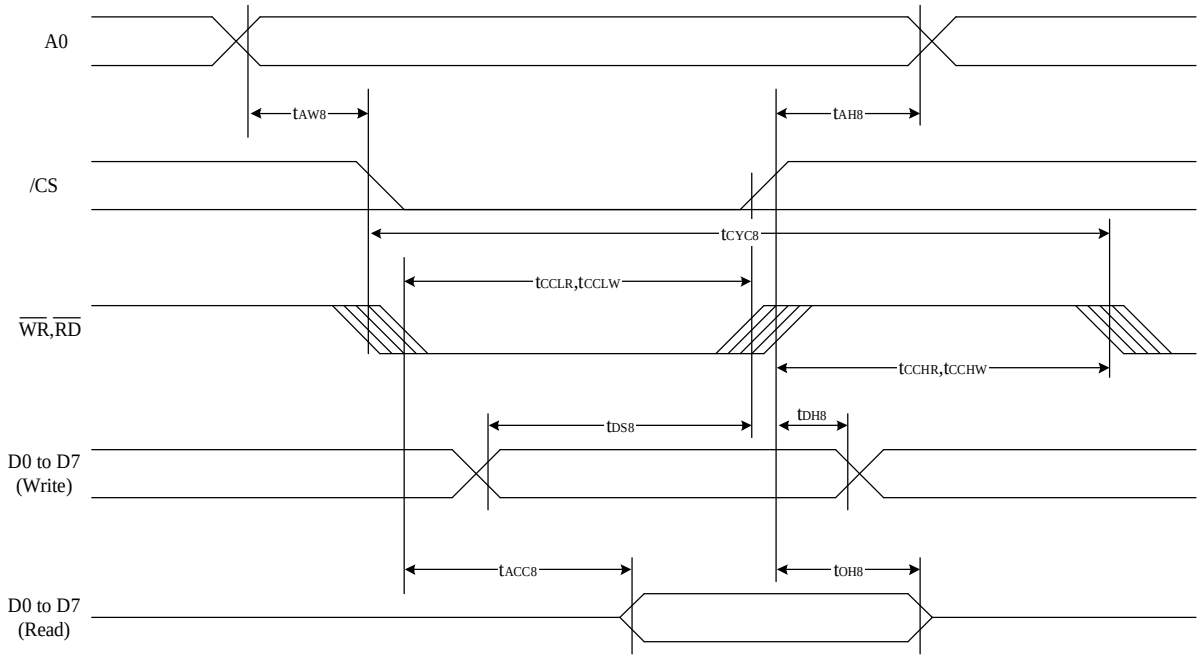


Figure 12.1

(V_{DD}=3.3V, Ta= –30 to 85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		30	—	ns
Address setup time		tAW8		30	—	
System cycle time (WRITE)	WR	tCYC8		340	—	
System frequency (WRITE)		fCYC8		2.94	—	MHz
/WR L pulse width (WRITE)		tCCLW		60	—	ns
/WR H pulse width (WRITE)		tCCHW		280	—	
System cycle time (READ)	RD	tCYC8		500	—	
/RD L pulse width (READ)		tCCLR		150	—	
/RD H pulse width (READ)		tCCHR		350	—	
WRITE data setup time	D0 to D7	tDS8		110	—	
WRITE data hold time		tDH8		30	—	
READ access time		tACC8	CL = 100 pF	—	70	
READ Output disable time		tOH8	CL = 100 pF	—	50	

(V_{DD}=2.8V,Ta= –30 to 85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		40	—	ns
Address setup time		tAW8		40	—	
System cycle time (WRITE)	WR	tCYC8		400	—	
System frequency (WRITE)		fCYC8		2.5	—	MHz
/WR L pulse width (WRITE)		tCCLW		70	—	ns
/WR H pulse width (WRITE)		tCCHW		330	—	
System cycle time (READ)	RD	tCYC8		600	—	
/RD L pulse width (READ)		tCCLR		190	—	
/RD H pulse width (READ)		tCCHR		410	—	
WRITE data setup time	D0 to D7	tDS8		120	—	
WRITE data hold time		tDH8		30	—	
READ access time		tACC8	CL = 100 pF	—	140	
READ Output disable time		tOH8	CL = 100 pF	—	100	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≦ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≦ (tCYC8 – tCCLR – tCCHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tCCLW and tCCLR are specified as the overlap between /CS being “L” and WR and RD being at the “L” level.

System Bus Read/Write Characteristics 1 (For the 6800 Series MPU)

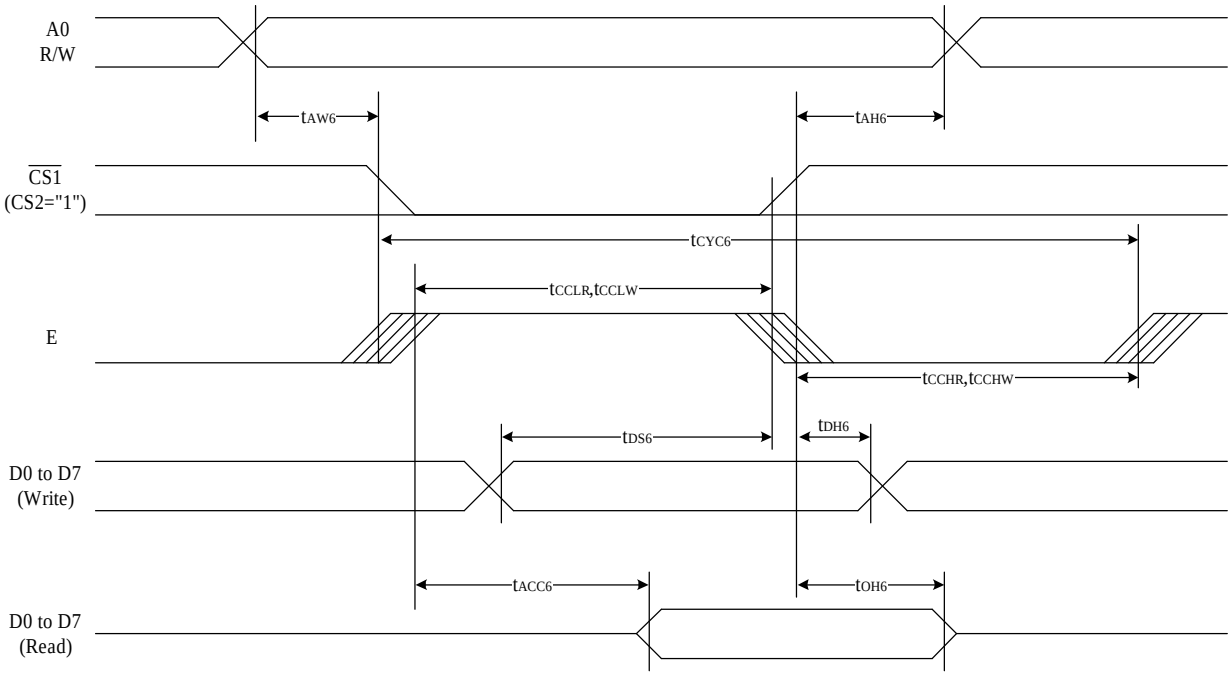


Figure 12.2

(V_{DD}=3.3V, Ta= –30 to 85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		30	—	ns
Address setup time		tAW8		30	—	
System cycle time (WRITE)	WR	tCYC8		340	—	
System frequency (WRITE)		fCYC8		2.94	—	MHz
Enable L pulse width (WRITE)		tCCLW		280	—	ns
Enable H pulse width (WRITE)		tCCHW		60	—	
System cycle time (READ)	RD	tCYC8		500	—	
Enable L pulse width (READ)		tCCLR		350	—	
Enable H pulse width (READ)		tCCHR		150	—	
WRITE data setup time	D0 to D7	tDS8		110	—	
WRITE data hold time		tDH8		30	—	
READ access time		tACC8	CL = 100 pF	—	70	
READ Output disable time		tOH8	CL = 100 pF	—	50	

(V_{DD}=2.8V, Ta= –30 to 85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		40	—	ns
Address setup time		tAW8		40	—	
System cycle time (WRITE)	WR	tCYC8		400	—	
System frequency (WRITE)		fCYC8		2.44	—	MHz
Enable L pulse width (WRITE)		tCCLW		330	—	ns
Enable H pulse width (WRITE)		tCCHW		70	—	
System cycle time (READ)	RD	tCYC8		600	—	
Enable L pulse width (READ)		tCCLR		410	—	
Enable H pulse width (READ)		tCCHR		190	—	
WRITE data setup time	D0 to D7	tDS8		120	—	
WRITE data hold time		tDH8		30	—	
READ access time		tACC8	CL = 100 pF	—	140	
READ Output disable time		tOH8	CL = 100 pF	—	100	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≦ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≦ (tCYC6 – tEWLR – tEWHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tEWLW and tEWLR are specified as the overlap between /CS being “L” and E.

Serial Interface Characteristics (For 4-Line Interface)

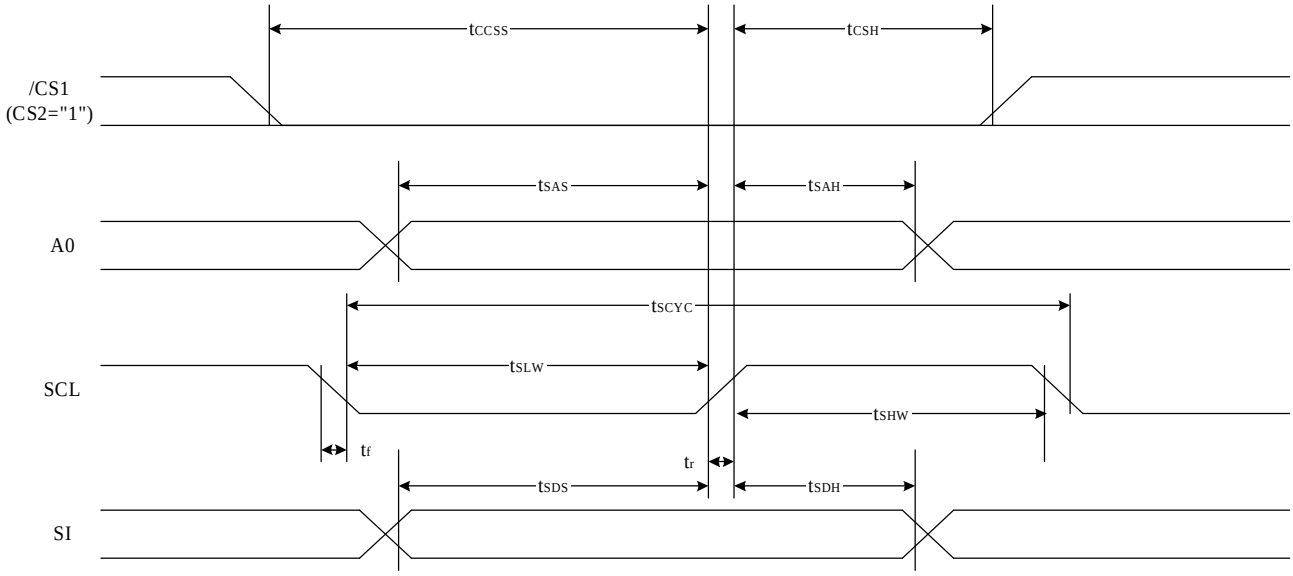


Fig 12.3

(V_{DD}=3.3V, Ta= –30 to 85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period	SCL	tSCYC		100	—	ns
Serial clock frequency		fSCYC		10	—	MHz
SCL “H” pulse width		tSHW		70	—	ns
SCL “L” pulse width		tSLW		30	—	
Address setup time	A0	tSAS		30	—	
Address hold time		tSAH		50	—	
Data setup time	SI	tSDS		20	—	
Data hold time		tSDH		50	—	
CS-SCL time	/CS	tCSS		40	—	
CS-SCL time		tCSH		80	—	

(V_{DD}=2.8V,Ta= –30 to 85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period	SCL	tSCYC		110	—	ns
Serial clock frequency		fSCYC		9.09	—	MHz
SCL “H” pulse width		tSHW		80	—	ns
SCL “L” pulse width		tSLW		30	—	
Address setup time	A0	tSAS		30	—	
Address hold time		tSAH		50	—	
Data setup time	SI	tSDS		20	—	
Data hold time		tSDH		50	—	
CS-SCL time	/CS	tCSS		40	—	
CS-SCL time		tCSH		80	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

Serial Interface Characteristics (For 3-Line Interface)

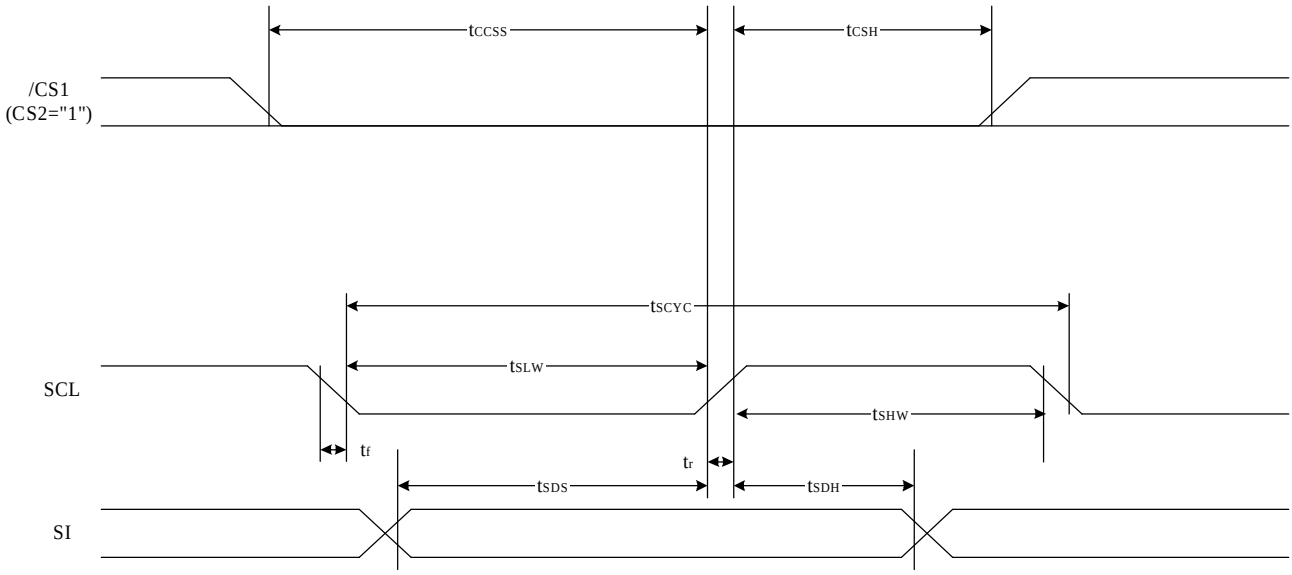


Fig 12.4

(V_{DD}=3.3V,Ta= –30 to 85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period	SCL	tSCYC		100	—	ns
Serial clock frequency		fSCYC		10	—	MHz
SCL “H” pulse width		tSHW		70	—	ns
SCL “L” pulse width		tSLW		30	—	
Data setup time	SI	tSDS		20	—	
Data hold time		tSDH		50	—	
CS-SCL time	/CS	tCSS		40	—	
CS-SCL time		tCSH		80	—	

(V_{DD}=2.8V,Ta= –30 to 85°C,die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period	SCL	tSCYC		110	—	ns
Serial clock frequency		fSCYC		9.09	—	MHz
SCL “H” pulse width		tSHW		80	—	ns
SCL “L” pulse width		tSLW		30	—	
Data setup time	SI	tSDS		20	—	
Data hold time		tSDH		50	—	
CS-SCL time	/CS	tCSS		40	—	
CS-SCL time		tCSH		80	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

(V_{DD}=2.8/3.3V, Ta= –30 to 85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
SCL clock frequency	SCL	FSCLK		—	400	kHZ
SCL clock low period	SCL	TLOW		1.3	—	us
SCL clock high period	SCL	THIGH		0.6	—	
Data set-up time	SI	TSU;Data		100	—	
Data hold time	SI	THD;Data		0	0.9	
SCL,SDA rise time	SCL	TR		20+0.1Cb	300	ns
SCL,SDA fall time	SCL	TF		20+0.1Cb	400	
Capacitive load represented by each bus line		Cb		—	400	
Setup time for a repeated START condition	SI	TSU;SUA		0.6	—	us
Start condition hold time	SI	THD;STA		0.6	—	
Setup time for STOP condition		TSU;STO		0.6	—	
Tolerable spike width on bus		TSW		—	50	
BUS free time between a STOP and START condition	SCL	TBUF		1.3	—	

13. RESET TIMING

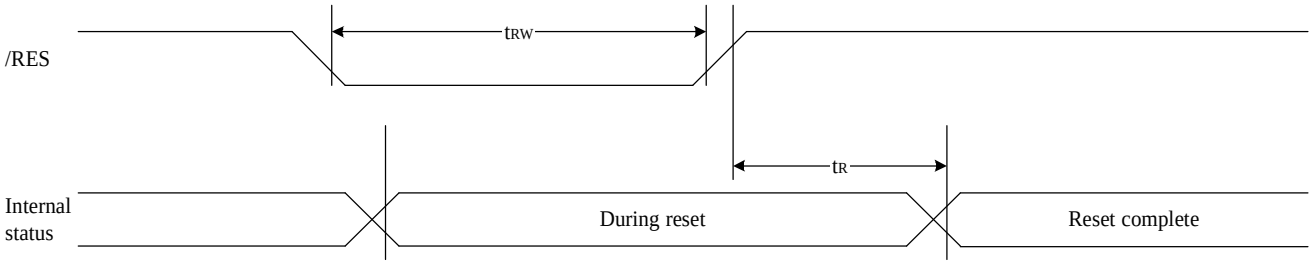


Fig 13.1

(VDD = 3.3V , Ta = –30 to 85°C, die)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		1	—	—	us
Reset “L” pulse width	RESB	tRW		1.2	—	—	us

(VDD = 2.7V , Ta = –30 to 85°C, die)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		1	—	—	us
Reset “L” pulse width	RESB	tRW		1.3	—	—	us

14. Display Application Examples between ST7636 and Panel

14.1 128 X 128 panel and CSEL=0 configuration

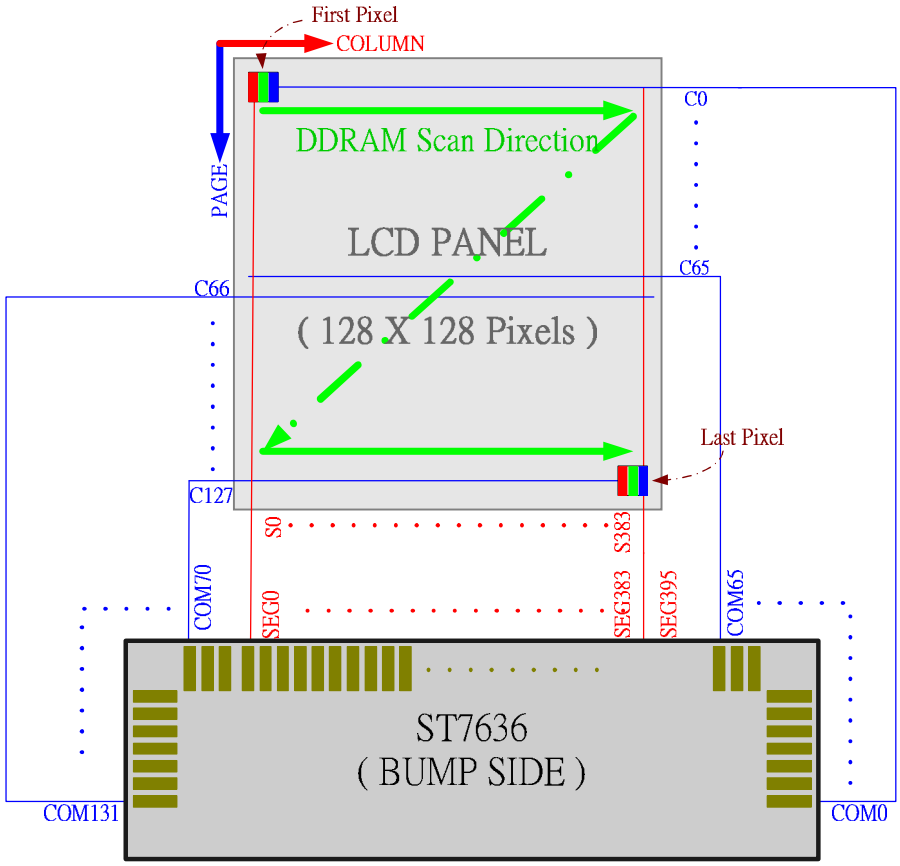


Figure 14.1 128 X 128 panel and CSEL=0 configuration

Initialize Setting：

Application Suggestion

VDD, VDD1 = 2.4 ~ 3.3 (V)
VDD2 ~ VDD5 = 2.4 ~ 3.3 (V)
Bias = 1 / 12
Duty = 128

Option Pin Setting:
CSEL = 0

Register Setting:		
COMMAND	PARAMETER	DESCRIPTION
BBH	P1 = 01H	Common scan direction
CAH	P2 = 31H	Duty = 128
75H	P1 = 0, P2 = 127	Page = 0 ~ 127
15H	P1 = 0, P2 = 127	Column = 0 ~ 127
BCH	P1 = 00H	Address scan direction
BCH	P2 = 00H	RGB arrangement

14.2 128 X 128 panel and CSEL=0 configuration

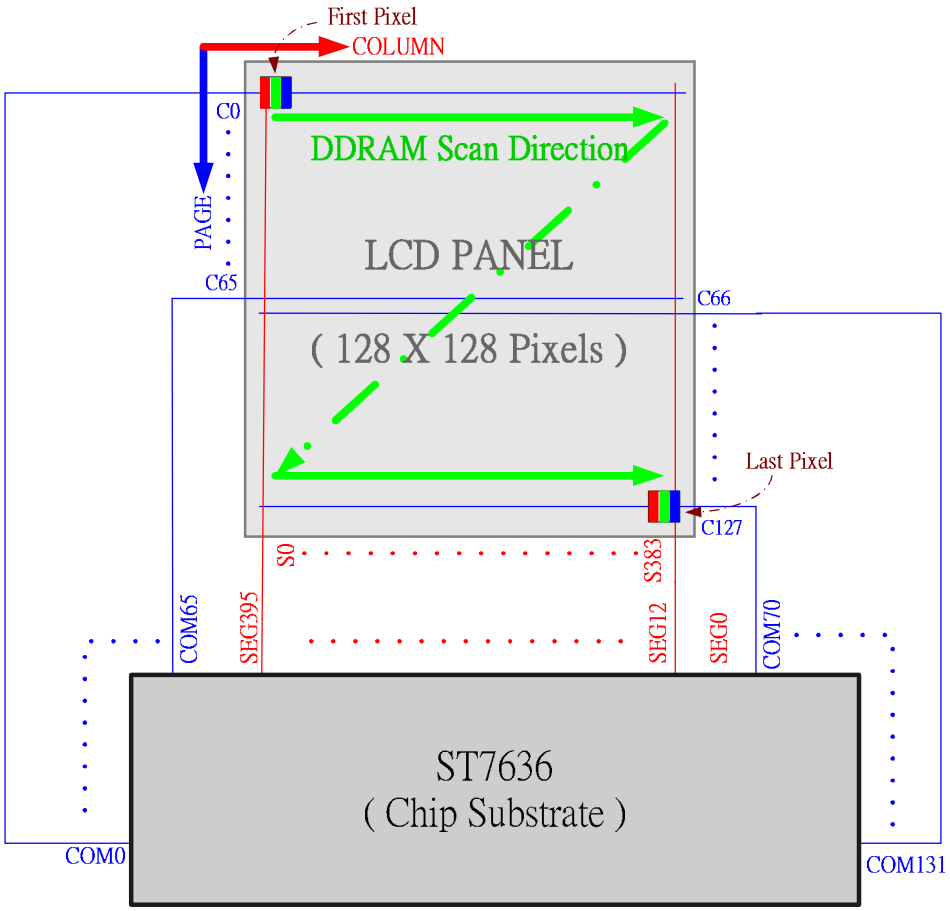


Figure 14.2 128 X 128 panel and CSEL=0 configuration

Initialize Setting：

Application Suggestion

VDD, VDD1 = 2.4 ~ 3.3 (V)
VDD2 ~ VDD5 = 2.4 ~ 3.3 (V)
Bias = 1 / 12
Duty = 128

Option Pin Setting:
CSEL = 0

Register Setting:		
COMMAND	PARAMETER	DESCRIPTION
BBH	P1 = 01H	Common scan direction
CAH	P2 = 31H	Duty = 128
75H	P1 = 0, P2 = 127	Page = 0 ~ 127
15H	P1 = 4, P2 = 131	Column = 4 ~ 131
BCH	P1 = 02H	Address scan direction
BCH	P2 = 01H	RGB arrangement

14.3 128 X 128 panel and CSEL=1 configuration

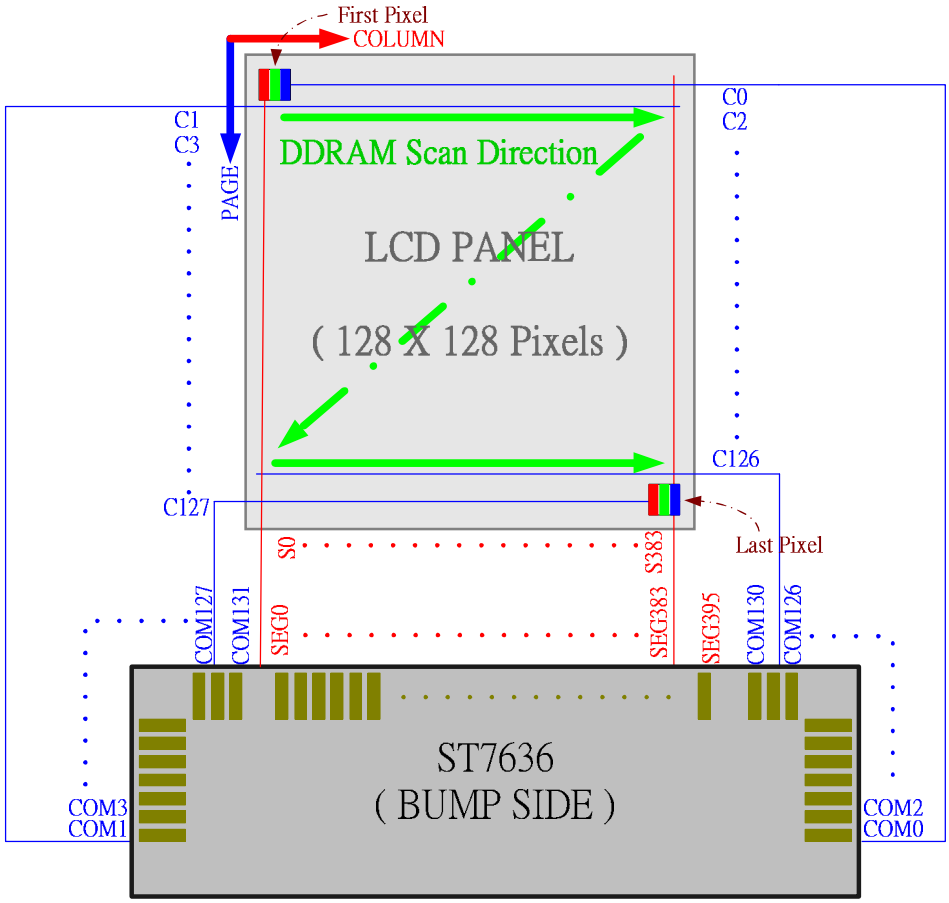


Figure 14.3 128 X 128 panel and CSEL=1 configuration

Initialize Setting：

Application Suggestion

VDD, VDD1 = 2.4 ~ 3.3 (V)
VDD2 ~ VDD5 = 2.4 ~ 3.3 (V)
Bias = 1/12
Duty = 128

Option Pin Setting:
CSEL = 1

Register Setting:		
COMMAND	PARAMETER	DESCRIPTION
CAH	P2 = 31H	Duty = 128
75H	P1 = 0, P2 = 127	Page = 0 ~ 127
15H	P1 = 0, P2 = 127	Column = 0 ~ 127
BCH	P1 = 00H	Address scan direction
BCH	P2 = 00H	RGB arrangement

14.4 128 X 128 panel and CSEL=1 configuration

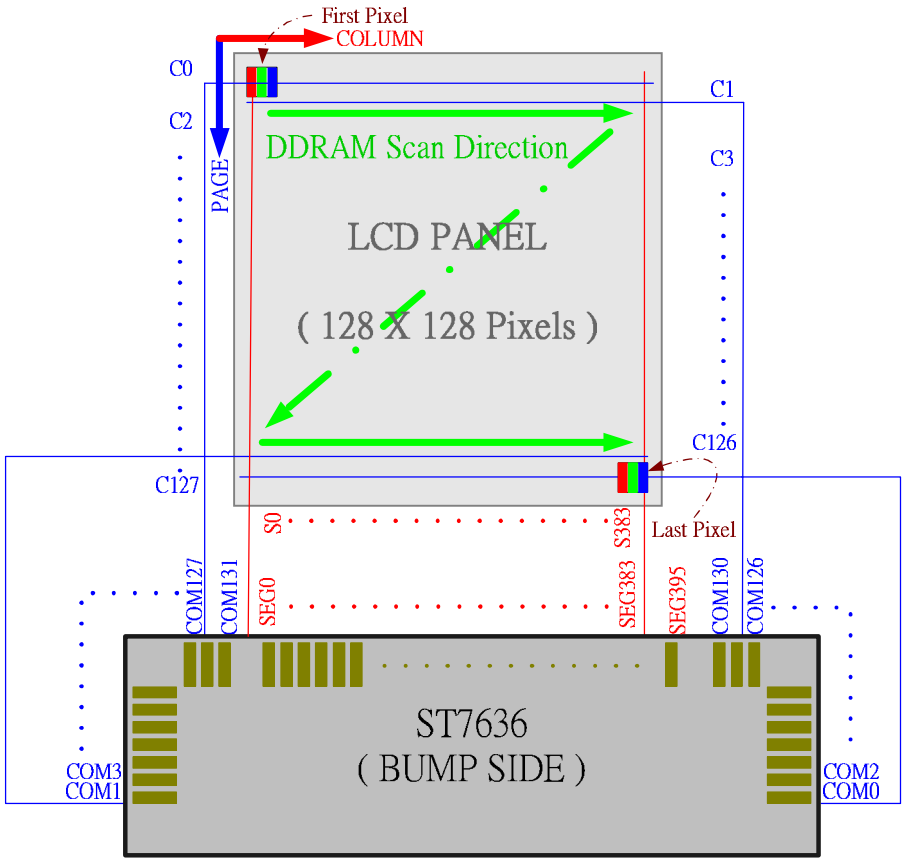


Figure 14.4 128 X 128 panel and CSEL=1 configuration

Initialize Setting：

Application Suggestion

VDD, VDD1 = 2.4 ~ 3.3 (V)
VDD2 ~ VDD5 = 2.4 ~ 3.3 (V)
Bias = 1/12
Duty = 128

Option Pin Setting:
CSEL = 1

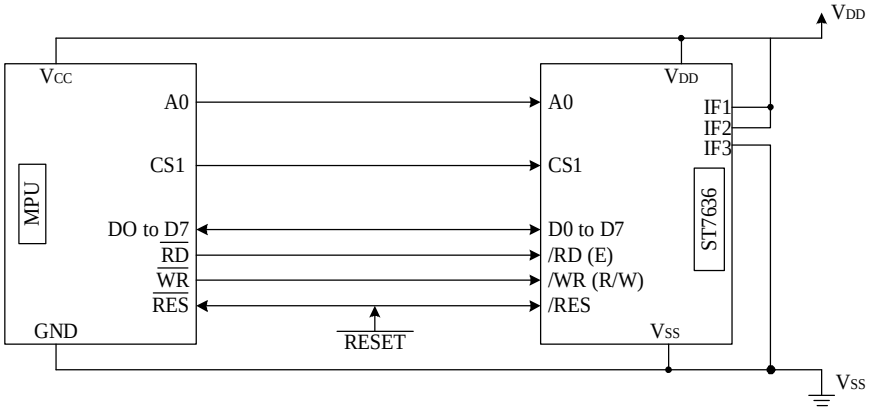
Register Setting:		
COMMAND	PARAMETER	DESCRIPTION
CAH	P2 = 31H	Duty = 128
75H	P1 = 0, P2 = 127	Page = 0 ~ 127
15H	P1 = 0, P2 = 127	Column = 0 ~ 127
BCH	P1 = 03H	Address scan direction
BCH	P2 = 00H	RGB arrangement

15. THE MPU INTERFACE (REFERENCE EXAMPLES)

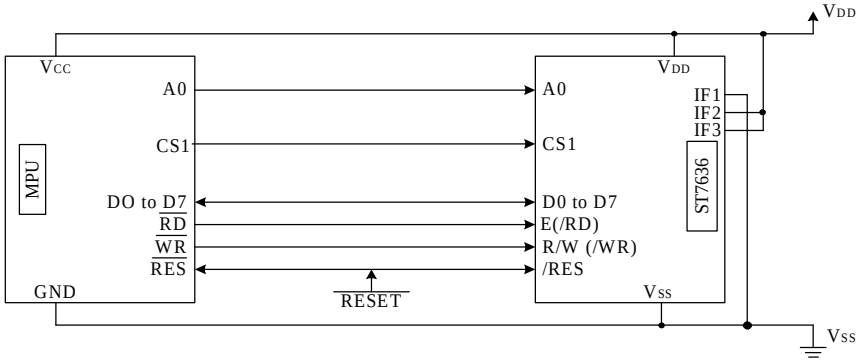
The ST7636 Series can be connected to either 8080 Series MPUs or to 6800 Series MPUs. Moreover, using the serial interface it is possible to operate the ST7636 series chips with fewer signal lines.

The display area can be enlarged by using multiple ST7636 Series chips. When this is done, the chip select signal can be used to select the individual Ics to access.

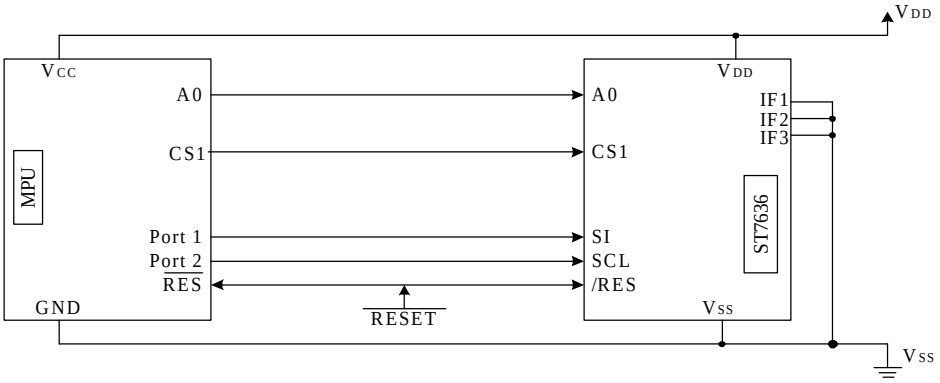
(1) 8080 Series MPUs



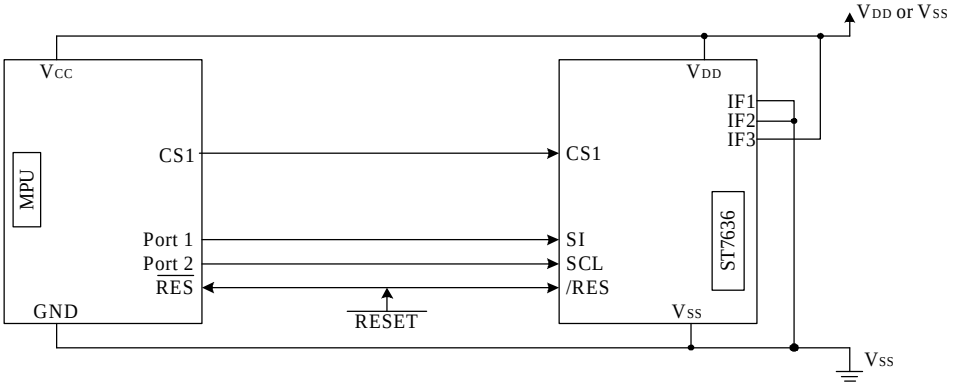
(2) 6800 Series MPUs



(3) Using the Serial Interface (4-line interface)

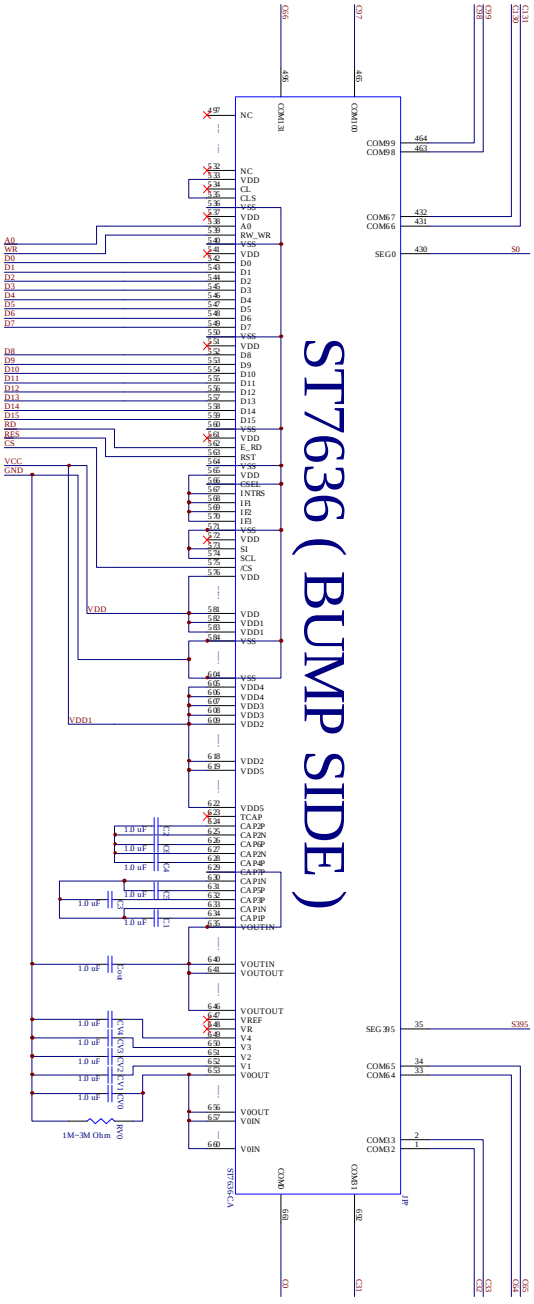


(4) Using the Serial Interface (3-line interface)



Application Circuits

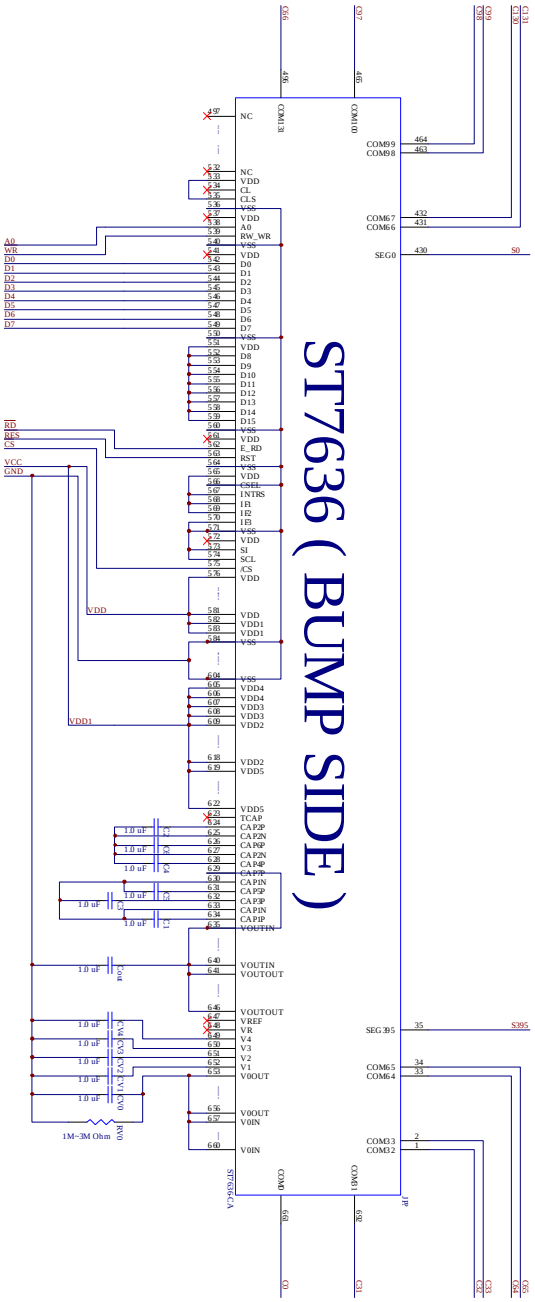
(A) 80 Series 16-bit Parallel Interface:



Interface: 80 series 16-bit Interface
Booster: 7x
Use Internal Resistors
Capacitor: 1.0 uF / 25V
Resistor: 1M ~ 3M Ohm

Application Circuits (Continue)

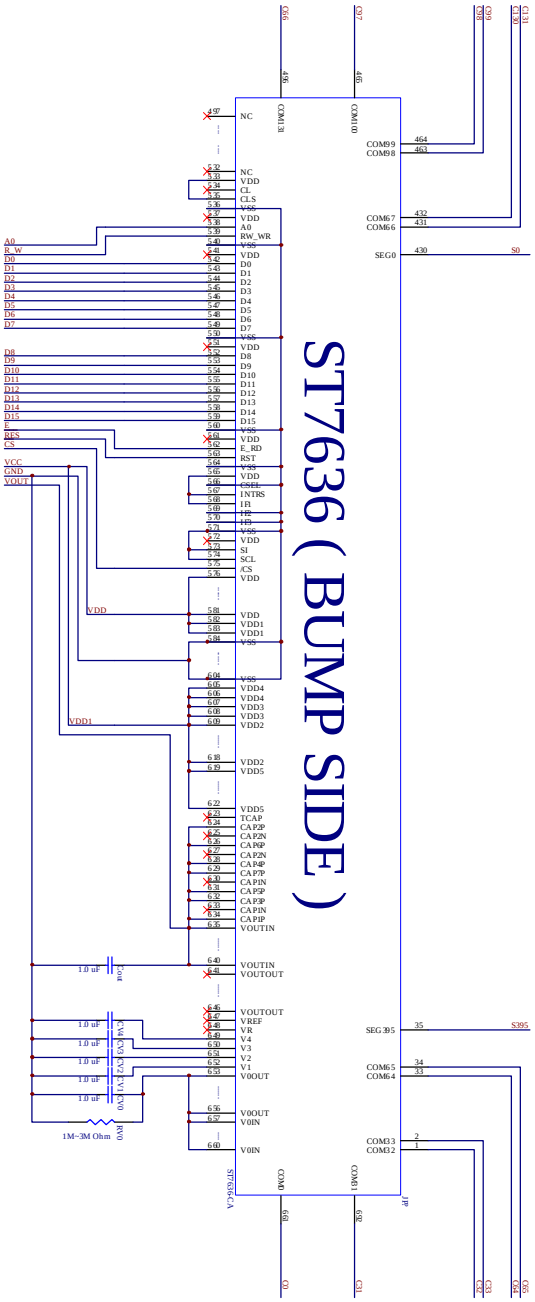
(B) 80 Series 8-bit Parallel Interface:



Interface: 80 series 8-bit Interface
Booster: 7x
Use Internal Resistors
Capacitor: 1.0 uF / 25V
Resistor: 1M ~ 3M Ohm

Application Circuits (Continue)

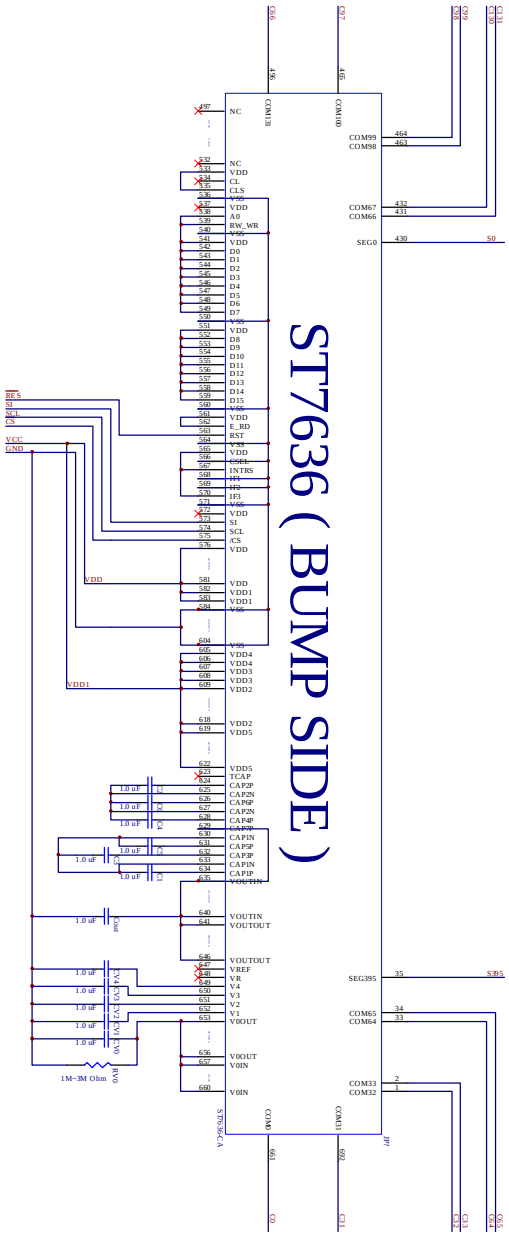
(C) 68 Series 16-bit Parallel Interface (with external power supply to VLCD):



Interface: 68 series 16-bit Interface
Booster: register VC = 0
Use External Power Supply to VLCD
Capacitor: 1.0 uF / 25V
Resistor: 1M ~ 3M Ohm

Application Circuits (Continue)

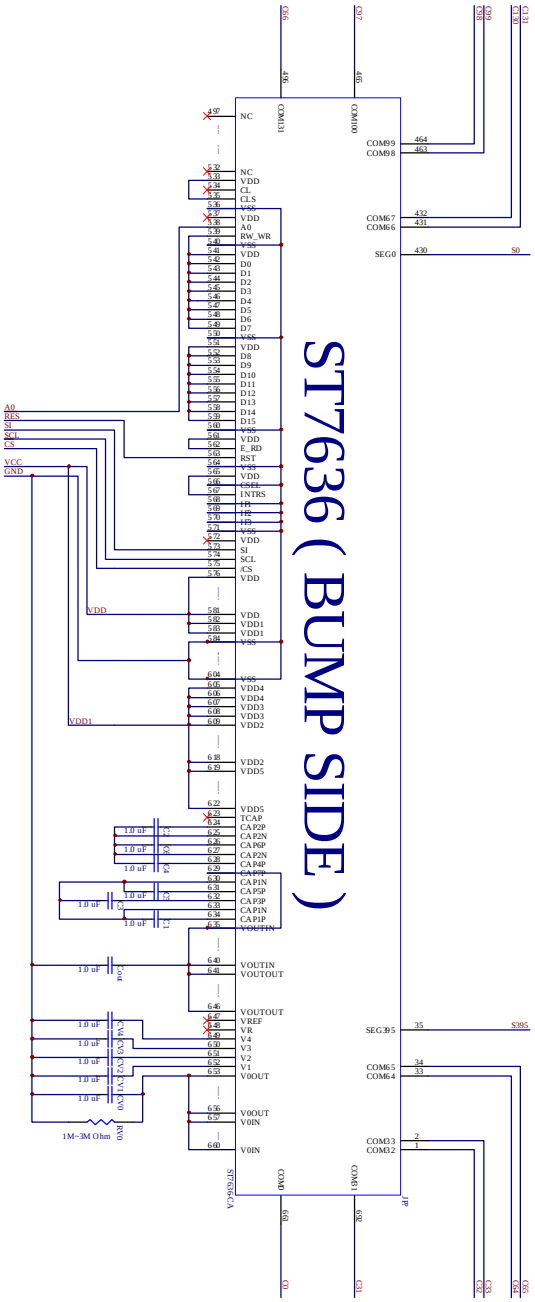
(D) 3 Line Serial Peripheral Interface:



Interface: 3 Line Serial Peripheral Interface
Booster: 7x
Use Internal Resistors
Capacitor: 1.0 uF / 25V
Resistor: 1M ~ 3M Ohm

Application Circuits (Continue)

(E) 4 Line Serial Peripheral Interface:



Interface: 4 Line Serial Peripheral Interface
Booster: 7x
Use Internal Resistors
Capacitor: 1.0 uF / 25V
Resistor: 1M ~ 3M Ohm

Microprocessor interface pins should not be floating in any operation mode.

ST7636 Serial Specification Revision History		
Version	**Date**	**Description**
1.0	2004/12/8	Remove preliminary and correct some typographic errors
1.1	2005/05/13	To change bump size, height and chip thickness To change some indications in 7.10 section, including voltage converter, thermal gradient, EEPROM setting flow and demo program WriteEEPROM() To add demo program LoadPaint() To correct some typographic errors
1.2	2005/9/15	1. Modify Limiting Value and DC Characteristic a. Temperature gradient (Add tolerance) b. Supply voltage (no tolerance). c. Bump height d. Operating and storage temperature. 2. Add die note. 3. Modify EEPROM $VOUT_{IN}$ must be more than 17V. 4. Delete about IIC function and 2-line.
1.3	2006/8/15	Add microprocessor notice item(p.16, p.98).