1 Introduction

The ST7735 is a single-chip controller/driver for 262K-color, graphic type TFT-LCD. It consists of 396 source line and 162 gate line driving circuits. This chip is capable of connecting directly to an external microprocessor, and accepts Serial Peripheral Interface (SPI), 8-bit/9-bit/16-bit/18-bit parallel interface. Display data can be stored in the on-chip display data RAM of 132 x 162 x 18 bits. It can perform display data RAM read/write operation with no external operation clock to minimize power consumption. In addition, because of the integrated power supply circuits necessary to drive liquid crystal, it is possible to make a display system with fewer components.

2 Features

Single chip TFT-LCD Controller/Driver with RAM

- On-chip Display Data RAM (i.e. Frame Memory)
  - 132 (H) x RGB x 162 (V) bits

LCD Driver Output Circuits:
- Source Outputs: 132 RGB channels
- Gate Outputs: 162 channels
- Common electrode output

Display Resolution
- 132 (RGB) x 162
  (GM[2:0]= "000", DDRAM: 132 x 18-bits x 162)
- 128 (RGB) x 160
  (GM[2:0]= "011", DDRAM: 128 x 18-bits x 160)

Display Colors (Color Mode)
- Full Color: 262K, RGB=(666) max., Idle Mode OFF
- Color Reduce: 8-color, RGB=(111), Idle Mode ON

Programmable Pixel Color Format (Color Depth) for Various Display Data input Format
- 12-bit/pixel: RGB=(444) using the 384k-bit frame memory and LUT
- 16-bit/pixel: RGB=(565) using the 384k-bit frame memory and LUT
- 18-bit/pixel: RGB=(666) using the 384k-bit frame memory and LUT

Various Interfaces
- Parallel 8080-series MCU Interface
  (8-bit, 9-bit, 16-bit & 18-bit)
- 3-line serial interface
- 4-line serial interface

Display Features
- Programmable partial display duty
- Line inversion, frame inversion
- Support both normal-black & normal-white LC
- Software programmable color depth mode

Built-in Circuits
- DC/DC converter
- Adjustable VCOM generation
- Non-volatile (NV) memory to store initial register setting
- Oscillator for display clock generation
- Factory default value (module ID, module version, etc) are stored in NV memory
- Timing controller

Built-in NV Memory for LCD Initial Register Setting
- 7-bits for ID2
- 8-bits for ID3
- 7-bits for VCOM adjustment

Wide Supply Voltage Range
- I/O Voltage (VDDI to DGND): 1.65V~VDD (VDDI ≤ VDD)
- Analog Voltage (VDD to AGND): 2.6V~3.3V

On-Chip Power System
- Source Voltage (GVDD to AGND): 3.0V~5.0V
- VCOM HIGH level (VCOMH to AGND): 2.5V to 5.0V
- VCOM LOW level (VCOML to AGND): -2.4V to 0.0V
- Gate driver HIGH level (VGH to AGND):
  +10.0V to +15V
- Gate driver LOW level (VGL to AGND):
  -12.4V to -7.5V

Operating Temperature: -30°C to +85°C
3 Pad arrangement
3.1 Output Bump Dimension

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Chip size (um x um): 9900 x 670
PAD coordinate: pad center
Coordinate origin: chip center
Chip thickness (um): 300 (TYP)
Bump height (um): 12 (TYP)
Bump hardness (HV): 75 (TYP)
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# Driver IC Pin Description

## 6.1 Power Supply Pin

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<td>I</td>
<td>Power supply for analog, digital system and booster circuit.</td>
<td>VDD</td>
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<tr>
<td>VDDI</td>
<td>I</td>
<td>Power supply for I/O system.</td>
<td>VDDI</td>
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<tr>
<td>AGND</td>
<td>I</td>
<td>System ground for analog system and booster circuit.</td>
<td>GND</td>
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<tr>
<td>DGND</td>
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<td>System ground for I/O system and digital system.</td>
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## 6.2 Interface logic pin

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<td>MCU Parallel interface bus and Serial interface select</td>
<td>DGND/VDDI</td>
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<td>IM2=’1’, Parallel interface</td>
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<tr>
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<td></td>
<td>IM2=’0’, Serial interface</td>
<td></td>
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<tr>
<td>IM1,IM0</td>
<td>I</td>
<td>- MCU parallel interface type selection</td>
<td>DGND/VDDI</td>
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<td>- If not used, please fix this pin at VDDI or DGND level.</td>
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<td><strong>Parallel interface</strong></td>
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<td>SPI4W</td>
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<td>- SPI4W=’0’, 3-line SPI enable.</td>
<td>DGND/VDDI</td>
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<td>- SPI4W=’1’, 4-line SPI enable.</td>
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<td>- If not used, please fix this pin at DGND level.</td>
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<td>RESX</td>
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<td>- This signal will reset the device and it must be applied to properly</td>
<td>MCU</td>
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<tr>
<td></td>
<td></td>
<td>initialize the chip.</td>
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<tr>
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<td>- Signal is active low.</td>
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<td>CSX</td>
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<td>- Chip selection pin</td>
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<td></td>
<td>- Low enable.</td>
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<tr>
<td>D/CX</td>
<td>I</td>
<td>- Display data/command selection pin in MCU interface.</td>
<td>MCU</td>
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<tr>
<td>(SCL)</td>
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<td>- D/CX=’1’: display data or parameter.</td>
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<tr>
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<td></td>
<td>- D/CX=’0’: command data.</td>
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<td>- In serial interface, this is used as SCL.</td>
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<td>- If not used, please fix this pin at VDDI or DGND level.</td>
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<td>RDX</td>
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<td>- Read enable in 8080 MCU parallel interface.</td>
<td>MCU</td>
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<td>- If not used, please fix this pin at VDDI or DGND level.</td>
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<td>WRX</td>
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<td>- Write enable in MCU parallel interface.</td>
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<td>(D/CX)</td>
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<td>- In 4-line SPI, this pin is used as D/CX (data/command selection).</td>
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<td>- If not used, please fix this pin at VDDI or DGND level.</td>
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<tr>
<td>D[17:0]</td>
<td>I/O</td>
<td>- D[17:0] are used as MCU parallel interface data bus.</td>
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- **D0** is the serial input/output signal in serial interface mode.
  - In serial interface, D[17:1] are not used and should be fixed at VDD or DGND level.

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<td>Tearing effect output pin to synchronize MCU to frame rate, activated by S/W command. If not used, please open this pin.</td>
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<td>OSC</td>
<td>Monitoring pin of internal oscillator clock and is turned ON/OFF by S/W command. When this pin is inactive (function OFF), this pin is DGND level. If not used, please open this pin.</td>
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**Note1.** When in parallel mode, no use data pin must be connected to “1” or “0”.

**Note2.** When CSX=“1”, there is no influence to the parallel and serial interface.
### 6.3 Mode selection pin

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<td><strong>EXTC</strong></td>
<td>I</td>
<td>-During normal operation, please open this pin</td>
<td>Open</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>EXTC</strong> Enable/disable modification of extend command</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
<td>System function command list can be used.</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>All command list can be used.</td>
<td></td>
</tr>
<tr>
<td><strong>GM2, GM1, GM0</strong></td>
<td>I</td>
<td>-Panel resolution selection pins.</td>
<td>VDDI/DGND</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>GM</strong> Selection of panel resolution</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>GM= '000' 132RGB x 162 (S1<del>S396 &amp; G1</del>G162 output)</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>GM= '011' 128RGB x 160 (S7<del>S390 &amp; G2</del>G161 output)</td>
<td></td>
</tr>
<tr>
<td><strong>SRGB</strong></td>
<td>I</td>
<td>-RGB direction select H/W pin for color filter setting.</td>
<td>VDDI/DGND</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>SRGB</strong> RGB arrangement</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
<td>S1, S2, S3 filter order = 'R', 'G', 'B'</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>S1, S2, S3 filter order = 'B', 'G', 'R'</td>
<td></td>
</tr>
<tr>
<td><strong>SMX</strong></td>
<td>I</td>
<td>-Module source output direction H/W selection pin.</td>
<td>VDDI/DGND</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>SMX</strong> Scanning direction of source output</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
<td>GM= '000' S1 -&gt; S396 S7 -&gt; S390</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>GM= '011' S396 -&gt; S1 S390 -&gt; S7</td>
<td></td>
</tr>
<tr>
<td><strong>SMY</strong></td>
<td>I</td>
<td>-Module Gate output direction H/W selection pin.</td>
<td>VDDI/DGND</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>SMY</strong> Scanning direction of gate output</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
<td>GM= '000' G1 -&gt; G162 G2 -&gt; G161</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>GM= '011' G162 -&gt; G1 G161 -&gt; G2</td>
<td></td>
</tr>
<tr>
<td><strong>LCM</strong></td>
<td>I</td>
<td>-Liquid crystal (LC) type selection pins.</td>
<td>VDDI/DGND</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>LCM</strong> Selection of LC type</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
<td>Normally white LC type</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>Normally black LC type</td>
<td></td>
</tr>
<tr>
<td><strong>GS</strong></td>
<td>I</td>
<td>-Gamma curve selection pin.</td>
<td>VDDI/DGND</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>GS</strong> Selection of gamma curve</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
<td>GC0=1.0, GC1=2.5, GC2=2.2, GC3=1.8</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>GC0=2.2, GC1=1.8, GC2=2.5, GC3=1.0</td>
<td></td>
</tr>
<tr>
<td>TESEL</td>
<td>Input pin to select horizontal line number in TE signal. This pin is only for GM[2:0]='000' mode</td>
<td></td>
<td></td>
</tr>
<tr>
<td>-------</td>
<td>------------------------------------------------------------------------------------------------</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>TESEL='0', TE output 162 lines</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>TESEL='1', TE output 160 lines</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VDDI/DGND</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### 6.4 Driver output pins

<table>
<thead>
<tr>
<th>Name</th>
<th>I/O</th>
<th>Description</th>
<th>Connect pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1 to S396</td>
<td>O</td>
<td>Source driver output pins.</td>
<td>-</td>
</tr>
<tr>
<td>G1 to G162</td>
<td>O</td>
<td>Gate driver output pins.</td>
<td>-</td>
</tr>
<tr>
<td>VCl1</td>
<td>I/O</td>
<td>- Hi-Z</td>
<td>-</td>
</tr>
<tr>
<td>AVDD</td>
<td>I</td>
<td>- Power input pin for analog circuits.</td>
<td>AVDDO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- In normal usage, connect it to AVDDO.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>- AVDD = 5.3V.</td>
<td></td>
</tr>
<tr>
<td>AVDDO</td>
<td>O</td>
<td>- Output of step-up circuit 1</td>
<td>Capacitor</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Connect a capacitor for stabilization.</td>
<td></td>
</tr>
<tr>
<td>VCL</td>
<td>O</td>
<td>- A power supply pin for generating VCOML.</td>
<td>Capacitor</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Connect a capacitor for stabilization.</td>
<td></td>
</tr>
<tr>
<td>VGH</td>
<td>I</td>
<td>- Power input pin for gate driver circuit.</td>
<td>VGHO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- In normal usage, connect it to VGHO.</td>
<td></td>
</tr>
<tr>
<td>VGHO</td>
<td>O</td>
<td>- Positive output pin of the step-up circuit 2.</td>
<td>Capacitor</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Connect a capacitor for stabilization.</td>
<td></td>
</tr>
<tr>
<td>VGL</td>
<td>I</td>
<td>- Power input pin for gate driver circuit.</td>
<td>Capacitor</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Negative output of the step-up circuit 2 is connected inside the driver.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Connect a capacitor for stabilization.</td>
<td></td>
</tr>
<tr>
<td>VREF</td>
<td>O</td>
<td>- A reference voltage for power system.</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- This test pin for Driver vender test used.</td>
<td></td>
</tr>
<tr>
<td>GVDD</td>
<td>O</td>
<td>- A power output of grayscale voltage generator.</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- When internal GVDD generator is not used, connect an external power supply (AVDD-0.5V) to this pin.</td>
<td></td>
</tr>
<tr>
<td>VCOMH</td>
<td>O</td>
<td>- Positive voltage output of VCOM.</td>
<td>Capacitor</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Connect a capacitor for stabilization.</td>
<td></td>
</tr>
<tr>
<td>VCOML</td>
<td>O</td>
<td>- Negative voltage output of VCOM.</td>
<td>Capacitor</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Connect a capacitor for stabilization.</td>
<td></td>
</tr>
<tr>
<td>VCOM</td>
<td>O</td>
<td>- A power supply for the TFT-LCD common electrode.</td>
<td>Common electrode</td>
</tr>
<tr>
<td>C11P, C11N</td>
<td>O</td>
<td>- Capacitor connecting pins for step-up circuit 1 (for AVDDO)</td>
<td>Step-up Capacitor</td>
</tr>
<tr>
<td>C22P, C22N</td>
<td>O</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C23P, C23N</td>
<td>O</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C41P, C41N</td>
<td>O</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### ST7735

<table>
<thead>
<tr>
<th>Name</th>
<th>I/O</th>
<th>Description</th>
<th>Connect pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDIO</td>
<td>O</td>
<td>-VDDI voltage output level for monitoring.</td>
<td>-</td>
</tr>
<tr>
<td>DGND</td>
<td>O</td>
<td>-DGND voltage output level for monitoring.</td>
<td>-</td>
</tr>
<tr>
<td>VCC</td>
<td>I</td>
<td>-Power input pin for internal digital reference voltage.</td>
<td>VCCO</td>
</tr>
<tr>
<td>VCCO</td>
<td>O</td>
<td>-Monitoring pin of internal digital reference voltage.</td>
<td>Capacitor</td>
</tr>
</tbody>
</table>

#### 6.5 Test pins

<table>
<thead>
<tr>
<th>Name</th>
<th>I/O</th>
<th>Description</th>
<th>Connect pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPI[2]</td>
<td>I</td>
<td>-These test pins for Driver vendor test used.</td>
<td>DGND</td>
</tr>
<tr>
<td>TPI[1]</td>
<td></td>
<td>-Please connect these pins to DGND.</td>
<td></td>
</tr>
<tr>
<td>TPO[8]</td>
<td>O</td>
<td>-These test pins for Driver vendor test used.</td>
<td>Open</td>
</tr>
<tr>
<td>TPO[7]</td>
<td></td>
<td>-Please open these pins.</td>
<td></td>
</tr>
<tr>
<td>TPO[6]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TPO[5]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TPO[4]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TPO[3]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TPO[2]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TPO[1]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dummy</td>
<td>-</td>
<td>-These pins are dummy (have no function inside).</td>
<td>Open</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-Can allow signal traces pass through these pads on TFT glass.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>-Please open these pins.</td>
<td></td>
</tr>
</tbody>
</table>
7 Driver electrical characteristics

7.1 Absolute operation range

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>VDD</td>
<td>-0.3 ~ +4.6</td>
<td>V</td>
</tr>
<tr>
<td>Supply voltage (Logic)</td>
<td>VDDI</td>
<td>-0.3 ~ +4.6</td>
<td>V</td>
</tr>
<tr>
<td>Supply voltage (Digital)</td>
<td>VCC</td>
<td>-0.3 ~ +1.95</td>
<td>V</td>
</tr>
<tr>
<td>Driver supply voltage</td>
<td>VGH-VGL</td>
<td>-0.3 ~ +30.0</td>
<td>V</td>
</tr>
<tr>
<td>Logic input voltage range</td>
<td>VIN</td>
<td>-0.3 ~ VDDI +0.3</td>
<td>V</td>
</tr>
<tr>
<td>Logic output voltage range</td>
<td>VO</td>
<td>-0.3 ~ VDDI +0.3</td>
<td>V</td>
</tr>
<tr>
<td>Operating temperature range</td>
<td>TOPR</td>
<td>-30 ~ +85</td>
<td>℃</td>
</tr>
<tr>
<td>Storage temperature range</td>
<td>TSTG</td>
<td>-40 ~ +125</td>
<td>℃</td>
</tr>
</tbody>
</table>

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

7.2 DC characteristic

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Specification</th>
<th>Unit</th>
<th>Related Pins</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>Power &amp; operation voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>System voltage</td>
<td>VDD</td>
<td>Operating voltage</td>
<td>2.6</td>
<td>2.75</td>
<td>3.3</td>
</tr>
<tr>
<td>Interface operation voltage</td>
<td>VDDI</td>
<td>I/O supply voltage</td>
<td>1.65</td>
<td>1.9</td>
<td>3.3</td>
</tr>
<tr>
<td>Gate driver high voltage</td>
<td>VGH</td>
<td></td>
<td>10</td>
<td></td>
<td>15</td>
</tr>
<tr>
<td>Gate driver low voltage</td>
<td>VGL</td>
<td></td>
<td>-12.4</td>
<td></td>
<td>-7.5</td>
</tr>
<tr>
<td>Gate driver supply voltage</td>
<td></td>
<td></td>
<td>17.5</td>
<td>27.5</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input / Output</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic-high input voltage</td>
<td>VIH</td>
<td></td>
<td>0.7VDDI</td>
<td>VDDI</td>
<td></td>
</tr>
<tr>
<td>Logic-low input voltage</td>
<td>VIL</td>
<td></td>
<td>VSS</td>
<td>0.3VDDI</td>
<td>V</td>
</tr>
<tr>
<td>Logic-high output voltage</td>
<td>VOH</td>
<td>IOH = -1.0mA</td>
<td>0.8VDDI</td>
<td>VDDI</td>
<td></td>
</tr>
<tr>
<td>Logic-low output voltage</td>
<td>VOL</td>
<td>IOL = +1.0mA</td>
<td>VSS</td>
<td>0.2VDDI</td>
<td>V</td>
</tr>
<tr>
<td>Logic-high input current</td>
<td>IIH</td>
<td>VIN = VDDI</td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Logic-low input current

<table>
<thead>
<tr>
<th></th>
<th>IIL</th>
<th>VIN = VSS</th>
<th></th>
<th></th>
<th></th>
<th>Note 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input leakage current</td>
<td>IIL</td>
<td>IOH = -1.0mA</td>
<td>-0.1</td>
<td></td>
<td>+0.1</td>
<td>uA</td>
</tr>
</tbody>
</table>

### VCOM voltage

<table>
<thead>
<tr>
<th>VCOM high voltage</th>
<th>VCOMH</th>
<th>Ccom=12nF</th>
<th></th>
<th></th>
<th></th>
<th>V</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCOM low voltage</td>
<td>VCOML</td>
<td>Ccom=12nF</td>
<td>-2.4</td>
<td></td>
<td>0.0</td>
<td>V</td>
</tr>
<tr>
<td>VCOM amplitude</td>
<td>VCOMAC</td>
<td>[VCOMH-VCOML]</td>
<td>4.0</td>
<td></td>
<td>6.0</td>
<td>V</td>
</tr>
</tbody>
</table>

### Source driver

<table>
<thead>
<tr>
<th>Source output range</th>
<th>Vsout</th>
<th></th>
<th></th>
<th>AVDD-0.1</th>
<th>V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gamma reference voltage</td>
<td>GVDD</td>
<td>3.0</td>
<td>5.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Source output settling time</td>
<td>Tr</td>
<td>Below with 99% precision</td>
<td>20</td>
<td>us</td>
<td>Note 2</td>
</tr>
<tr>
<td>Output offset voltage</td>
<td>Voffset</td>
<td>35</td>
<td>mV</td>
<td>Note 3</td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**

1. VDDI=1.65 to 3.3V, VDD=2.6 to 3.3V, AGND=DGND=0V, TA= -30 to 85°C
2. Source channel loading= 2KΩ+12pF/channel, Gate channel loading=5KΩ+40pF/channel.
3. The Max. value is between measured point of source output and gamma setting value.
## 7.3 Power consumption

VDD=2.8V, VDDI=1.8V, Ta=25°C, Frame rate = 60Hz, the registers setting are IC default setting.

<table>
<thead>
<tr>
<th>Operation mode</th>
<th>Inversion mode</th>
<th>Image</th>
<th>Current consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Typical</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IDDI (mA)</td>
</tr>
<tr>
<td>Normal mode</td>
<td>One Line</td>
<td>Note 1</td>
<td>0.01</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Note 2</td>
<td>0.01</td>
</tr>
<tr>
<td>Partial + Idle mode</td>
<td>One Line</td>
<td>Note 1</td>
<td>0.01</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Note 2</td>
<td>0.01</td>
</tr>
<tr>
<td>Sleep-in mode</td>
<td>N/A</td>
<td>N/A</td>
<td>0.005</td>
</tr>
</tbody>
</table>

Notes:

1. All pixels black.
2. All pixels white.
3. The Current Consumption is DC characteristics of ST7735.
8 Timing chart
8.1 Parallel interface characteristics: 18, 16, 9 or 8-bit bus (8080 series MCU interface)

<table>
<thead>
<tr>
<th>Signal</th>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D/CX</td>
<td>TAST</td>
<td>Address setup time</td>
<td>10</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>TAHT</td>
<td>Address hold time (Write/Read)</td>
<td>10</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CSX</td>
<td>TCHW</td>
<td>Chip select “H” pulse width</td>
<td>0</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>TCS</td>
<td>Chip select setup time (Write)</td>
<td>15</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>TRCS</td>
<td>Chip select setup time (Read ID)</td>
<td>45</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>TRCSFM</td>
<td>Chip select setup time (Read FM)</td>
<td>350</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>TCSF</td>
<td>Chip select wait time (Write/Read)</td>
<td>10</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>TCSH</td>
<td>Chip select hold time</td>
<td>10</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>WRX</td>
<td>TWC</td>
<td>Write cycle</td>
<td>100</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>TWRH</td>
<td>Control pulse “H” duration</td>
<td>30</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>TWRL</td>
<td>Control pulse “L” duration</td>
<td>30</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RDX (ID)</td>
<td>TRC</td>
<td>Read cycle (ID)</td>
<td>160</td>
<td>ns</td>
<td></td>
<td>When read ID data</td>
</tr>
<tr>
<td></td>
<td>TRDH</td>
<td>Control pulse “H” duration (ID)</td>
<td>90</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>TRDL</td>
<td>Control pulse “L” duration (ID)</td>
<td>45</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RDX (FM)</td>
<td>TRCFM</td>
<td>Read cycle (FM)</td>
<td>450</td>
<td>ns</td>
<td></td>
<td>When read from frame memory</td>
</tr>
<tr>
<td></td>
<td>TRDHF</td>
<td>Control pulse “H” duration (FM)</td>
<td>150</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>TRDLFM</td>
<td>Control pulse “L” duration (FM)</td>
<td>150</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Table 8.1.1 Parallel Interface Characteristics

<table>
<thead>
<tr>
<th>D[17:0]</th>
<th>TDST</th>
<th>Data setup time</th>
<th>10 ns</th>
</tr>
</thead>
<tbody>
<tr>
<td>TDHT</td>
<td></td>
<td>Data hold time</td>
<td>10 ns</td>
</tr>
<tr>
<td>TRAT</td>
<td></td>
<td>Read access time (ID)</td>
<td>40 ns</td>
</tr>
<tr>
<td>TRATFM</td>
<td></td>
<td>Read access time (FM)</td>
<td>40 ns</td>
</tr>
<tr>
<td>TODH</td>
<td></td>
<td>Output disable time</td>
<td>80 ns</td>
</tr>
</tbody>
</table>

Note: VDDI=1.65 to 3.3V, VDD=2.6 to 3.3V, AGND=DGND=0V, Ta=25 °C

V_{IH} = 0.7 \times VDDI
V_{IL} = 0.3 \times VDDI
T_R = T_F \leq 15 \text{ns}

For CL=30pF

V_{OH} = 0.8 \times VDDI
V_{OL} = 0.2 \times VDDI
T_R = T_F \leq 15 \text{ns}

Note: The rising time and falling time (T_R, T_F) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for input signals.
8.2 Serial interface characteristics (3-line serial)

![3-line serial interface timing diagram]

**Table 8.2.1 3-line Serial Interface Characteristics**

<table>
<thead>
<tr>
<th>Signal</th>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSX</td>
<td>TCSS</td>
<td>Chip select setup time (write)</td>
<td>15</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TCSH</td>
<td>Chip select hold time (write)</td>
<td>15</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TCSS</td>
<td>Chip select setup time (read)</td>
<td>60</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TSCC</td>
<td>Chip select hold time (read)</td>
<td>65</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TCHW</td>
<td>Chip select “H” pulse width</td>
<td>40</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SCL</td>
<td>TSCYCW</td>
<td>Serial clock cycle (Write)</td>
<td>66</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TSHW</td>
<td>SCL “H” pulse width (Write)</td>
<td>30</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TSLW</td>
<td>SCL “L” pulse width (Write)</td>
<td>30</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TSCYCR</td>
<td>Serial clock cycle (Read)</td>
<td>150</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TSHR</td>
<td>SCL “H” pulse width (Read)</td>
<td>60</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TSLR</td>
<td>SCL “L” pulse width (Read)</td>
<td>60</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SDA</td>
<td>TSDS</td>
<td>Data setup time</td>
<td>10</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>(DIN)</td>
<td>TSDH</td>
<td>Data hold time</td>
<td>10</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>(DOUT)</td>
<td>TACC</td>
<td>Access time</td>
<td>10</td>
<td>50</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TOH</td>
<td>Output disable time</td>
<td>50</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

Table 8.2.1 3-line Serial Interface Characteristics

**Note 1:** VDDI=1.65 to 3.3V, VDD=2.6 to 3.3V, AGND=DGND=0V, Ta=25 °C

**Note 2:** The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for input signals.
8.3 Serial interface characteristics (4-line serial)

![Fig. 8.3.1 4-line serial interface timing](image)

<table>
<thead>
<tr>
<th>Signal</th>
<th>Symbol</th>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>Unit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSX</td>
<td>TCSS</td>
<td>Chip select setup time (write)</td>
<td>15</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TCSH</td>
<td>Chip select hold time (write)</td>
<td>15</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TCSS</td>
<td>Chip select setup time (read)</td>
<td>60</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TSCC</td>
<td>Chip select hold time (read)</td>
<td>65</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TCHW</td>
<td>Chip select “H” pulse width</td>
<td>40</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SCL</td>
<td>TSCYCW</td>
<td>Serial clock cycle (Write)</td>
<td>66</td>
<td></td>
<td>ns</td>
<td>-write command &amp; data ram</td>
</tr>
<tr>
<td></td>
<td>TSHW</td>
<td>SCL “H” pulse width (Write)</td>
<td>30</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TSLW</td>
<td>SCL “L” pulse width (Write)</td>
<td>30</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TSCYCR</td>
<td>Serial clock cycle (Read)</td>
<td>150</td>
<td></td>
<td>ns</td>
<td>-read command &amp; data ram</td>
</tr>
<tr>
<td></td>
<td>TSHR</td>
<td>SCL “H” pulse width (Read)</td>
<td>60</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TSLR</td>
<td>SCL “L” pulse width (Read)</td>
<td>60</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>D/CX</td>
<td>TDCS</td>
<td>D/CX setup time</td>
<td></td>
<td>0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TDCH</td>
<td>D/CX hold time</td>
<td></td>
<td>10</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SDA (DIN) (DOUT)</td>
<td>TSDS</td>
<td>Data setup time</td>
<td>10</td>
<td></td>
<td>ns</td>
<td>For maximum CL=30pF</td>
</tr>
<tr>
<td></td>
<td>TSDH</td>
<td>Data hold time</td>
<td>10</td>
<td></td>
<td>ns</td>
<td>For minimum CL=8pF</td>
</tr>
<tr>
<td></td>
<td>TACC</td>
<td>Access time</td>
<td>10</td>
<td>50</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TOH</td>
<td>Output disable time</td>
<td>50</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

Table 8.3.1 4-line Serial Interface Characteristics

*Note 1: VDDI=1.65 to 3.3V, VDD=2.6 to 3.3V, AGND=DGND=0V, Ta=25 °C*

*Note 2: The rising time and falling time (Tr, Tt) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for input signals.*
9 Function description
9.1 Interface type selection

The selection of given interfaces are done by setting IM2, IM1, and IM0 pins as shown in following table.

<table>
<thead>
<tr>
<th>IM2</th>
<th>IM1</th>
<th>IM0</th>
<th>Interface</th>
<th>Read back selection</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>-</td>
<td>-</td>
<td>3-line serial</td>
<td>Via the read instruction</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>8080 MCU 8-bit parallel</td>
<td>RDX strobe (8-bit read data and 8-bit read parameter)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>8080 MCU 16-bit parallel</td>
<td>RDX strobe (16-bit read data and 8-bit read parameter)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>8080 MCU 9-bit parallel</td>
<td>RDX strobe (9-bit read data and 8-bit read parameter)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>8080 MCU 18-bit parallel</td>
<td>RDX strobe (18-bit read data and 8-bit read parameter)</td>
</tr>
</tbody>
</table>

Table 9.1.1 Selection of MCU interface

<table>
<thead>
<tr>
<th>IM2</th>
<th>IM1</th>
<th>IM0</th>
<th>Interface</th>
<th>RDX</th>
<th>WRX</th>
<th>D/CX</th>
<th>Read back selection</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>-</td>
<td>-</td>
<td>3-line serial</td>
<td>Note1</td>
<td>Note1</td>
<td>SCL</td>
<td>D[17:1]: unused, D0: SDA</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>8080 8-bit parallel</td>
<td>RDX</td>
<td>WRX</td>
<td>D/CX</td>
<td>D[17:8]: unused, D7-D0: 8-bit data</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>8080 16-bit parallel</td>
<td>RDX</td>
<td>WRX</td>
<td>D/CX</td>
<td>D[17:16]: unused, D15-D0: 16-bit data</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>8080 9-bit parallel</td>
<td>RDX</td>
<td>WRX</td>
<td>D/CX</td>
<td>D[17:9]: unused, D8-D0: 9-bit data</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>8080 18-bit parallel</td>
<td>RDX</td>
<td>WRX</td>
<td>D/CX</td>
<td>D17-D0: 18-bit data</td>
</tr>
</tbody>
</table>

Table 9.1.2 Pin connection according to various MCU interface

Note1: Unused pins can be open, or connected to DGND or VDDI.
9.2  8080-series MCU parallel interface

The MCU can use one of the following interfaces: 11-lines with 8-data parallel interface, 12-lines with 9-data parallel interface, 19-line with 16-data parallel interface or 21-lines with 18-data parallel interface. The chip-select CSX (active low) enables/disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write enable, RDX is the parallel data read enable and D[17:0] is parallel data bus.

The LCD driver reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX=‘1’, D[17:0] bits is either display data or command parameter. When D/CX=‘0’, D[17:0] bits is command. The interface functions of 8080-series parallel interface are given in following table.

<table>
<thead>
<tr>
<th>IM2</th>
<th>IM1</th>
<th>IM0</th>
<th>Interface</th>
<th>D/CX</th>
<th>RDX</th>
<th>WRX</th>
<th>Read back selection</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>8-bit parallel</td>
<td>0</td>
<td>1</td>
<td>↑</td>
<td>Write 8-bit command (D7 to D0)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>1</td>
<td>↑</td>
<td>Write 8-bit display data or 8-bit parameter (D7 to D0)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>Read 8-bit display data (D7 to D0)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>Read 8-bit parameter or status (D7 to D0)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>16-bit parallel</td>
<td>0</td>
<td>1</td>
<td>↑</td>
<td>Write 8-bit command (D7 to D0)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>1</td>
<td>↑</td>
<td>Write 16-bit display data or 8-bit parameter (D15 to D0)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>Read 16-bit display data (D15 to D0)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>Read 8-bit parameter or status (D7 to D0)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>9-bit parallel</td>
<td>0</td>
<td>1</td>
<td>↑</td>
<td>Write 8-bit command (D7 to D0)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>1</td>
<td>↑</td>
<td>Write 9-bit display data or 8-bit parameter (D8 to D0)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>Read 9-bit display data (D8 to D0)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>Read 8-bit parameter or status (D7 to D0)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>18-bit parallel</td>
<td>0</td>
<td>1</td>
<td>↑</td>
<td>Write 8-bit command (D7 to D0)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>1</td>
<td>↑</td>
<td>Write 18-bit display data or 8-bit parameter (D17 to D0)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>Read 18-bit display data (D17 to D0)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>Read 8-bit parameter or status (D7 to D0)</td>
</tr>
</tbody>
</table>

Table 9.2.1 The function of 8080-series parallel interface

Note: applied for command code: DAh, DBh, DCCh, 04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh
9.2.1 Write cycle sequence
The write cycle means that the host writes information (command or data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control signals (D/CX, RDX, WRX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (‘0’) and vice versa it is data (‘1’).

Fig. 9.2.1 8080-series WRX protocol

*Note: WRX is an unsynchronized signal (It can be stopped).*

Fig. 9.2.2 8080-series parallel bus protocol, write to register or display RAM

CMD: write command code
PA: parameter or display data
Signals on D[17:0], D/CX, R/WX, E pins during CSX=1 are ignored.
9.2.2 Read cycle sequence
The read cycle (RDX high-low-high sequence) means that the host reads information from LCD driver via interface. The driver sends data (D[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

![Diagram showing read cycle sequence]

The driver starts to control D[17:0] lines when there is a falling edge of the RDX.
The host read D[17:0] lines when there is a rising edge of RDX.
The driver stops to control D[17:0] lines.

Fig. 9.2.3 8080-series RDX protocol

Note: RDX is an unsynchronized signal (It can be stopped).

![Diagram showing 8080-series parallel bus protocol]

Read parameter  Read display data

D[17:0]  CMD  DM  PA  CMD  DM & data  Data  Data  P
RESX "1"  
CSX  
D/CX  
RDX  
WRX  
D[17:0]  CMD  DM  PA  CMD  DM & data  Data  Data  P
Host D[17:0]  Host to LCD  
Driver D[17:0]  LCD to Host  
CMD: write command code  PA: parameter or display data  
Signals on D[17:0], D/CX, R/WX, E pins during CSX=1 are ignored.

Fig. 9.2.4 8080-series parallel bus protocol, read data from register or display RAM
9.3 Serial interface

The selection of this interface is done by IM2. See the Table 9.3.1.

<table>
<thead>
<tr>
<th>IM2</th>
<th>SPIiW</th>
<th>Interface</th>
<th>Read back selection</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>3-line serial interface</td>
<td>Via the read instruction (8-bit, 24-bit and 32-bit read parameter)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>4-line serial interface</td>
<td>Via the read instruction (8-bit, 24-bit and 32-bit read parameter)</td>
</tr>
</tbody>
</table>

Table 9.3.1 Selection of serial interface

The serial interface is either 3-line/9-bit or 4-line/8-bit bi-directional interface for communication between the micro controller and the LCD driver. The 3-line serial interface use: CSX (chip enable), SCL (serial clock) and SDA (serial data input/output), and the 4-line serial interface use: CSX (chip enable), D/CX (data/command flag), SCL (serial clock) and SDA (serial data input/output). Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

9.3.1 Command Write Mode

The write mode of the interface means the micro controller writes commands and data to the LCD driver. 3-line serial data packet contains a control bit D/CX and a transmission byte. In 4-line serial interface, data packet contains just transmission byte and control bit D/CX is transferred by the D/CX pin. If D/CX is “low”, the transmission byte is interpreted as a command byte. If D/CX is “high”, the transmission byte is stored in the display data RAM (memory write command), or command register as parameter.

Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

![Fig. 9.3.1 Serial interface data stream format](image)

When CSX is “high”, SCL clock is ignored. During the high period of CSX the serial interface is initialized. At the falling edge of CSX, SCL can be high or low (see Fig 9.3.2). SDA is sampled at the rising edge of SCL. D/CX indicates whether the byte is command (D/CX=0) or parameter/RAM data (D/CX=1). D/CX is sampled when first rising edge of SCL (3-line serial interface) or 8th rising edge of SCL (4-line serial interface). If CSX stays low after the last bit of command/data byte, the serial interface expects the D/CX bit (3-line serial interface) or D7 (4-line serial interface) of the next byte at the next rising edge of SCL.
Fig. 9.3.2 3-line serial interface write protocol (write to register with control bit in transmission)

CSX can be "H" between parameter/command and parameter/command SCL, and SDA during CSX="H" is ignored.

Fig. 9.3.3 4-line serial interface write protocol (write to register with control bit in transmission)

CSX can be "H" between parameter/command and parameter/command SCL, and SDA during CSX="H" is ignored.
9.3.2 Read Functions

The read mode of the interface means that the micro controller reads register value from the driver. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

9.3.3 3-line serial protocol

3-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):

3-line serial protocol (for RDDID command: 24-bit read):

3-line Serial Protocol (for RDDST command: 32-bit read):

Fig. 9.3.4 3-line serial interface read protocol
9.3.4 4-line serial protocol

4-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):

4-line serial protocol (for RDDID command: 24-bit read)

4-line Serial Protocol (for RDDST command: 32-bit read)

Fig. 9.3.5 4-line serial interface read protocol
9.4 Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been HIGH state. See the following example.

If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following example.

If 1, 2 or more parameter commands are being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.
If a 2 or more parameter commands are being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.
9.5 Data transfer pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select line is released after a whole byte of a frame memory data or multiple parameter data has been completed, then driver will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select line is released after a whole byte of a command has been completed, then the display module will receive either the command’s parameters (if appropriate) or a new command when the chip select line is next enabled as shown below.

This applies to the following 4 conditions:
1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

9.5.1 Serial interface pause

Fig. 9.5.1 Serial interface pause protocol (pause by CSX)

9.5.2 Parallel interface pause

Fig. 9.5.2 Parallel bus pause protocol (paused by CSX)
9.6 Data Transfer Modes
The module has three kinds color modes for transferring data to the display RAM. These are 12-bit color per pixel, 16-bit color per pixel and 18-bit color per pixel. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

9.6.1 Method 1
The image data is sent to the frame memory in successive frame writes, each time the frame memory is filled, the frame memory pointer is reset to the start point and the next frame is written.

9.6.2 Method 2
The image data is sent and at the end of each frame memory download, a command is sent to stop frame memory write. Then start memory write command is sent, and a new frame is downloaded.

Note 1: These apply to all data transfer Color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.
9.7 Data Color Coding

9.7.1 8-bit Parallel Interface (IM2, IM1, IM0= "100")
Different display data formats are available for three Colors depth supported by listed below.
- 4k colors, RGB 4,4,4-bit input.
- 65k colors, RGB 5,6,5-bit input.
- 262k colors, RGB 6,6,6-bit input.

9.7.2 8-bit data bus for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH= “03h”

Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.
Note 2: 3-time transfer is used to transmit 1 pixel data with the 12-bit color depth information.
Note 3: '-' = Don't care - Can be set to '0' or '1'
9.7.3 8-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH= “05h”

There is 1 pixel (3 sub-pixels) per 2-byte

8080-series control pins

Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don’t care - Can be set to '0' or '1'
8-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH = “06h”

There is 1 pixel (3 sub-pixels) per 3-bytes.

**8080-series control pins**

- **RESX**
- **IM[2:0]**
- **CSX**
- **D/CX**
- **WRX**
- **RDX**

**Note 1:** The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

**Note 2:** 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

**Note 3:** ‘-’ = Don’t care - Can be set to ‘0’ or ‘1’
9.7.5 16-Bit Parallel Interface (IM2, IM1, IM0= “101”)
Different display data formats are available for three colors depth supported by listed below.
- 4k colors, RGB 4,4,4-bit input
- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input

9.7.6 16-bit data bus for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH= “03h”
There is 1 pixel (3 sub-pixels) per 1 byte

Note 1: The data order is as follows, MSB=D11, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.
Note 2: 1-times transfer (D11 to D0) is used to transmit 1 pixel data with the 12-bit color depth information.
9.7.7 16-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH= “05h”

There is 1 pixel (3 sub-pixels) per 1 byte

Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-times transfer (D15 to D0) is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care - Can be set to '0' or '1'
9.7.8 16-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH= “06h”

There are 2 pixels (6 sub-pixels) per 3 bytes

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**8080-series control pins**

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**Frame memory**

- **18 bits**
- **18 bits**

**Note 1:** The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

**Note 2:** 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

**Note 3:** ‘-’ = Don’t care - Can be set to ‘0’ or ‘1’
9.7.9 9-Bit Parallel Interface (IM2, IM1, IM0="110")
Different display data formats are available for three colors depth supported by listed below.
-262k colors, RGB 6,6,6-bit input

9.7.10 Write 9-bit data for RGB 6-6-6-bit input (262k-color)
There is 1 pixel (6 sub-pixels) per 3 bytes

<table>
<thead>
<tr>
<th>RESX</th>
<th>IM[2:0]</th>
<th>CSX</th>
<th>D/CX</th>
<th>WRX</th>
<th>RDX</th>
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<td>&quot;1&quot;</td>
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</tbody>
</table>

**Note 1:** The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.
**Note 2:** 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.
**Note 3:** '-' = Don’t care - Can be set to ‘0’ or ‘1’
### 9.7.11 18-Bit Parallel Interface (IM2, IM1, IM0=“111”)

Different display data formats are available for three colors depth supported by listed below.

- 4k colors, RGB 4,4,4-bit input
- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input.

### 9.7.12 18-bit data bus for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH=“03h”

There is 1 pixel (3 sub-pixels) per 1 byte.

**Note 1:** The data order is as follows, MSB=D11, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

**Note 2:** 1-times transfer is used to transmit 1 pixel data with the 12-bit color depth information.
9.7.13  18-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH="05h"
There is 1 pixel (3 sub-pixels) per 1 byte

Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.
9.7.14 18-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH="06h"

There is 1 pixel (3 sub-pixels) per 1 byte

Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Read, Green and Blue data.

Note 2: 1-times transfer (D17 to D0) is used to transmit 1 pixel data with the 18-bit color depth information.
9.7.15 3-line serial Interface

Different display data formats are available for three colors depth supported by the LCM listed below.

4k colors, RGB 4-4-4-bit input
65k colors, RGB 5-6-5-bit input
262k colors, RGB 6-6-6-bit input

9.7.16 Write data for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH=“03h”

Note 1: Pixel data with the 12-bit color depth information
Note 2: The most significant bits are: Rx3, Gx3 and Bx3
Note 3: The least significant bits are: Rx0, Gx0 and Bx0
9.7.17 Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH="05h"

Note 1: Pixel data with the 16-bit color depth information
Note 2: The most significant bits are: Rx4, Gx5 and Bx4
Note 3: The least significant bits are: Rx0, Gx0 and Bx0
9.7.18 Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH="06h"

Note 1: Pixel data with the 18-bit color depth information
Note 2: The most significant bits are: Rx5, Gx5 and Bx5
Note 3: The least significant bits are: Rx0, Gx0 and Bx0
9.7.19 4-line serial Interface
Different display data formats are available for three colors depth supported by the LCM listed below.
- 4k colors, RGB 4-4-4-bit input
- 65k colors, RGB 5-6-5-bit input
- 262k colors, RGB 6-6-6-bit input

9.7.20 Write data for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH="03h"

Note 1: Pixel data with the 12-bit color depth information
Note 2: The most significant bits are: Rx3, Gx3 and Bx3
Note 3: The least significant bits are: Rx0, Gx0 and Bx0
9.7.21 Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH="05h"

Note 1: Pixel data with the 16-bit color depth information
Note 2: The most significant bits are: Rx4, Gx5 and Bx4
Note 3: The least significant bits are: Rx0, Gx0 and Bx0
9.7.22 Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH=“06h”

Note 1: Pixel data with the 18-bit color depth information
Note 2: The most significant bits are: Rx5, Gx5 and Bx5
Note 3: The least significant bits are: Rx0, Gx0 and Bx0
9.8 Display Data RAM

9.8.1 Configuration (GM[2:0] = “000”)  
The display module has an integrated 132x162x18-bit graphic type static RAM. This 384,912-bit memory allows storing on-chip a 132xRGBx162 image with an 18-bpp resolution (262K-color). There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

Fig. 9.8.1 Display data RAM organization
9.8.2 Memory to Display Address Mapping

9.8.2.1 When using 128RGB x 160 resolution (GM[2:0] = “011”, SMX=SMY=SRGB= ‘0’)

Note
RA = Row Address,
CA = Column Address
SA = Scan Address
MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command
MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command
ML = Scan direction parameter, D4 parameter of MADCTL command
RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command
9.8.2.2 When using 132RGB x 162 resolution (GM[2:0] = “000”, SMX=SMY=SRGB= ‘0’)

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<th>S2</th>
<th>S3</th>
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<tr>
<td>ML=0</td>
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</tr>
<tr>
<td>RA</td>
<td>Source Out</td>
<td>S1</td>
<td>S2</td>
<td>S3</td>
<td>S4</td>
<td>S5</td>
<td>S6</td>
<td>––</td>
<td>S391</td>
<td>S392</td>
<td>S393</td>
<td>S394</td>
<td>S395</td>
<td>S396</td>
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<td>MY=1</td>
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<td>MY=1</td>
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</tr>
</tbody>
</table>

Note:
- RA = Row Address
- CA = Column Address
- SA = Scan Address
- MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command
- MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command
- ML = Scan direction parameter, D4 parameter of MADCTL command
- RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command
9.8.3 Normal Display On or Partial Mode On

9.8.3.1 When using 128RGB x 160 resolution (GM[2:0] = “011”)

In this mode, the content of the frame memory within an area where column pointer is 00h to 7Fh and page pointer is 00h to 9Fh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

1). Example for Normal Display On (MX=MY=ML=’0’, SMX=SMY=’0’)

2). Example for Partial Display On (PSL[7:0]=04h,PEL[7:0]=9Bh, MX=MV=ML=’0’, SMX=SMY=’0’)

---

128 Columns

Scan Order

128 Columns

128 x 160 x18bit Frame RAM

128RGB x 160 LCD Panel

128 Columns

Scan Order

128 Columns

128 x 160 x18bit Frame RAM

128RGB x 160 LCD Panel

Non-Display area =4 lines

Display area =152 lines

Non-Display area =4 lines
9.8.3.2 When using 132RGB x 162 resolution (GM[2:0] = “000”)

In this mode, contents of the frame memory within an area where column pointer is 00h to 83h and page pointer is 00h to A1h is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0)

1). Example for Normal Display On (MX=MY=ML=’0’, SMX=SMY=’0’)

2). Example for Partial Display On (PSL[7:0]=04h,PEL[7:0] =9Dh, MX=MV=ML=’0’ ,SMX=SMY=’0’)

Non-Display area =4 lines

Display area =155 lines

Non-Display area =4lines
9.9 Address Counter

The address counter sets the addresses of the display data RAM for writing and reading. Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 6-6-6-bit), according to the data formats. As soon as this pixel-data information is complete the “Write access” is activated on the RAM.

The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=131 (83h) and Y=0 to Y=161 (A1h). Addresses outside these ranges are not allowed. Before writing to the RAM, a window must be defined that will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=127 (83h), YE=161 (A1h).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands “CASET, RASET and MADCTL” (see section 10 command list), define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Section 9.10 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data must be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as section 9.10 below

<table>
<thead>
<tr>
<th>Condition</th>
<th>Column Counter</th>
<th>Row Counter</th>
</tr>
</thead>
<tbody>
<tr>
<td>When RAMWR/RAMRD command is accepted</td>
<td>Return to “Start Column (XS)”</td>
<td>Return to “Start Row (YS)”</td>
</tr>
<tr>
<td>Complete Pixel Read / Write action</td>
<td>Increment by 1</td>
<td>No change</td>
</tr>
<tr>
<td>The Column counter value is larger than “End Column (XE)”</td>
<td>Return to “Start Column (XS)”</td>
<td>Increment by 1</td>
</tr>
<tr>
<td>The Column counter value is larger than “End Column (XE)” and the Row counter value is larger than “End Row (YE)”</td>
<td>Return to “Start Column (XS)”</td>
<td>Return to “Start Row (YS)”</td>
</tr>
</tbody>
</table>
9.10 Memory Data Write/Read Direction

The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” Command, bits B5 (MV), B6 (MX), B7 (MY) as described below.

![Diagram of data streaming order](image)

Fig. 9.10.1 Data streaming order

### 9.10.1 When 128RGBx160 (GM= “011”)

<table>
<thead>
<tr>
<th>MV</th>
<th>MX</th>
<th>MY</th>
<th>CASET</th>
<th>RASET</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Direct to Physical Column Pointer</td>
<td>Direct to Physical Row Pointer</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Direct to Physical Column Pointer</td>
<td>Direct to (159-Physical Row Pointer)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Direct to (127-Physical Column Pointer)</td>
<td>Direct to Physical Row Pointer</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Direct to (127-Physical Column Pointer)</td>
<td>Direct to (159-Physical Row Pointer)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Direct to Physical Row Pointer</td>
<td>Direct to Physical Column Pointer</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Direct to (159-Physical Row Pointer)</td>
<td>Direct to Physical Column Pointer</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Direct to Physical Row Pointer</td>
<td>Direct to (127-Physical Column Pointer)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Direct to (159-Physical Row Pointer)</td>
<td>Direct to (127-Physical Column Pointer)</td>
</tr>
</tbody>
</table>

### 9.10.2 When 132RGBx162 (GM= “000”)

<table>
<thead>
<tr>
<th>MV</th>
<th>MX</th>
<th>MY</th>
<th>CASET</th>
<th>RASET</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Direct to Physical Column Pointer</td>
<td>Direct to Physical Row Pointer</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Direct to Physical Column Pointer</td>
<td>Direct to (161-Physical Row Pointer)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Direct to (131-Physical Column Pointer)</td>
<td>Direct to Physical Row Pointer</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Direct to (131-Physical Column Pointer)</td>
<td>Direct to (161-Physical Row Pointer)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Direct to Physical Row Pointer</td>
<td>Direct to Physical Column Pointer</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Direct to (161-Physical Row Pointer)</td>
<td>Direct to Physical Column Pointer</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Direct to Physical Row Pointer</td>
<td>Direct to (131-Physical Column Pointer)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Direct to (161-Physical Row Pointer)</td>
<td>Direct to (131-Physical Column Pointer)</td>
</tr>
</tbody>
</table>

Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7 (MY), B6 (MX), B5 (MV). The write order for each pixel unit is

```plaintext
<table>
<thead>
<tr>
<th>DL7</th>
<th>DL6</th>
<th>DL5</th>
<th>DL4</th>
<th>DL3</th>
<th>DL2</th>
<th>DL1</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R5</td>
<td>R4</td>
<td>R3</td>
<td>R2</td>
<td>R1</td>
<td>R0</td>
<td>C5</td>
<td>G4</td>
<td>G3</td>
<td>C2</td>
<td>C1</td>
<td>OO</td>
<td>B5</td>
<td>B4</td>
<td>B3</td>
<td>B2</td>
<td>B1</td>
<td>B0</td>
</tr>
</tbody>
</table>
```

One pixel unit represents 1 column and 1 page counter value on the Frame Memory.
### 9.10.3 Frame Data Write Direction According to the MADCTL parameters (MV, MX and MY)

<table>
<thead>
<tr>
<th>Display Data Direction</th>
<th>MADCTL Parameter</th>
<th>Image in the Host (MPU)</th>
<th>Image in the Driver (DDRAM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal</td>
<td>MV, MX, MY</td>
<td><img src="image1" alt="Diagram" /></td>
<td><img src="image2" alt="Diagram" /></td>
</tr>
<tr>
<td>Y-Mirror</td>
<td>0, 0, 1</td>
<td><img src="image3" alt="Diagram" /></td>
<td><img src="image4" alt="Diagram" /></td>
</tr>
<tr>
<td>X-Mirror</td>
<td>0, 1, 0</td>
<td><img src="image5" alt="Diagram" /></td>
<td><img src="image6" alt="Diagram" /></td>
</tr>
<tr>
<td>X-Mirror Y-Mirror</td>
<td>0, 1, 1</td>
<td><img src="image7" alt="Diagram" /></td>
<td><img src="image8" alt="Diagram" /></td>
</tr>
<tr>
<td>X-Y Exchange</td>
<td>1, 0, 0</td>
<td><img src="image9" alt="Diagram" /></td>
<td><img src="image10" alt="Diagram" /></td>
</tr>
<tr>
<td>X-Y Exchange Y-Mirror</td>
<td>1, 0, 1</td>
<td><img src="image11" alt="Diagram" /></td>
<td><img src="image12" alt="Diagram" /></td>
</tr>
<tr>
<td>X-Y Exchange X-Mirror</td>
<td>1, 1, 0</td>
<td><img src="image13" alt="Diagram" /></td>
<td><img src="image14" alt="Diagram" /></td>
</tr>
<tr>
<td>X-Y Exchange X-Mirror Y-Mirror</td>
<td>1, 1, 1</td>
<td><img src="image15" alt="Diagram" /></td>
<td><img src="image16" alt="Diagram" /></td>
</tr>
</tbody>
</table>
9.11 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

9.11.1 Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:

Vertical timing scale

\[ \text{tvdh} = \text{The LCD display is not updated from the Frame Memory} \]
\[ \text{tvdl} = \text{The LCD display is updated from the Frame Memory (except Invisible Line -- see above)} \]

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 162 H-sync pulses per field.

Vertical timing scale

\[ \text{thdh} = \text{The LCD display is not updated from the Frame Memory} \]
\[ \text{thdl} = \text{The LCD display is updated from the Frame Memory (except Invisible Line -- see above)} \]

Note: During Sleep In Mode, the Tearing Output Pin is active Low.
9.11.2 Tearing Effect Line Timings

The Tearing Effect signal is described below:

Table 9.11.1 AC characteristics of Tearing Effect Signal Idle Mode Off (Frame Rate = 60 Hz, Ta=25°C)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>min</th>
<th>max</th>
<th>unit</th>
<th>description</th>
</tr>
</thead>
<tbody>
<tr>
<td>tvdl</td>
<td>Vertical Timing Low Duration</td>
<td>13</td>
<td>-</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>tvdh</td>
<td>Vertical Timing High Duration</td>
<td>1000</td>
<td>-</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>thdl</td>
<td>Horizontal Timing Low Duration</td>
<td>33</td>
<td>-</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>thdh</td>
<td>Horizontal Timing Low Duration</td>
<td>25</td>
<td>500</td>
<td>µs</td>
<td></td>
</tr>
</tbody>
</table>

Note: The timings in Table 9.10.1 apply when MADCTL ML=0 and ML=1

The signal’s rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:
9.11.3 Example 1: MPU Write is faster than panel read

Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:

Data to be sent

Image on LCD
9.11.4 Example 2: MPU write is slower than panel read

The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.
9.12 Power ON/OFF Sequence

VDD must be powered on before the VDDI.
VDDI must be powered off before the VDD.
During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.
During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.
CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note 1: There will be no damage to the display module if the power sequences are not met.
Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below

9.12.1 Uncontrolled Power Off

The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the display (blank display) and remains blank until “Power On Sequence” powers it up.
9.13 Power Level Definition

9.13.1 Power Level

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
   In this mode, the display is able to show maximum 262,144 colors.

   In this mode part of the display is used with maximum 262,144 colors.

   In this mode, the full display area is used but with 8 colors.

   In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode
   In this mode, the DC: DC converter, internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.

6. Power Off Mode
   In this mode, both VDD and VDDI are removed.

*Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.*
9.13.2 Power Flow Chart

- Normal display mode on = NOR ON
- Partial display mode on = PTL ON
- Idle mode off = IDM OFF
- Idle mode on = IDM ON
- Sleep out = SLP OUT
- Sleep in = SLP IN

Power on sequence
HW reset
SW reset

Sleep out
- Normal display mode on
- Idle mode off

Idm ON
Idm OFF

Sleep in
- Normal display mode on
- Idle mode off
### 9.14 Reset Table


<table>
<thead>
<tr>
<th>Item</th>
<th>After Power On</th>
<th>After H/W Reset</th>
<th>After S/W Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frame memory</td>
<td>Random</td>
<td>No Change</td>
<td>No Change</td>
</tr>
<tr>
<td>Sleep In/Out</td>
<td>In</td>
<td>In</td>
<td>In</td>
</tr>
<tr>
<td>Display On/Off</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>Display mode (normal/partial)</td>
<td>Normal</td>
<td>Normal</td>
<td>Normal</td>
</tr>
<tr>
<td>Display Inversion On/Off</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>Column: Start Address (XS)</td>
<td>0000h</td>
<td>0000h</td>
<td>0000h</td>
</tr>
<tr>
<td>Column: End Address (XE)</td>
<td>007Fh</td>
<td>007Fh</td>
<td>007Fh (127d) (when MV=0) 009Fh (159d) (when MV=1)</td>
</tr>
<tr>
<td>Row: Start Address (YS)</td>
<td>0000h</td>
<td>0000h</td>
<td>0000h</td>
</tr>
<tr>
<td>Row: End Address (YE)</td>
<td>009Fh</td>
<td>009Fh</td>
<td>009Fh (159d) (when MV=0) 007Fh (127d) (when MV=1)</td>
</tr>
<tr>
<td>Gamma setting</td>
<td>GC0</td>
<td>GC0</td>
<td>GC0</td>
</tr>
<tr>
<td>RGB for 4k and 65k Color Mode</td>
<td>See Section 9.17</td>
<td>See Section 9.17</td>
<td>No Change</td>
</tr>
<tr>
<td>Partial: Start Address (PSL)</td>
<td>0000h</td>
<td>0000h</td>
<td>0000h</td>
</tr>
<tr>
<td>Partial: End Address (PEL)</td>
<td>009Fh</td>
<td>009Fh</td>
<td>009Fh</td>
</tr>
<tr>
<td>Tearing: On/Off</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>Tearing Effect Mode (*1)</td>
<td>0 (Mode1)</td>
<td>0 (Mode1)</td>
<td>0 (Mode1)</td>
</tr>
<tr>
<td>Memory Data Access Control (MY/MX/MV/ML/RGB)</td>
<td>0/0/0/0/0/0</td>
<td>0/0/0/0/0/0</td>
<td>No Change</td>
</tr>
<tr>
<td>Interface Pixel Color Format</td>
<td>6 (18-Bit/Pixel)</td>
<td>6 (18-Bit/Pixel)</td>
<td>No Change</td>
</tr>
<tr>
<td>RDDPM</td>
<td>08h</td>
<td>08h</td>
<td>08h</td>
</tr>
<tr>
<td>RDDMAADCTL</td>
<td>00h</td>
<td>00h</td>
<td>No Change</td>
</tr>
<tr>
<td>RDDCOLMOD</td>
<td>6 (18-Bit/Pixel)</td>
<td>6 (18-Bit/Pixel)</td>
<td>No Change</td>
</tr>
<tr>
<td>RDDIM</td>
<td>00h</td>
<td>00h</td>
<td>00h</td>
</tr>
<tr>
<td>RDDSM</td>
<td>00h</td>
<td>00h</td>
<td>00h</td>
</tr>
<tr>
<td>RDDSDR</td>
<td>00h</td>
<td>00h</td>
<td>00h</td>
</tr>
<tr>
<td>ID2</td>
<td>NV value</td>
<td>NV value</td>
<td>NV value</td>
</tr>
<tr>
<td>ID3</td>
<td>NV value</td>
<td>NV value</td>
<td>NV value</td>
</tr>
</tbody>
</table>

*Note: TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only*
### 9.14.2 Reset Table (GM[2:0]= “000”, 132RGB x 162)

<table>
<thead>
<tr>
<th>Item</th>
<th>After Power On</th>
<th>After H/W Reset</th>
<th>After S/W Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frame memory</td>
<td>Random</td>
<td>No Change</td>
<td>No Change</td>
</tr>
<tr>
<td>Sleep In/Out</td>
<td>In</td>
<td>In</td>
<td>In</td>
</tr>
<tr>
<td>Display On/Off</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>Display mode (normal/partial)</td>
<td>Normal</td>
<td>Normal</td>
<td>Normal</td>
</tr>
<tr>
<td>Display Inversion On/Off</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>Display Idle Mode On/Off</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>Column: Start Address (XS)</td>
<td>0000h</td>
<td>0000h</td>
<td>0000h</td>
</tr>
<tr>
<td>Column: End Address (XE)</td>
<td>0083h</td>
<td>0083h</td>
<td>0083h (131d) (when MV=0)</td>
</tr>
<tr>
<td>Row: Start Address (YS)</td>
<td>0000h</td>
<td>0000h</td>
<td>0000h</td>
</tr>
<tr>
<td>Row: End Address (YE)</td>
<td>00A1h</td>
<td>00A1h</td>
<td>00A1h (161d) (when MV=0)</td>
</tr>
<tr>
<td>Gamma setting</td>
<td>GC0</td>
<td>GC0</td>
<td>GC0</td>
</tr>
<tr>
<td>RGB for 4k and 65k Color Mode</td>
<td>See Section 9.17</td>
<td>See Section 9.17</td>
<td>No Change</td>
</tr>
<tr>
<td>Partial: Start Address (PSL)</td>
<td>0000h</td>
<td>0000h</td>
<td>0000h</td>
</tr>
<tr>
<td>Partial: End Address (PEL)</td>
<td>00A1h</td>
<td>00A1h</td>
<td>00A1h</td>
</tr>
<tr>
<td>Tearing: On/Off</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>Tearing Effect Mode (*1)</td>
<td>0 (Mode1)</td>
<td>0 (Mode1)</td>
<td>0 (Mode1)</td>
</tr>
<tr>
<td>Memory Data Access Control (MY/MX/MV/ML/RGB)</td>
<td>0/0/0/0/0/0</td>
<td>0/0/0/0/0/0</td>
<td>No Change</td>
</tr>
<tr>
<td>Interface Pixel Color Format</td>
<td>6 (18-Bit/ Pixel)</td>
<td>6 (18-Bit/ Pixel)</td>
<td>No Change</td>
</tr>
<tr>
<td>RDDPM</td>
<td>08h</td>
<td>08h</td>
<td>08h</td>
</tr>
<tr>
<td>RDDMADCTL</td>
<td>00h</td>
<td>00h</td>
<td>No Change</td>
</tr>
<tr>
<td>RDDCOLMOD</td>
<td>6 (18-Bit/ Pixel)</td>
<td>6 (18-Bit/ Pixel)</td>
<td>No Change</td>
</tr>
<tr>
<td>RDDIM</td>
<td>00h</td>
<td>00h</td>
<td>00h</td>
</tr>
<tr>
<td>RDDSM</td>
<td>00h</td>
<td>00h</td>
<td>00h</td>
</tr>
<tr>
<td>RDDSDR</td>
<td>00h</td>
<td>00h</td>
<td>00h</td>
</tr>
<tr>
<td>ID2</td>
<td>NV value</td>
<td>NV value</td>
<td>NV value</td>
</tr>
<tr>
<td>ID3</td>
<td>NV value</td>
<td>NV value</td>
<td>NV value</td>
</tr>
</tbody>
</table>

*Note: TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only*
## 9.15 Module Input/Output Pins

### 9.15.1 Output or Bi-directional (I/O) Pins

<table>
<thead>
<tr>
<th>Output or Bi-directional pins</th>
<th>After Power On</th>
<th>After Hardware Reset</th>
<th>After Software Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>TE</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>D7 to D0 (Output driver)</td>
<td>High-Z (Inactive)</td>
<td>High-Z (Inactive)</td>
<td>High-Z (Inactive)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Input pins</th>
<th>During Power On Process</th>
<th>After Power On</th>
<th>After Hardware Reset</th>
<th>After Software Reset</th>
<th>During Power Off Process</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESX</td>
<td>See 9.14</td>
<td>Input valid</td>
<td>Input valid</td>
<td>Input valid</td>
<td>See 9.14</td>
</tr>
<tr>
<td>CSX</td>
<td>Input invalid</td>
<td>Input valid</td>
<td>Input valid</td>
<td>Input valid</td>
<td>Input invalid</td>
</tr>
<tr>
<td>D/CX</td>
<td>Input invalid</td>
<td>Input valid</td>
<td>Input valid</td>
<td>Input valid</td>
<td>Input invalid</td>
</tr>
<tr>
<td>WRX</td>
<td>Input invalid</td>
<td>Input valid</td>
<td>Input valid</td>
<td>Input valid</td>
<td>Input invalid</td>
</tr>
<tr>
<td>RDX</td>
<td>Input invalid</td>
<td>Input valid</td>
<td>Input valid</td>
<td>Input valid</td>
<td>Input invalid</td>
</tr>
<tr>
<td>D7 to D0</td>
<td>Input invalid</td>
<td>Input valid</td>
<td>Input valid</td>
<td>Input valid</td>
<td>Input invalid</td>
</tr>
</tbody>
</table>

*Note: There will be no output from D7-D0 during Power On/Off sequence, Hardware Reset and Software Reset.*
9.16 Reset Timing

![Diagram of Reset Timing]

**Table 9.16.1 Reset timing**

<table>
<thead>
<tr>
<th>Related Pins</th>
<th>Symbol</th>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESX</td>
<td>tRESW</td>
<td>Reset pulse duration</td>
<td>10</td>
<td>-</td>
<td>us</td>
</tr>
<tr>
<td></td>
<td>tREST</td>
<td>Reset cancel</td>
<td>-</td>
<td>5</td>
<td>ms</td>
</tr>
</tbody>
</table>

**Notes:**

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from EEPROM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (IRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

<table>
<thead>
<tr>
<th>RESX Pulse</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shorter than 5us</td>
<td>Reset Rejected</td>
</tr>
<tr>
<td>Longer than 9us</td>
<td>Reset</td>
</tr>
<tr>
<td>Between 5us and 9us</td>
<td>Reset starts</td>
</tr>
</tbody>
</table>

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:

![Spike Rejection Diagram]

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.
## 9.17 Color Depth Conversion Look Up Tables

### 9.17.1 65536 Color to 262,144 Color

<table>
<thead>
<tr>
<th>Color</th>
<th>Look Up Table Output</th>
<th>Default value after H/W Reset</th>
<th>RGBSET Parameter</th>
<th>Look Up Table Input Data 65K Color (5-bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RED</td>
<td>R005 R004 R003 R002 R001 R000</td>
<td>000000</td>
<td>1</td>
<td>00000</td>
</tr>
<tr>
<td></td>
<td>R015 R014 R013 R012 R011 R010</td>
<td>000010</td>
<td>2</td>
<td>00001</td>
</tr>
<tr>
<td></td>
<td>R025 R024 R023 R022 R021 R020</td>
<td>000100</td>
<td>3</td>
<td>00010</td>
</tr>
<tr>
<td></td>
<td>R035 R034 R033 R032 R031 R030</td>
<td>001110</td>
<td>4</td>
<td>00111</td>
</tr>
<tr>
<td></td>
<td>R045 R044 R043 R042 R041 R040</td>
<td>010000</td>
<td>5</td>
<td>00100</td>
</tr>
<tr>
<td></td>
<td>R055 R054 R053 R052 R051 R050</td>
<td>010100</td>
<td>6</td>
<td>01010</td>
</tr>
<tr>
<td></td>
<td>R065 R064 R063 R062 R061 R060</td>
<td>011100</td>
<td>7</td>
<td>00111</td>
</tr>
<tr>
<td></td>
<td>R075 R074 R073 R072 R071 R070</td>
<td>011110</td>
<td>8</td>
<td>00111</td>
</tr>
<tr>
<td></td>
<td>R085 R084 R083 R082 R081 R080</td>
<td>010000</td>
<td>9</td>
<td>01000</td>
</tr>
<tr>
<td></td>
<td>R095 R094 R093 R092 R091 R090</td>
<td>010100</td>
<td>10</td>
<td>01010</td>
</tr>
<tr>
<td></td>
<td>R105 R104 R103 R102 R101 R100</td>
<td>011100</td>
<td>11</td>
<td>01110</td>
</tr>
<tr>
<td></td>
<td>R115 R114 R113 R112 R111 R110</td>
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<td>12</td>
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<tr>
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<td>R125 R124 R123 R122 R121 R120</td>
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<td>01100</td>
</tr>
<tr>
<td></td>
<td>R135 R134 R133 R132 R131 R130</td>
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<td>14</td>
<td>01101</td>
</tr>
<tr>
<td></td>
<td>R145 R144 R143 R142 R141 R140</td>
<td>001100</td>
<td>15</td>
<td>01110</td>
</tr>
<tr>
<td></td>
<td>R155 R154 R153 R152 R151 R150</td>
<td>011110</td>
<td>16</td>
<td>01111</td>
</tr>
<tr>
<td></td>
<td>R165 R164 R163 R162 R161 R160</td>
<td>100001</td>
<td>17</td>
<td>10000</td>
</tr>
<tr>
<td></td>
<td>R175 R174 R173 R172 R171 R170</td>
<td>100011</td>
<td>18</td>
<td>10001</td>
</tr>
<tr>
<td></td>
<td>R185 R184 R183 R182 R181 R180</td>
<td>100101</td>
<td>19</td>
<td>10010</td>
</tr>
<tr>
<td></td>
<td>R195 R194 R193 R192 R191 R190</td>
<td>100111</td>
<td>20</td>
<td>10011</td>
</tr>
<tr>
<td></td>
<td>R205 R204 R203 R202 R201 R200</td>
<td>101001</td>
<td>21</td>
<td>10100</td>
</tr>
<tr>
<td></td>
<td>R215 R214 R213 R212 R211 R210</td>
<td>101101</td>
<td>22</td>
<td>10110</td>
</tr>
<tr>
<td></td>
<td>R225 R224 R223 R222 R221 R220</td>
<td>101111</td>
<td>23</td>
<td>10111</td>
</tr>
<tr>
<td></td>
<td>R235 R234 R233 R232 R231 R230</td>
<td>111111</td>
<td>24</td>
<td>11111</td>
</tr>
<tr>
<td></td>
<td>R245 R244 R243 R242 R241 R240</td>
<td>111111</td>
<td>25</td>
<td>11111</td>
</tr>
<tr>
<td></td>
<td>R255 R254 R253 R252 R251 R250</td>
<td>111111</td>
<td>26</td>
<td>11111</td>
</tr>
<tr>
<td></td>
<td>R265 R264 R263 R262 R261 R260</td>
<td>111111</td>
<td>27</td>
<td>11111</td>
</tr>
<tr>
<td></td>
<td>R275 R274 R273 R272 R271 R270</td>
<td>111111</td>
<td>28</td>
<td>11111</td>
</tr>
<tr>
<td></td>
<td>R285 R284 R283 R282 R281 R280</td>
<td>111111</td>
<td>29</td>
<td>11111</td>
</tr>
<tr>
<td></td>
<td>R295 R294 R293 R292 R291 R290</td>
<td>111111</td>
<td>30</td>
<td>11111</td>
</tr>
<tr>
<td></td>
<td>R305 R304 R303 R302 R301 R300</td>
<td>111111</td>
<td>31</td>
<td>11111</td>
</tr>
<tr>
<td></td>
<td>R315 R314 R313 R312 R311 R310</td>
<td>111111</td>
<td>32</td>
<td>11111</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>GREEN</th>
<th>Look Up Table Output</th>
<th>Default value after H/W Reset</th>
<th>RGBSET Parameter</th>
<th>Look Up Table Input Data 65K Color (5-bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>G005 G004 G003 G002 G001 G000</td>
<td>000000</td>
<td>33</td>
<td>000000</td>
</tr>
<tr>
<td></td>
<td>G015 G014 G013 G012 G011 G010</td>
<td>000001</td>
<td>34</td>
<td>000001</td>
</tr>
<tr>
<td></td>
<td>G025 G024 G023 G022 G021 G020</td>
<td>000010</td>
<td>35</td>
<td>000010</td>
</tr>
<tr>
<td></td>
<td>G035 G034 G033 G032 G031 G030</td>
<td>000111</td>
<td>36</td>
<td>000111</td>
</tr>
<tr>
<td></td>
<td>G045 G044 G043 G042 G041 G040</td>
<td>001011</td>
<td>37</td>
<td>001011</td>
</tr>
<tr>
<td></td>
<td>G055 G054 G053 G052 G051 G050</td>
<td>001111</td>
<td>38</td>
<td>001111</td>
</tr>
<tr>
<td></td>
<td>G065 G064 G063 G062 G061 G060</td>
<td>001110</td>
<td>39</td>
<td>001110</td>
</tr>
<tr>
<td></td>
<td>G075 G074 G073 G072 G071 G070</td>
<td>001111</td>
<td>40</td>
<td>001111</td>
</tr>
<tr>
<td></td>
<td>G085 G084 G083 G082 G081 G080</td>
<td>010000</td>
<td>41</td>
<td>001000</td>
</tr>
<tr>
<td></td>
<td>G095 G094 G093 G092 G091 G090</td>
<td>010001</td>
<td>42</td>
<td>001001</td>
</tr>
<tr>
<td></td>
<td>G105 G104 G103 G102 G101 G100</td>
<td>010100</td>
<td>43</td>
<td>001010</td>
</tr>
<tr>
<td></td>
<td>G115 G114 G113 G112 G111 G110</td>
<td>010101</td>
<td>44</td>
<td>001100</td>
</tr>
<tr>
<td></td>
<td>G125 G124 G123 G122 G121 G120</td>
<td>010110</td>
<td>45</td>
<td>001100</td>
</tr>
<tr>
<td></td>
<td>G135 G134 G133 G132 G131 G130</td>
<td>010111</td>
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<td>001101</td>
</tr>
<tr>
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"-": Don’t care
### Table 10.1.2 System Function command List (2)

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Refer</th>
<th>D/C</th>
<th>WR</th>
<th>D0</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>D4</th>
<th>D5</th>
<th>D6</th>
<th>D7</th>
<th>Hex</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLPIN</td>
<td>10.1.10</td>
<td>0</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>(10h)</td>
<td>Sleep in &amp; booster off</td>
</tr>
<tr>
<td>SLPOUT</td>
<td>10.1.11</td>
<td>0</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>(11h)</td>
<td>Sleep out &amp; booster on</td>
</tr>
<tr>
<td>PTLON</td>
<td>10.1.12</td>
<td>0</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>(12h)</td>
<td>Partial mode on</td>
</tr>
<tr>
<td>NORON</td>
<td>10.1.13</td>
<td>0</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>(13h)</td>
<td>Partial off (Normal)</td>
</tr>
<tr>
<td>INVOFF</td>
<td>10.1.14</td>
<td>0</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>(20h)</td>
<td>Display inversion off</td>
</tr>
<tr>
<td>INVON</td>
<td>10.1.15</td>
<td>0</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>(21h)</td>
<td>Display inversion on</td>
</tr>
<tr>
<td>SLPIN</td>
<td>10.1.16</td>
<td>0</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>(26h)</td>
<td>Gamma curve select</td>
<td></td>
</tr>
<tr>
<td>DISPOFF</td>
<td>10.1.17</td>
<td>0</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>(28h)</td>
<td>Display off</td>
</tr>
<tr>
<td>DISPON</td>
<td>10.1.18</td>
<td>0</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>(29h)</td>
<td>Display on</td>
</tr>
<tr>
<td>CASET</td>
<td>10.1.19</td>
<td>0</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>(2Ah)</td>
<td>Column address set</td>
</tr>
<tr>
<td>RASET</td>
<td>10.1.20</td>
<td>0</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>(2Bh)</td>
<td>Row address set</td>
</tr>
<tr>
<td>RAMWR</td>
<td>10.1.21</td>
<td>0</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>(2Ch)</td>
<td>Memory write</td>
</tr>
<tr>
<td>RAMRD</td>
<td>10.1.22</td>
<td>0</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>(2 Eh)</td>
<td>Memory read</td>
</tr>
</tbody>
</table>

"-" : Don't care
### Table 10.1.3 System Function command List (3)

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Refer</th>
<th>D/CX</th>
<th>WRX</th>
<th>RDX</th>
<th>D17-8</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>Hex</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>PTLAR</td>
<td>10.1.23</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>(30h)</td>
<td>Partial start/end address set</td>
</tr>
<tr>
<td>TEOFF</td>
<td>10.1.24</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>(34h)</td>
<td>Tearing effect line off</td>
</tr>
<tr>
<td>TEON</td>
<td>10.1.25</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>(35h)</td>
<td>Tearing effect mode set &amp; on</td>
</tr>
<tr>
<td>MADCTL</td>
<td>10.1.26</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>(36h)</td>
<td>Memory data access control</td>
</tr>
<tr>
<td>IDMOFF</td>
<td>10.1.27</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>(38h)</td>
<td>Idle mode off</td>
</tr>
<tr>
<td>IDMON</td>
<td>10.1.28</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>(39h)</td>
<td>Idle mode on</td>
</tr>
<tr>
<td>COLMOD</td>
<td>10.1.29</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>(3Ah)</td>
<td>Interface pixel format</td>
</tr>
<tr>
<td>RDID1</td>
<td>10.1.30</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>(DAh)</td>
<td>Read ID1</td>
</tr>
<tr>
<td>RDID2</td>
<td>10.1.31</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>(DBh)</td>
<td>Read ID2</td>
</tr>
<tr>
<td>RDID3</td>
<td>10.1.32</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>(DCh)</td>
<td>Read ID3</td>
</tr>
</tbody>
</table>

"-": Don’t care

**Note 1:** After the HW reset by RESX pin or S/W reset by SWRESET command, each internal register becomes default state (Refer "RESET TABLE" section)

**Note 2:** Undefined commands are treated as NOP (00 h) command.

**Note 3:** B0 to D9 and DA to F are for factory use of driver supplier.

**Note 4:** Commands 10h, 12h, 13h, 20h, 21h, 26h, 28h, 29h, 30h, 36h (ML parameter only), 38h and 39h are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately.

Read status (09h), Read Display Power Mode (0Ah), Read Display MADCTL (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh).
### 10.1.1 NOP (00h)

<table>
<thead>
<tr>
<th>Inst / Para</th>
<th>D/CX</th>
<th>WRX</th>
<th>RDX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOP</td>
<td>0</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>00h</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>No Parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Description</td>
<td>This command is empty command.</td>
</tr>
</tbody>
</table>

"-" Don't care
### 10.1.2 SWRESET (01h): Software Reset

#### Description

- "-" Don’t care
- If Software Reset is applied during Sleep In mode, it will be necessary to wait 120msec before sending next command.
- The display module loads all default values to the registers during 120msec.
- If Software Reset is applied during Sleep Out or Display On Mode, it will be necessary to wait 120msec before sending next command.

#### Flow Chart

- SWRESET
- Display whole blank screen
- Set Commands to S/W Default Value
- Sleep In Mode

#### Legend

- Command
- Parameter
- Display
- Action
- Mode
- Sequential tranfer
10.1.3 RDDID (04h): Read Display ID

### Description

- This read byte returns 24-bit display identification information.
- The 1st parameter is dummy data
- The 2nd parameter (ID17 to ID10): LCD module’s manufacturer ID.
- The 3rd parameter (ID26 to ID20): LCD module/drive version ID
- The 4th parameter (ID37 to UD30): LCD module/drive ID.

- Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively.
- "-" Don’t care

### Default

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>0x5C NV Value</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>0x5C NV Value</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>0x5C NV Value</td>
</tr>
</tbody>
</table>

### Flow Chart

Serial I/F Mode

1. Read 04h
2. Send 2nd parameter
3. Send 3rd parameter
4. Send 4th parameter

Parallel I/F Mode

1. Read 04h
2. Send 2nd parameter
3. Send 3rd parameter
4. Send 4th parameter

Legend

- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer
### 10.1.4 RDDST (09h): Read Display Status

<table>
<thead>
<tr>
<th>09H</th>
<th>RDDST (Read Display Status)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inst / Para</td>
<td>D/CX</td>
</tr>
<tr>
<td>RDDST</td>
<td>0</td>
</tr>
<tr>
<td>1st parameter</td>
<td>1</td>
</tr>
<tr>
<td>2nd parameter</td>
<td>1</td>
</tr>
<tr>
<td>3rd parameter</td>
<td>1</td>
</tr>
<tr>
<td>4th parameter</td>
<td>1</td>
</tr>
<tr>
<td>5th parameter</td>
<td>1</td>
</tr>
</tbody>
</table>

This command indicates the current status of the display as described in the table below:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>BSTON</td>
<td>Booster Voltage Status</td>
<td>'1' = Booster on, '0' = Booster off</td>
</tr>
<tr>
<td>MY</td>
<td>Row Address Order (MY)</td>
<td>'1' = Decrement, (Bottom to Top, when MADCTL (36h) D7='1') '0' = Increment, (Top to Bottom, when MADCTL (36h) D7='0')</td>
</tr>
<tr>
<td>MX</td>
<td>Column Address Order (MX)</td>
<td>'1' = Decrement, (Right to Left, when MADCTL (36h) D6='1') '0' = Increment, (Left to Right, when MADCTL (36h) D6='1')</td>
</tr>
<tr>
<td>MV</td>
<td>Row/Column Exchange (MV)</td>
<td>'1' = Row/column exchange, (when MADCTL (36h) D5='1') '0' = Normal, (when MADCTL (36h) D5='0')</td>
</tr>
<tr>
<td>ML</td>
<td>Scan Address Order (ML)</td>
<td>'0' = Decrement, (LCD refresh Top to Bottom, when MADCTL (36h) D4='0') '1' = Increment, (LCD refresh Bottom to Top, when MADCTL (36h) D4='1')</td>
</tr>
<tr>
<td>RGB</td>
<td>RGB/ BGR Order (RGB)</td>
<td>'1' = BGR, (When MADCTL (36h) D3='1') '0' = RGB, (When MADCTL (36h) D3='0')</td>
</tr>
<tr>
<td>MH</td>
<td>Horizontal Order</td>
<td>'0' = Decrement, (LCD refresh Left to Right, when MADCTL (36h) D2='0') '1' = Increment, (LCD refresh Right to Left, when MADCTL (36h) D2='1')</td>
</tr>
<tr>
<td>ST24</td>
<td>For Future Use</td>
<td>'0'</td>
</tr>
<tr>
<td>ST23</td>
<td>For Future Use</td>
<td>'0'</td>
</tr>
<tr>
<td>IFPF2</td>
<td>Interface Color Pixel Format</td>
<td>'011' = 12-bit / pixel, '101' = 16-bit / pixel, '110' = 18-bit / pixel, others are no define</td>
</tr>
<tr>
<td>IFPF1</td>
<td>Definition</td>
<td></td>
</tr>
<tr>
<td>IFPF0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IDMON</td>
<td>Idle Mode On/Off</td>
<td>'1' = On, '0' = Off</td>
</tr>
<tr>
<td>PTLON</td>
<td>Partial Mode On/Off</td>
<td>'1' = On, '0' = Off</td>
</tr>
<tr>
<td>SLPOUT</td>
<td>Sleep In/Out</td>
<td>'1' = Out, '0' = In</td>
</tr>
<tr>
<td>NORON</td>
<td>Display Normal Mode On/Off</td>
<td>'1' = Normal Display, '0' = Partial Display</td>
</tr>
<tr>
<td>ST15</td>
<td>Vertical Scrolling Status (Not Used)</td>
<td>'1' = Scroll on,&quot;0&quot; = Scroll off</td>
</tr>
<tr>
<td>ST14</td>
<td>Horizontal Scroll Status (Not Used)</td>
<td>'0'</td>
</tr>
<tr>
<td>INVON</td>
<td>Inversion Status</td>
<td>'1' = On, '0' = Off</td>
</tr>
<tr>
<td>ST12</td>
<td>All Pixels On (Not Used)</td>
<td>'0'</td>
</tr>
<tr>
<td>Register</td>
<td>Description</td>
<td>Default Value (ST31 to ST0)</td>
</tr>
<tr>
<td>----------</td>
<td>-------------</td>
<td>-----------------------------</td>
</tr>
<tr>
<td>DISON</td>
<td>Display On/Off</td>
<td>‘1’ = On, ‘0’ = Off</td>
</tr>
<tr>
<td>TEON</td>
<td>Tearing effect line on/off</td>
<td>‘1’ = On, ‘0’ = Off</td>
</tr>
<tr>
<td>GCSEL2</td>
<td>Gamma Curve Selection</td>
<td>“000” = GC0</td>
</tr>
<tr>
<td>GCSEL1</td>
<td></td>
<td>“001” = GC1</td>
</tr>
<tr>
<td>GCSEL0</td>
<td></td>
<td>“010” = GC2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>“011” = GC3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>“100” to “111” = Not defined</td>
</tr>
<tr>
<td>TELOM</td>
<td>Tearing effect line mode</td>
<td>‘0’ = mode1, ‘1’ = mode2</td>
</tr>
<tr>
<td>ST4</td>
<td>For Future Use</td>
<td>‘0’</td>
</tr>
<tr>
<td>ST3</td>
<td>For Future Use</td>
<td>‘0’</td>
</tr>
<tr>
<td>ST2</td>
<td>For Future Use</td>
<td>‘0’</td>
</tr>
<tr>
<td>ST1</td>
<td>For Future Use</td>
<td>‘0’</td>
</tr>
<tr>
<td>ST0</td>
<td>For Future Use</td>
<td>‘0’</td>
</tr>
</tbody>
</table>

* '-' Don’t care

### Status

<table>
<thead>
<tr>
<th>Power On Sequence</th>
<th>Default Value (ST31 to ST0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000-0000</td>
<td>0110-0001 0000-0000 0000-0000</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>0xxxx0xx0 0xxx-0001 0000-0000 0000-0000</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>0000-0000 0110-0001 0000-0000 0000-0000</td>
</tr>
</tbody>
</table>

### Flow Chart

**Serial I/F Mode**

1. RDDST 09h
2. Dummy Clock
3. Send 2nd parameter
4. Send 3rd parameter
5. Send 4th parameter
6. Send 5th parameter

**Parallel I/F Mode**

1. RDDST 09h
2. Dummy Read
3. Send 2nd parameter
4. Send 3rd parameter
5. Send 4th parameter
6. Send parameter

### Legend

- **Command**
- **Parameter**
- **Display**
- **Action**
- **Mode**
- **Sequential transfer**
### 10.1.5 RDDPM (0Ah): Read Display Power Mode

<table>
<thead>
<tr>
<th>0AH</th>
<th>RDDPM (Read Display Power Mode)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inst / Para</td>
<td>D/CX</td>
</tr>
<tr>
<td>RDDPM</td>
<td>0</td>
</tr>
<tr>
<td>1st parameter</td>
<td>1</td>
</tr>
<tr>
<td>2nd parameter</td>
<td>1</td>
</tr>
</tbody>
</table>

This command indicates the current status of the display as described in the table below:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>BSTON</td>
<td>Booster Voltage Status</td>
<td>‘1’ = Booster on, ‘0’ = Booster off</td>
</tr>
<tr>
<td>IDMOM</td>
<td>Idle Mode On/Off</td>
<td>‘1’ = Idle Mode On, ‘0’ = Idle Mode Off</td>
</tr>
<tr>
<td>PTLON</td>
<td>Partial Mode On/Off</td>
<td>‘1’ = Partial Mode On, ‘0’ = Partial Mode Off</td>
</tr>
<tr>
<td>SLPON</td>
<td>Sleep In/Out</td>
<td>‘1’ = Sleep Out, ‘0’ = Sleep In</td>
</tr>
<tr>
<td>NORON</td>
<td>Display Normal Mode/On/Off</td>
<td>‘1’ = Normal Display, ‘0’ = Partial Display</td>
</tr>
<tr>
<td>DISON</td>
<td>Display On/Off</td>
<td>‘1’ = Display On, ‘0’ = Display Off</td>
</tr>
<tr>
<td>D1</td>
<td>Not Used</td>
<td>‘0’</td>
</tr>
<tr>
<td>D0</td>
<td>Not Used</td>
<td>‘0’</td>
</tr>
</tbody>
</table>

**Legend**

- Command
- Display
- Parameter
- Action
- Mode
- Sequential transfer

**Default**

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value (D7 to D0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>0000_1000(08h)</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>0000_1000(08h)</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>0000_1000(08h)</td>
</tr>
</tbody>
</table>

**Flow Chart**

- **Serial I/F Mode**: RDDPM 0Ah
  - Send 2nd parameter
- **Parallel I/F Mode**: RDDPM 0Ah
  - Dummy Read
  - Send 2nd parameter
10.1.6 RDDMADCTL (0Bh): Read Display MADCTL

<table>
<thead>
<tr>
<th>Inst / Para</th>
<th>RDDMADCTL (Read Display MADCTL)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0BH</td>
<td>D/CX</td>
</tr>
<tr>
<td>RDDMADCTL</td>
<td>0</td>
</tr>
<tr>
<td>1st parameter</td>
<td>1</td>
</tr>
<tr>
<td>2nd parameter</td>
<td>1</td>
</tr>
</tbody>
</table>

This command indicates the current status of the display as described in the table below:

```
<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>MX</td>
<td>Column Address Order</td>
<td>'1' = Right to Left (When MADCTL B6='1')&lt;br&gt; '0' = Left to Right (When MADCTL B6='0')</td>
</tr>
<tr>
<td>MY</td>
<td>Row Address Order</td>
<td>'1' = Bottom to Top (When MADCTL B7='1')&lt;br&gt; '0' = Top to Bottom (When MADCTL B7='0')</td>
</tr>
<tr>
<td>MV</td>
<td>Row/Column Order (MV)</td>
<td>'1' = Row/column exchange (MV=1)&lt;br&gt; '0' = Normal (MV=0)</td>
</tr>
<tr>
<td>ML</td>
<td>Vertical Refresh Order</td>
<td>'1' = LCD Refresh Bottom to Top&lt;br&gt; '0' = LCD Refresh Top to Bottom</td>
</tr>
<tr>
<td>RGB</td>
<td>RGB/BGR Order</td>
<td>'1' = BGR, '0' = RGB</td>
</tr>
<tr>
<td>MH</td>
<td>Horizontal Refresh Order</td>
<td>LCD horizontal refresh direction control&lt;br&gt; '0' = LCD horizontal refresh Left to right&lt;br&gt; '1' = LCD horizontal refresh right to left</td>
</tr>
<tr>
<td>D1</td>
<td>Not Used</td>
<td>'0'</td>
</tr>
<tr>
<td>D0</td>
<td>Not Used</td>
<td>'0'</td>
</tr>
</tbody>
</table>
```

Status | Default Value (D7 to D0)
---|---
Power On Sequence | 0000_0000 (00h)
S/W Reset | No change
H/W Reset | 0000_0000 (00h)

Flow Chart

Legend

Command<br>Parameter<br>Display<br>Action<br>Mode<br>Sequential transfer
### 10.1.7 RDDCOLMOD (0Ch): Read Display Pixel Format

<table>
<thead>
<tr>
<th>Inst / Para</th>
<th>D/CX</th>
<th>WRX</th>
<th>RDDX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>RDDCOLMOD</td>
<td>0</td>
<td>↑</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>(0Ch)</td>
</tr>
<tr>
<td>1st parameter</td>
<td>1</td>
<td>1</td>
<td>↑</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>2nd parameter</td>
<td>1</td>
<td>1</td>
<td>↑</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>-</td>
<td>IFPF2</td>
</tr>
</tbody>
</table>

**Description**

This command indicates the current status of the display as described in the table below:

<table>
<thead>
<tr>
<th>IFPF[2:0]</th>
<th>MCU Interface Color Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>011</td>
<td>12-bit/pixel</td>
</tr>
<tr>
<td>101</td>
<td>16-bit/pixel</td>
</tr>
<tr>
<td>110</td>
<td>18-bit/pixel</td>
</tr>
<tr>
<td>111</td>
<td>No used</td>
</tr>
</tbody>
</table>

Others are no define and invalid

"-" Don't care

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>0110 (18 bits/pixel)</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>No Change</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>0110 (18 bits/pixel)</td>
</tr>
</tbody>
</table>

**Flow Chart**

[Diagram showing Serial and Parallel I/F Modes with RDDCOLMOD 0Ch, Send 2nd parameter, Dummy Read, and Send 2nd parameter]

**Legend**

- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer
10.1.8 RDDIM (0Dh): Read Display Image Mode

<table>
<thead>
<tr>
<th>Inst / Para</th>
<th>D/CX</th>
<th>WRX</th>
<th>RDX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>RDDIM</td>
<td>0</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0Dh</td>
<td></td>
</tr>
<tr>
<td>1st parameter</td>
<td>1</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>2nd parameter</td>
<td>1</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td>0VSSON</td>
<td>INVON</td>
<td>D6</td>
<td>D4</td>
<td>D3</td>
<td>GCS2</td>
<td>GCS1</td>
<td>GCS0</td>
<td></td>
</tr>
</tbody>
</table>

This command indicates the current status of the display as described in the table below:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSSON</td>
<td>Reversed</td>
<td>&quot;0&quot;</td>
</tr>
<tr>
<td>D6</td>
<td>Reversed</td>
<td>&quot;0&quot;</td>
</tr>
</tbody>
</table>
| INVON      | Inversion On/Off     | "1" = Inversion is On,  
              |            | "0" = Inversion is Off  |
| D4         | All Pixels On        | "0" (Not used)  |
| D3         | All Pixels Off       | "0" (Not used)  |
| GCS2       | Gamma Curve Selection| "000" = GC0,  
              |            | "001" = GC1,  
              |            | "010" = GC2,  
              |            | "011" = GC3, "100" to "111" = Not defined |

### Default

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value (D7 to D0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>0000_0000 (00h)</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>0000_0000 (00h)</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>0000_0000 (00h)</td>
</tr>
</tbody>
</table>

### Flow Chart

**Serial I/F Mode**
- RDDIM 0Dh
  - Send 2nd parameter

**Parallel I/F Mode**
- RDDIM 0Dh
  - Dummy Read
  - Send 2nd parameter

### Legend
- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer
**10.1.9 RDDSM (0Eh): Read Display Signal Mode**

<table>
<thead>
<tr>
<th>Inst / Para</th>
<th>D/CX</th>
<th>WRX</th>
<th>RDX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>RDDSM</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>(0Eh)</td>
</tr>
<tr>
<td>1&quot; parameter</td>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2&quot; parameter</td>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

This command indicates the current status of the display as described in the table below:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>TEON</td>
<td>Tearing Effect Line On/Off</td>
<td>&quot;1&quot; = On, &quot;0&quot; = Off</td>
</tr>
<tr>
<td>TELOM</td>
<td>Tearing effect line mode</td>
<td>&quot;1&quot; = mode2, &quot;0&quot; = mode1</td>
</tr>
<tr>
<td>D5</td>
<td>Not Used</td>
<td>&quot;1&quot; = On, &quot;0&quot; = Off</td>
</tr>
<tr>
<td>D4</td>
<td>Not Used</td>
<td>&quot;1&quot; = On, &quot;0&quot; = Off</td>
</tr>
<tr>
<td>D3</td>
<td>Not Used</td>
<td>&quot;1&quot; = On, &quot;0&quot; = Off</td>
</tr>
<tr>
<td>D2</td>
<td>Not Used</td>
<td>&quot;1&quot; = On, &quot;0&quot; = Off</td>
</tr>
<tr>
<td>D1</td>
<td>Not Used</td>
<td>&quot;1&quot; = On, &quot;0&quot; = Off</td>
</tr>
<tr>
<td>D0</td>
<td>Not Used</td>
<td>&quot;1&quot; = On, &quot;0&quot; = Off</td>
</tr>
</tbody>
</table>

**Default**

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value(D7~D0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>0000_0000 (00h)</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>0000_0000 (00h)</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>0000_0000 (00h)</td>
</tr>
</tbody>
</table>
Flow Chart

Serial I/F Mode
- Read RDDSM
  - Send 2nd parameter

Parallel I/F Mode
- Read RDDSM
  - Dummy Read
    - Send 2nd parameter

Legend
- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer
10.1.10 SLPIN (10h): Sleep In

<table>
<thead>
<tr>
<th>Parameter</th>
<th>No Parameter</th>
</tr>
</thead>
</table>

**Description**
- This command causes the LCD module to enter the minimum power consumption mode.
- In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.

**Restriction**
- This command has no effect when module is already in Sleep In mode. Sleep In Mode can only be exit by the Sleep Out Command (11h).
- When IC is in Sleep Out or Display On mode, it is necessary to wait 120msec before sending next command because of the stabilization timing for the supply voltages and clock circuits.

**Default**

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>Sleep in mode</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>Sleep in mode</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>Sleep in mode</td>
</tr>
</tbody>
</table>

**Flow Chart**

- SLPIN
- Display whole blank screen (Automatic No effect to DISP ON/OFF Commands)
- Drain Charge From LCD Panel
- Stop DC-DC Converter
- Stop Internal Oscillator
- Sleep In Mode

**Legend**
- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer
10.1.11 SLPOUT (11h): Sleep Out

<table>
<thead>
<tr>
<th>11H</th>
<th>D/CX</th>
<th>WRX</th>
<th>RDX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLPOUT</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1 (11h)</td>
</tr>
</tbody>
</table>

Parameter: No Parameter

- This command turns off sleep mode.
- In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.

Description

Restriction

- This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10h).
- When IC is in Sleep In mode, it is necessary to wait 120msec before sending next command because of the stabilization timing for the supply voltages and clock circuits.
- When IC is in Sleep Out or Display On mode, it is necessary to wait 120msec before sending next command due to the download of default value of registers and the execution of self-diagnostic function.

Default

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>Sleep in mode</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>Sleep in mode</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>Sleep in mode</td>
</tr>
</tbody>
</table>

Flow Chart

Legend

- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer

Legend
### 10.1.12 PTLON (12h): Partial Display Mode On

<table>
<thead>
<tr>
<th>Inst / Para</th>
<th>D/CX</th>
<th>WRX</th>
<th>RDX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>PTLON</td>
<td>0</td>
<td>↑</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>(12h)</td>
</tr>
<tr>
<td>Parameter</td>
<td>No Parameter</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Description**
- This command turns on Partial mode. The partial mode window is described by the Partial Area command (30h).
- To leave Partial mode, the Normal Display Mode On command (13h) should be written.
- * - Don't care

**Default**

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>Normal Mode On</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>Normal Mode On</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>Normal Mode On</td>
</tr>
</tbody>
</table>

**Flow Chart**
See Partial Area (30h)
### 10.1.13 NORON (13h): Normal Display Mode On

<table>
<thead>
<tr>
<th>Inst / Para</th>
<th>D/CX</th>
<th>WRX</th>
<th>RDX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>NORON</td>
<td>0</td>
<td>↑</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>(13h)</td>
</tr>
</tbody>
</table>

Parameter: No Parameter

**Description**
- This command returns the display to normal mode.
- Normal display mode on means Partial mode off.
- Exit from NORON by the Partial mode On command (12h)
- * Don’t care

**Default**

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>Normal Mode On</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>Normal Mode On</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>Normal Mode On</td>
</tr>
</tbody>
</table>

**Flow Chart**
See Partial Area Definition Descriptions for details of when to use this command
10.1.14 INVOFF (20h): Display Inversion Off

<table>
<thead>
<tr>
<th>20H</th>
<th>Inst / Para</th>
<th>D/CX</th>
<th>WRX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>INVOFF</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>(20h)</td>
</tr>
<tr>
<td>Parameter</td>
<td>No Parameter</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

**Description**
- This command is used to recover from display inversion mode.
- "*" Don’t care

(Example)

```
Top-Left
(0,0)
```

**Default**

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>Display Inversion off</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>Display Inversion off</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>Display Inversion off</td>
</tr>
</tbody>
</table>

**Flow Chart**

Legend

- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer

```
Display Inversion On
Mode

INVOFF (20h)

Display Inversion OFF
Mode
```

Memory    Display

```
Top-Left
(0,0)
```
### 10.1.15 INVON (21h): Display Inversion On

<table>
<thead>
<tr>
<th>Inst / Para</th>
<th>D/CX</th>
<th>WRX</th>
<th>RDX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>INVON</td>
<td>0</td>
<td>↑</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>(21h)</td>
</tr>
</tbody>
</table>

#### Parameter
- No Parameter

#### Description
- This command is used to enter into display inversion mode.
- To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.
- *: Don’t care

#### Flow Chart

![Flow Chart](image)

#### Legend
- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer

#### Default

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>Display Inversion off</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>Display Inversion off</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>Display Inversion off</td>
</tr>
</tbody>
</table>
10.1.16 GAMSET (26h): Gamma Set

This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table.

<table>
<thead>
<tr>
<th>GC [7:0]</th>
<th>Parameter</th>
<th>Curve Selected</th>
</tr>
</thead>
<tbody>
<tr>
<td>GS=1</td>
<td>GC0</td>
<td>Gamma Curve 1 (G2.2) Gamma Curve 1 (G1.0)</td>
</tr>
<tr>
<td>GS=0</td>
<td>GC1</td>
<td>Gamma Curve 2 (G1.8) Gamma Curve 2 (G2.5)</td>
</tr>
<tr>
<td></td>
<td>GC2</td>
<td>Gamma Curve 3 (G2.5) Gamma Curve 3 (G2.2)</td>
</tr>
<tr>
<td></td>
<td>GC3</td>
<td>Gamma Curve 4 (G1.0) Gamma Curve 4 (G1.8)</td>
</tr>
</tbody>
</table>

Note: All other values are undefined.

Default

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>01h</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>01h</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>01h</td>
</tr>
</tbody>
</table>

Flow Chart

Legend

- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer

GAMSET (26h) -> 1st parameter: GC[7:0] -> New Gamma Curve Loaded
10.1.17 DISPOFF (28h): Display Off

<table>
<thead>
<tr>
<th>28H</th>
<th>DISPOFF (Display Off)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inst / Para</td>
<td>D/CX</td>
</tr>
<tr>
<td>DISPOFF</td>
<td>0</td>
</tr>
<tr>
<td>Parameter</td>
<td>No Parameter</td>
</tr>
</tbody>
</table>

- This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.
- This command makes no change of contents of frame memory.
- This command does not change any other status.
- There will be no abnormal visible effect on the display.
- Exit from this command by Display On (29h)
- The delay time between DISPON and DISPOFF needs 120ms at least.

Note1: Complete 1 frame display (ex: continue 2-falling edges of VS)

Note2: Please use command 28h (display off) combined with command 10h (sleep in) to make module into display off status. Please check the application note of ST7735 when using display off function.

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>Display off</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>Display off</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>Display off</td>
</tr>
</tbody>
</table>

Flow Chart

Legend
- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer
### 10.1.18 DISPON (29h): Display On

<table>
<thead>
<tr>
<th>29H</th>
<th>DISPON (Display On)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DISPON</td>
<td>0 1 - 0 0 1 0 0 1 (29h)</td>
</tr>
<tr>
<td>Parameter</td>
<td>No Parameter</td>
</tr>
</tbody>
</table>
| Description | - This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.  
- This command makes no change of contents of frame memory.  
- This command does not change any other status.  
- The delay time between DISPON and DISPOFF needs 120ms at least |

#### Default

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>Display off</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>Display off</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>Display off</td>
</tr>
</tbody>
</table>

#### Flow Chart

- **Legend**
  - Command
  - Parameter
  - Display
  - Action
  - Mode
  - Sequential transfer

- **Display Off Mode**
- **DISPON**
- **Display On Mode**
# 10.1.19 CASET (2Ah): Column Address Set

<table>
<thead>
<tr>
<th>Inst / Para</th>
<th>D/CX</th>
<th>WRX</th>
<th>RDX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>CASET(2Ah)</td>
<td>0</td>
<td>↑</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>(2Ah)</td>
</tr>
<tr>
<td>1st parameter</td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>-</td>
<td>XS15</td>
<td>XS14</td>
<td>XS13</td>
<td>XS12</td>
<td>XS11</td>
<td>XS10</td>
<td>XS9</td>
<td>XS8</td>
<td></td>
</tr>
<tr>
<td>2nd parameter</td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>-</td>
<td>XS7</td>
<td>XS6</td>
<td>XS5</td>
<td>XS4</td>
<td>XS3</td>
<td>XS2</td>
<td>XS1</td>
<td>XS0</td>
<td></td>
</tr>
<tr>
<td>3rd parameter</td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>-</td>
<td>XE15</td>
<td>XE14</td>
<td>XE13</td>
<td>XE12</td>
<td>XE11</td>
<td>XE10</td>
<td>XE9</td>
<td>XE8</td>
<td></td>
</tr>
<tr>
<td>4th parameter</td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>-</td>
<td>XE7</td>
<td>XE6</td>
<td>XE5</td>
<td>XE4</td>
<td>XE3</td>
<td>XE2</td>
<td>XE1</td>
<td>XE0</td>
<td></td>
</tr>
</tbody>
</table>

### Description

- The value of XS [7:0] and XE [7:0] are referred when RAMWR command comes.
- Each value represents one column line in the Frame Memory.

![Frame Memory Diagram]

### Restriction

XS [15:0] always must be equal to or less than XE [15:0]

When XS [15:0] or XE [15:0] is greater than maximum address like below, data of out of range will be ignored.

1. 128X160 memory base (GM = '011')
   - (Parameter range: 0 < XS [15:0] < XE [15:0] < 127 (007Fh)): MV='0'
   - (Parameter range: 0 < XS [15:0] < XE [15:0] < 159 (009Fh)): MV='1'

2. 132X162 memory base (GM = '000')
   - (Parameter range: 0 < XS [15:0] < XE [15:0] < 131 (0083h)): MV='0'
   - (Parameter range: 0 < XS [15:0] < XE [15:0] < 161 (00A1h)): MV='1'

### Default

<table>
<thead>
<tr>
<th>GM Status</th>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>GM='011'</td>
<td>Power On Sequence</td>
<td>0000h</td>
</tr>
<tr>
<td>(128x160</td>
<td>S/W Reset</td>
<td>0000h</td>
</tr>
<tr>
<td>memory base)</td>
<td>H/W Reset</td>
<td>0000h</td>
</tr>
<tr>
<td></td>
<td></td>
<td>007Fh (127)</td>
</tr>
<tr>
<td></td>
<td>007Fh (127)</td>
<td>009Fh (159)</td>
</tr>
<tr>
<td></td>
<td>`</td>
<td></td>
</tr>
<tr>
<td>GM='000'</td>
<td>Power On Sequence</td>
<td>0000h</td>
</tr>
<tr>
<td>(132x162</td>
<td>S/W Reset</td>
<td>0000h</td>
</tr>
<tr>
<td>memory base)</td>
<td>H/W Reset</td>
<td>0000h</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0083h (131)</td>
</tr>
<tr>
<td></td>
<td>0083h (131)</td>
<td>00A1h (161)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Flow Chart

1. CASET
   - 1st parameter XS[15:0]
   - 2nd parameter XE[15:0]

2. PASET

3. CASET
   - 1st parameter YS[15:0]
   - 2nd parameter YE[15:0]

4. RAMWR

5. Image Data:
   - D1[7:0], D2[7:0]
   - ... , Dn[7:0]

6. Any Command

Legend:
- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer

If needed
## 10.1.20 RASET (2Bh): Row Address Set

### Description

The value of YS [7:0] and YE [7:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.

![Frame Memory Diagram](image)

### Restriction

YS [15:0] always must be equal to or less than YE [15:0]

When YS [15:0] or YE [15:0] are greater than maximum row address like below, data of out of range will be ignored.

1. 128X160 memory base (GM = '011')
   - (Parameter range: 0 < YS [15:0] < YE [15:0] < 159 (009Fh)): MV="0"
   - (Parameter range: 0 < YS [15:0] < YE [15:0] < 127 (007Fh)): MV="1"

2. 132X162 memory base (GM = '000')
   - (Parameter range: 0 < YS [15:0] < YE [15:0] < 161 (00A1h)): MV="0"
   - (Parameter range: 0 < YS [15:0] < YE [15:0] < 131 (0083h)): MV="1"

### Default

<table>
<thead>
<tr>
<th>GM status</th>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>GM='011' (128x160 memory base)</td>
<td>Power On Sequence</td>
<td>0000h</td>
</tr>
<tr>
<td></td>
<td>S/W Reset</td>
<td>0000h</td>
</tr>
<tr>
<td></td>
<td>H/W Reset</td>
<td>0000h</td>
</tr>
<tr>
<td>GM='000' (132x162 memory base)</td>
<td>Power On Sequence</td>
<td>0000h</td>
</tr>
<tr>
<td></td>
<td>S/W Reset</td>
<td>0000h</td>
</tr>
<tr>
<td></td>
<td>H/W Reset</td>
<td>0000h</td>
</tr>
</tbody>
</table>
Flow Chart

1st parameter XS[15:0]
2nd parameter XE[15:0] → CASET

1st parameter YS[15:0]
2nd parameter YE[15:0] → PASET

Image Data D1[7:0], D2[7:0], ..., Dn[7:0] → RAMWR

Any Command
### 10.1.21 RAMWR (2Ch): Memory Write

<table>
<thead>
<tr>
<th>2Ch (C/#)</th>
<th>RAMWR (Memory Write)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inst / Para</td>
<td>D/CX WRX RDX D17-8 D7 D6 D5 D4 D3 D2 D1 D0 HEX</td>
</tr>
<tr>
<td>RAMWR</td>
<td>0 ↑ 1 - 0 0 1 0 1 1 0 0 (2Ch)</td>
</tr>
<tr>
<td>1st parameter</td>
<td>1 ↑ 1 D17-8 D7 D6 D5 D4 D3 D2 D1 D0</td>
</tr>
<tr>
<td></td>
<td>1 ↑ 1 ↓ 1 ↓ 1 ↓ 1 ↓ 1 ↓ 1 ↓ 1 ↓ 1 ↓ 1</td>
</tr>
<tr>
<td>Nth parameter</td>
<td>1 ↑ 1 D17-8 D7 D6 D5 D4 D3 D2 D1 D0</td>
</tr>
</tbody>
</table>

#### Description

In all color modes, there is no restriction on length of parameters.

1. **128X160 memory base (GM = '011')**
   
   128x160x18-bit memory can be written by this command.
   
   Memory range: (0000h, 0000h) -> (007Fh, 09Fh)

2. **132x162 memory base (GM = '000')**
   
   132x162x18-bit memory can be written on this command.
   
   Memory range: (0000h, 0000h) -> (0083h, 00A1h)

#### Default

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>Contents of memory is set randomly</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>Contents of memory is not cleared</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>Contents of memory is not cleared</td>
</tr>
</tbody>
</table>

#### Flow Chart

- **Legend**
  - Command
  - Parameter
  - Display
  - Action
  - Mode
  - Sequential transfer

- **RAMWR**

- **Image Data**
  - D1[7:0], D2[7:0]
  - ... Dn[7:0]

- **Any Command**
### 10.1.22 RAMRD (2Eh): Memory Read

<table>
<thead>
<tr>
<th>Inst / Para</th>
<th>D/CX</th>
<th>WRX</th>
<th>RDX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAMHD</td>
<td>0</td>
<td>↑</td>
<td>-</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
<td>(2Eh)</td>
</tr>
<tr>
<td>1st parameter</td>
<td>1</td>
<td>↑</td>
<td></td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2nd parameter</td>
<td>1</td>
<td>↑</td>
<td></td>
<td>D17-8</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td></td>
</tr>
<tr>
<td>(N+1)th parameter</td>
<td>1</td>
<td>↑</td>
<td></td>
<td>D17-8</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td></td>
</tr>
</tbody>
</table>

**Description**

- This command is used to transfer data from frame memory to MCU.
- When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.
- The Start Column/Start Row positions are different in accordance with MADCTL setting.
- Then D[17:0] is read back from the frame memory and the column register and the row register incremented as section 9.10
- Frame Read can be cancelled by sending any other command.
- The data color coding is fixed to 18-bit in reading function. Please see section 9.8 “Data color coding” for color coding (18-bit cases), when there is used 8, 9, 16 and 18-bit data lines for image data.

**Note1:** The Command 3Ah should be set to 66h when reading pixel data from frame memory. Please check the LUT in chapter 9.17 when using memory read function.

**Default**

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>Contents of memory is set randomly</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>Contents of memory is not cleared</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>Contents of memory is not cleared</td>
</tr>
</tbody>
</table>

**Flow Chart**

Legend:
- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer

Diagram:

```
RAMRD

Dummy

Image Data
D1[7:0], D2[7:0], ...
```

```
Any Command
```
### 10.1.23 PTLAR (30h): Partial Area

<table>
<thead>
<tr>
<th>Inst / Para</th>
<th>D/CX</th>
<th>WRX</th>
<th>RDX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>PTLAR</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>(30h)</td>
</tr>
<tr>
<td>1st parameter</td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>-</td>
<td>PSL15</td>
<td>PSL14</td>
<td>PSL13</td>
<td>PSL12</td>
<td>PSL11</td>
<td>PSL10</td>
<td>PSL9</td>
<td>PSL8</td>
<td></td>
</tr>
<tr>
<td>2nd parameter</td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>-</td>
<td>PSL7</td>
<td>PSL6</td>
<td>PSL5</td>
<td>PSL4</td>
<td>PSL3</td>
<td>PSL2</td>
<td>PSL1</td>
<td>PSL0</td>
<td></td>
</tr>
<tr>
<td>3rd parameter</td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>-</td>
<td>PEL15</td>
<td>PEL14</td>
<td>PEL13</td>
<td>PEL12</td>
<td>PEL11</td>
<td>PEL10</td>
<td>PEL9</td>
<td>PEL8</td>
<td></td>
</tr>
<tr>
<td>4th parameter</td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>-</td>
<td>PEL7</td>
<td>PEL6</td>
<td>PEL5</td>
<td>PEL4</td>
<td>PEL3</td>
<td>PEL2</td>
<td>PEL1</td>
<td>PEL0</td>
<td></td>
</tr>
</tbody>
</table>

Description:
- This command defines the partial mode's display area.
- There are 4 parameters associated with this command, the first defines the Start Row (PSL) and the second the End Row (PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory row address counter.

- If End Row > Start Row, when MADCTL ML='0'

- If End Row < Start Row, when MADCTL ML='0'

- If End Row = Start Row then the Partial Area will be one row deep.

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>PSL [15:0]</td>
<td>GM[2:0]=&quot;xxx&quot;</td>
</tr>
<tr>
<td>PEL [15:0]</td>
<td>GM[2:0]=&quot;011&quot;</td>
</tr>
<tr>
<td>GM[2:0]</td>
<td>GM[2:0]=&quot;000&quot;</td>
</tr>
<tr>
<td>Power On Sequence</td>
<td>0000h</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>0000h</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>0000h</td>
</tr>
</tbody>
</table>
1. TO Enter Partial Mode:
- PLTAR
- SR[15:0]
- ER[15:0]
- PTLOM
- Partial Mode

2. Leave Partial Mode
- Partial Mode
- DISPOFF
- NORON
- Partial Mode
- OFF
- RAMRW
- Image Data D[7:0], D2[7:0], ...
- DISPON

Legend:
- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer
10.1.24 TEOFF (34h): Tearing Effect Line OFF

<table>
<thead>
<tr>
<th>34H</th>
<th>D/CX</th>
<th>WRX</th>
<th>RDX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>TEOFF</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>(34h)</td>
</tr>
</tbody>
</table>

Parameter: No Parameter

Description: This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>OFF</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>OFF</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>OFF</td>
</tr>
</tbody>
</table>

Flow Chart:

1. TE Line Output ON
2. TEOFF
3. TE Line Output OFF

Legend:
- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer
10.1.25 TEON (35h): Tearing Effect Line ON

-This command is used to turn ON the Tearing Effect output signal from the TE signal line.
-This output is not affected by changing MADCTL bit ML.
-The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line:
-When TELOM = '0': The Tearing Effect output line consists of V-Blanking information only
-When TELOM = '1': The Tearing Effect output line consists of both V-Blanking and H-Blanking information

Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>Tearing effect off &amp; TELOM=0</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>Tearing effect off &amp; TELOM=0</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>Tearing effect off &amp; TELOM=0</td>
</tr>
</tbody>
</table>

Flow Chart

Legend
- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer

Table:

<table>
<thead>
<tr>
<th>35H</th>
<th>D/CX</th>
<th>WRX</th>
<th>RDX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>TEON</td>
<td>0</td>
<td>↑</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>(35h)</td>
</tr>
<tr>
<td>Parameter</td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>TEOM</td>
<td></td>
</tr>
</tbody>
</table>

Description

Vertical time scale

TE Line Output OFF

TE ON

TELOM

TE Line Output ON
10.1.26 MADCTL (36h): Memory Data Access Control

<table>
<thead>
<tr>
<th>36H</th>
<th>MADCTL (Memory Data Access Control)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inst / Para</td>
<td>D/CX WRX RDX D17-8 D7 D6 D5 D4 D3 D2 D1 D0 HEX</td>
</tr>
<tr>
<td>MADCTL</td>
<td>0 ↑ 1 - 0 0 1 1 0 1 1 0 (36h)</td>
</tr>
<tr>
<td>Parameter</td>
<td>1 ↑ 1 - MY MX MV ML RGB MH - -</td>
</tr>
</tbody>
</table>

- This command defines read/write scanning direction of frame memory.

<table>
<thead>
<tr>
<th>Bit</th>
<th>NAME</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>MY</td>
<td>Row Address Order</td>
<td>These 3bits controls MCU to memory write/read direction.</td>
</tr>
<tr>
<td>MX</td>
<td>Column Address Order</td>
<td></td>
</tr>
<tr>
<td>MV</td>
<td>Row/Column Exchange</td>
<td></td>
</tr>
<tr>
<td>ML</td>
<td>Vertical Refresh Order</td>
<td>LCD vertical refresh direction control '0' = LCD vertical refresh Top to Bottom '1' = LCD vertical refresh Bottom to Top</td>
</tr>
<tr>
<td>RGB</td>
<td>RGB-BGR ORDER</td>
<td>Color selector switch control '0' = RGB color filter panel, '1' = BGR color filter panel</td>
</tr>
<tr>
<td>MH</td>
<td>Horizontal Refresh Order</td>
<td>LCD horizontal refresh direction control '0' = LCD horizontal refresh Left to right '1' = LCD horizontal refresh right to left</td>
</tr>
</tbody>
</table>

- Bit Assignment

**Description**

<table>
<thead>
<tr>
<th>RGB=&quot;0&quot;</th>
<th>R G B</th>
<th>SIG1</th>
<th>SIG2</th>
<th>SIG132</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCD panel</td>
<td>R G B</td>
<td>R G B</td>
<td>R G B</td>
<td>R G B</td>
</tr>
<tr>
<td>Driver IC</td>
<td>R G B</td>
<td>R G B</td>
<td>R G B</td>
<td>R G B</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>RGB=&quot;1&quot;</th>
<th>R G B</th>
<th>SIG1</th>
<th>SIG2</th>
<th>SIG132</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCD panel</td>
<td>B G R</td>
<td>B G R</td>
<td>B G R</td>
<td>B G R</td>
</tr>
<tr>
<td>Driver IC</td>
<td>B G R</td>
<td>B G R</td>
<td>B G R</td>
<td>B G R</td>
</tr>
</tbody>
</table>
ST7735

Memory Display

Top-left (0, 0)  Top-left (0, 0)

ML="0"

Top-left (0, 0)  Top-left (0, 0)

ML="1"

Top-left (0, 0)  Top-left (0, 0)

Display

Send first
Send 2nd
Send 3rd
Send last
Send first
Send 2nd
Send 3rd
Send last

Legend

Command
Parameter
Display
Action
Mode
Sequential transfer

Flow Chart

Status

<table>
<thead>
<tr>
<th></th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>No Change</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0</td>
</tr>
</tbody>
</table>

Default Value

Power On Sequence MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0
S/W Reset No Change
H/W Reset MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0
### 10.1.27 IDMOFF (38h): Idle Mode Off

<table>
<thead>
<tr>
<th>38H</th>
<th>IDMOFF (Idle Mode Off)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inst / Para</td>
<td>D/CX</td>
</tr>
<tr>
<td>IDMOFF</td>
<td>0</td>
</tr>
<tr>
<td>Parameter</td>
<td>No Parameter</td>
</tr>
</tbody>
</table>

**Description**
- This command is used to recover from Idle mode on.
- In the idle off mode,
  1. LCD can display 4096, 65k or 262k colors.
  2. Normal frame frequency is applied.

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>Idle Mode Off</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>Idle Mode Off</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>Idle Mode Off</td>
</tr>
</tbody>
</table>

**Legend**
- Command
- Parameter
- Display
- Action
- Mode
- Sequential transter

---

**Flow Chart**

1. Idle on mode
2. IDMOFF
3. Idle off mode
10.1.28 IDMON (39h): Idle Mode On

- This command is used to enter into Idle mode on.
- There will be no abnormal visible effect on the display mode change transition.
- In the idle on mode,
  1. Color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.
  2. 8-Color mode frame frequency is applied.
  3. Exit from IDMON by Idle Mode Off (38h) command

<table>
<thead>
<tr>
<th>Color</th>
<th>R5</th>
<th>R4</th>
<th>R3</th>
<th>R2</th>
<th>R1</th>
<th>R0</th>
<th>G5</th>
<th>G4</th>
<th>G3</th>
<th>G2</th>
<th>G1</th>
<th>G0</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Black</td>
<td>0xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Blue</td>
<td>0xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Red</td>
<td>1xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Magenta</td>
<td>1xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Green</td>
<td>0xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cyan</td>
<td>0xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Yellow</td>
<td>1xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>White</td>
<td>1xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Register Availability

<table>
<thead>
<tr>
<th>Status</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal Mode On, Idle Mode Off, Sleep Out</td>
<td>Yes</td>
</tr>
<tr>
<td>Normal Mode On, Idle Mode On, Sleep Out</td>
<td>Yes</td>
</tr>
<tr>
<td>Partial Mode On, Idle Mode Off, Sleep Out</td>
<td>No</td>
</tr>
<tr>
<td>Partial Mode On, Idle Mode On, Sleep Out</td>
<td>No</td>
</tr>
<tr>
<td>Sleep In</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Default

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>Idle Mode Off</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>Idle Mode Off</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>Idle Mode Off</td>
</tr>
</tbody>
</table>
Flow Chart

Legend
- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer

- Idle off mode
- IDMON
- Idle on mode
10.1.29 COLMOD (3Ah): Interface Pixel Format

This command is used to define the format of RGB picture data, which is to be transferred via the MCU interface. The formats are shown in the table:

<table>
<thead>
<tr>
<th>IFPF[2:0]</th>
<th>MCU Interface Color Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>011</td>
<td>3 12-bit/pixel</td>
</tr>
<tr>
<td>101</td>
<td>5 16-bit/pixel</td>
</tr>
<tr>
<td>110</td>
<td>6 18-bit/pixel</td>
</tr>
<tr>
<td>111</td>
<td>7 No used</td>
</tr>
</tbody>
</table>

Note1: In 12-bit/Pixel, 16-bit/Pixel or 18-bit/Pixel mode, the LUT is applied to transfer data into the Frame Memory.

Note2: When writing 16-bit/pixel data into frame memory, the Command 3Ah should be set at 55h, but re-set to 66h when reading pixel data from frame memory. Please check the LUT in chapter 9.17 when using memory read function.

<table>
<thead>
<tr>
<th>Status</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal Mode On, Idle Mode Off, Sleep Out</td>
<td>Yes</td>
</tr>
<tr>
<td>Normal Mode On, Idle Mode On, Sleep Out</td>
<td>Yes</td>
</tr>
<tr>
<td>Partial Mode On, Idle Mode Off, Sleep Out</td>
<td>No</td>
</tr>
<tr>
<td>Partial Mode On, Idle Mode On, Sleep Out</td>
<td>No</td>
</tr>
<tr>
<td>Sleep In</td>
<td>Yes</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>IFPF[2:0]</td>
<td>VIPF[3:0]</td>
</tr>
<tr>
<td>Power On Sequence</td>
<td>0110(18-bit/ Pixel)</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>No Change</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>0110(18-bit/ Pixel)</td>
</tr>
</tbody>
</table>
10.1.30 RDID1 (DAh): Read ID1 Value

<table>
<thead>
<tr>
<th>DAH</th>
<th>RDID1 (Read ID1 Value)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inst / Para</td>
<td>D/CX</td>
</tr>
<tr>
<td>RDID1</td>
<td>0</td>
</tr>
<tr>
<td>1st parameter</td>
<td>1</td>
</tr>
<tr>
<td>2nd parameter</td>
<td>1</td>
</tr>
</tbody>
</table>

Description
- This read byte returns 8-bit LCD module’s manufacturer ID
- The 1st parameter is dummy data
- The 2nd parameter (ID17 to ID10): LCD module’s manufacturer ID.

NOTE: See command RDDID (04h), 2nd parameter.

Register Availability

<table>
<thead>
<tr>
<th>Status</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal Mode On, Idle Mode Off, Sleep Out</td>
<td>Yes</td>
</tr>
<tr>
<td>Normal Mode On, Idle Mode On, Sleep Out</td>
<td>Yes</td>
</tr>
<tr>
<td>Partial Mode On, Idle Mode Off, Sleep Out</td>
<td>No</td>
</tr>
<tr>
<td>Partial Mode On, Idle Mode On, Sleep Out</td>
<td>No</td>
</tr>
<tr>
<td>Sleep In</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Default

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>0x5C</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>0x5C</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>0x5C</td>
</tr>
</tbody>
</table>

Flow Chart

<table>
<thead>
<tr>
<th>Serial I/F Mode</th>
<th>Parallel I/F Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read ID1</td>
<td>Read ID1</td>
</tr>
<tr>
<td>Send 2nd parameter</td>
<td>Dummy Read</td>
</tr>
<tr>
<td></td>
<td>Send 2nd parameter</td>
</tr>
</tbody>
</table>
10.1.31 RDID2 (DBh): Read ID2 Value

<table>
<thead>
<tr>
<th>RDID2</th>
<th>Inst / Para</th>
<th>D/CX</th>
<th>WRX</th>
<th>RXD</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>-</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>(DBh)</td>
</tr>
<tr>
<td>1st parameter</td>
<td>1</td>
<td>1</td>
<td>↑</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>2nd parameter</td>
<td>1</td>
<td>1</td>
<td>↑</td>
<td>-</td>
<td>1</td>
<td>ID26</td>
<td>ID25</td>
<td>ID24</td>
<td>ID23</td>
<td>ID22</td>
<td>ID21</td>
<td>ID20</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- This read byte returns 8-bit LCD module/driver version ID
- The 1st parameter is dummy data
- The 2nd parameter (ID26 to ID20): LCD module/driver version ID
- Parameter Range: ID=80h to FFh

<table>
<thead>
<tr>
<th>ID26 to ID20</th>
<th>Version</th>
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NOTE: See command RDDID (04h), 3rd parameter.
### 10.1.32 RDID3 (DCh): Read ID3 Value

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#### Description
- This read byte returns 8-bit LCD module/driver ID.
- The 1st parameter is dummy data.
- The 2nd parameter (ID37 to ID30): LCD module/driver ID.

**NOTE:** See command RDDID (04h), 4th parameter.

#### Register Availability

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#### Default

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<td>H/W Reset</td>
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#### Flow Chart

**Serial I/F Mode**
- Read ID3
- Send 2nd parameter

**Parallel I/F Mode**
- Read ID3
- Dummy Read
- Send 2nd parameter

**Legend**
- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer
### 10.2 Panel Function Command List and Description

#### Table 10.2.1 Panel Function Command List (1)

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<th>Instruction</th>
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<th>WRX</th>
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Note 1: C0h to C7h are fixed for about power controller
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<td>Sapa</td>
<td>Sapa</td>
<td>Sapa</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>[2]</td>
<td>[1]</td>
<td>[0]</td>
<td>[2]</td>
<td>[1]</td>
<td>[0]</td>
<td>[2]</td>
<td>[1]</td>
<td>[0]</td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>NVCTR1</td>
<td>10.2.16</td>
<td>0 ↑ 1</td>
<td>- 1 1 0 1 1 0 0 0 1</td>
<td>(D9)</td>
<td>EEPROM control status</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td></td>
<td></td>
<td>1 ↑ 1</td>
<td>- 0 0 VMF_EN</td>
<td>ID2_EN</td>
<td>0 0 0 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NVCTR2</td>
<td>10.2.17</td>
<td>0 ↑ 1</td>
<td>- 1 1 0 1 1 1 1 0</td>
<td>(DEh)</td>
<td>EEPROM Read Command</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 ↑ 1</td>
<td>- 1 0 1 0 0 1 0 1 0 1</td>
<td>A5</td>
<td>Action code</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
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</tr>
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<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NVCTR3</td>
<td>10.2.18</td>
<td>0 ↑ 1</td>
<td>- EE_IB7</td>
<td>EE_IB6</td>
<td>EE_IB5</td>
<td>EE_IB4</td>
<td>EE_IB3</td>
<td>EE_IB2</td>
<td>EE_IB1</td>
<td>EE_IB0</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 ↑ 1</td>
<td>- EE_CMD7</td>
<td>EE_CMD6</td>
<td>EE_CMD5</td>
<td>EE_CMD4</td>
<td>EE_CMD3</td>
<td>EE_CMD2</td>
<td>EE_CMD1</td>
<td>EE_CMD0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: The D1h to D3h registers are fixed for about ID code setting.
Note 2: The D9h, DEh and DFh registers are used for NV Memory function controller. (Ex: write, clear, etc.)
<table>
<thead>
<tr>
<th>Instruction</th>
<th>Refer</th>
<th>D/CX</th>
<th>WRX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>Hex</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
<td>(E0h)</td>
<td>Set</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>1</td>
<td>1</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Gamma adjustment (+ polarity)</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>1</td>
<td>1</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Gamma adjustment (- polarity)</td>
</tr>
</tbody>
</table>

**EXTCTRL**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Refer</th>
<th>D/CX</th>
<th>WRX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>Hex</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
<td>(F0h)</td>
<td>Extension Command Control</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
<td>0</td>
<td>(F0h)</td>
<td>Extension Command Control</td>
</tr>
</tbody>
</table>

**VCOMU**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Refer</th>
<th>D/CX</th>
<th>WRX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>Hex</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>(F0h)</td>
<td>Vcom 4 Level control</td>
</tr>
</tbody>
</table>

**GAMCTR**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Refer</th>
<th>D/CX</th>
<th>WRX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>Hex</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Gamma adjustment (+ polarity)</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>1</td>
<td>1</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Gamma adjustment (- polarity)</td>
</tr>
</tbody>
</table>

**Table 10.2.4 Panel Function Command List (4)**

**Note 1:** E0-E1 registers are fixed for adjusting Gamma
### 10.2.1 FRMCTR1 (B1h): Frame Rate Control (In normal mode/ Full colors)

<table>
<thead>
<tr>
<th>B1H</th>
<th>FRMCTR1 (Frame Rate Control)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Inst / Para</td>
</tr>
<tr>
<td>FRMCTR1</td>
<td>0</td>
</tr>
<tr>
<td>1st parameter</td>
<td>1</td>
</tr>
<tr>
<td>2nd parameter</td>
<td>1</td>
</tr>
<tr>
<td>3rd parameter</td>
<td>1</td>
</tr>
</tbody>
</table>

### Description
- Set the frame frequency of the full colors normal mode.
  - Frame rate = fosc / ((RTNA + 20) x (LINE + FPA + BPA))
  - 1 < FPA(front porch) + BPA(back porch) ; Back porch ≠ 0

Note: fosc = 333kHz

### Default

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>GM[2:0] = &quot;000&quot;</td>
</tr>
<tr>
<td></td>
<td>GM[2:0] = &quot;011&quot;</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>02h/2Ch/2Dh</td>
</tr>
<tr>
<td></td>
<td>02h/2Dh/2Eh</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>02h/2Ch/2Dh</td>
</tr>
<tr>
<td></td>
<td>02h/2Dh/2Eh</td>
</tr>
</tbody>
</table>

### Flow Chart

#### Legend
- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer

---

1st Parameter
2nd parameter
10.2.2 FRMCTR2 (B2h): Frame Rate Control (In Idle mode/ 8-colors)

<table>
<thead>
<tr>
<th>Inst / Para</th>
<th>D/CX</th>
<th>WRX</th>
<th>RDX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>FRMCTR2</td>
<td>0</td>
<td>↑</td>
<td>1</td>
<td>-</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>(B2h)</td>
</tr>
<tr>
<td>1st parameter</td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>RTNB3</td>
</tr>
<tr>
<td>2nd parameter</td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>FPB5</td>
<td>FPB4</td>
<td>FPB3</td>
<td>FPB2</td>
<td>FPB1</td>
<td>FPB0</td>
</tr>
<tr>
<td>3rd parameter</td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>BPB5</td>
<td>BPB4</td>
<td>BPB3</td>
<td>BPB2</td>
<td>BPB1</td>
<td>BPB0</td>
</tr>
</tbody>
</table>

Description

- Set the frame frequency of the Idle mode.
- Frame rate = \( \frac{f_{osc}}{(RTNB + 20) \times (LINE + FPB + BPB)} \)
- \( 1 < \text{FPB(front porch)} + \text{BPB(back porch)} \); Back porch \( \neq 0 \)

Note: \( f_{osc} = 333kHz \)

Default

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>( \text{GM}[2:0] = &quot;000&quot; ) ( \text{GM}[2:0] = &quot;011&quot; )</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>02h/2Ch/2Dh</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>02h/2Ch/2Dh</td>
</tr>
</tbody>
</table>

Flow Chart
10.2.3 FRMCTR3 (B3h): Frame Rate Control (In Partial mode/ full colors)

### Description
- Set the frame frequency of the Partial mode/full colors.
- 1st parameter to 3rd parameter are used in line inversion mode.
- 4th parameter to 6th parameter are used in frame inversion mode.
- Frame rate = \( f_{osc} / ((RTNC + 20) \times (LINE + FPC + BPC)) \)
- \( 1 < FPC \) (front porch) + \( BPC \) (back porch) ; Back porch \( \neq 0 \)

#### Note: \( f_{osc} = 333\text{kHz} \)

### Default

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>GM[2:0] = &quot;000&quot;</td>
<td>GM[2:0] = &quot;011&quot;</td>
</tr>
<tr>
<td>Power On Sequence</td>
<td>02h/2Ch/2Dh/02h/2Ch/2Dh 02h/2Dh/2Eh/02h/2Dh/2Eh</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>02h/2Ch/2Dh/02h/2Ch/2Dh 02h/2Dh/2Eh/02h/2Dh/2Eh</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>02h/2Ch/2Dh/02h/2Ch/2Dh 02h/2Dh/2Eh/02h/2Dh/2Eh</td>
</tr>
</tbody>
</table>

### Flow Chart

#### Legend
- **Legend**
  - Command
  - Parameter
  - Display
  - Action
  - Mode
  - Sequential transfer

#### Flow Chart

1. Set the frame frequency of the Partial mode/full colors.
2. 1st parameter to 3rd parameter are used in line inversion mode.
3. 4th parameter to 6th parameter are used in frame inversion mode.
4. Frame rate = \( f_{osc} / ((RTNC + 20) \times (LINE + FPC + BPC)) \)
5. \( 1 < FPC \) (front porch) + \( BPC \) (back porch) ; Back porch \( \neq 0 \)

#### Note: \( f_{osc} = 333\text{kHz} \)
### 10.2.4 INVCTR (B4h): Display Inversion Control

<table>
<thead>
<tr>
<th>B4H</th>
<th>D/CX</th>
<th>WRX</th>
<th>RDX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>INVCTR</td>
<td>0</td>
<td>↑</td>
<td>1</td>
<td>-</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>(B4h)</td>
</tr>
<tr>
<td>Parameter</td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>NLA</td>
<td>NLB</td>
<td>NLC</td>
<td></td>
</tr>
</tbody>
</table>

**Description**

- **Display Inversion mode control**
  - **NLA**: Inversion setting in full colors normal mode (Normal mode on)
    - 0: Line Inversion
    - 1: Frame Inversion
  - **NLB**: Inversion setting in Idle mode (Idle mode on)
    - 0: Line Inversion
    - 1: Frame Inversion
  - **NLC**: Inversion setting in full colors partial mode (Partial mode on / Idle mode off)
    - 0: Line Inversion
    - 1: Frame Inversion

**Default**

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
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</thead>
<tbody>
<tr>
<td>NLA</td>
<td>NLB</td>
</tr>
<tr>
<td>Power On Sequence</td>
<td>1d</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>1d</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>1d</td>
</tr>
</tbody>
</table>

**Flow Chart**

[Flow Chart Diagram]

**Legend**

- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer
10.2.5 DISSET5 (B6h): Display Function set 5

<table>
<thead>
<tr>
<th>B6H</th>
<th>DISSET (Display Function set 5)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inst / Para</td>
<td>D/CX</td>
</tr>
<tr>
<td>DISSET5</td>
<td>0</td>
</tr>
<tr>
<td>1st parameter</td>
<td>1</td>
</tr>
<tr>
<td>2nd parameter</td>
<td>1</td>
</tr>
</tbody>
</table>

1st parameter: Set output waveform relation.

- **NO[1:0]**: Set the amount of non-overlap of the gate output

<table>
<thead>
<tr>
<th>NO[1:0]</th>
<th>Amount of non-overlap of the gate output</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>00h</td>
</tr>
<tr>
<td>01</td>
<td>01h</td>
</tr>
<tr>
<td>10</td>
<td>02h</td>
</tr>
<tr>
<td>11</td>
<td>03h</td>
</tr>
</tbody>
</table>

- **SDT[1:0]**: Set delay amount from gate signal rising edge of the source output.

<table>
<thead>
<tr>
<th>SDT[1:0]</th>
<th>Delay amount form gate signal rising edge of the source output</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>00h</td>
</tr>
<tr>
<td>01</td>
<td>01h</td>
</tr>
<tr>
<td>10</td>
<td>02h</td>
</tr>
<tr>
<td>11</td>
<td>03h</td>
</tr>
</tbody>
</table>

- **EQ[1:0]**: Set the Equalizing period

<table>
<thead>
<tr>
<th>EQ[1:0]</th>
<th>Equalizing period</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>00h</td>
</tr>
<tr>
<td>01</td>
<td>01h</td>
</tr>
<tr>
<td>10</td>
<td>02h</td>
</tr>
<tr>
<td>11</td>
<td>03h</td>
</tr>
</tbody>
</table>

2nd parameter: Set the output waveform in non-display area.

- **PTG[1:0]**: Determine gate output in a non-display area in the partial mode

<table>
<thead>
<tr>
<th>PTG[1:0]</th>
<th>Gate output in a non-display area</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>00h</td>
</tr>
<tr>
<td>01</td>
<td>01h</td>
</tr>
<tr>
<td>10</td>
<td>02h</td>
</tr>
<tr>
<td>11</td>
<td>03h</td>
</tr>
</tbody>
</table>

- **PT[1:0]**: Determine Source /VCOM output in a non-display area in the partial mode

<table>
<thead>
<tr>
<th>PT[1:0]</th>
<th>Source output on non-display area</th>
<th>VCOM output on non-display area</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>00h</td>
<td>V63</td>
</tr>
<tr>
<td>01</td>
<td>01h</td>
<td>V0</td>
</tr>
<tr>
<td>10</td>
<td>02h</td>
<td>AGND</td>
</tr>
<tr>
<td>11</td>
<td>03h</td>
<td>Hi-z</td>
</tr>
</tbody>
</table>

Description

- **Gn**: Gate
- **Gn+1**: Gate
- **Sn**: Source
- **VCOM**: VCOM
- **EQ period**: Equalizing period
- **Delay time for source output**: Delay time for source output
- **Gate Non-Overlap period**: Gate Non-Overlap period

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### ST7735

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Default B6h</td>
<td></td>
</tr>
<tr>
<td>Power On Sequence</td>
<td>15h/00h</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>15h/00h</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>15h/00h</td>
</tr>
</tbody>
</table>

#### Flow Chart

- **DISSET5**
- **1st Parameter**
- **2nd Parameter**

**Legend**

- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer
10.2.6 PWCTR1 (C0h): Power Control 1

<table>
<thead>
<tr>
<th>C0H</th>
<th>PWCTR1 (Power Control 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inst / Para</td>
<td>D/CX</td>
</tr>
<tr>
<td>PWCTR1</td>
<td>0</td>
</tr>
<tr>
<td>1(^{st}) parameter</td>
<td>1</td>
</tr>
<tr>
<td>2(^{nd}) parameter</td>
<td>1</td>
</tr>
</tbody>
</table>

- Set the GVDD voltage
- Note: AVDD=5.3V

<table>
<thead>
<tr>
<th>VRH[4:0]</th>
<th>GVDD</th>
</tr>
</thead>
<tbody>
<tr>
<td>00000</td>
<td>5.00</td>
</tr>
<tr>
<td>00001</td>
<td>01h</td>
</tr>
<tr>
<td>00010</td>
<td>02h</td>
</tr>
<tr>
<td>00011</td>
<td>03h</td>
</tr>
<tr>
<td>00100</td>
<td>04h</td>
</tr>
<tr>
<td>00101</td>
<td>05h</td>
</tr>
<tr>
<td>00110</td>
<td>06h</td>
</tr>
<tr>
<td>00111</td>
<td>07h</td>
</tr>
<tr>
<td>01000</td>
<td>08h</td>
</tr>
<tr>
<td>01001</td>
<td>09h</td>
</tr>
<tr>
<td>01010</td>
<td>0Ah</td>
</tr>
<tr>
<td>01011</td>
<td>0Bh</td>
</tr>
<tr>
<td>01100</td>
<td>0Ch</td>
</tr>
<tr>
<td>01101</td>
<td>0Dh</td>
</tr>
<tr>
<td>01110</td>
<td>0 Eh</td>
</tr>
<tr>
<td>01111</td>
<td>0Fh</td>
</tr>
<tr>
<td>10000</td>
<td>10h</td>
</tr>
<tr>
<td>10001</td>
<td>11h</td>
</tr>
<tr>
<td>10010</td>
<td>12h</td>
</tr>
<tr>
<td>10011</td>
<td>13h</td>
</tr>
<tr>
<td>10100</td>
<td>14h</td>
</tr>
<tr>
<td>10101</td>
<td>15h</td>
</tr>
<tr>
<td>10110</td>
<td>16h</td>
</tr>
<tr>
<td>10111</td>
<td>17h</td>
</tr>
<tr>
<td>11000</td>
<td>18h</td>
</tr>
<tr>
<td>11001</td>
<td>19h</td>
</tr>
<tr>
<td>11010</td>
<td>1Ah</td>
</tr>
<tr>
<td>11011</td>
<td>1Bh</td>
</tr>
<tr>
<td>11100</td>
<td>1Ch</td>
</tr>
<tr>
<td>11101</td>
<td>1Dh</td>
</tr>
<tr>
<td>11110</td>
<td>1 Eh</td>
</tr>
<tr>
<td>11111</td>
<td>1Fh</td>
</tr>
</tbody>
</table>

Description

- If this register not using the register need be reserved.
- The deviation value of GVDD between with Measurement and Specification : Max <= 50mV

<table>
<thead>
<tr>
<th>IB_SEL[1:0]</th>
<th>AVDD</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>00h</td>
</tr>
<tr>
<td>01</td>
<td>01h</td>
</tr>
<tr>
<td>10</td>
<td>02h</td>
</tr>
<tr>
<td>11</td>
<td>03h</td>
</tr>
</tbody>
</table>

Restriction

Register Availability

<table>
<thead>
<tr>
<th>Status</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal Mode On, Idle Mode Off, Sleep Out</td>
<td>Yes</td>
</tr>
<tr>
<td>Normal Mode On, Idle Mode On, Sleep Out</td>
<td>Yes</td>
</tr>
<tr>
<td>Partial Mode On, Idle Mode Off, Sleep Out</td>
<td>Yes</td>
</tr>
<tr>
<td>Partial Mode On, Idle Mode On, Sleep Out</td>
<td>Yes</td>
</tr>
<tr>
<td>Sleep In</td>
<td>Yes</td>
</tr>
</tbody>
</table>
### Default Status

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>02h/70h</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>02h/70h</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>02h/70h</td>
</tr>
</tbody>
</table>

### Flow Chart

**Legend**
- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer

Flowchart diagram:

1. PWCTR1
2. 1st Parameter
3. 2nd Parameter
## 10.2.7 PWCTR2 (C1h): Power Control 2

### Description

- Set the VGH and VGL supply power level

<table>
<thead>
<tr>
<th>BT[2:0]</th>
<th>VGH</th>
<th>VGL</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>4X 9.8</td>
<td>-3X  -7.35</td>
</tr>
<tr>
<td>001</td>
<td>4X 9.8</td>
<td>-4X  -9.8</td>
</tr>
<tr>
<td>010</td>
<td>5X 12.25</td>
<td>-3X  -7.35</td>
</tr>
<tr>
<td>011</td>
<td>5X 12.25</td>
<td>-4X  -9.8</td>
</tr>
<tr>
<td>100</td>
<td>5X 12.25</td>
<td>-5X  -12.25</td>
</tr>
<tr>
<td>101</td>
<td>6X 14.7</td>
<td>-3X  -7.35</td>
</tr>
<tr>
<td>110</td>
<td>6X 14.7</td>
<td>-4X  -9.8</td>
</tr>
<tr>
<td>111</td>
<td>6X 14.7</td>
<td>-5X  -12.25</td>
</tr>
</tbody>
</table>

### Restriction

- If this register not using the register need be reserved.
- The deviation value of VGH/ VGL between with Measurement and Specification: Max <= 1V
- VGH-VGL <= 32V

### Register Availability

<table>
<thead>
<tr>
<th>Status</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal Mode On, Idle Mode Off, Sleep Out</td>
<td>Yes</td>
</tr>
<tr>
<td>Normal Mode On, Idle Mode On, Sleep Out</td>
<td>Yes</td>
</tr>
<tr>
<td>Partial Mode On, Idle Mode Off, Sleep Out</td>
<td>Yes</td>
</tr>
<tr>
<td>Partial Mode On, Idle Mode On, Sleep Out</td>
<td>Yes</td>
</tr>
<tr>
<td>Sleep In</td>
<td>Yes</td>
</tr>
</tbody>
</table>

### Default

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>05h</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>05h</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>05h</td>
</tr>
</tbody>
</table>

### Flow Chart

![Flow Chart Diagram]

Legend:
- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer
## 10.2.8 PWCTR3 (C2h): Power Control 3 (in Normal mode/Full colors)

<table>
<thead>
<tr>
<th>Inst / Para</th>
<th>D/CX</th>
<th>WRX</th>
<th>RDX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWCTR3</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

### Description

- Set the amount of current in Operational amplifier in normal mode/full colors.
- Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

#### AP[2:0] Amount of Current in Operational Amplifier

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>00h Operation of the operational amplifier stops</td>
</tr>
<tr>
<td>001</td>
<td>01h Small</td>
</tr>
<tr>
<td>010</td>
<td>02h Medium Low</td>
</tr>
<tr>
<td>011</td>
<td>03h Medium</td>
</tr>
<tr>
<td>100</td>
<td>04h Medium High</td>
</tr>
<tr>
<td>101</td>
<td>05h Large</td>
</tr>
<tr>
<td>110</td>
<td>06h Reserved</td>
</tr>
<tr>
<td>111</td>
<td>07h Reserved</td>
</tr>
</tbody>
</table>

#### DC[2:0] Step-up cycle in Booster circuit

<table>
<thead>
<tr>
<th>Value</th>
<th>Step-up cycle in Booster circuit 1</th>
<th>Step-up cycle in Booster circuit 2,4</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>00h BCLK / 1</td>
<td>BCLK / 1</td>
</tr>
<tr>
<td>001</td>
<td>01h BCLK / 1</td>
<td>BCLK / 2</td>
</tr>
<tr>
<td>010</td>
<td>02h BCLK / 1</td>
<td>BCLK / 4</td>
</tr>
<tr>
<td>011</td>
<td>03h BCLK / 2</td>
<td>BCLK / 2</td>
</tr>
<tr>
<td>100</td>
<td>04h BCLK / 2</td>
<td>BCLK / 4</td>
</tr>
<tr>
<td>101</td>
<td>05h BCLK / 4</td>
<td>BCLK / 4</td>
</tr>
<tr>
<td>110</td>
<td>06h BCLK / 4</td>
<td>BCLK / 8</td>
</tr>
<tr>
<td>111</td>
<td>07h BCLK / 4</td>
<td>BCLK / 16</td>
</tr>
</tbody>
</table>

Note: BCLK is Clock frequency for Booster circuit

### Restriction

- If this register not using the register need be reserved.

### Register Availability

<table>
<thead>
<tr>
<th>Status</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal Mode On, Idle Mode Off, Sleep Out</td>
<td>Yes</td>
</tr>
<tr>
<td>Normal Mode On, Idle Mode On, Sleep Out</td>
<td>Yes</td>
</tr>
<tr>
<td>Partial Mode On, Idle Mode Off, Sleep Out</td>
<td>Yes</td>
</tr>
<tr>
<td>Partial Mode On, Idle Mode On, Sleep Out</td>
<td>Yes</td>
</tr>
<tr>
<td>Sleep In</td>
<td>Yes</td>
</tr>
</tbody>
</table>

### Default

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>01h/01h</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>01h/01h</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>01h/01h</td>
</tr>
</tbody>
</table>
### 10.2.9 PWCTR4 (C3h): Power Control 4 (in Idle mode/ 8-colors)

<table>
<thead>
<tr>
<th>C3H</th>
<th>PWCTR4 (Power Control 4)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inst / Para</td>
<td>D/CX</td>
</tr>
<tr>
<td>PWCTR4</td>
<td>0</td>
</tr>
</tbody>
</table>

**1st parameter**

<table>
<thead>
<tr>
<th>Inst / Para</th>
<th>D/CX</th>
<th>WRX</th>
<th>RDX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st parameter</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>APB2 APB1 APB0</td>
</tr>
</tbody>
</table>

**2nd parameter**

<table>
<thead>
<tr>
<th>Inst / Para</th>
<th>D/CX</th>
<th>WRX</th>
<th>RDX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>2nd parameter</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>DCB2 DCB1 DCB0</td>
</tr>
</tbody>
</table>

**Description**

- Set the amount of current in Operational amplifier in Idle mode/8 colors.
- Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

<table>
<thead>
<tr>
<th>AP[2:0]</th>
<th>Amount of Current in Operational Amplifier</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>00h Operation of the operational amplifier stops</td>
</tr>
<tr>
<td>001</td>
<td>01h Small</td>
</tr>
<tr>
<td>010</td>
<td>02h Medium Low</td>
</tr>
<tr>
<td>011</td>
<td>03h Medium</td>
</tr>
<tr>
<td>100</td>
<td>04h Medium High</td>
</tr>
<tr>
<td>101</td>
<td>05h Large</td>
</tr>
<tr>
<td>110</td>
<td>06h Reserved</td>
</tr>
<tr>
<td>111</td>
<td>07h Reserved</td>
</tr>
</tbody>
</table>

- Set the Booster circuit Step-up cycle in Idle mode/8 colors.

<table>
<thead>
<tr>
<th>DC[2:0]</th>
<th>Step-up cycle in Booster circuit 1</th>
<th>Step-up cycle in Booster circuit 2,4</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>00h BCLK / 1</td>
<td>BCLK / 1</td>
</tr>
<tr>
<td>001</td>
<td>01h BCLK / 1</td>
<td>BCLK / 2</td>
</tr>
<tr>
<td>010</td>
<td>02h BCLK / 1</td>
<td>BCLK / 4</td>
</tr>
<tr>
<td>011</td>
<td>03h BCLK / 2</td>
<td>BCLK / 2</td>
</tr>
<tr>
<td>100</td>
<td>04h BCLK / 2</td>
<td>BCLK / 4</td>
</tr>
<tr>
<td>101</td>
<td>05h BCLK / 4</td>
<td>BCLK / 4</td>
</tr>
<tr>
<td>110</td>
<td>06h BCLK / 4</td>
<td>BCLK / 8</td>
</tr>
<tr>
<td>111</td>
<td>07h BCLK / 4</td>
<td>BCLK / 16</td>
</tr>
</tbody>
</table>

**Note:** BCLK is Clock frequency for Booster circuit

**Restriction**

- If this register not using the register need be reserved.

<table>
<thead>
<tr>
<th>Status</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal Mode On, Idle Mode Off, Sleep Out</td>
<td>Yes</td>
</tr>
<tr>
<td>Normal Mode On, Idle Mode On, Sleep Out</td>
<td>Yes</td>
</tr>
<tr>
<td>Partial Mode On, Idle Mode Off, Sleep Out</td>
<td>Yes</td>
</tr>
<tr>
<td>Partial Mode On, Idle Mode On, Sleep Out</td>
<td>Yes</td>
</tr>
<tr>
<td>Sleep In</td>
<td>Yes</td>
</tr>
</tbody>
</table>

**Default**

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>02h/07h</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>02h/07h</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>02h/07h</td>
</tr>
</tbody>
</table>
## 10.2.10 PWCTR5 (C4h): Power Control 5 (in Partial mode/ full-colors)

<table>
<thead>
<tr>
<th>C4H</th>
<th>PWCTR5 (Power Control 5)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inst / Para</td>
<td>D/CX</td>
</tr>
<tr>
<td>PWCTR5</td>
<td>0</td>
</tr>
<tr>
<td>1st parameter</td>
<td>1</td>
</tr>
<tr>
<td>2nd parameter</td>
<td>1</td>
</tr>
</tbody>
</table>

### Description

- Set the amount of current in Operational amplifier in Partial mode/ full-colors.
- Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.

<table>
<thead>
<tr>
<th>AP[2:0]</th>
<th>Amount of Current in Operational Amplifier</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>00h Operation of the operational amplifier stops</td>
</tr>
<tr>
<td>001</td>
<td>01h Small</td>
</tr>
<tr>
<td>010</td>
<td>02h Medium Low</td>
</tr>
<tr>
<td>011</td>
<td>03h Medium</td>
</tr>
<tr>
<td>100</td>
<td>04h Medium High</td>
</tr>
<tr>
<td>101</td>
<td>05h Large</td>
</tr>
<tr>
<td>110</td>
<td>06h Reserved</td>
</tr>
<tr>
<td>111</td>
<td>07h Reserved</td>
</tr>
</tbody>
</table>

- Set the Booster circuit Step-up cycle in Partial mode/ full-colors.

<table>
<thead>
<tr>
<th>DC[2:0]</th>
<th>Step-up cycle in Booster circuit 1</th>
<th>Step-up cycle in Booster circuit 2.4</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>00h BCLK / 1</td>
<td>BCLK / 1</td>
</tr>
<tr>
<td>001</td>
<td>01h BCLK / 1</td>
<td>BCLK / 2</td>
</tr>
<tr>
<td>010</td>
<td>02h BCLK / 1</td>
<td>BCLK / 4</td>
</tr>
<tr>
<td>011</td>
<td>03h BCLK / 2</td>
<td>BCLK / 2</td>
</tr>
<tr>
<td>100</td>
<td>04h BCLK / 2</td>
<td>BCLK / 4</td>
</tr>
<tr>
<td>101</td>
<td>05h BCLK / 4</td>
<td>BCLK / 4</td>
</tr>
<tr>
<td>110</td>
<td>06h BCLK / 4</td>
<td>BCLK / 8</td>
</tr>
<tr>
<td>111</td>
<td>07h BCLK / 4</td>
<td>BCLK / 16</td>
</tr>
</tbody>
</table>

Note: BCLK is Clock frequency for Booster circuit

### Restriction

- If this register not using the register need be reserved.

### Register Availability

<table>
<thead>
<tr>
<th>Status</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal Mode On, Idle Mode Off, Sleep Out</td>
<td>Yes</td>
</tr>
<tr>
<td>Normal Mode On, Idle Mode On, Sleep Out</td>
<td>Yes</td>
</tr>
<tr>
<td>Partial Mode On, Idle Mode Off, Sleep Out</td>
<td>Yes</td>
</tr>
<tr>
<td>Partial Mode On, Idle Mode On, Sleep Out</td>
<td>Yes</td>
</tr>
<tr>
<td>Sleep In</td>
<td>Yes</td>
</tr>
</tbody>
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### Default

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Flow Chart

PWCTR5

1st Parameter
2nd parameter

Legend

- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer
### 10.2.11 VMCTR1 (C5h): VCOM Control 1

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#### Set VCOMH Voltage

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<td>2.825</td>
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-Set VCOML Voltage

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Restriction
- If this register not using the register need be reserved.
- The VCOMAC = VCOMH – VCOML

Register Availability

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Default

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### 10.2.12 VMOFCTR (C7h): VCOM Offset Control

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<th>ROX</th>
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<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
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**Description**

- Set VCOM Voltage level for reducing the flicker issue

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<th>VMF[4:0]</th>
<th>VCOMH, VCOML Output Level</th>
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<tr>
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<td>00001</td>
<td>&quot;VMH&quot;-15d, &quot;VML&quot;-15d</td>
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<td>02h</td>
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<td>&quot;VMH&quot;-14d, &quot;VML&quot;-14d</td>
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<td>01110</td>
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<td>10001</td>
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</tr>
<tr>
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<td>10010</td>
<td>&quot;VMMH&quot;+2d, &quot;VML&quot;+2d</td>
</tr>
<tr>
<td></td>
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<td>1Eh</td>
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<td>&quot;VMMH&quot;+14d, &quot;VML&quot;+14d</td>
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<td>1Fh</td>
<td>11111</td>
<td>&quot;VMMH&quot;+15d, &quot;VML&quot;+15d</td>
</tr>
</tbody>
</table>

- 1d=25mV, 2d=50mV, 3d=75mV...
- 2.5V <= VMH ± nd <= 5.0V; -2.5V <= VML ± nd <= 0V (n=0~15,16)

**Restriction**

- If this register is not using the register need be reserved.

**Register Availability**

<table>
<thead>
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<th>Status</th>
<th>Availability</th>
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<td>Normal Mode On, Idle Mode Off, Sleep Out</td>
<td>Yes</td>
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<tr>
<td>Normal Mode On, Idle Mode On, Sleep Out</td>
<td>Yes</td>
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<tr>
<td>Partial Mode On, Idle Mode Off, Sleep Out</td>
<td>Yes</td>
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<td>Partial Mode On, Idle Mode On, Sleep Out</td>
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<td>Sleep In</td>
<td>Yes</td>
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**Default**

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<th>Default Value</th>
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<td>Power On Sequence</td>
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<td>S/W Reset</td>
<td>F0h</td>
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<tr>
<td>H/W Reset</td>
<td>F0h</td>
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</table>

**Flow Chart**

```
  VMOFCTR (C7h)  
   /\               
  VMF[4:0] Enable CMD D9h Para 20h  
   /\                         
  Modify VMF[4:0] register CMD C7h Para XXh  
   /\               
  VMF[4:0] disable CMD D9h Para 00h  
   /\               
  EEPROM Prog flow  
```

**Legend**

- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer
### 10.2.13 WRID2 (D1h): Write ID2 Value

<table>
<thead>
<tr>
<th>D1H</th>
<th>Inst / Para</th>
<th>WRX</th>
<th>RDX</th>
<th>D17</th>
<th>D16</th>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>WRID2</td>
<td>0</td>
<td>↑</td>
<td>1</td>
<td>-</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Parameter</td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td>ID26</td>
<td>ID25</td>
<td>ID24</td>
<td>ID23</td>
<td>ID22</td>
<td>ID21</td>
<td>ID20</td>
</tr>
</tbody>
</table>

#### Description

- Write 7-bit data of LCD module version to save it to EEPROM.
- The parameter ID2[6:0] is LCD Module version ID.

#### Flow Chart

```
NVCTR3 (D1h) ➔
ID2[6:0] Enable CMD D9h Para 10h ➔
Modify ID2[6:0] register CMD D1h Para XXh ➔
ID2[6:0] disable CMD D9h Para 00h ➔
EEPROM Prog flow
```

### Legend

- **Command**
- **Parameter**
- **Display**
- **Action**
- **Mode**
- **Sequential transfer**
10.2.14 WRID3 (D2h): Write ID3 Value

<table>
<thead>
<tr>
<th>D2H</th>
<th>Inst / Para</th>
<th>WRX</th>
<th>RDX</th>
<th>D17:8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>WRID3</td>
<td>0 ↑ 1</td>
<td>-</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>(D2h)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Parameter</td>
<td>1 ↑ 1</td>
<td>-</td>
<td>ID37</td>
<td>ID36</td>
<td>ID35</td>
<td>ID34</td>
<td>ID33</td>
<td>ID32</td>
<td>ID31</td>
<td>ID30</td>
<td>-</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Description**
- Write 8-bit data of project code module to save it to EEPROM.
- The parameter ID3[7:0] is product project ID.

**Flow Chart**

![Flow Chart](chart.png)
### 10.2.15 PWCTR6 (FCh): Power Control 5 (in Partial mode + Idle mode)

<table>
<thead>
<tr>
<th>FCH</th>
<th>PWCTR6 (Gamma control adjust)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inst / Para</td>
<td>D/CX WRX RDX D17-8 D7 D6 D5 D4 D3 D2 D1 D0 HEX</td>
</tr>
<tr>
<td>PWCTR6</td>
<td>0 ↑ 1 - 1 1 1 1 1 1 0 0 (FCh)</td>
</tr>
<tr>
<td>1st parameter</td>
<td>1 ↑ 1 - - Sapa2 Sapa1 Sapa0 - Sapb2 Sapb1 Sapb0</td>
</tr>
<tr>
<td>2nd parameter</td>
<td>1 ↑ 1 - - Sapc2 Sapc1 Sapc0 - DCD2 DCD1 DCD0</td>
</tr>
</tbody>
</table>

**Description**
- Set the amount of current in Operational amplifier in Partial mode + Idle mode.

#### Default

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>11h/15h</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>11h/15h</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>11h/15h</td>
</tr>
</tbody>
</table>

#### Flow Chart

![Flow Chart Diagram](image-url)
### 10.2.16 NVFCTR1 (D9h): EEPROM Control Status

<table>
<thead>
<tr>
<th>Inst / Para</th>
<th>D/CX</th>
<th>WRX</th>
<th>RDX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>NVFCTR1 parameter</td>
<td>0</td>
<td>↑</td>
<td>1</td>
<td>-</td>
<td>1</td>
<td>1</td>
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<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>(D9h)</td>
</tr>
</tbody>
</table>

**Description**

- EEPROM control status

<table>
<thead>
<tr>
<th>Bit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>VMF_EN</td>
<td>&quot;1&quot; = Command C7h enable ; &quot;0&quot; = Command C7h disable</td>
</tr>
<tr>
<td>ID2_EN</td>
<td>&quot;1&quot; = Command D1h enable ; &quot;0&quot; = Command D1h disable</td>
</tr>
</tbody>
</table>

**Default**

<table>
<thead>
<tr>
<th>Status</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On Sequence</td>
<td>00h</td>
</tr>
<tr>
<td>S/W Reset</td>
<td>00h</td>
</tr>
<tr>
<td>H/W Reset</td>
<td>00h</td>
</tr>
</tbody>
</table>

**Flow Chart**

1. NVCT (D9h)
2. 1st Parameter

**Legend**

- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer
### 10.2.17 NVFCTR2 (DEh): EEPROM Read Command

<table>
<thead>
<tr>
<th>DEH</th>
<th>NVFCTR1 (NV Memory Function Controller 2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inst / Para</td>
<td>D/CX</td>
</tr>
<tr>
<td>NVFCTR2</td>
<td>0</td>
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<tr>
<td>parameter</td>
<td>1</td>
</tr>
</tbody>
</table>

**Description**
EEPROM Read Command

**NOTE:** "-" Don't care

---

**Flow Chart**

![Flow Chart Diagram]

Legend:
- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer

1st Parameter : A5h

---
10.2.18 NVFCTR3 (DFh): EEPROM Write Command

<table>
<thead>
<tr>
<th>DFH</th>
<th>NVFCTR1 (NV Memory Function Controller 3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inst / Para</td>
<td>D/CX</td>
</tr>
<tr>
<td>NVFCTR1</td>
<td>0</td>
</tr>
<tr>
<td>1st parameter</td>
<td>1</td>
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<tr>
<td>2nd parameter</td>
<td>1</td>
</tr>
<tr>
<td>3rd parameter</td>
<td>1</td>
</tr>
</tbody>
</table>

Description

- EEPROM Write Command
- EE_IB[7:0] : Select Command. ; ADDR: C7h, D1h, D2h
- EE_CMD[7:0] : Select to Program/Erase ; Program command : 3Ah ; Erase command : C5h

NOTE: "-" Don't care

Flow Chart

Modify CMD register (C7h,D1h,D2h)

Enable EEPROM : EXTC="1"
CMD F1h, 84h
External VGH = 19V ON

Erase CMD DFh
1st Para (C7h,D1h,D2h) / 2nd Para 3Ah
3rd Para A5h

Program CMD DFh
1st Para (C7h,D1h,D2h) / 2nd Para 3Ah
3rd Para A5h

Wait 20ms

Disable EEPROM : EXTC="0"
CMD F1h, 04h
External VGH = 19V OFF

Wait 20ms

Legend

Command
Parameter
Display
Action
Mode
Sequencia transfer
## 10.2.19 GMCTRP1 (E0h): Gamma (+ polarity) Correction Characteristics Setting

<table>
<thead>
<tr>
<th>E0H</th>
<th>GMCTRP0 (Gamma + polarity Correction Characteristics Setting)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inst / Para</td>
<td>D/CX</td>
</tr>
<tr>
<td>GMCTRP1</td>
<td>0</td>
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<tr>
<td>1st parameter</td>
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<td>2nd parameter</td>
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<td>3rd parameter</td>
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<td>4th parameter</td>
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<td>11th parameter</td>
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<td>13th parameter</td>
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<td>14th parameter</td>
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<tr>
<td>15th parameter</td>
<td>1</td>
</tr>
<tr>
<td>16th parameter</td>
<td>1</td>
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</tbody>
</table>

### Description

#### Register Group
- **High level adjustment**: VRF0P[5:0]
  - VRF0P[5:0]: The voltage of V0 grayscale is selected by the 64 to 1 selector
  - Variable resistor VRHP
- **Mid level adjustment**: SELV0P[5:0]
  - SELV0P[5:0]: The voltage of V1 grayscale is selected by the 64 to 1 selector
  - PK1P[5:0]: The voltage of V3 grayscale is selected by the 64 to 1 selector
  - PK2P[5:0]: The voltage of V6 grayscale is selected by the 64 to 1 selector
  - PK3P[5:0]: The voltage of V11 grayscale is selected by the 64 to 1 selector
  - PK4P[5:0]: The voltage of V19 grayscale is selected by the 64 to 1 selector
  - PK5P[5:0]: The voltage of V27 grayscale is selected by the 64 to 1 selector
  - PK6P[5:0]: The voltage of V36 grayscale is selected by the 64 to 1 selector
  - PK7P[5:0]: The voltage of V44 grayscale is selected by the 64 to 1 selector
  - PK8P[5:0]: The voltage of V52 grayscale is selected by the 64 to 1 selector
  - PK9P[5:0]: The voltage of V60 grayscale is selected by the 64 to 1 selector
  - SELV62P[5:0]: The voltage of V62 grayscale is selected by the 64 to 1 selector
  - SELV63P[5:0]: The voltage of V63 grayscale is selected by the 64 to 1 selector
- **Low level adjustment**: VOS0P[5:0]
  - VOS0P[5:0]: Variable resistor VRLP
### 10.2.20 GMCTRN1 (E1h): Gamma '-' polarity Correction Characteristics Setting

<table>
<thead>
<tr>
<th>Inst / Para</th>
<th>GMCTRP0 (Gamma '-' polarity Correction Characteristics Setting)</th>
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<td>Inst / Para</td>
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</table>
### 10.2.21 EXTCTRL (F0h): Extension Command Control

<table>
<thead>
<tr>
<th>F0H</th>
<th>Inst / Para</th>
<th>D/CX</th>
<th>WRX</th>
<th>RDX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>HEX</th>
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</thead>
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<tr>
<td></td>
<td>EXTCTRL</td>
<td>0</td>
<td>↑</td>
<td>1</td>
<td>-</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>(F0h)</td>
</tr>
<tr>
<td>parameter</td>
<td>1 ↑ 1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>01h</td>
<td></td>
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</table>

**Description**

When EXTC PIN = "L", this command will enable extension command.

**NOTE:** "-" Don't care

**Flow Chart**

- EXTCTRL
  - 1st Parameter: 0th
### 10.2.22 VCOM4L (FFh): Vcom 4 Level Control

<table>
<thead>
<tr>
<th>Inst / Para</th>
<th>VCOM4L</th>
<th>FFH</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter3</td>
<td>1 ↑ 1 - 0 0 0 1 1 0 1 0 (1Ah)</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>FFH</th>
<th>VCOM4L (Vcom 4 level control)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inst / Para</td>
<td>D/CX</td>
</tr>
<tr>
<td>Parameter3</td>
<td>1 ↑ 1 - 0 0 0 1 1 0 1 0 (1Ah)</td>
</tr>
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</table>

<table>
<thead>
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<td>1111</td>
<td>15 clock</td>
<td>1111</td>
<td>15 clock</td>
</tr>
</tbody>
</table>

**Description**

- **TC1[3:0]** Delay time
- **TC2[3:0]** Delay time
- **TC3[3:0]** Delay time

**NOTE:** "-" Don't care
11 Power structure
11.1 Driver IC Operating Voltage Specification

![Diagram of power structure](image)

Fig 11.1.1 Power Booster Level
11.2 Power Booster Circuit
## 11.2.1 EXTERNAL COMPONENTS CONNECTION

<table>
<thead>
<tr>
<th>Pad Name</th>
<th>Connection</th>
<th>Rated (Min) Voltage</th>
<th>Typical capacitance value</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDI</td>
<td>VDDI (Logic Power)</td>
<td>6.3V</td>
<td>1.0 uF</td>
</tr>
<tr>
<td>VDD</td>
<td>VDD (Analog Power)</td>
<td>6.3V</td>
<td>1.0 uF</td>
</tr>
<tr>
<td>VCC</td>
<td>Connect to Capacitor: VCC -------</td>
<td></td>
<td>-------- GND</td>
</tr>
<tr>
<td>C41P, C41N</td>
<td>Connect to Capacitor: C41P -------</td>
<td></td>
<td>--- -----C41N</td>
</tr>
<tr>
<td>C22P, C22N</td>
<td>Connect to Capacitor: C22P -------</td>
<td></td>
<td>---- ----C22N</td>
</tr>
<tr>
<td>C23P, C23N</td>
<td>Connect to Capacitor: C23P -------</td>
<td></td>
<td>------ C23N</td>
</tr>
<tr>
<td>C11P, C11N</td>
<td>Connect to Capacitor: C11P -------</td>
<td></td>
<td>-- C11N</td>
</tr>
<tr>
<td>AVDD</td>
<td>Connect to Capacitor: AVDD -------</td>
<td></td>
<td>-------- GND</td>
</tr>
<tr>
<td>VGH</td>
<td>Connect to Capacitor: VGH -------</td>
<td></td>
<td>-------- GND</td>
</tr>
<tr>
<td>VGL</td>
<td>Connect to Capacitor: VGL -------</td>
<td></td>
<td>-------- GND</td>
</tr>
<tr>
<td>VCL</td>
<td>Connect to Capacitor: VCL -------</td>
<td></td>
<td>-------- GND</td>
</tr>
<tr>
<td>VCOMH</td>
<td>Connect to Capacitor: VCOMH-------</td>
<td></td>
<td>-------- GND</td>
</tr>
<tr>
<td>VCOML</td>
<td>Connect to Capacitor: VCOML-------</td>
<td></td>
<td>-------- GND</td>
</tr>
</tbody>
</table>

Note: For the typical specification of capacitor, the surge voltage is 125% of rated voltage. The capacitor of rated voltage of 16V can be only used for the case of VGH < 12.8V and VGL > -12.8V to prevent from stability issue. For normal usage, please use the capacitor of 25V rating.
12 Gamma structure
12.1 TRUCTURE OF GRAYSCALE AMPLIFIER
The structure of grayscale amplifier is shown as below. 16 voltage levels (VIN0-VIN15) between GVDD and VGS are determined by the high/ mid/ low level adjustment registers. Each mid-adjustment level is split into 64 levels again by the internal ladder resistor network. As a result, grayscale amplifier generates 64 voltage levels ranging from V0 to V63 and outputs one of 64 levels.
### 12.2 Gamma Voltage Formula (Positive/ Negative Polarity)

<table>
<thead>
<tr>
<th>Gray Level</th>
<th>Voltage Formula (Positive)</th>
<th>Voltage Formula (Negative)</th>
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</thead>
<tbody>
<tr>
<td>0</td>
<td>VINP0</td>
<td>VINN0</td>
</tr>
<tr>
<td>1</td>
<td>VINP1</td>
<td>VINN1</td>
</tr>
<tr>
<td>2</td>
<td>VINP2</td>
<td>VINN2</td>
</tr>
<tr>
<td>3</td>
<td>VINP3</td>
<td>VINN3</td>
</tr>
<tr>
<td>4</td>
<td>V3-(V3-V6)*$^{(11/30)}$</td>
<td>V3-(V3-V6)*$^{(11/30)}$</td>
</tr>
<tr>
<td>5</td>
<td>V3-(V3-V6)*$^{(21/30)}$</td>
<td>V3-(V3-V6)*$^{(21/30)}$</td>
</tr>
<tr>
<td>6</td>
<td>VINP4</td>
<td>VINN4</td>
</tr>
<tr>
<td>7</td>
<td>V6-(V6-V11)*$^{(7/30)}$</td>
<td>V6-(V6-V11)*$^{(7/30)}$</td>
</tr>
<tr>
<td>8</td>
<td>V6-(V6-V11)*$^{(14/30)}$</td>
<td>V6-(V6-V11)*$^{(14/30)}$</td>
</tr>
<tr>
<td>9</td>
<td>V6-(V6-V11)*$^{(20/30)}$</td>
<td>V6-(V6-V11)*$^{(20/30)}$</td>
</tr>
<tr>
<td>10</td>
<td>V6-(V6-V11)*$^{(25/30)}$</td>
<td>V6-(V6-V11)*$^{(25/30)}$</td>
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<tr>
<td>11</td>
<td>VINP5</td>
<td>VINN5</td>
</tr>
<tr>
<td>12</td>
<td>V11-(V11-V19)*$^{(4/32)}$</td>
<td>V11-(V11-V19)*$^{(4/32)}$</td>
</tr>
<tr>
<td>13</td>
<td>V11-(V11-V19)*$^{(8/32)}$</td>
<td>V11-(V11-V19)*$^{(8/32)}$</td>
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<tr>
<td>14</td>
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<td>V11-(V11-V19)*$^{(12/32)}$</td>
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<tr>
<td>15</td>
<td>V11-(V11-V19)*$^{(16/32)}$</td>
<td>V11-(V11-V19)*$^{(16/32)}$</td>
</tr>
<tr>
<td>16</td>
<td>V11-(V11-V19)*$^{(20/32)}$</td>
<td>V11-(V11-V19)*$^{(20/32)}$</td>
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<tr>
<td>17</td>
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<td>V11-(V11-V19)*$^{(24/32)}$</td>
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<td>18</td>
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<td>V11-(V11-V19)*$^{(28/32)}$</td>
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<td>19</td>
<td>VINP6</td>
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<tr>
<td>21</td>
<td>V19-(V19-V27)*$^{(8/32)}$</td>
<td>V19-(V19-V27)*$^{(8/32)}$</td>
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<td>22</td>
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<td>V19-(V19-V27)*$^{(12/32)}$</td>
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<td>23</td>
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<td>V19-(V19-V27)*$^{(1632)}$</td>
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<td>24</td>
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<td>25</td>
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<td>V19-(V19-V27)*$^{(24/32)}$</td>
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<td>26</td>
<td>V19-(V19-V27)*$^{(28/32)}$</td>
<td>V19-(V19-V27)*$^{(28/32)}$</td>
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<td>27</td>
<td>VINP7</td>
<td>VINN7</td>
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<tr>
<td>28</td>
<td>V27-(V27-V36)*$^{(4/36)}$</td>
<td>V27-(V27-V36)*$^{(4/36)}$</td>
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<td>29</td>
<td>V27-(V27-V36)*$^{(8/36)}$</td>
<td>V27-(V27-V36)*$^{(8/36)}$</td>
</tr>
<tr>
<td>30</td>
<td>V27-(V27-V36)*$^{(12/36)}$</td>
<td>V27-(V27-V36)*$^{(12/36)}$</td>
</tr>
<tr>
<td>31</td>
<td>V27-(V27-V36)*$^{(16/36)}$</td>
<td>V27-(V27-V36)*$^{(16/36)}$</td>
</tr>
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<td>32</td>
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<td>V27-(V27-V36)*$^{(20/36)}$</td>
</tr>
<tr>
<td>33</td>
<td>V27-(V27-V36)*$^{(24/36)}$</td>
<td>V27-(V27-V36)*$^{(24/36)}$</td>
</tr>
<tr>
<td>34</td>
<td>V27-(V27-V36)*$^{(28/36)}$</td>
<td>V27-(V27-V36)*$^{(28/36)}$</td>
</tr>
<tr>
<td>35</td>
<td>V27-(V27-V36)*$^{(32/36)}$</td>
<td>V27-(V27-V36)*$^{(32/36)}$</td>
</tr>
<tr>
<td>36</td>
<td>VINP8</td>
<td>VINN8</td>
</tr>
<tr>
<td>37</td>
<td>V36-(V36-V44)*$^{(4/32)}$</td>
<td>V36-(V36-V44)*$^{(4/32)}$</td>
</tr>
<tr>
<td>38</td>
<td>V36-(V36-V44)*$^{(8/32)}$</td>
<td>V36-(V36-V44)*$^{(8/32)}$</td>
</tr>
<tr>
<td>39</td>
<td>V36-(V36-V44)*$^{(12/32)}$</td>
<td>V36-(V36-V44)*$^{(12/32)}$</td>
</tr>
<tr>
<td></td>
<td>V36-(V36-V44)*(16/32)</td>
<td>V36-(V36-V44)*(16/32)</td>
</tr>
<tr>
<td>---</td>
<td>-----------------------</td>
<td>-----------------------</td>
</tr>
<tr>
<td>41</td>
<td>V36-(V36-V44)*(20/32)</td>
<td>V36-(V36-V44)*(20/32)</td>
</tr>
<tr>
<td>42</td>
<td>V36-(V36-V44)*(24/32)</td>
<td>V36-(V36-V44)*(24/32)</td>
</tr>
<tr>
<td>43</td>
<td>V36-(V36-V44)*(28/32)</td>
<td>V36-(V36-V44)*(28/32)</td>
</tr>
<tr>
<td>44</td>
<td>VINP9</td>
<td>VINN9</td>
</tr>
<tr>
<td>45</td>
<td>V44-(V44-V52)*(4/32)</td>
<td>V44-(V44-V52)*(4/32)</td>
</tr>
<tr>
<td>46</td>
<td>V44-(V44-V52)*(8/32)</td>
<td>V44-(V44-V52)*(8/32)</td>
</tr>
<tr>
<td>47</td>
<td>V44-(V44-V52)*(12/32)</td>
<td>V44-(V44-V52)*(12/32)</td>
</tr>
<tr>
<td>48</td>
<td>V44-(V44-V52)*(16/32)</td>
<td>V44-(V44-V52)*(16/32)</td>
</tr>
<tr>
<td>49</td>
<td>V44-(V44-V52)*(20/32)</td>
<td>V44-(V44-V52)*(20/32)</td>
</tr>
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<td>50</td>
<td>V44-(V44-V52)*(24/32)</td>
<td>V44-(V44-V52)*(24/32)</td>
</tr>
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<td>51</td>
<td>V44-(V44-V52)*(28/32)</td>
<td>V44-(V44-V52)*(28/32)</td>
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<td>52</td>
<td>VINP10</td>
<td>VINN10</td>
</tr>
<tr>
<td>53</td>
<td>V52-(V52-V57)*(5/30)</td>
<td>V52-(V52-V57)*(5/30)</td>
</tr>
<tr>
<td>54</td>
<td>V52-(V52-V57)*(11/30)</td>
<td>V52-(V52-V57)*(11/30)</td>
</tr>
<tr>
<td>55</td>
<td>V52-(V52-V57)*(17/30)</td>
<td>V52-(V52-V57)*(17/30)</td>
</tr>
<tr>
<td>56</td>
<td>V52-(V52-V57)*(23/30)</td>
<td>V52-(V52-V57)*(23/30)</td>
</tr>
<tr>
<td>57</td>
<td>VINP11</td>
<td>VINN11</td>
</tr>
<tr>
<td>58</td>
<td>V57-(V57-V60)*(8/30)</td>
<td>V57-(V57-V60)*(8/30)</td>
</tr>
<tr>
<td>59</td>
<td>V57-(V57-V60)*(18/30)</td>
<td>V57-(V57-V60)*(18/30)</td>
</tr>
<tr>
<td>60</td>
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<td>VINN12</td>
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<td>61</td>
<td>VINP13</td>
<td>VINN13</td>
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<tr>
<td>62</td>
<td>VINP14</td>
<td>VINN14</td>
</tr>
<tr>
<td>63</td>
<td>VINP15</td>
<td>VINN15</td>
</tr>
</tbody>
</table>
13 Example Connection with Panel direction and Different Resolution

13.1 Application of connection with panel direction

Case 1: (This is default case)
- 1st Pixel is at Left Top of the panel
- RGB filter order = RGB

- Direction default setting (H/W)
  SMX = ‘0’
  SMY = ‘0’
  SRGB = ‘0’
  S1 = Filter R
  S2 = Filter G
  S3 = Filter B
- Display direction control (S/W)
  - X-Mirror control by MX
  - Y-Mirror control by MY
  - XY-Exchange control by MV

Case 2:
- 1st Pixel is at Left Top of the panel
- RGB filter order = BGR

- Direction default setting (H/W)
  SMX = ‘0’
  SMY = ‘0’
  SRGB = ‘1’
  S1 = Filter B
  S2 = Filter G
  S3 = Filter R
- Display direction control (S/W)
  - X-Mirror control by MX
  - Y-Mirror control by MY
  - XY-Exchange control by MV
Case 3:
- 1st Pixel is at Right Bottom of the panel
- RGB filter order = RGB

- Direction default setting (H/W)
  SMX = '1'
  SMY = '1'
  SRGB = '0'
  S1 = Filter R
  S2 = Filter G
  S3 = Filter B
- Display direction control (S/W)
- X-Mirror control by MX
- Y-Mirror control by MY
- XY-Exchange control by MV

Case 4:
- 1st Pixel is at Right Bottom of the panel
- RGB filter order = BGR

- Direction default setting (H/W)
  SMX = '1'
  SMY = '1'
  SRGB = '1'
  S1 = Filter B
  S2 = Filter G
  S3 = Filter R
- Display direction control (S/W)
- X-Mirror control by MX
- Y-Mirror control by MY
- XY-Exchange control by MV
13.2 Application of connection with Different resolution

Case 1 of Resolution (128RGB x 160) (GM[2:0] = “011”)
RAM size = 128 x 160 x 18-bit (Used)
Display size = 128RGB x 160

1). Example for SMX=SMY=’0’

- Display direction control (S/W)
- X-Mirror control by MX
- Y-Mirror control by MY
- XY-Exchange control by MV

2). Example for SMX=SMY=’1’

- Display direction control (S/W)
- X-Mirror control by MX
- Y-Mirror control by MY
- XY-Exchange control by MV

- Direction default setting (H/W)
  SMX = ‘1’
  SMY = ‘1’
  SRGB = ‘1’
Case 2 of Resolution (132RGB x 162) \(\text{GM}[2:0] = "000"\)
RAM size = 132 x 162 x 18-bit (Used)
Display size = 132RGB x 162

1). Example for SMX = SMY = '0'

- Display direction control (S/W)
- X-Mirror control by MX
- Y-Mirror control by MY
- XY-Exchange control by MV

2). Example for SMX = SMY = '1'

- Direction default setting (H/W)
  SMX = '1'
  SMY = '0'
  SRGB = '0'

GRAM size = 132 x 162 x 18-bits
13.3 MicroProcessor Interface applications
8080-Series MCU + SPI Interface (IM2='1')

13.3.1 8080-Series MCU Interface for 8-bit data bus (IM1, IM0='00')

```
Host

RESX
TE
D/CX (SCL)
WRX
RDX
D7 to D1
D0
“0”
“0”

Driver IC

RESX
TE
SCL
SDA
D/CX
WRX
RDX
D7 to D1
D0
D15 to D8
D17 to D16

Note:
IM2='0', SPI I/F
IM2='1', MCU I/F

Fig. 13.3.1 8080 Series MCU Interface for 8-bit data bus
```

13.3.2 8080-Series MCU Interface for 16-bit data bus (IM1, IM0='01')

```
Host

RESX
TE
D/CX (SCL)
WRX
RDX
D7 to D1
D0
“D15 to D8”
“0”
“01”
IM2

Driver IC

RESX
TE
SCL
SDA
D/CX
WRX
RDX
D7 to D1
D0
D15 to D8
D17 to D16

Note:
IM2='0', SPI I/F
IM2='1', MCU I/F

Fig. 13.3.2 8080 Series MCU Interface for 16-bit data bus
```
13.3.3 8080-Series MCU Interface for 9-bit data bus (IM1, IM0=“10”)

![Diagram 13.3.3 8080 Series MCU Interface for 9-bit data bus]

Note:
IM2=’0’, SPI I/F
IM2=’1’, MCU I/F

13.3.4 8080-Series MCU Interface for 18-bit data bus (IM1, IM0=“11”)

![Diagram 13.3.4 8080 Series MCU Interface for 18-bit data bus]

Note:
IM2=’0’, SPI I/F
IM2=’1’, MCU I/F
<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>2008/11/27</td>
<td>First issue.</td>
</tr>
<tr>
<td>1.1</td>
<td>2009/01/05</td>
<td>Modify address counter description (P58)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Modify DISPOFF(28h) and DISPON(29h) command description (P97~98)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Modify frame rate control command (B1<del>B3h) description (P122</del>124)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Modify ROM code default value (P122~140)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Modify external components table, AVDD capacitance value change and schottky diode remove. (P154~155)</td>
</tr>
<tr>
<td>1.2</td>
<td>2009/03/09</td>
<td>Modify VCC maximum absolute operating voltage (P18)</td>
</tr>
<tr>
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<td>Modify power consumption condition (P20)</td>
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<td></td>
<td></td>
<td>Modify VMCTR1(C5h) command restriction (P138)</td>
</tr>
<tr>
<td>1.3</td>
<td>2009/08/05</td>
<td>Modify the parameter of command 0xDF(P145)</td>
</tr>
<tr>
<td>1.4</td>
<td>2009/08/28</td>
<td>Add AVDD, VCI1 voltage.(P16,P128, P154)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Add IOSC value (P122, P123, P124)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Modify the setting values of VCOM table with HEX.</td>
</tr>
<tr>
<td>1.5</td>
<td>2009/09/01</td>
<td>Modify AVDD voltage.( P154)</td>
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<tr>
<td></td>
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<td>Modify the descriptions in command table with HEX.</td>
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<tr>
<td>1.6</td>
<td>2009/09/23</td>
<td>Modify EXTC description.(P14)</td>
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<td>Modify VC11 description to Hi-Z.(P16)</td>
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<tr>
<td>1.7</td>
<td>2009/12/04</td>
<td>Modify DISSET5 (B6h) command (P126)</td>
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<td>1.8</td>
<td>2009/12/24</td>
<td>Modify command 0xDF description (P146)</td>
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<tr>
<td>1.9</td>
<td>2010/01/20</td>
<td>Add Chip information drawing (P5)</td>
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<tr>
<td>2.0</td>
<td>2010/02/01</td>
<td>Modify bump height 12 um (TYP) (P5)</td>
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<tr>
<td>2.1</td>
<td>2010/5/5</td>
<td>Modify ID1 value (P82, P116)</td>
</tr>
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</table>