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ST8009

96 Output LCD Common/ Segment Driver IC

Notice: Sitronix Technology Corp. reserves the right to change the contents in this document without prior notice. This is not a final specification. Some parameters are subject to change.

1. DESCRIPTION

The ST8009 is a 96-output segment/common driver IC suitable for driving small/medium scale dot matrix LCD panels, and is used in PDA or electronic dictionary. The ST8009 is good as a segment driver, a common driver or a common/segment driver, and it can create low power consumption, high-resolution LCD. The ST8009 have eight modes can selected to set common and segment numbers by selecting register. The ST8009 also have analog DC/DC converter to use.

2. FEATURES

- Number of LCD drive outputs: 96
- Supply voltage for LCD drive (V_{OUT}): Max +16V
- Supply voltage for logic system (V_{DD}): +2.5 ~ +5.5V
- Low power consumption and low output impedance
- Display duty selectable by internal select register

DU_2,DU_1,DU_0	DUTY
0 0 0	---
0 0 1	1/16
0 1 0	1/32
0 1 1	1/48
1 0 0	1/64
1 0 1	1/80
1 1 0	1/96
1 1 1	1/96

- Abundant command functions

  LCD bias set, electronic volume, V_{SS} voltage regulation internal resistor ratio and booster frequency.

  All Functions have initial value, user can set by programmed.

- Low-power liquid crystal display power supply circuit equipped internally.

  Booster circuit (with Boost ratio of 2X/3X/4X/5X/6X)

  Regulator circuit

  Follower circuit

- Package: 124-pin COB.

(Segment mode)

- Shift clock frequency

  - 20 MHz (MAX.): V_{DD} = +5.0 ± 0.5 V
  - 15 MHz (MAX.): V_{DD} = +3.0 to + 4.5 V
  - 12 MHz (MAX.): V_{DD} = +2.5 to + 3.0 V

- Adopts a data bus system
- 4-bit parallel / serial input modes are selectable by programmable.
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 16、32、48、64、80、96 bits of input data
- Line latch circuits are reset when XDISPOFF active

(Common mode)

- Shift clock frequency: 4 MHz (MAX.)
- Built-in X-bit shift register
- Available in a single mode
- CS0 → CSX Single mode

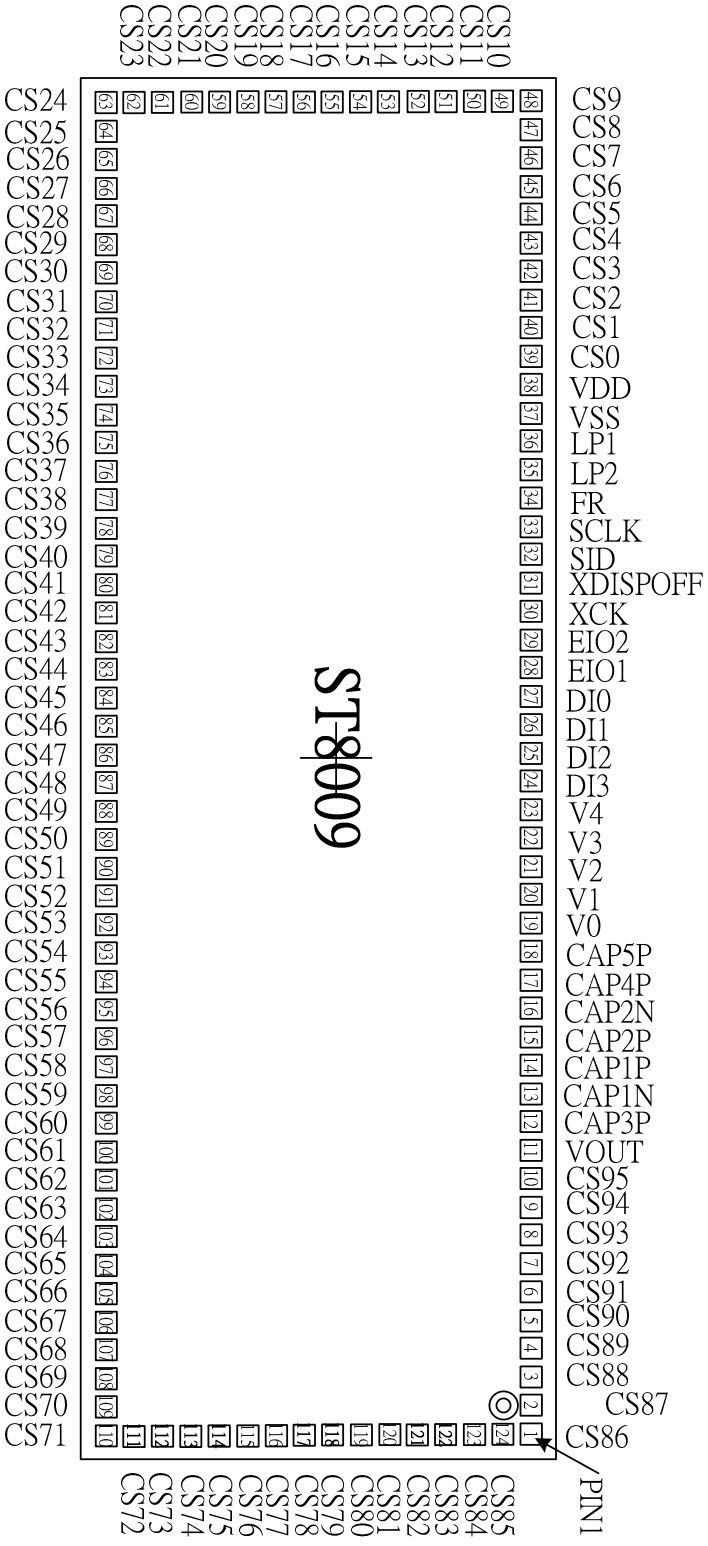
  CSX → CS0 Single mode

  PS:X=15、31、47、63、79、95

  The above 4 shift directions are register selectable
- Shift register circuits are reset when XDISPOFF active

3. PAD ARRANGEMENT

Chip size: 5070.0(um) x1790.0 (um)
Pad size：80 (um) x80 (um)
Pad pin pitch: 100 (um) ~ 140 (um)
Origin : chip center (0,0)
Chip Thickness：19 mil



Substrate Connect to V_{SS}.

4. PAD CONFIGURATION

Pad No.	Function	X	Y
1	CS[86]	2450	810
2	CS[87]	2310	810
3	CS[88]	2180	810
4	CS[89]	2060	810
5	CS[90]	1950	810
6	CS[91]	1850	810
7	CS[92]	1750	810
8	CS[93]	1650	810
9	CS[94]	1550	810
10	CS[95]	1450	810
11	V_{OUT}	1350	810
12	CAP3P	1250	810
13	CAP1N	1150	810
14	CAP1P	1050	810
15	CAP2P	950	810
16	CAP2N	850	810
17	CAP4P	750	810
18	CAP5P	650	810
19	V0	550	810
20	V1	450	810
21	V2	350	810
22	V3	250	810
23	V4	150	810
24	ED[3]	50	810
25	ED[2]	-50	810
26	ED[1]	-150	810
27	ED[0]	-250	810
28	EIO1	-350	810
29	EIO2	-450	810
30	XCK	-550	810
31	XDISPOFF	-650	810
32	SID	-750	810

Pad No.	Function	X	Y
33	SCLK	-850	810
34	FR	-950	810
35	LP2	-1050	810
36	LP1	-1150	810
37	V_{SS}	-1250	810
38	V_{DD}	-1350	810
39	CS[0]	-1450	810
40	CS[1]	-1550	810
41	CS[2]	-1650	810
42	CS[3]	-1750	810
43	CS[4]	-1850	810
44	CS[5]	-1950	810
45	CS[6]	-2060	810
46	CS[7]	-2180	810
47	CS[8]	-2310	810
48	CS[9]	-2450	810
49	CS[10]	-2450	680
50	CS[11]	-2450	560
51	CS[12]	-2450	450
52	CS[13]	-2450	350
53	CS[14]	-2450	250
54	CS[15]	-2450	150
55	CS[16]	-2450	50
56	CS[17]	-2450	-50
57	CS[18]	-2450	-150
58	CS[19]	-2450	-250
59	CS[20]	-2450	-350
60	CS[21]	-2450	-450
61	CS[22]	-2450	-560
62	CS[23]	-2450	-680
63	CS[24]	-2450	-810
64	CS[25]	-2310	-810

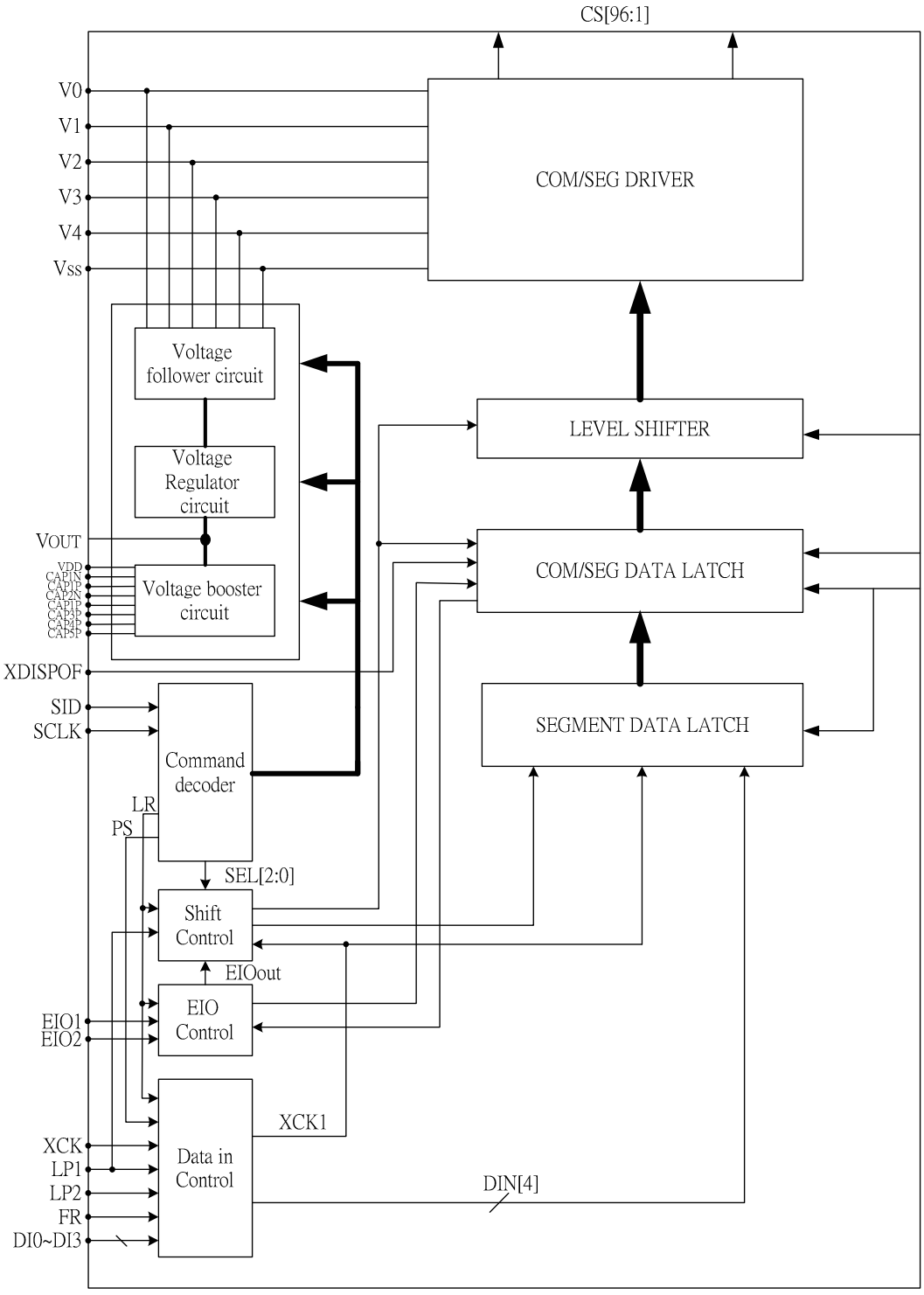
Pad No.	Function	X	Y
65	CS[26]	-2180	-810
66	CS[27]	-2060	-810
67	CS[28]	-1950	-810
68	CS[29]	-1850	-810
69	CS[30]	-1750	-810
70	CS[31]	-1650	-810
71	CS[32]	-1550	-810
72	CS[33]	-1450	-810
73	CS[34]	-1350	-810
74	CS[35]	-1250	-810
75	CS[36]	-1150	-810
76	CS[37]	-1050	-810
77	CS[38]	-950	-810
78	CS[39]	-850	-810
79	CS[40]	-750	-810
80	CS[41]	-650	-810
81	CS[42]	-550	-810
82	CS[43]	-450	-810
83	CS[44]	-350	-810
84	CS[45]	-250	-810
85	CS[46]	-150	-810
86	CS[47]	-50	-810
87	CS[48]	50	-810
88	CS[49]	150	-810
89	CS[50]	250	-810
90	CS[51]	350	-810
91	CS[52]	450	-810
92	CS[53]	550	-810
93	CS[54]	650	-810
94	CS[55]	750	-810
95	CS[56]	850	-810
96	CS[57]	950	-810
97	CS[58]	1050	-810

Pad No.	Function	X	Y
98	CS[59]	1150	-810
99	CS[60]	1250	-810
100	CS[61]	1350	-810
101	CS[62]	1450	-810
102	CS[63]	1550	-810
103	CS[64]	1650	-810
104	CS[65]	1750	-810
105	CS[66]	1850	-810
106	CS[67]	1950	-810
107	CS[68]	2060	-810
108	CS[69]	2180	-810
109	CS[70]	2310	-810
110	CS[71]	2450	-810
111	CS[72]	2450	-680
112	CS[73]	2450	-560
113	CS[74]	2450	-450
114	CS[75]	2450	-350
115	CS[76]	2450	-250
116	CS[77]	2450	-150
117	CS[78]	2450	-50
118	CS[79]	2450	50
119	CS[80]	2450	150
120	CS[81]	2450	250
121	CS[82]	2450	350
122	CS[83]	2450	450
123	CS[84]	2450	560
124	CS[85]	2450	680

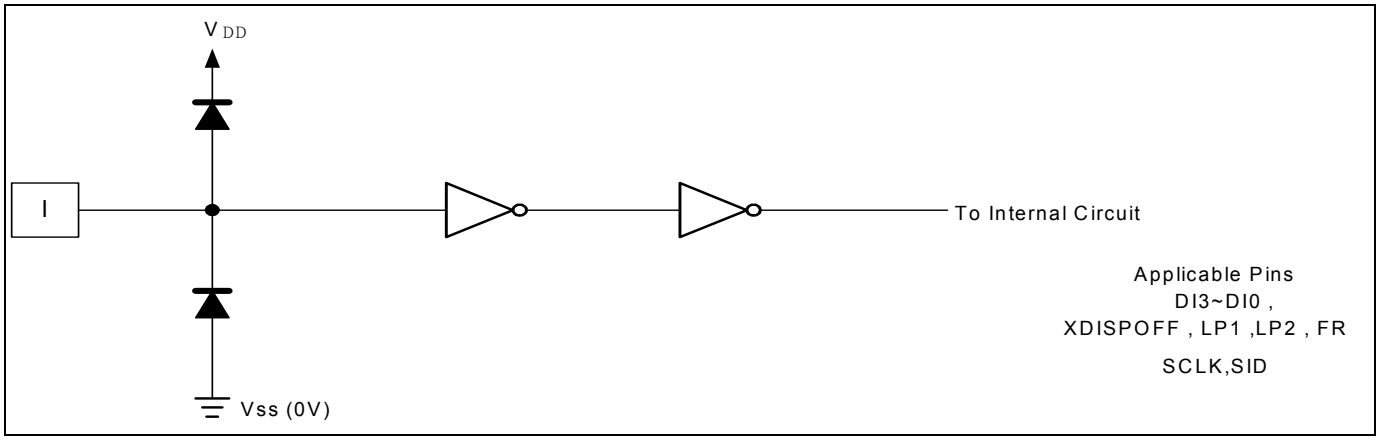
5. PIN DESCRIPTION

SYMBOL	I/O	DESCRIPTION	No of Num
CS0~CS95	O	LCD drive output	96
V0~V4	P	Power supply for LCD drive	5
V_{DD}	P	Power supply for logic system (+2.5 to +5.5 V)	1
EIO2, EIO1	I/O	Input/output for chip selection at segment mode and FLM input output function at com/seg mix mode or common mode	2
DI0~DI3	I	Display data input at segment mode	4
XCK	I	Clock input for taking display data at segment mode	1
XDISPOFF	I	Control input for output of ground level	1
LP1	I	Latch pulse input for display data at segment mode	1
LP2	I	Shift clock input for shift register at common mode	1
FR	I	AC-converting signal input for LCD drive waveform	1
V_{SS}	P	Ground (0 V)	1
CAP1-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.	1
CAP1+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.	1
CAP2-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.	1
CAP2+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.	1
CAP3+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.	1
CAP4+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.	1
CAP5+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.	
V_{OUT}	O	DC/DC voltage converter. Connect a capacitor between this terminal and V_{SS}.	1
SID	I	The command data. See Figure1	1
SCLK	I	The serial clock input. See Figure1	1

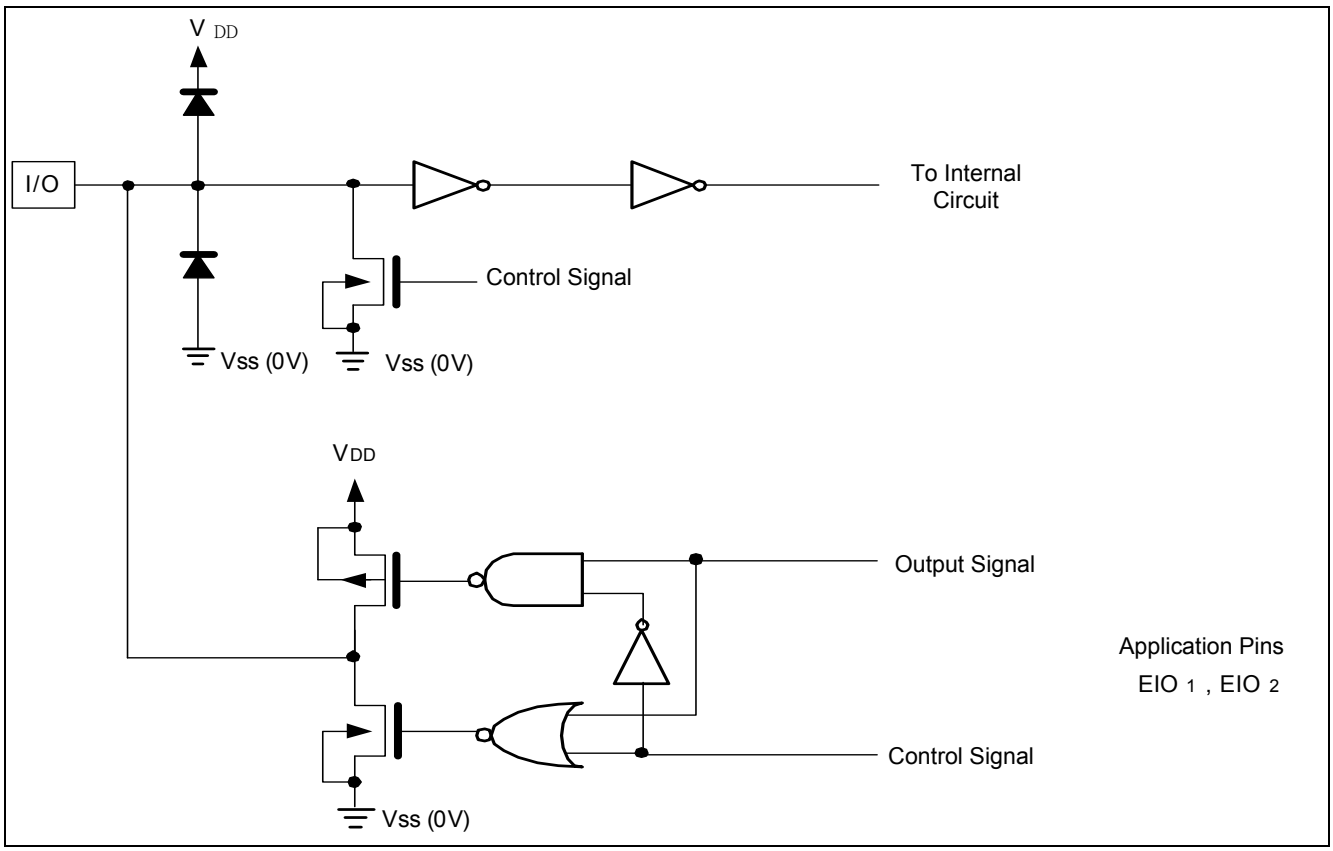
6. BLOCK DIAGRAM



7. INPUT/OUTPUT CIRCUITS



Input Circuit (1)



Input/Output Circuit

8. PIN FUNCTIONAL DESCRIPTION

8.1 Pin Functions

(Segment mode)

SYMBOL	FUNCTION
V_{DD}	Logic system power supply pin, connected to +2.5 to +5.5 V.
V_{SS}	Ground pin, connected to 0 V.
V0 , V1 V2 , V3 V4	When the internal power supply circuit turns on • The internal power supply circuit will produce the LCD bias voltage set(V0 ~ V4), and those voltages are setting by the “LCD Bias Set” register. When the internal power supply circuit turns off • Supply the bias voltages set by a resistor divider externally , and had better use follower circuit to hold those voltages. • Ensure that voltages are set such that V0 ≧V1 ≧V2 ≧V3 ≧V4 ≧V_{SS}
DI3~DI0	Input pins for display data • In 4-bit parallel input mode, connect data to the 4 pins, DI3-DI0. • In serial input mode, connect data to the DI0 pin, and DI3-DI1 must be connected to V_{SS} . • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
LP1	Latch pulse input pin for display data • Data is latched at the falling edge of the clock pulse.
XCK	Clock input for taking display data at segment mode
XDISPOFF	The switch for turn on or turn off the LCD display • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to V_{SS} level "L", the LCD drive output pins (CS0-CS95) are set to level V_{SS}. • When set to "L", the contents of the line latch are reset, but the display data are read in the data latch regardless of the condition of XDISPOFF. When the XDISPOFF function is canceled, the driver outputs non-select level (V2 or V3), then outputs the contents of the data latch at the next falling edge of the LP. At that time, if XDISPOFF removal time does not correspond to what is shown in AC characteristics, it cannot output the reading data correctly. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
FR	AC signal input pin for LCD drive waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.

EIO1, EIO2	Input/output pins for chip selection. • When L/R register is set '0' , EIO1 is set for output, and EIO2 is set for input(connect to V_{SS}). • When L/R register is set '1', EIO1 is set for input(connect to V_{SS}), and EIO2 is set for output. • During output, set to "H" while LP • XCK is "H" and after 96 bits of data have been read, set to "L" for one cycle (from falling edge to failing edge of XCK), after which it returns to "H". • During input, the chip is selected while EI is set to "L" after the LP signal is input. The chip is non-selected after 96 bits of data have been read.
CS0~CS95	LCD drive output pins • Corresponding directly to each bit of the data latch, one level (V0, V2 ,V3, V_{SS}) is selected and output. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
CAP1-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
CAP1+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
CAP2-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
CAP2+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
CAP3+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
CAP4+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
V_{OUT}	DC/DC voltage converter. Connect a capacitor between this terminal and V_{SS}.
SID	The serial command data. See Figure1
SCLK	The serial clock input. See Figure1

(Common mode)

SYMBOL	FUNCTION
V_{DD}	Logic system power supply pin, connected to +2.5 to +5.5 V.
V_{SS}	Ground pin, connected to 0 V.
V0, V1 V2, V3 V4	When the internal power supply circuit turns on • The internal power supply circuit will produce the LCD bias voltage set(V0 ~ V4), and those voltages are setting by the "LCD Bias Set" register. When the internal power supply circuit turns off • Supply the bias voltages set by a resistor divider externally , and had better use follower circuit to hold those voltages. • Ensure that voltages are set such that V0 ≧V1 ≧V2 ≧V3 ≧V4 ≧V_{SS}
DI3-DI0	Not used. Connect DI3-DI0 to V_{SS}, not floating.
LP2	Shift clock pulse input pin for bi-directional shift register • * Data is shifted at the falling edge of the clock pulse. • When use gray scale mode, then must use the pin. • When use monochrome mode, then the pin should be shorted to LP1.
XCK	Not used • Not let it floating , connect to V_{SS}

XDISPOFF	The switch for turn on or turn off the LCD display • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to V_{SS} level "L", the LCD drive output pins (CS0-CS95) are set to level V_{SS}. • When set to "L", the contents of the shift register are reset to not reading data. When the /DISPOFF function is canceled, the driver outputs non-select level (V1 or V4), and the shift data is read at the next falling edge of the LP. At that time, if /DISPOFF removal time does not correspond to what is shown in AC characteristics, the shift data is not read correctly. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
FR	AC signal input pin for LCD drive waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the shift register output signal and the FR signal. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
CS0 ~CS95	LCD drive output pins • Corresponding directly to each bit of the shift register, one level (V0 V1, V4, or V_{SS}) is selected and output. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
EIO1, EIO2	Shift data Input/output pins for shift register • EIO1 is output pin when L/R is at V_{SS} level “L”, EIO1 is input pin when L/R is at V_{DD} level “H” • When L/R register =’1’, EIO1 is used as input pin, it will be connect to FLM. • When L/R register =’0’, EIO1 is used as output pin, it won’t be connect to FLM. • EIO2 is input pin when L/R is at V_{SS} level “L”, EIO1 is output pin when L/R is at V_{DD} level “H” • When L/R register =’1’, EIO2 is used as output pin, it won’t be connect to FLM, • When L/R register =’0’, EIO2 is used as input pin, it will be connect to FLM • Refer to “RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS” in Functional Operations.
CAP1-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
CAP1+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
CAP2-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
CAP2+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
CAP3+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
CAP4+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
V_{OUT}	DC/DC voltage converter. Connect a capacitor between this terminal and V_{SS}.
SID	The serial command data. See Figure1
SCLK	The serial clock input. See Figure1

(common /segment mix mode)

SYMBOL	FUNCTION
V_{DD}	Logic system power supply pin, connected to +2.5 to +5.5 V.
V_{SS}	Ground pin, connected to 0 V.
V0 , V1 V2 , V3 V4	When the internal power supply circuit turns on : • The internal power supply circuit will produce the LCD bias voltage set(V0 ~ V4), and those voltages are setting by the “LCD Bias Set” register. When the internal power supply circuit turns off : • Supply the bias voltages set by a resistor divider externally , and had better use follower circuit to hold those voltages. • Ensure that voltages are set such that V0 ≧V1 ≧V2 ≧V3 ≧V4 ≧V_{SS}
DI3~DI0	Input pins for display data • In 4-bit parallel input mode, input data into the 4 pins, DI3~DI0. • In serial input mode, connect data to the DI0 pin, and DI3-DI1 must be connected to V_{SS} . • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
XCK	Clock input pin for taking display data • Data is read at the falling edge of the clock pulse.
LP1	Latch pulse input pin for display data • Data is latched at the falling edge of the clock pulse.
LP2	Shift clock pulse input pin for bi-directional shift register • Data is shifted at the falling edge of the clock pulse. • When use gray scale mode, then must use the pin. • When use monochrome mode, then the pin should be shorted to LP1.
XDISPOFF	The switch for turn on or turn off the LCD display • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to V_{SS} level "L", the LCD drive output pins (CS0-CS95) are set to level V_{SS}. • When set to "L", the contents of the line latch are reset, but the display data are read in the data latch regardless of the condition of XDISPOFF. When the XDISPOFF function is canceled, the driver outputs non-select level (V2 or V3), then outputs the contents of the data latch at the next falling edge of the LP. At that time, if XDISPOFF removal time does not correspond to what is shown in AC characteristics, it cannot output the reading data correctly. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
FR	AC signal input pin for LCD drive waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal, and it inputs a frame inversion signal normally. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.

EIO1, EIO2	Input/output pins for chip selection • When L/R register is '0', EIO1 is set output, and EIO2 is set for input. EIO1 : segment chip enable output, as default segment is enabled internally and be non-selected after 16,32,48,64 or 80 bits of data have been read. Depend on select mode. EIO2 :common shift data input, no sift data output • When L/R register is '1', EIO1 is set for input, and EIO2 is set for output. EIO1 :common shift data, no shift data output EIO2 : segment chip enable output, as default segment is enabled internally and be non-selected after 16,32,48,64 or 80 bits of data have been read. Depend on select mode. • During output, set to "H" while LP • XCK is "H" and after 96 bits of data have been read, set to "L" for one cycle (from falling edge to failing edge of XCK), after which it returns to "H". • During input, the chip is selected while EI is set to "L" after the LP signal is input. The chip is non-selected after 96 bits of data have been read.
CS0 ~CS95	LCD drive output pins • Corresponding directly to each bit of the data latch, one level (V0, V2, V3, V_{SS}) is selected and output. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
CAP1-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
CAP1+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
CAP2-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
CAP2+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
CAP3+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
CAP4+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
V_{OUT}	DC/DC voltage converter. Connect a capacitor between this terminal and V_{SS}.
XCS	This is the command mode select pin. When XCS="L" then write command to the LCD, when not used the command mode then must fixed to V_{DD} . See Figure1
SID	The command data. See Figure1
SCLK	The serial clock input. See Figure1

8.2 Functional Operations

8.2.1 TRUTH TABLE

(Segment Mode)

FR	LATCH DATA	/DISPOFF	LCD DRIVE OUTPUT VOLTAGE LEVEL (CS0-CS95)
L	L	H	V3
L	H	H	V_{SS}
H	L	H	V2
H	H	H	V0
X	X	L	V_{SS}

(Common Mode)

FR	LATCH DATA	/DISPOFF	LCD DRIVE OUTPUT VOLTAGE LEVEL (CS0-CS95)
L	L	H	V4
L	H	H	V0
H	L	H	V1
H	H	H	V_{SS}
X	X	L	V_{SS}

NOTES:

- L : V_{SS} (0 V), H : V_{DD} (+2.5 to +5.5 V), X : Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.

  There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver.

  Supply regular voltage that is assigned by specification for each power pin.

8.2.2 RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS

(Segment Mode)

(A) 4-bit Parallel Input Mode

L/R	EIO1	EIO2	DATA INPUT	NUMBER OF CLOCKS						
				24 CLOCK	23 CLOCK	22 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
L	Output	Input	DI0	CS0	CS4	CS8	…	CS84	CS88	CS92
			DI1	CS1	CS5	CS9	…	CS85	CS89	CS93
			DI2	CS2	CS6	CS10	…	CS86	CS90	CS94
			DI3	CS3	CS7	CS11	…	CS87	CS91	CS95
H	Input	Output	DI0	CS95	CS91	CS87	…	CS11	CS7	CS3
			DI1	CS94	CS90	CS86	…	CS10	CS6	CS2
			DI2	CS93	CS89	CS85	…	CS9	CS5	CS1
			DI3	CS92	CS88	CS84	…	CS8	CS4	CS0

(B) Serial Input Mode

L/R	EIO1	EIO2	DATA INPUT	NUMBER OF CLOCKS						
				120 CLOCK	119 CLOCK	118 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
L	Output	Input	DI0	CS0	CS1	CS2	…	CS93	CS94	CS95
			DI1	X	X	X	X	X	X	X
			DI2	X	X	X	X	X	X	X
			DI3	X	X	X	X	X	X	X
H	Input	Output	DI0	CS95	CS94	CS93	…	CS2	CS1	CS0
			DI1	X	X	X	X	X	X	X
			DI2	X	X	X	X	X	X	X
			DI3	X	X	X	X	X	X	X

(Common Mode)

L/R	DATA TRANSFER DIRECTION	EIO1	EIO2
L	CS95 → CS0	Output	Input
H	CS0 → CS95	Input	Output

MIX MODE(SEGMENT/ COMMON MODE)

When (DU2,DU1,DU0)=(0,1,0)➔ SELECT THE 32 COM / 64 SEGMENT MODE

THEN SEGMENT SIDE OF MIX MODE

(A) 4-bit Parallel Input Mode

L/R	EIO1	EIO2	DATA INPUT	NUMBER OF CLOCKS						
				16 CLOCK	15 CLOCK	14 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
L	Seg_end Output	Com_FLM Input	DI0	CS0	CS4	CS8	…	CS52	CS56	CS60
			DI1	CS1	CS5	CS9	…	CS53	CS57	CS61
			DI2	CS2	CS6	CS10	…	CS54	CS58	CS62
			DI3	CS3	CS7	CS11	…	CS55	CS59	CS63
H	Com_FLM Input	Seg_end Output	DI0	CS95	CS91	CS87	…	CS43	CS39	CS35
			DI1	CS94	CS90	CS86	…	CS42	CS38	CS34
			DI2	CS93	CS89	CS85	…	CS41	CS37	CS33
			DI3	CS92	CS88	CS84	…	CS40	CS36	CS32

(B) Serial Input Mode

L/R	EIO1	EIO2	DATA INPUT	NUMBER OF CLOCKS						
				64 CLOCK	63 CLOCK	62CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
L	Seg_end Output	Com_FLM Input	DI0	CS0	CS1	CS2	…	CS61	CS62	CS63
			DI1	X	X	X	X	X	X	X
			DI2	X	X	X	X	X	X	X
			DI3	X	X	X	X	X	X	X
H	Com_FLM Input	Seg_end Output	DI0	CS95	CS94	CS93	…	CS34	CS33	CS32
			DI1	X	X	X	X	X	X	X
			DI2	X	X	X	X	X	X	X
			DI3	X	X	X	X	X	X	X

COMMON SIDE OF MIX MODE

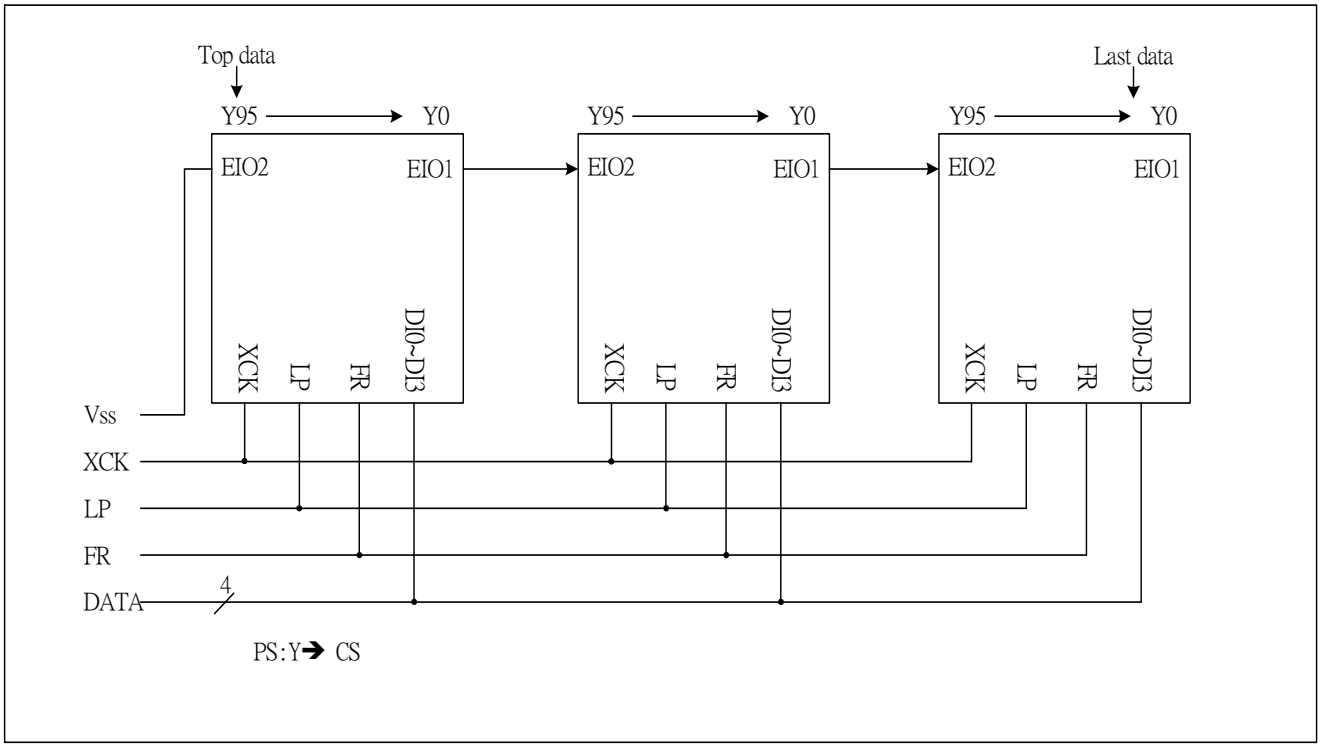
L/R	DATA TRANSFER DIRECTION	EIO1	EIO2
L	CS95 → CS62	Seg_end output	Input
H	CS0 → CS31	Input	Seg_end output

NOTES:

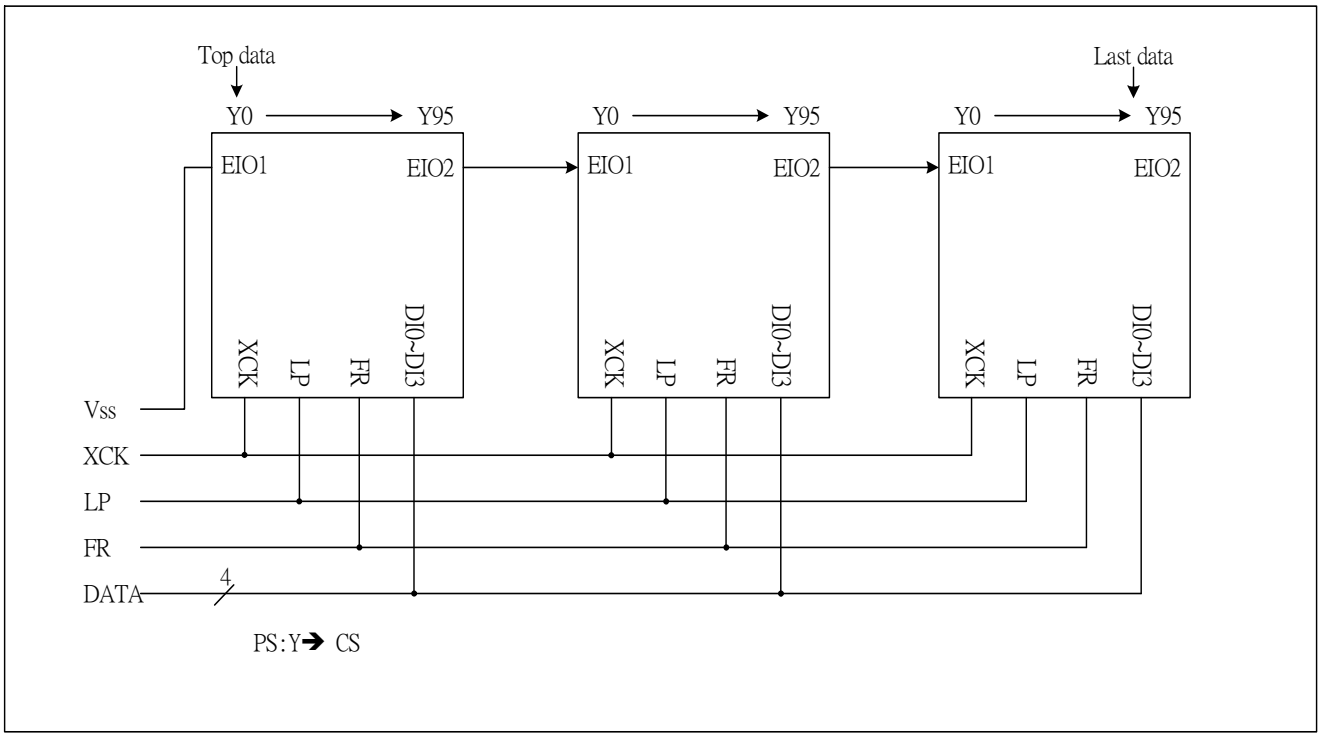
- L : V_{SS} (0 V), H : V_{DD} (+2.5 to +5.5 V), X : Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.

8.2.3 Connection examples of plural segment drivers in 4-bits interface(288 segment)

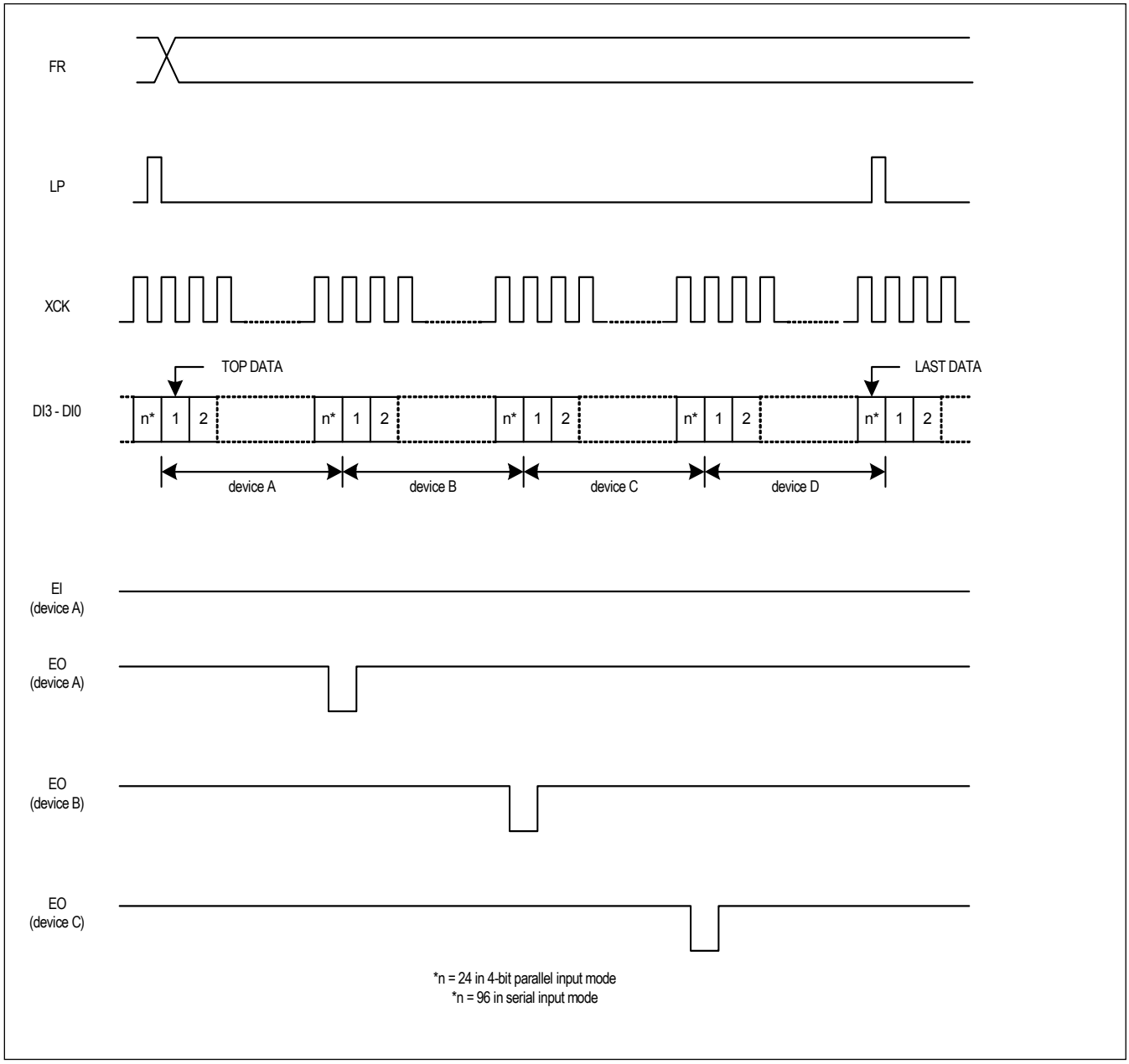
(a) When the L/R register set "L" level



(b) When the L/R register set "H" level

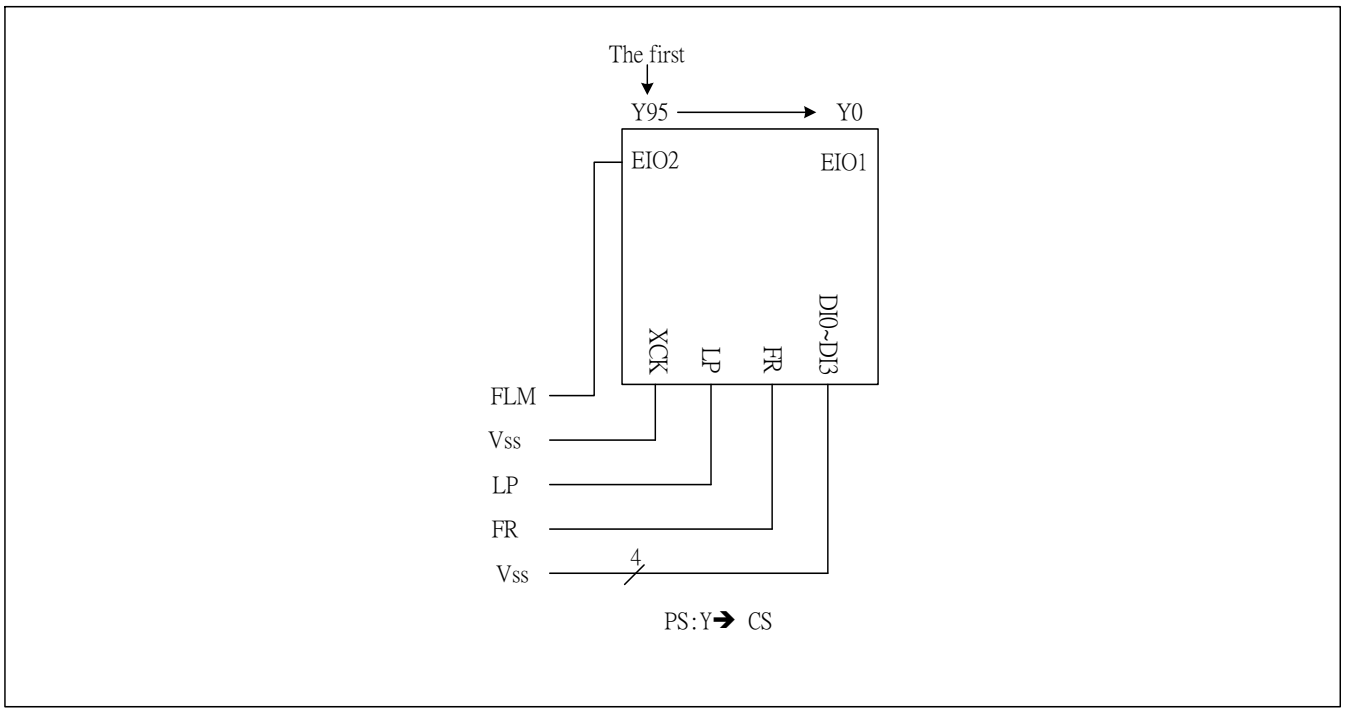


8.2.4 Timing chart of 4-device cascade connection of segment drivers

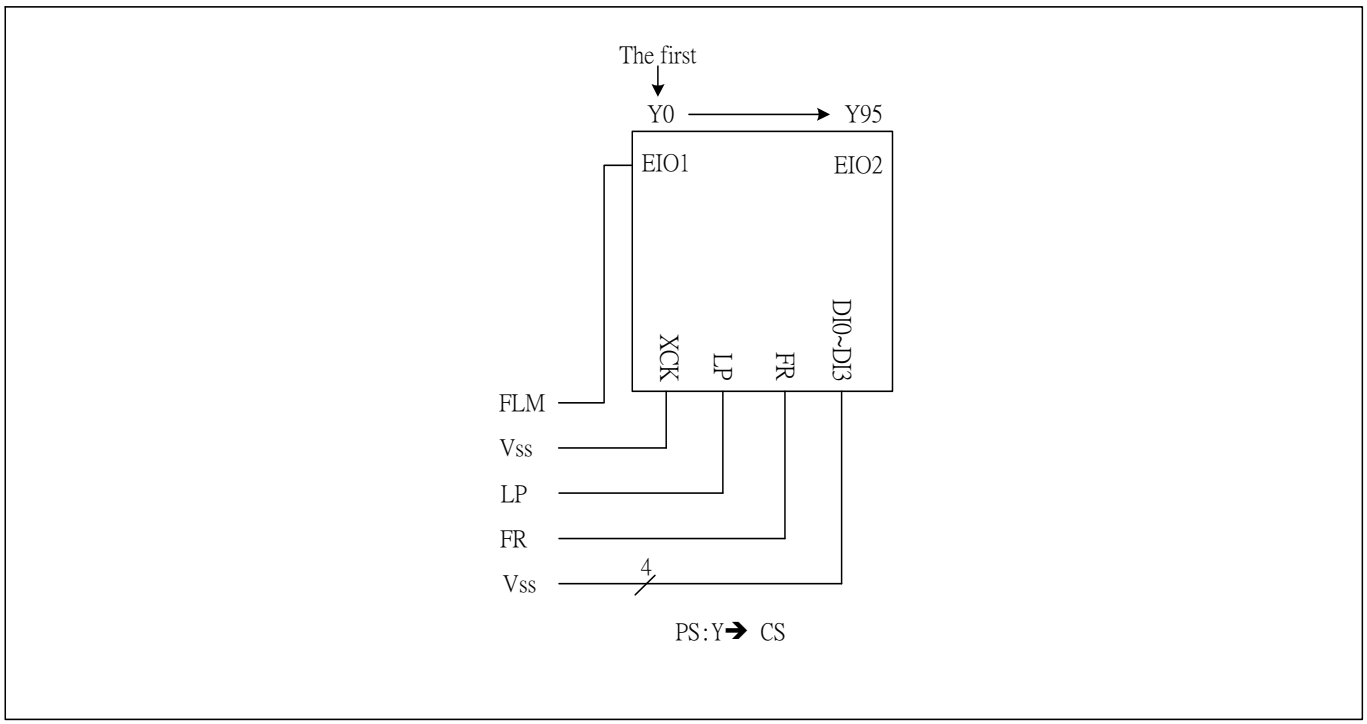


8.2.5 Connection examples for signal common drivers (96 common)

(c) When the L/R register set "L" level



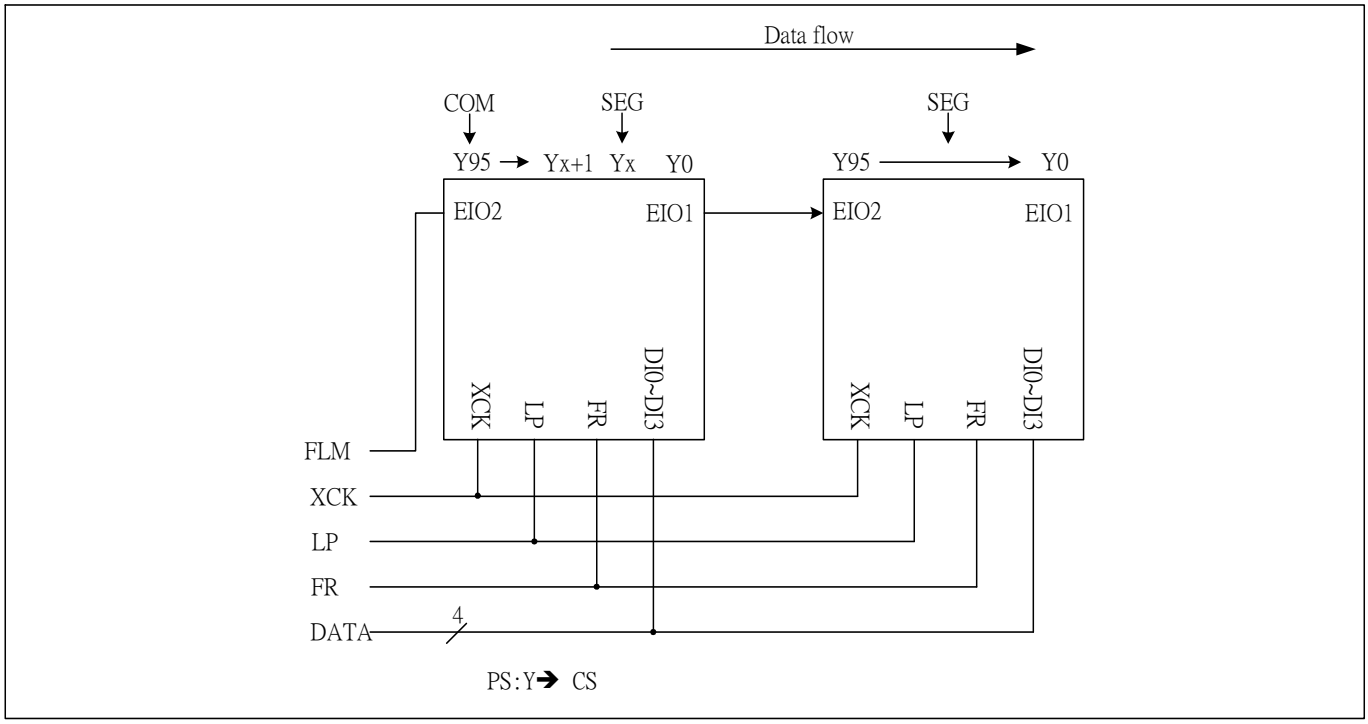
(d) When the L/R register set "H" level



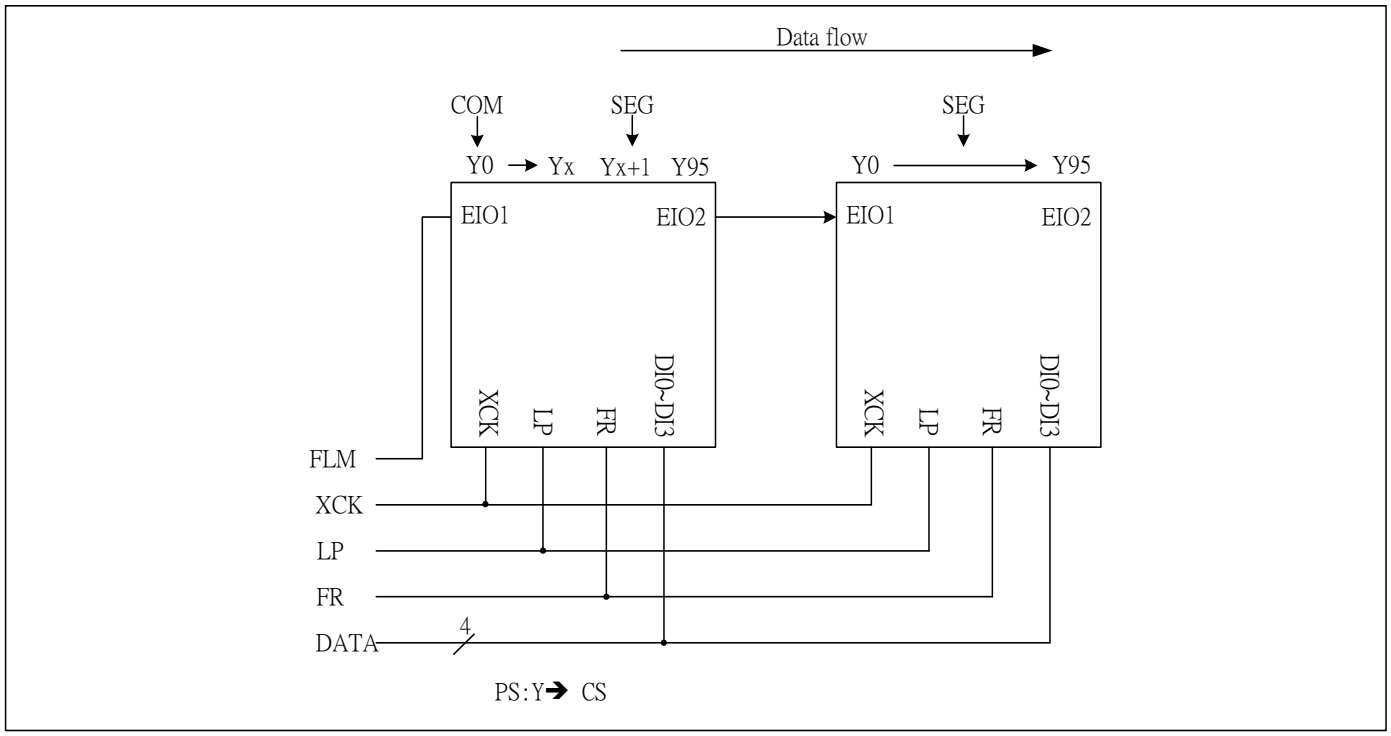
8.2.6 Connection examples for plural common/segment (mix mode) drivers

The mix mode is 1/16, 1/32, 1/48, 1/64, 1/80, 1/96 duty mode

(e) When the L/R register set "L" level



(f) When the L/R register set "H" level



9. PRECAUTIONS

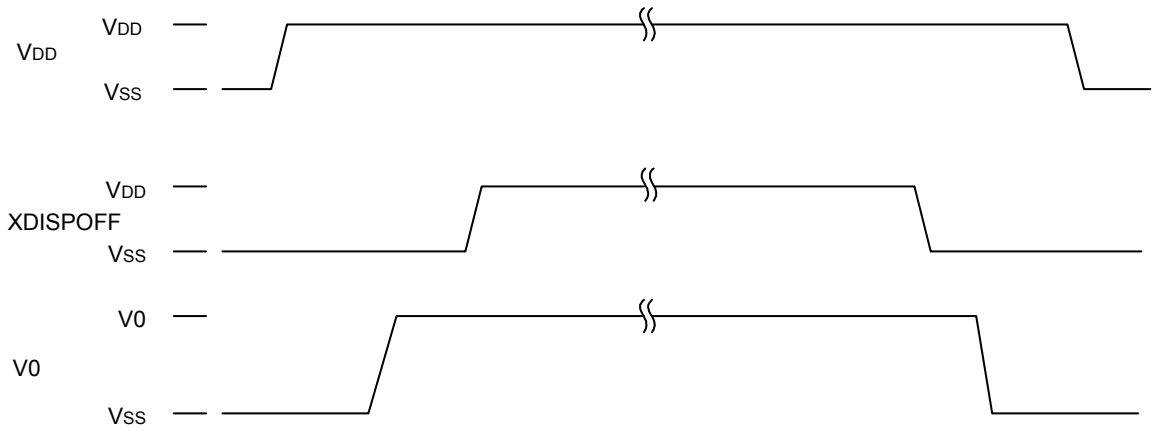
Precautions when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so a high current that may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating may permanently damage it. The details are as follows,

When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power

And when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on XDISPOFF function. After that, cancel the XDISPOFF function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level V_{SS} on XDISPOFF function. Then disconnect the logic system power after disconnecting the LCD drive power.

When connecting the power supply, follow the recommended sequence shown here



10. HARDWARE CIRCUIT DESCRIPTION

The LCD Data Bus Interface

There are two kinds of interfaces for LCD data bus. One is 4-bit parallel data interface and the other is the serial interface. These two kinds of interfaces are selected by setting the P/S bit in the “Interface Control Selection” register, and see detail in the Table 1. D1~D3 on data bus must be fixed to ground when “1” for P/S bit is selected.

Table 1

P/S	Data Bus Mode
1	Parallel Interface(D0~D3)
0	Serial Interface (D0)

The Command Registers Setting Interface

The command registers for ST8009 is setting by serial interface, SCLK and SID. The timing of serial interface is shown in Fig.1 and Fig.2 Both SCLK and SID must be connected to pull-up resistors.

START AND STOP CONDITIONS

Both SID and SCLK must be kept at high when the bus is not busy, and if SCLK is high at the falling edge of SID, ST8009 will enter the “Start Condition” for beginning to receive command. Otherwise, if SCLK is high at the rising edge of SID, ST8009 will enter the “Stop Condition” for finishing command transfer. The start and stop conditions are illustrated in Fig.3

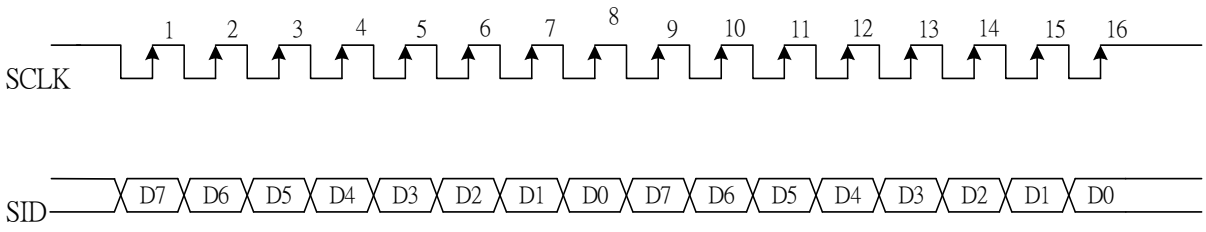


Fig .1 Write command timing diagram

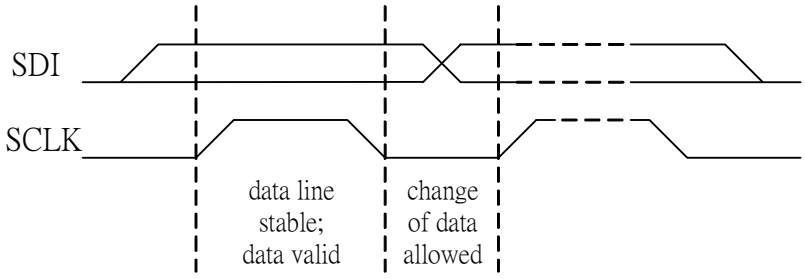


Fig .2 Bit transfer

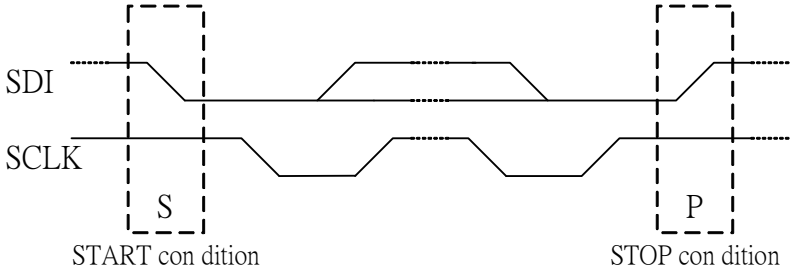


Fig .3 Definition of START and STOP conditions

The Power Supply Circuits

The power supply circuits generate the LCD bias for LCD drive. The power supply circuits are consisted of booster circuit, voltage regulator circuit, and voltage follower circuit. They only enabled when ST8009 is in common mode or common/segment mode. The power supply circuits can turn on or turn off the booster circuit, voltage regulator circuit, and voltage follower circuit independently by setting the "Power Control Set" register. Table 2 shows the detail for "Power Control Set" register.

Table2

Bit			Function	Status	
				"1"	"0"
D2	D1	D0	Booster circuit control bit	ON	OFF
D2	D1	D0	Voltage regulator circuit control bit (V/R circuit)	ON	OFF
D2	D1	D0	Voltage follower circuit control bit (V/F circuit)	ON	OFF

The Step-up Voltage Circuits

By applying the step-up voltage circuit for ST8009, it is possible to produce a voltage which is 2, 3, 4, 5, or 6 times of V_{DD} level. Here must notice that the **6X step-up application only support for V_{DD} less than +2.7V**, or the ST8009 may be damaged permanently by V_{OUT} over +16V. By the same reason, the **5X step-up application only can be used when V_{DD} inside +3.3V**, and the 4X step-up application circuit only can be used when V_{DD} inside +4V. If the voltage of V_{OUT} which is generated by ST8009 internal booster circuit is almost over absolute maximum voltage(+16V) , we suggest using the external voltage regulator to stabilize the V_{DD} power, or the V_{OUT} may be over the absolute maximum voltage(+16V) when the V_{DD} power is not stable.

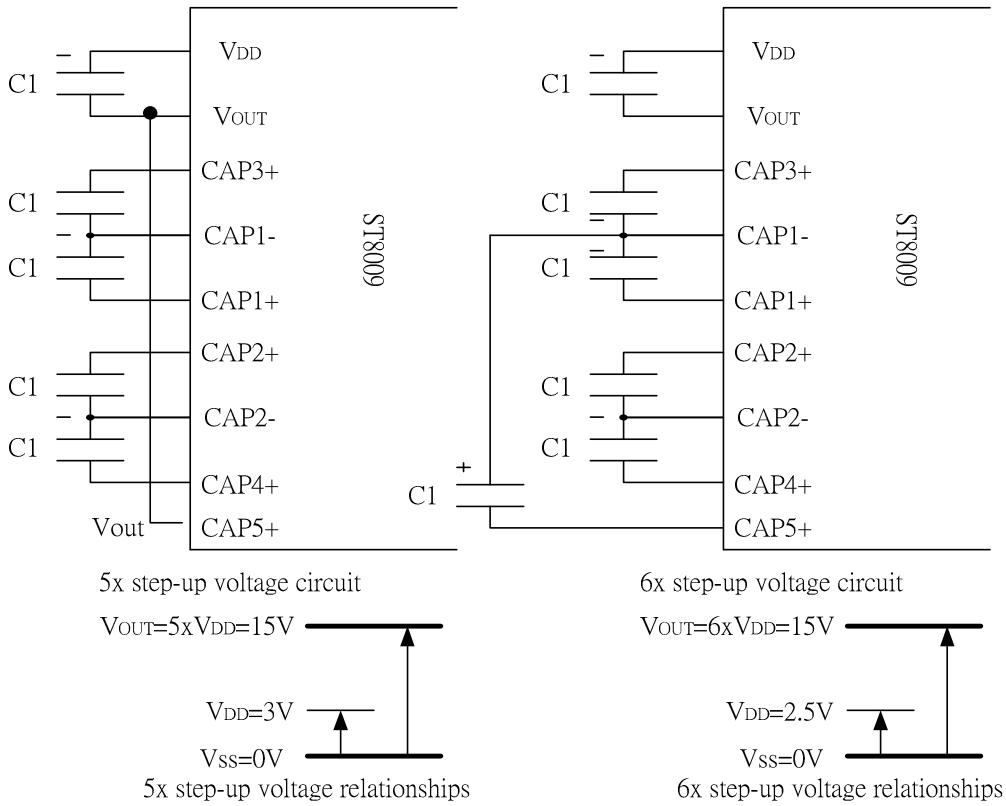


Fig 4.1

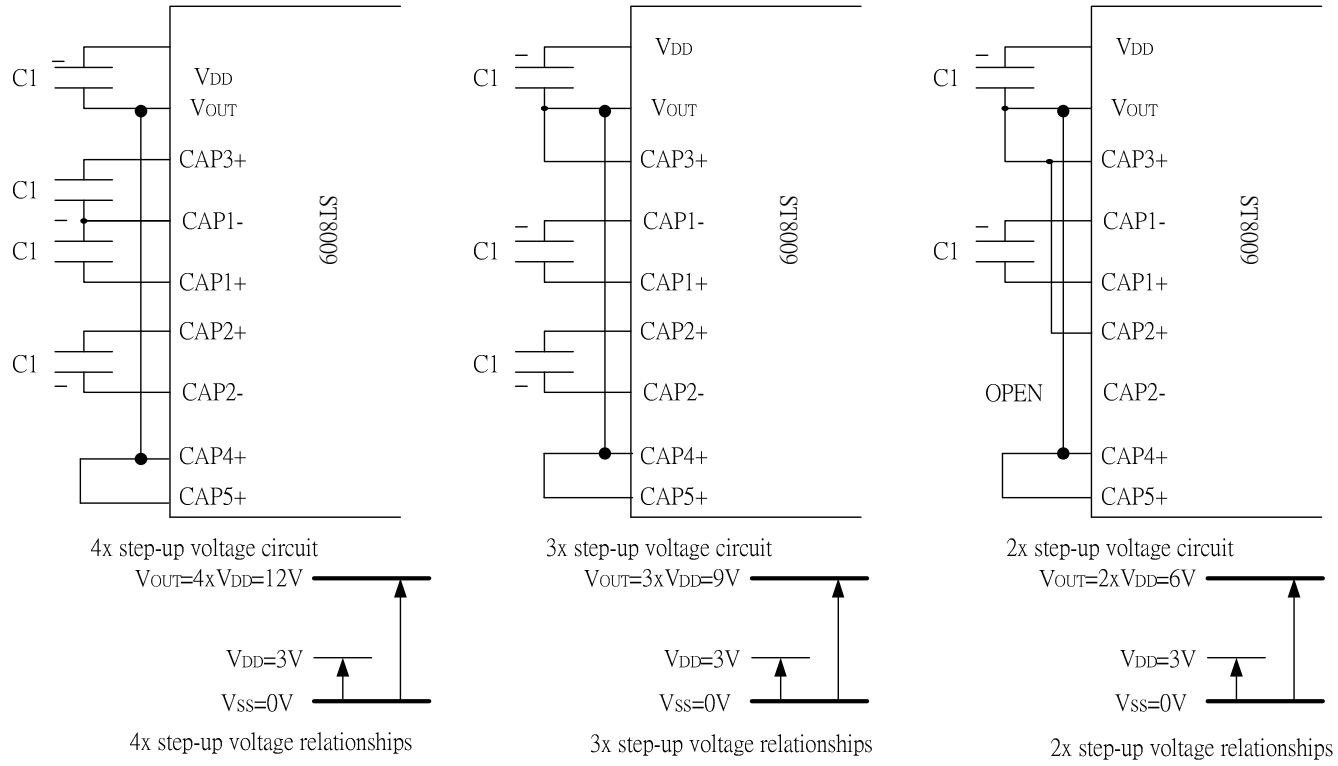


Fig 4.2

* The V_{DD} voltage range must be set properly so that the voltage on V_{OUT} does not exceed the absolute maximum rated value.

The Voltage Regulator Circuit

There is a high-accuracy digital to analog circuit with 64-level electronic volume function and variable resistor inside ST8009. Systems can be constructed without high-accuracy voltage regulator circuit, if the voltage on V_{OUT} terminal is much less than absolute maximum voltage.(V_{REG} thermal gradients approximate -0.15%/°C). Through using the V0 voltage regulator internal resistors and the electronic volume function, the liquid crystal power supply voltage V0 can be controlled by command register alone (without adding any external resistors), and making it possible to adjust the liquid crystal display brightness. The V0 voltage can be calculated using following equation over the range where | V0 | < | V_{OUT}|

V_{REG} is the IC-internal fixed voltage supply, and its voltage at Ta = 25°C is as shown in Table 4.

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \bullet V_{EV}$$

$$= \left(1 + \frac{Rb}{Ra}\right) \bullet \left(1 - \frac{\alpha}{200}\right) \bullet V_{REG}$$

$$\left[\because V_{EV} = \left(1 - \frac{\alpha}{200}\right) \bullet V_{REG}\right]$$

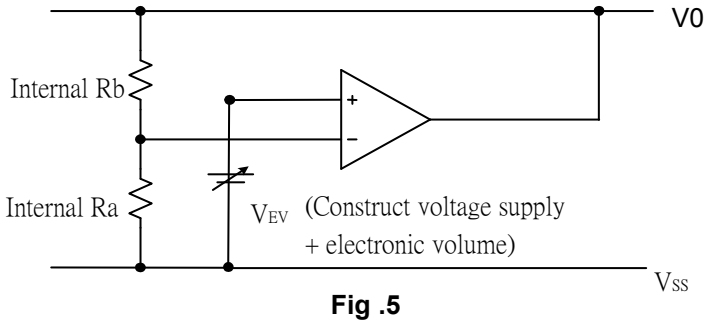


Fig .5

Part no.	Equipment Type	Thermal Gradient	V_{REG}
ST8009	Internal Power Supply	–0.15 %/°C	2.1V

Table4

α is set to one of the 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronic volume register. Table 5 shows the value for α depending on the electronic volume register settings. Rb/Ra is the V0 voltage regulator internal resistor ratio, and can be set to 8 different levels through the V0 voltage regulator internal resistor ratio set command. The Rb/Ra ratio assumes the values shown in Table 6 depending on the 3-bit data settings in the V_{DD} voltage regulator internal resistor ratio register.

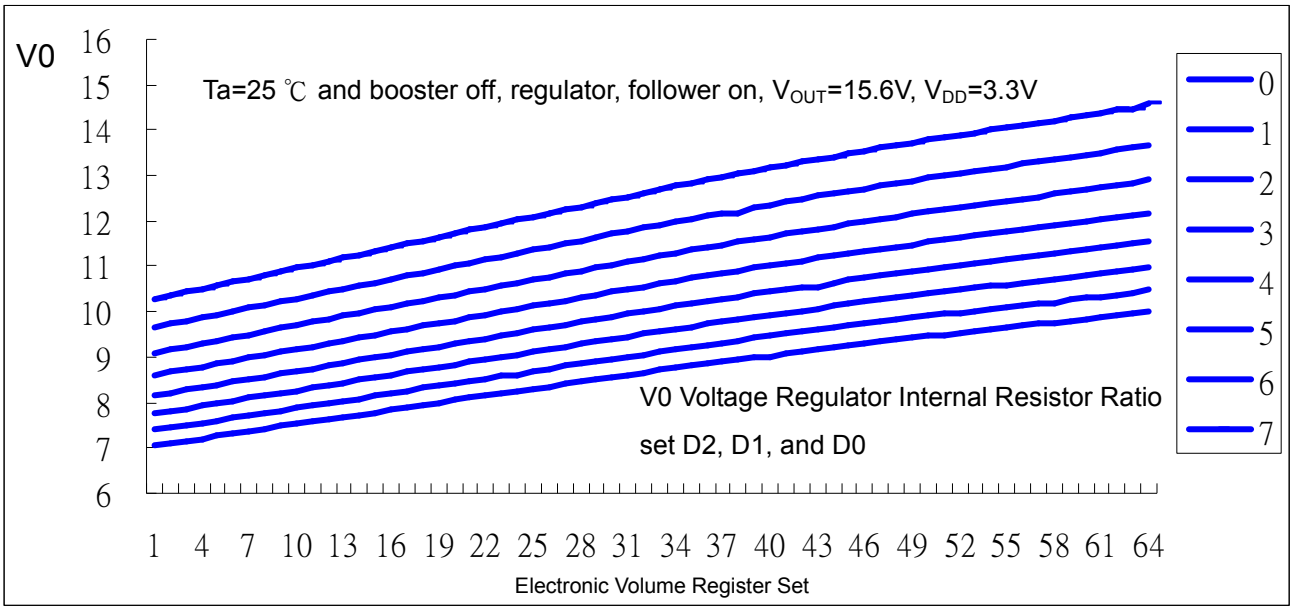
Table5

D5	D4	D3	D2	D1	D0	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
			:			:
			:			:
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

V0 voltage regulator internal resistance ratio register value and (1 + Rb/Ra) ratio (Reference value)

Table6

Register			ST8009
D2	D1	D0	(1) –0.15 %/°C
0	0	0	5.0
0	0	1	5.22
0	1	0	5.48
0	1	1	5.76
1	0	0	6.07
1	0	1	6.42
1	1	0	6.81
1	1	1	7.25



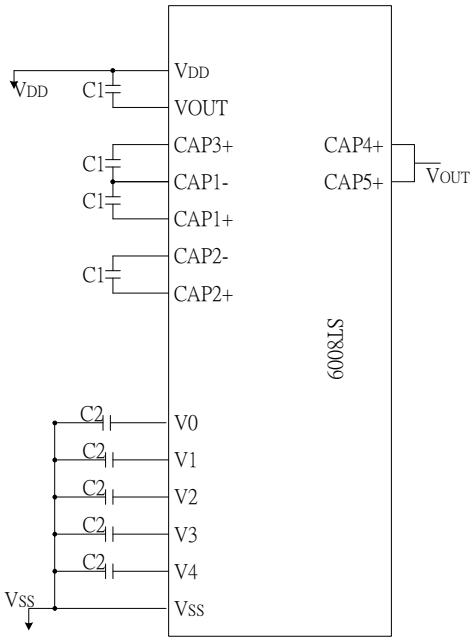
The LCD Voltage Generator Circuit

The V0 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V1, V2, V3, and V4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V1, V2, V3 and V4 to the liquid crystal drive circuit.

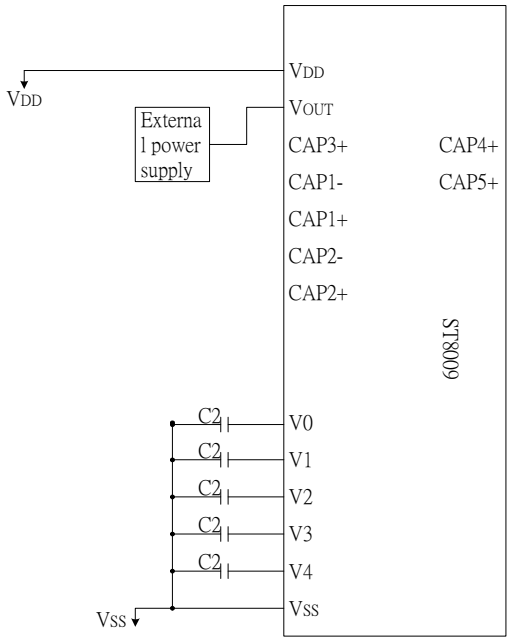
Reference Circuit Examples

1. When the step-up circuit, voltage regulating circuit and V/F circuit are used.

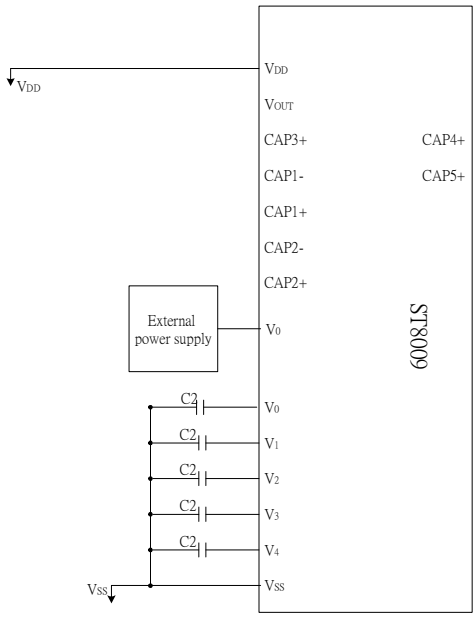
   (Example with 4x setup-up)



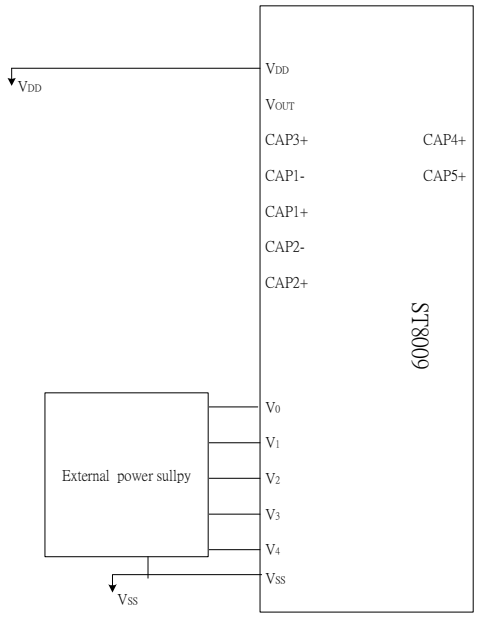
2. When only the voltage regulator circuit and V/F circuit are used



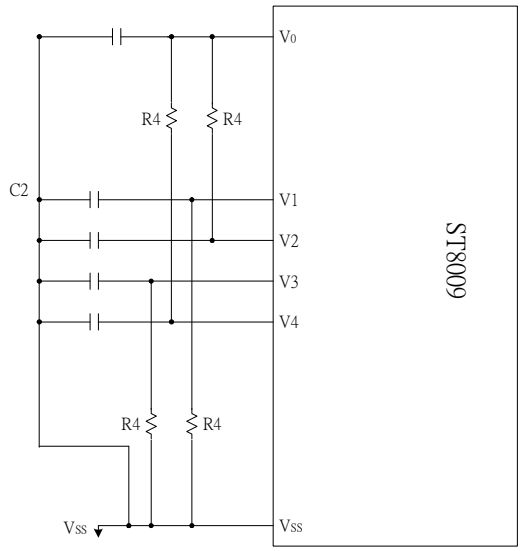
3. When only the V/F circuit is used



4. When the built-in power is not use



5. When the built-in power circuit is used to drive a liquid crystal panel with heavy load, it is recommended to connect an external resistor to stabilize potentials of V1, V2, V3 and V4 which are output from the built-in voltage follower.



R4 : 100KΩ ~ 1MΩ, it is recommended to set an optimum resistance value for R4 according to the quality of liquid crystal display and the drive waveform

* 1. Because the VR terminal input impedance is high, use short leads and shielded lines.
* 2. C1 and C2 are determined by the size of the LCD being driven. Select a value that can stabilize the liquid crystal drive voltage in the Table 7.

Item	Set value	units
c1	1.0 to 4.7	uF
c2	0.1 to 4.7	uF

Table7

Following steps are the examples about how to determine the value for these capacitors:

- Turn the voltage regulator circuit and voltage follower circuit on and supply a voltage to V_{OUT} externally.
- Determine C2 by displaying an LCD pattern with a heavy load (such as horizontal stripes), and select a value for C2 that can stabilize the liquid crystal drive voltages (V1 to V4). Note that all C2 capacitors must have the same capacitance value.
- Next, turn on all the power supply circuits to determine C1

11. INSTRUCTION TABLE

Instruction	Instruction Code								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
Interface control selection	0	0	0	0	0	M	LR	PS	Interface selection and set
Software Reset	0	0	0	1	0	0	0	RST	Software reset, when set the register then the ST8009 will be reset
LCD Duty selection	0	0	1	0	0	DU2	DU1	DU0	The register can select the LCD duty numbers
LCD Bias Set	0	0	1	1	0	B2	B1	B0	The register can select the LCD bias
Power Controller Set	0	1	0	1	0	B	R	F	Set the power mode. The register contain three power circuits can select (booster, regulator, follow)
Booster Frequency Set	1	0	0	0	0	F2	F1	F0	Set the booster frequency
V0 Voltage Regulator Internal Resistor Ratio Set	1	0	0	1	0	Rab2	Rab1	Rab0	Select internal resistor ratio (Ra/Rb) mode
Electronic Volume Register Set	1	1	E5	E4	E3	E2	E1	E0	Set the V0 output voltage electronic volume register

12. INSTRUCTION DESCRIPTION

The ST8009 identify the data bus signals by a combination between SID and SCLK signals.

Interface Control

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	M	LR	PS

The register can control frame direction, common, segment, common/segment direction and serial or parallel (4-bits) input data Interface.

M: Frame direction control bit

When M=" Height", the internal frame direction and external frame direction are the same (normally).

When M=" Low", the internal frame direction and external frame direction are adverse.

LR: CS output direction control bit

LR="H"	CS0	→	CS95
LR="L"	CS95	→	CS0

PS: Data Interface mode select control bit

When PS="Low", the data input interface is serial

When PS=" Height", the data input interface is parallel (4-bits)

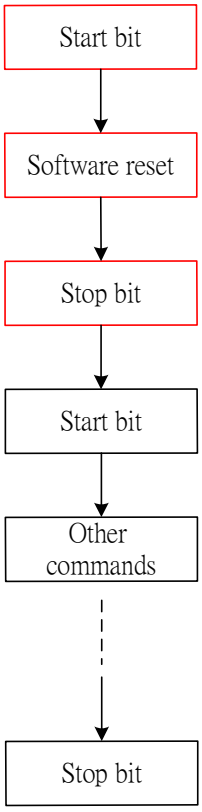
Software Reset

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0	RST

When RST="1" , do software reset action.

Software reset need "Start bit" at the beginning to start the action, and also need "Stop bit" at the end to release the initializing state. It is different to other commands so can't set continuously with other commands.

Note: Other commands can be set continuously with only one start bit at beginning and stop bit at end:



LCD Duty Selection

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	DU2	DU1	DU0

"LCD Duty Selection" register can set the duty for LCD display. Detail in the following column:

DU2	DU1	DU0	COM Num.	SEG Num.
0	0	0	0	96
0	0	1	16	80
0	1	0	32	64
0	1	1	48	48
1	0	0	64	32
1	0	1	80	16
1	1	0	96	0
1	1	1	96	0

LCD Bias Set

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	B2	B1	B0

This register can select the voltage bias ratio which is required for the liquid crystal display. There are eight bias modes can be selected in ST8009.

B2	B1	B0	Bias select
0	0	0	1/4
0	0	1	1/5
0	1	0	1/6
0	1	1	1/7
1	0	0	1/8
1	0	1	1/9
1	1	0	1/10
1	1	1	1/11

Power Controller Set

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	B	R	F

This register can enable or disable the power supply circuit in ST8009. See details in “The Power Supply Circuit”.

B	R	F	Status
0	--	--	Booster circuit : off
1	--	-	Booster circuit : on
--	0	--	Regulator circuit : off
--	1	--	Regulator circuit : on
--	--	0	Follower circuit : off
--	--	1	Follower circuit : on

Booster Frequency Set

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	F2	F1	F0

This register can select one of the booster frequency in the following column:

F2	F1	F0	Booster Frequency
0	0	0	1K
0	0	1	2K
0	1	0	3K
0	1	1	4K
1	0	0	5K
1	0	1	6K
1	1	0	7K
1	1	1	8K

V0 Voltage Regulator Internal Resistor Ratio Set

This register can set the V0 voltage regulator internal resistor ratio.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	Rab2	Rab1	Rab0

Rab2	Rab1	Rab0	Ra/Rb Ratio
0	0	0	Small ↓ Large
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Electronic Volume Register Set

D7	D6	D5	D4	D3	D2	D1	D0
1	1	E5	E4	E3	E2	E1	E0

This register can control the V0 in 64 steps of voltage level to adjust the brightness of the liquid crystal display. This register had better set under 0xE0. Because when the value of this register set over 0xE0, the V0 will be inaccuracy. The inaccurate value of V0 will exceed in ±0.1V when this register set over 0xE0. By this limit, if we need a higher voltage for V0, we had better set the bigger value for "V0 Voltage Regulator Internal Resistor Ratio" register, and then adjust the value of "Electronic Volume" register to produce the proper voltage for V0 terminal.

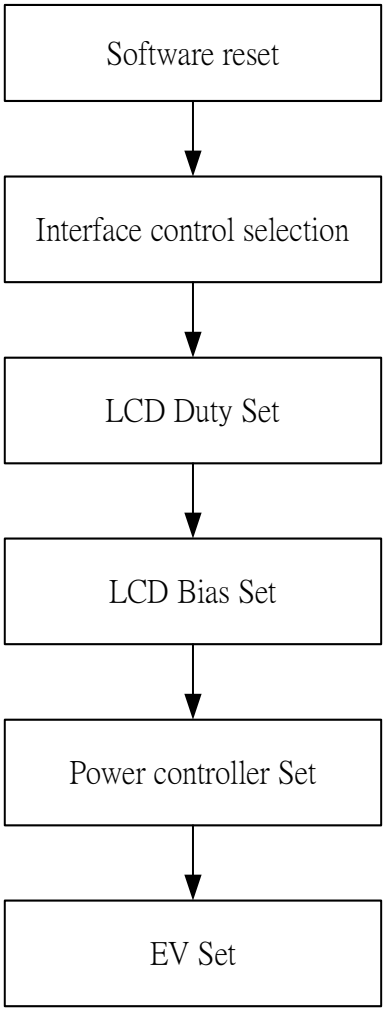
E5	E4	E3	E2	E1	E0	Ra/Rb Ratio
0	0	0	0	0	0	Small ↓
0	0	0	0	0	1	
0	0	0	0	1	0	
⋮	⋮	⋮	⋮	⋮	⋮	
1	1	1	1	0	1	
1	1	1	1	1	0	
1	1	1	1	1	1	Large

Initializing by internal Reset circuit

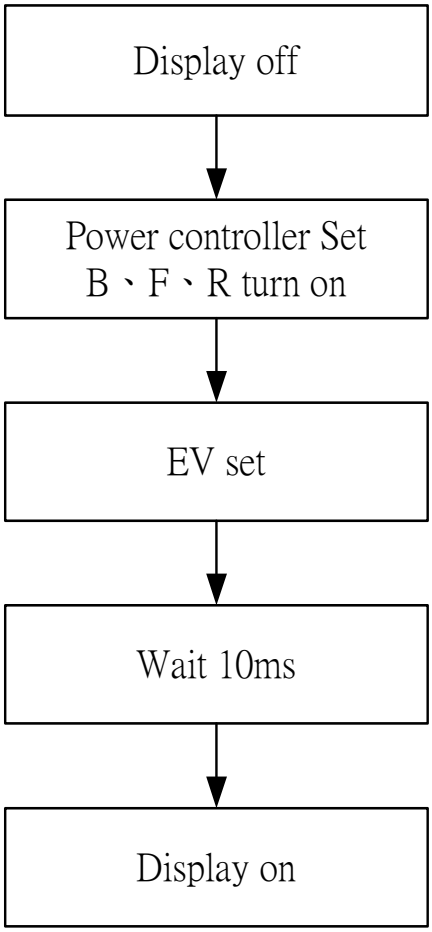
An internal reset circuit initializes the ST8009 after software reset has set. Following are the initial value of command registers after software reset:

1. Interface control selection
   FR: 0
   LR: 0
   PS: 1
2. LCD Duty selection
   The segment mode (96 segments) is selected by default.
3. LCD Bias Set
   1/4 bias is selected by default.
4. Power Controller Set
   All the power circuits (booster, regulator and follower) will be turned off by default.
5. Booster Frequency Set
   Volume is 1 0 0 by default
6. V0 Voltage Regulator Internal Resistor Ratio Set
   Volume is 1 0 0 by default
7. Electronic Volume Register Set
   Volume is 1 0 0 0 0 0 by default

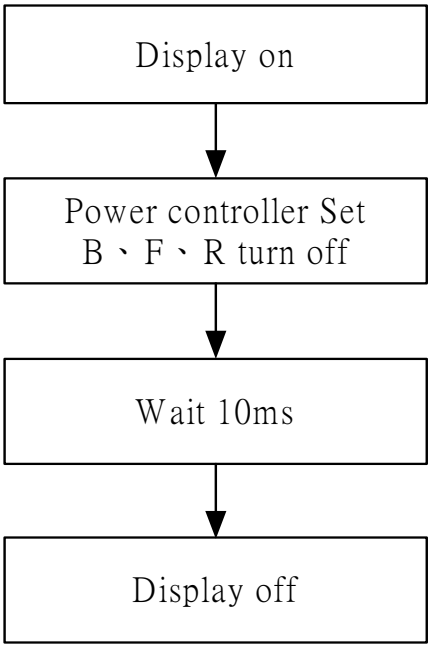
Initial Flow



Power on Flow



Power off Flow



13. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	2.5~5.5	V	1,2
Supply voltage (2)	V1	V1	V_{DD} +10~ V_{DD} +0.3	V	
	V2	V2	V_{DD} +10~ V_{DD} +0.3		
	V3	V3	-0.3~ V_{SS} +10	V	
	V4	V4	-0.3~ V_{SS} +10	V	
Input voltage	VI	D14-DI0, XCK, FR, EIO1, EIO2, XDISPOFF	-0.3 to V_{DD} +0.3	V	
Storage temperature	TSTG		-45 to +125	°C	

NOTES:

1. TA = +25 °C
2. The maximum applicable voltage on any pin with respect to V_{SS} (0 V).

14. RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	+2.5		+5.5	V	1, 2
Supply voltage (2)	V0	V0	+5.0		+16.0	V	
Operating temperature	TOPR		-20		+85	°C	

NOTES:

1. The applicable voltage on any pin with respect to V_{SS} (0 V).
2. Ensure that voltages are set such that V0 ≧V1 ≧V2 ≧V3 ≧V4 ≧V_{SS}.

15. ELECTRICAL CHARACTERISTICS

15.1 DC Characteristics

(Segment Mode) (V_{SS} = 0 V, V_{DD} = +2.5 to +5.5 V, V0 = + 5.0 to +16.0 V, T_{OPR} = -20 to +85°C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		DI7-DI0, XCK, FR, EIO1, EIO2,XDISPOFF			$0.2V_{DD}$	V	
Input "High" voltage	V_{IH}			$0.8V_{DD}$			V	
Output "Low" voltage	V_{OL}	I_{OL} = +0.4 mA	EIO1, EIO2			+0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -0.4 mA		V_{DD}-0.4			V	
Input leakage current	I_{LIL}	$V_I = V_{SS}$	DI7-DI0, XCK, LP, FR, EIO1, EIO2,XDISPOFF			-10	µA	
	I_{LIH}	$V_I = V_{DD}$				+10	µA	
Output resistance	R_{ON}	$\lvert\Delta V_{ON}\rvert$ =0.5V, V0 = 16V	CS0-CS95		1.0	1.5	kΩ	
Standby current	I_{STB}		V_{SS}			5.0	µA	1
Supply current (1) (Non-selection)	I_{DD1}		V_{DD}			2.0	mA	2
Supply current (2) (Selection)	I_{DD2}		V_{DD}			7.0	mA	3
Supply current (3)	I_0		V0			0.9	mA	4

NOTES:

1. V_{DD} = +5.0 V, V0 = +16.0 V, $V_I = V_{SS}$.
2. V_{DD} = +5.0 V, V0 = +16.0 V, f_{XCK} = 8 MHz, no-load, EI = V_{DD}. The input data is turned over by data taking clock (4-bit parallel input mode).
3. V_{DD} = +5.0 V, V0 = +16.0 V, f_{XCK} = 8MHz, f_{LP} = 19.2 kHz, f_{FR} = 80 Hz, no-load. The input data is turned over by data taking clock (4-bit parallel input mode).

(Common Mode) (V_{SS} = 0 V, V_{DD} = +2.5 to +5.5 V, V0 = +5.0 to +16.0 V, T_{OPR} = -20 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABL E PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		DI4-DI0, XCK, FR, EIO1, EIO2, XDISPOFF			$0.2V_{DD}$	V	
Input "High" voltage	V_{IH}			$0.8V_{DD}$			V	
Output "Low" voltage	V_{OL}	I_{OL} = +0.4 mA	EIO1, EIO2			+0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -0.4 mA		V_{DD}-0.4			V	
Input leakage current	I_{LIL}	$V_I = V_{SS}$	DI4-DI0, XCK, FR, P/S, EIO1, EIO2, XDISPOFF			-10.0	µA	
	I_{LIH}	$V_I = V_{DD}$	DI4-DI0,FR,XDISPOFF			+10.0	µA	
Input pull-down current	I_{PD}	$V_I = V_{DD}$	XCK, EIO1, EIO2			100	µA	
Output resistance	R_{ON}	$\lvert\Delta V_{ON}\rvert$=0.5V V0 = 16V	CS0-CS95		1.0	1.5	kΩ	
Standby current	I_{SPD}		V_{SS}			5.0	µA	1
Supply current (1)	I_{DD}		V_{DD}			80	µA	2
Supply current (2)	I_0		V0			130	µA	2

NOTES:
1. V_{DD} = +5.0 V, V0 = +16.0 V, $V_I = V_{SS}$
2. V_{DD} = +5.0 V, V0 = +16.0 V, f_{LP} =19.2 kHz, f_{FR} = 80 Hz, 1/96 duty operation, no-load.

15.2 AC Characteristics

(Segment Mode 1) (V_{SS} = 0 V, V_{DD} = +2.5 to +3.0 V, V0 = + 5.0 to +16.0 V, T_{OPR} = -20 10+85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R,t_F ≤ 11ns	125			ns	1
Shift clock "H" pulse width	t_{WCKH}		51			ns	
Shift clock "L" pulse width	t_{WCKL}		51			ns	
Data setup time	t_{DS}		30			ns	
Data hold time	t_{DH}		40			ns	
Latch pulse "H" pulse width	t_{WLPH}		51			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		51			ns	
Latch pulse rise to shift clock rise time	t_{LS}		51			ns	
Latch pulse fall to shift clock fall time	t_{LH}		51			ns	
Latch pulse fall to shift clock rise time	t_{LSW}		50			ns	
Enable setup time	t_S		36			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			78	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

NOTES:
1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Segment Mode 2) (V_{SS} = 0 V, V_{DD} = +5.0±0.5 V, V0 = + 5.0 to +16.0 V, T_{OPR} = -20 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R,t_F ≤ 10ns	66			ns	1
Shift clock "H" pulse width	t_{WCKH}		23			ns	
Shift clock "L" pulse width	t_{WCKL}		23			ns	
Data setup time	t_{DS}		15			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		50			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Latch pulse fall to shift clock rise time	t_{LSW}		50			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			41	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

NOTES:
1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Segment Mode 3) (V_{SS} = 0 V, V_{DD} = +3.0 to +4.5 V, V0 = + 5.0 to +16.0 V, T_{OPR} = -20 10+85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R,t_F ≤ 10ns	82			ns	1
Shift clock "H" pulse width	t_{WCKH}		28			ns	
Shift clock "L" pulse width	t_{WCKL}		28			ns	
Data setup time	t_{DS}		20			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		51			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Latch pulse fall to shift clock rise time	t_{LSW}		50			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			57	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

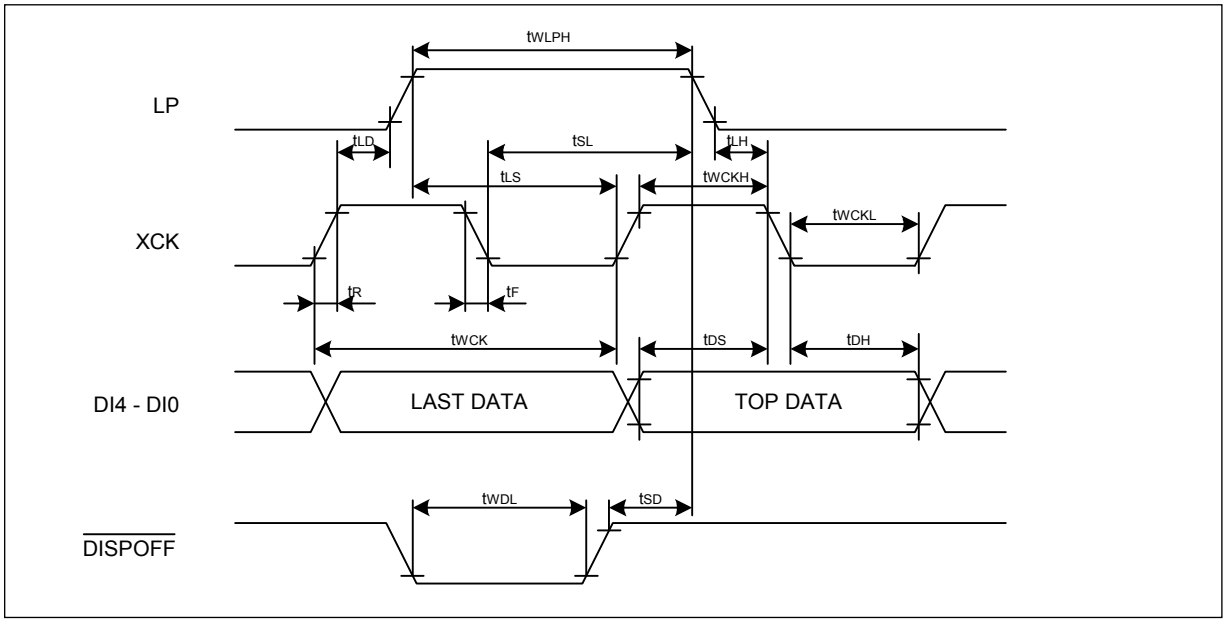
NOTES: 1. Takes the cascade connection into consideration.

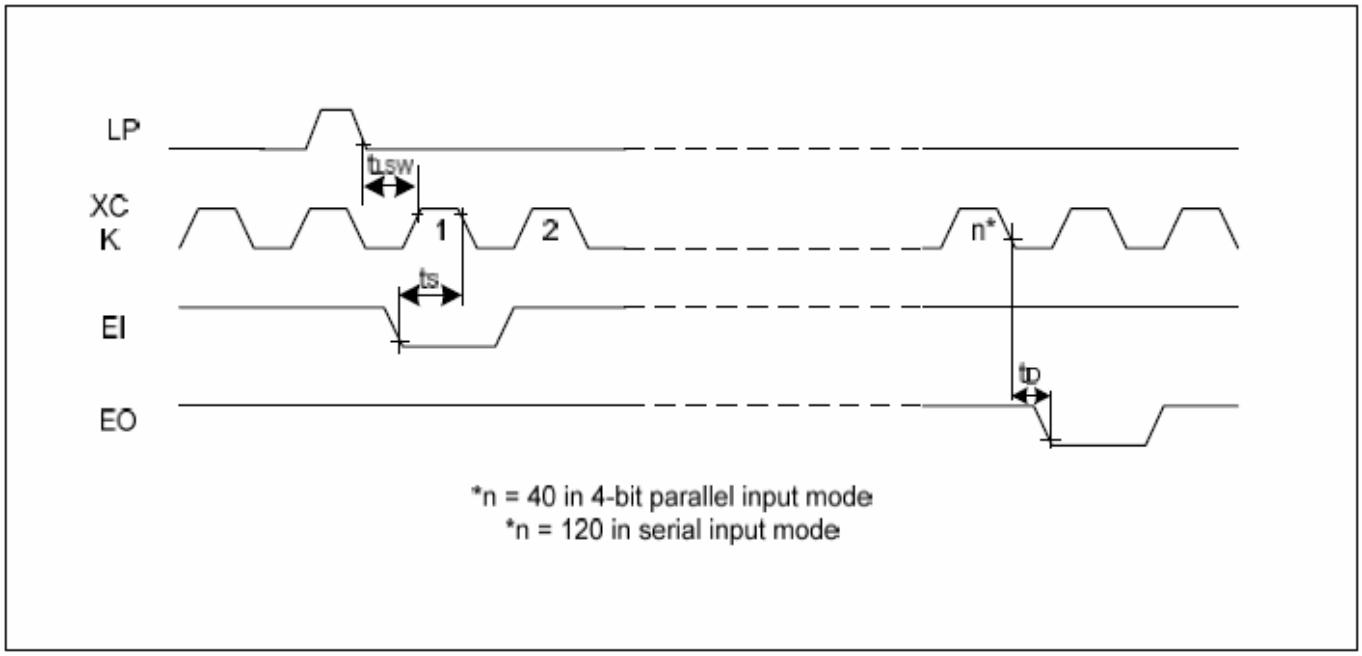
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

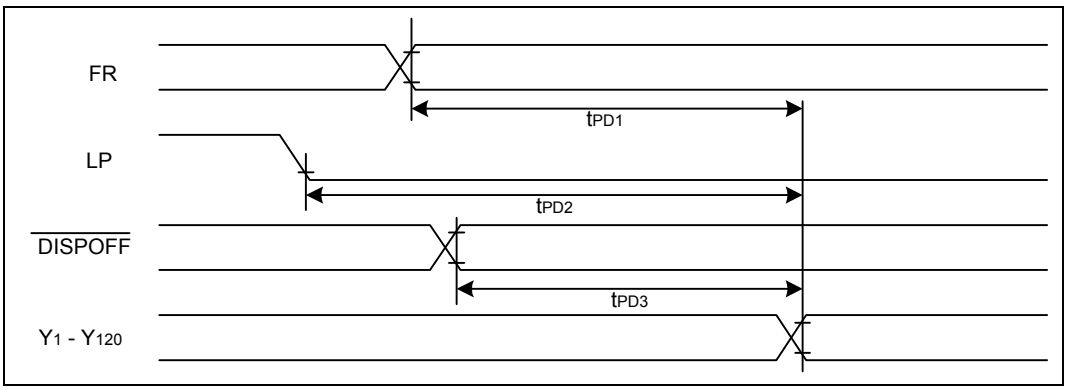
(Common Mode) (V_{SS} = 0 V, V_{DD} = +2.5 to +5.5 V, V0 = + 5.0 to +16.0 V, T_{OPR} = -20 10+85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Shift clock period	t_{WLP}	t_R, t_F 20ns	250			ns
Shift clock “H” pulse width	t_{WLPH}	V_{DD} =5± 0.5V V_{DD} =2.5~4.5V	15 30			ns
Data setup time	t_{SU}		30			ns
Data hold time	t_H		50			ns
Input signal rise time	t_R				50	ns
Input signal fall time	t_F				50	ns
DISPOFF removal time	t_{SD}		100			ns
DISPOFF “L” pulse width	t_{WDL}		1.2			us
Output delay time (1)	t_{DL}	CL=10pF			200	ns
Output delay time (2)	t_{PD1},t_{PD2}	CL=10pF			1.2	us
Output delay time (3)	t_{PD3}	CL=10pF			1.2	us

15.3 Timing Chart of Segment Mode





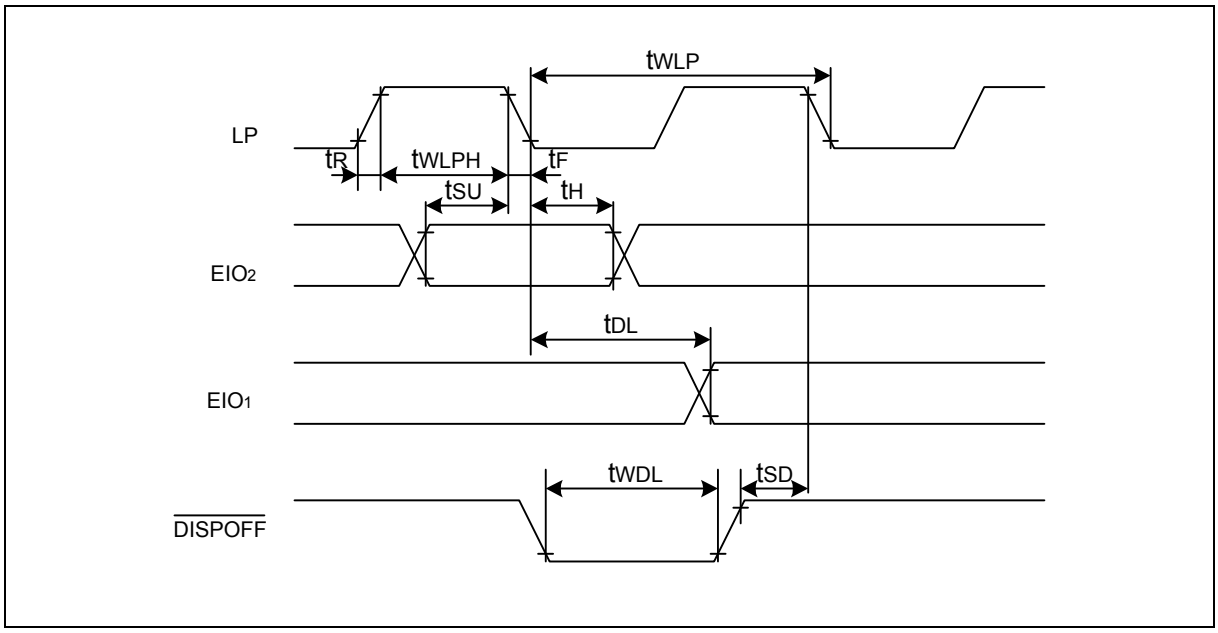


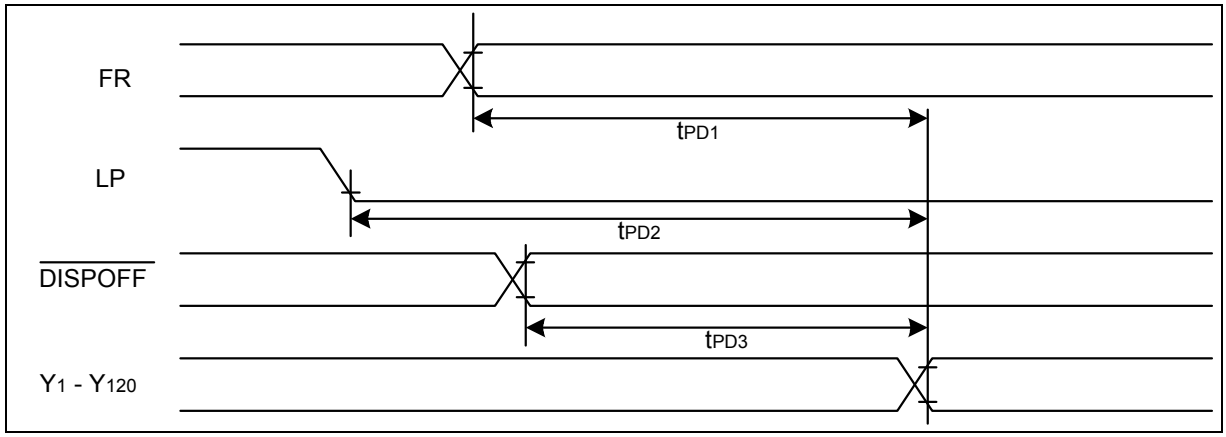
Timing Characteristics (3)

(Common Mode) (V_{SS} = 0 V, V_{DD} = +2.5 to +5.5 V, V0 = +5.0 to +16.0 V, T_{OPR} = -20 to +85° C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Shift clock period	t_{WLP}	t_R,t_F ≤ 20ns	250			ns
Shift clock "H" pulse width	t_{WLPH}	V_{DD} = +5.0± 0.5V	15			ns
		V_{DD} = +2.5+ 4.5V	30			ns
Data setup time	t_{SU}		30			ns
Data hold time	t_H		50			ns
Input signal rise time	t_R				50	ns
Input signal fall time	t_F				50	ns
DISPOFF removal time	t_{SD}		100			ns
DISPOFF "L" pulse width	t_{WDL}		1.2			µs
Output delay time (1)	t_{DL}	CL = 15 pF			200	ns
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs

15.4 Timing Chart of Common Mode



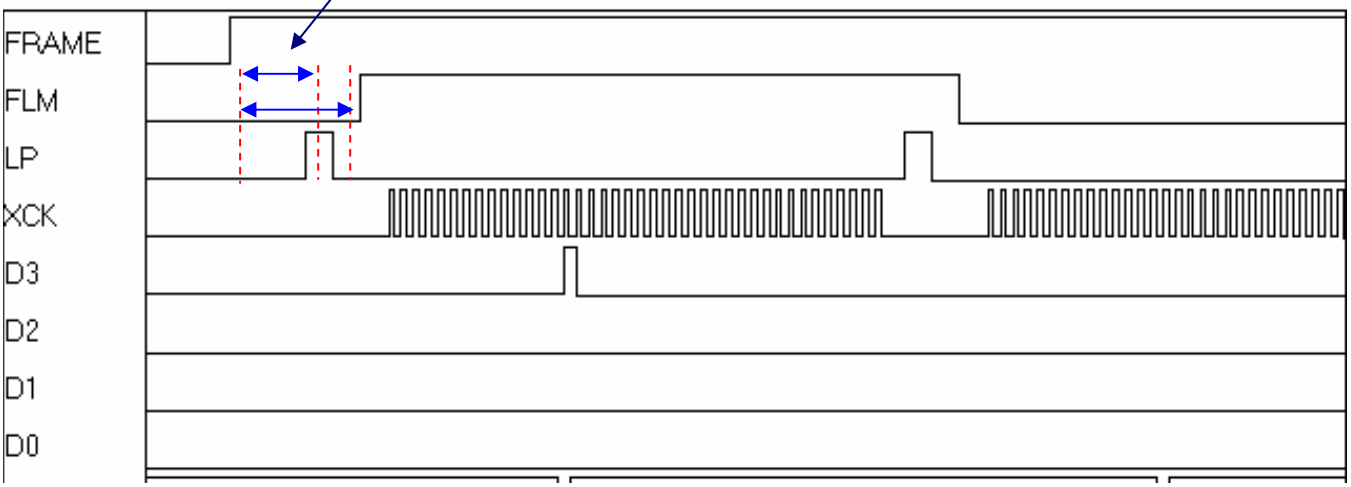


15.5 Application Timing Block:

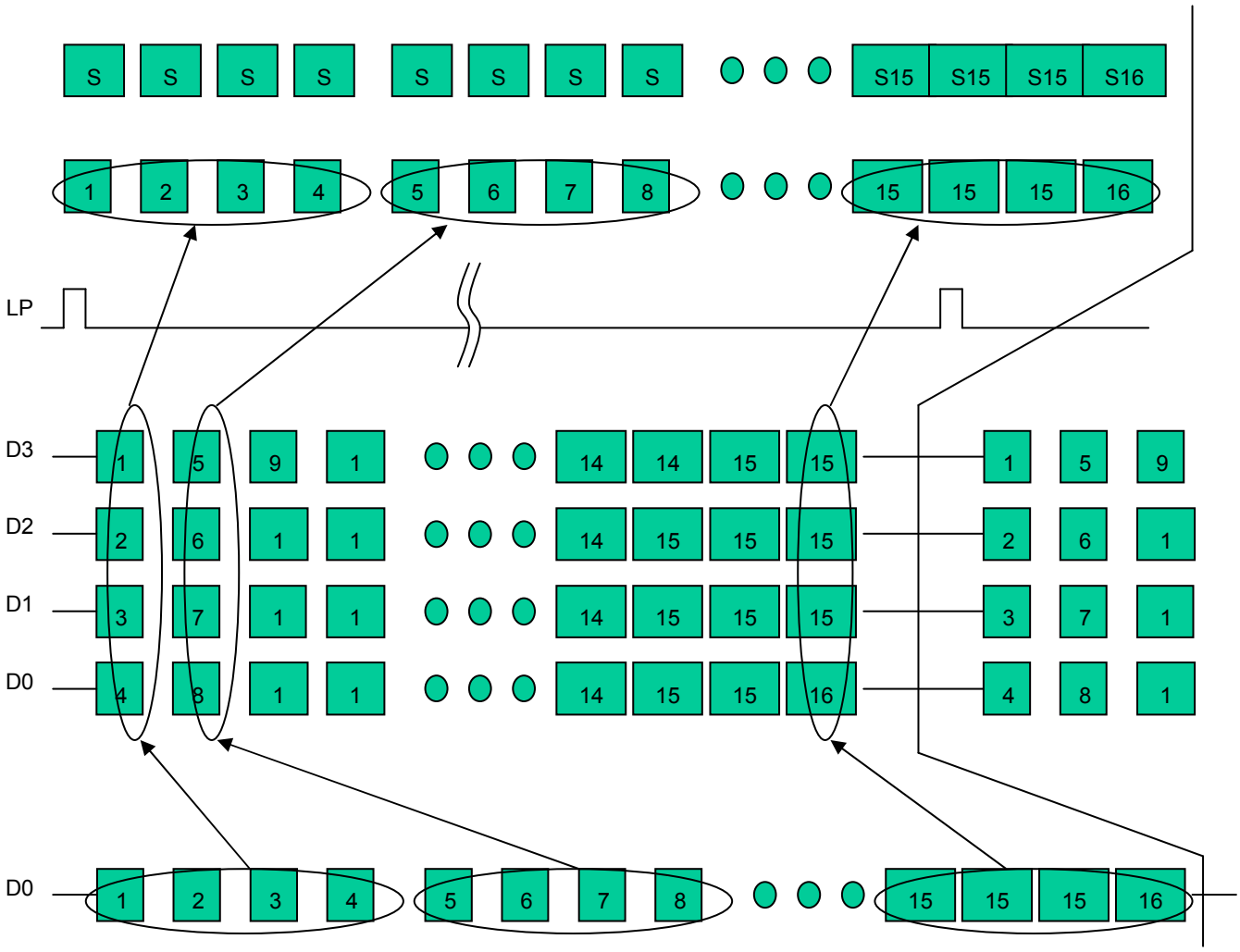
Example 160X80

Frame and Lp falling edge (or rising edge) must >10ns

Grid Size = No Grid

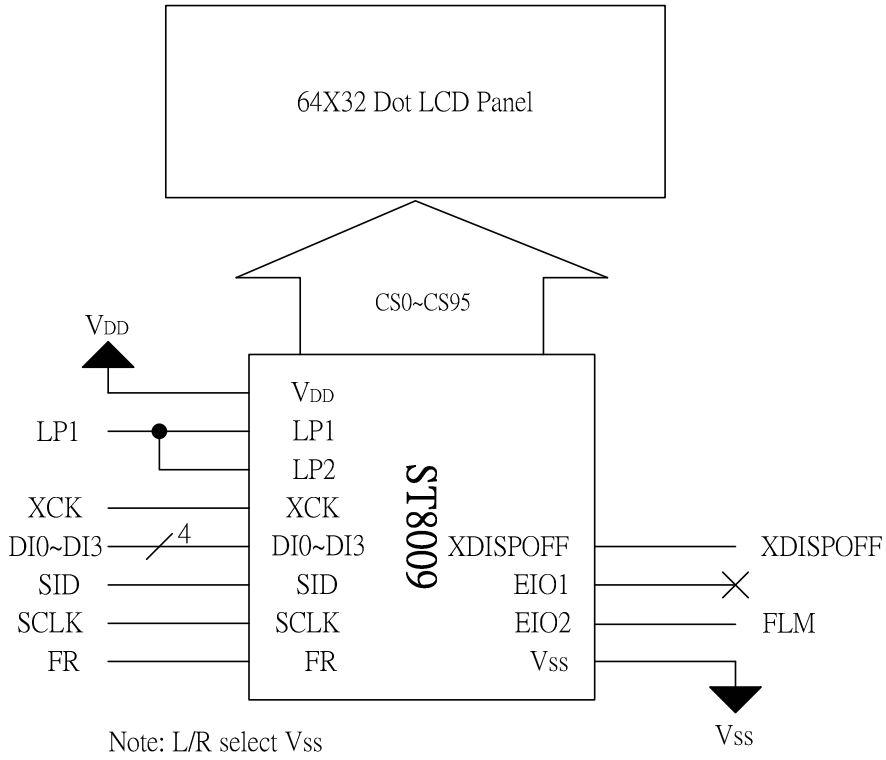


15.6 Parallel vs. Serial Interface Diagram:

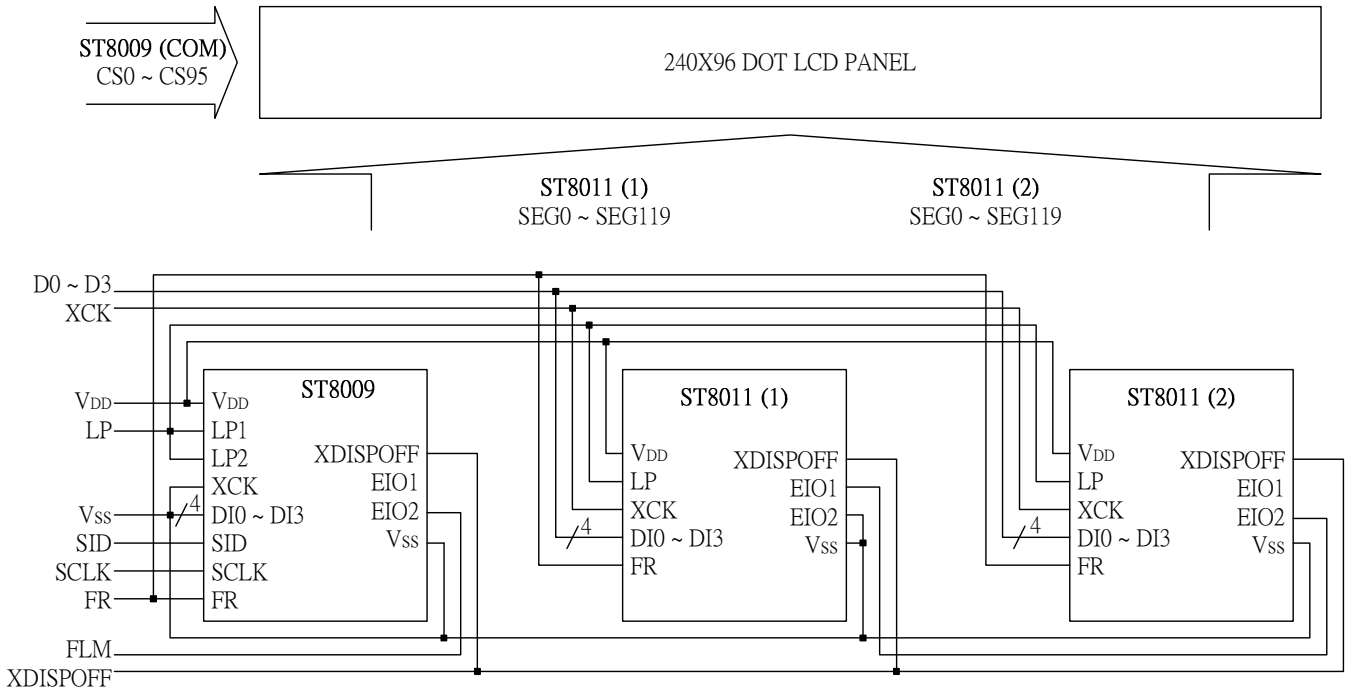


16. Application Circuit

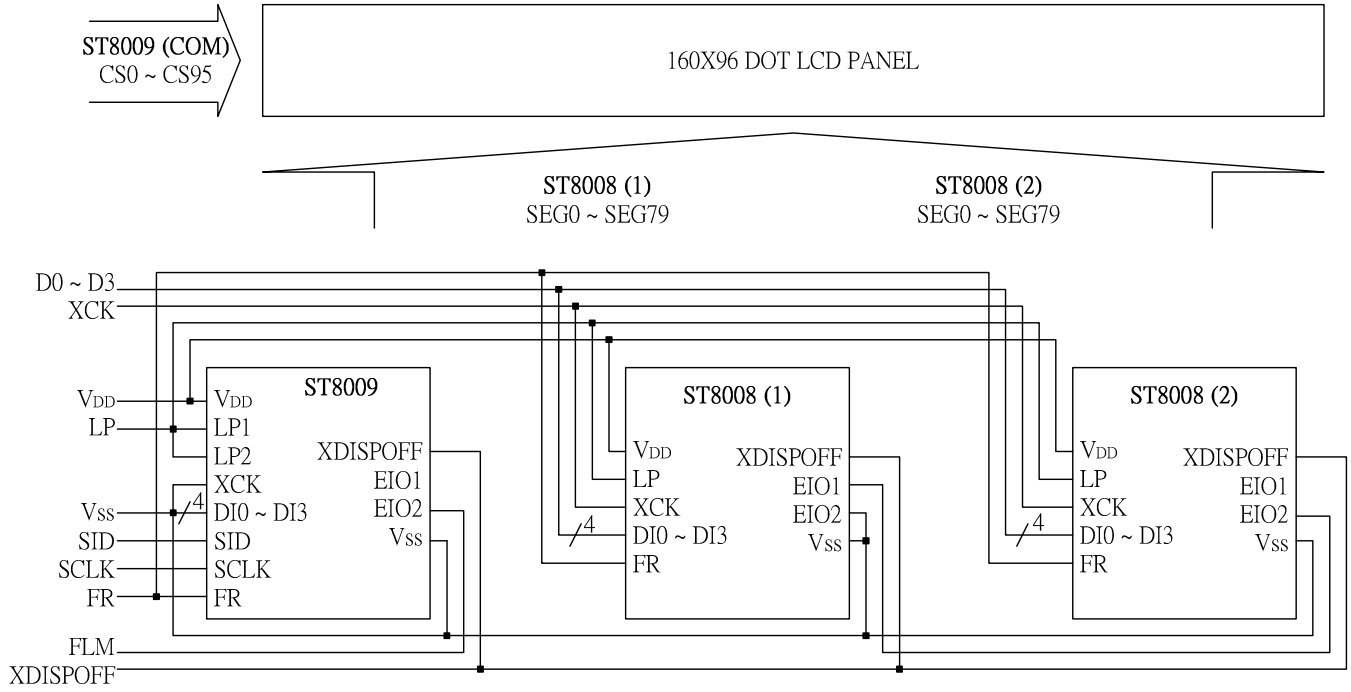
(a) When only use one ST8009 in mix mode (64X32)



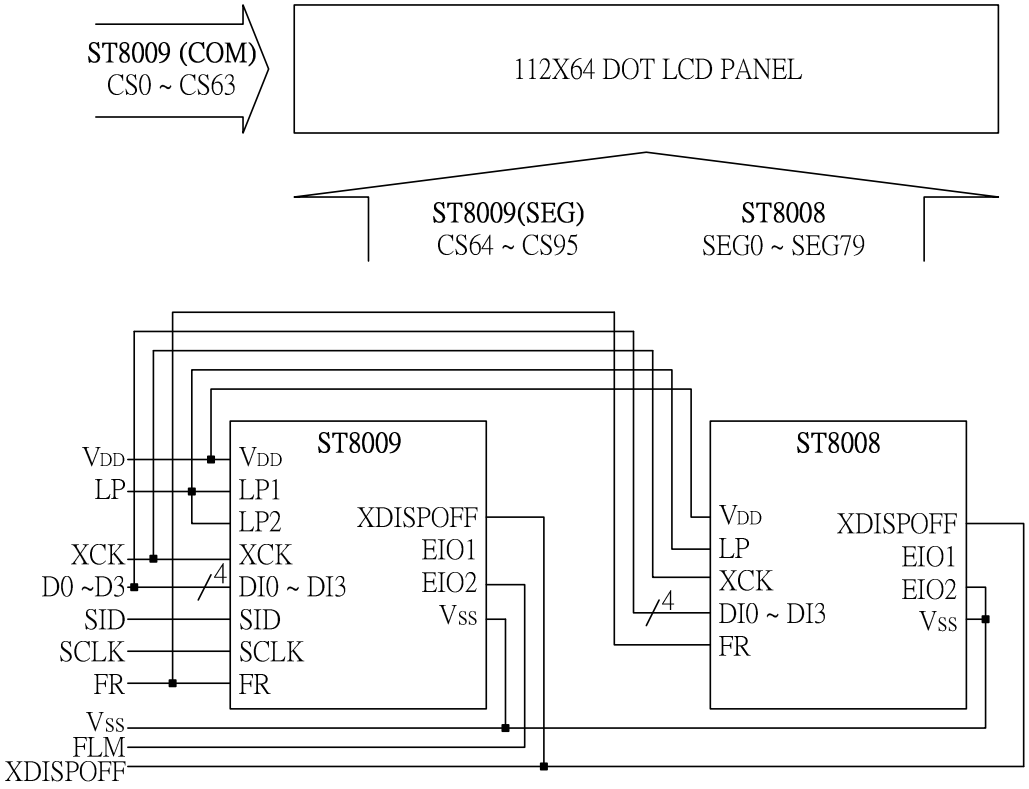
(b) When use one ST8009 and two ST8011 (240X96)



(c) When use one ST8009 and two ST8008 (160X96)



(d) When use one ST8009 and one ST8008 (112X64)



ST8009 Serial Specification Revision History

ST8009 Serial Specification Revision History		
Version	**Date**	**Description**
0.0	**2003/12/25**	**Preliminary version**
0.1	**2004/1/28**	**Modify registers**
0.2	**2004/3/11**	**Modify registers**
0.3	**2004/4/5**	**Add application timing block disgram**
0.4	**2004/5/20**	**Add initial flow**
0.5	**2004/09/08**	**Define timing of segment Mode. P41~P44**
0.6	**2005/02/14**	**Revise graph of ST8008,ST8011(SID, SCLK)**
0.7	**2005/04/19**	**Modify stand-by current to 5uA (max)**
1.0	**2005/05/12**	**New version update**
1.1	**2006/11/01**	**Fixing the XCS error in the fig.1**

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