Sitronix

ST8011

120 Output LCD Segment driver IC

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■ DESCRIPTION

The ST8011 is a 120-output segment driver IC suitable for driving small/medium scale dot matrix LCD panels, and is used in PDA or electronic dictionary . The ST8011 is good as a segment driver, and it can create a low power consuming, high-resolution LCD.

■ FEATURES

- Number of LCD drive outputs: 120
- Supply voltage for LCD drive: Max +16V
- Supply voltage for the logic system: +2.5 to +5.5 V
- Low power consumption
- Package: 136-pin COB.

(Segment mode)

- Shift clock frequency
  - 20 MHz (MAX.): V_{DD} = +5.0 ± 0.5 V
  - 15 MHz (MAX.): V_{DD} = +3.0 to + 4.5 V
  - 12 MHz (MAX.): V_{DD} = +2.5 to + 3.0 V
- Adopts a data bus system
- 4-bit parallel / serial input modes are selectable with a mode (P/S) pin
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 120 bits of input data
- Line latch circuits are reset when XDISPOFF active

■ ST8011 Serial Specification Revision History

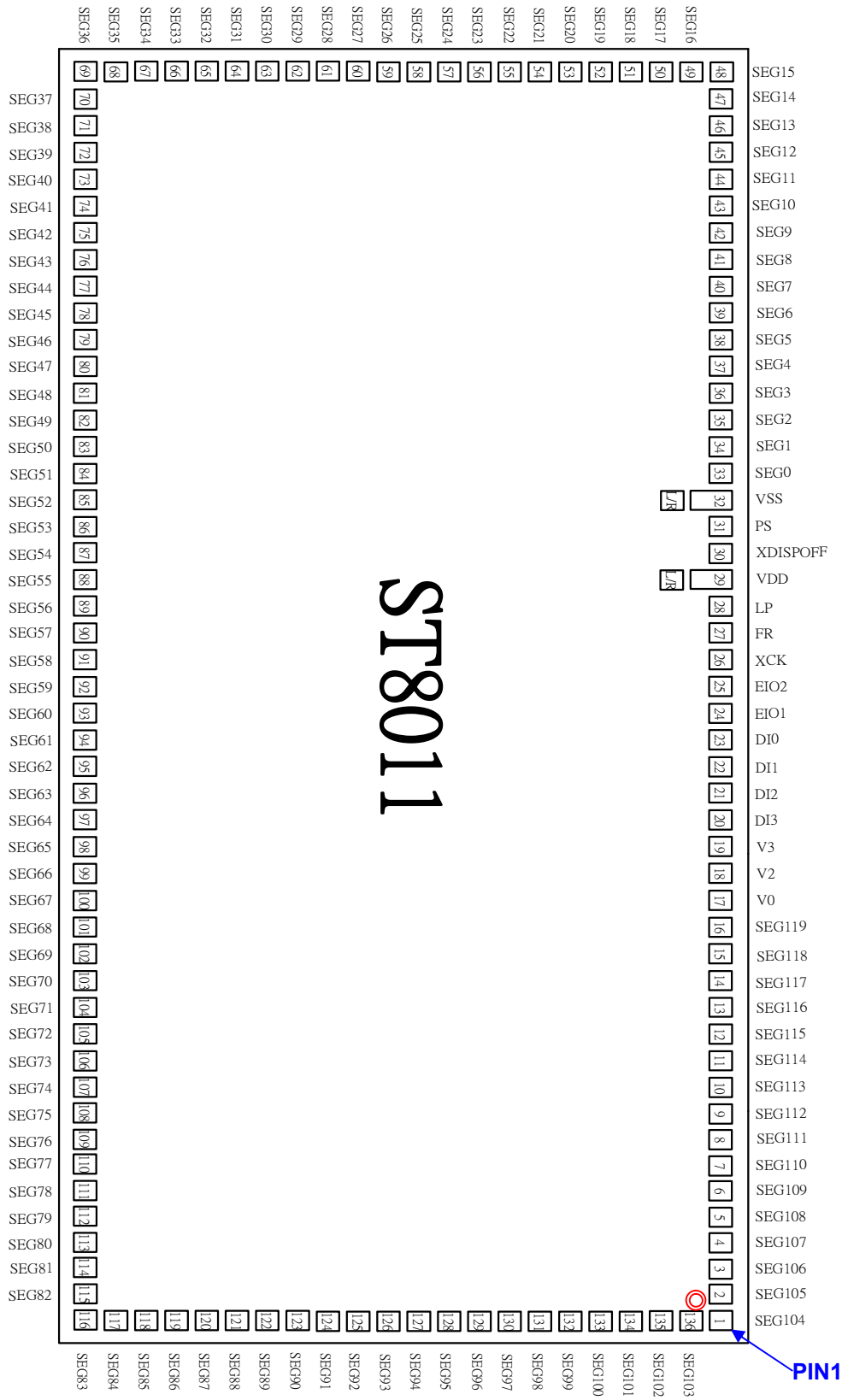
ST8011 Serial Specification Revision History		
Version	**Date**	**Description**
0.0B	2002/10/14	Preliminary version
1.0	2003/07/28	Final Version
1.1	2003/11/12	Modify the pin pitch
1.2	2004/04/05	Add application timing block diagram
1.3	2004/09/08	Define timing(t_{LSW}) of Segment Mode. P17~P19

■ Pad Arrangement

Chip size: 4860(μm) × 2220(μm)

Pad size: 80(μm) × 80(μm)

Pin Pitch: 100~110 μm



Substrate Connect to Vss.

Pad Location Coordinates

Pad.No	Function	X	Y
1	SEG104	2385.00	1065.00
2	SEG105	2265.00	1065.00
3	SEG106	2155.00	1065.00
4	SEG107	2050.00	1065.00
5	SEG108	1950.00	1065.00
6	SEG109	1850.00	1065.00
7	SEG110	1750.00	1065.00
8	SEG111	1650.00	1065.00
9	SEG112	1550.00	1065.00
10	SEG113	1450.00	1065.00
11	SEG114	1350.00	1065.00
12	SEG115	1250.00	1065.00
13	SEG116	1150.00	1065.00
14	SEG117	1050.00	1065.00
15	SEG118	950.00	1065.00
16	SEG119	850.00	1065.00
17	V0	750.00	1065.00
18	V2	650.00	1065.00
19	V3	550.00	1065.00
20	DI3	450.00	1065.00
21	DI2	350.00	1065.00
22	DI1	250.00	1065.00
23	DI0	150.00	1065.00
24	EIO1	50.00	1065.00
25	EIO2	-50.00	1065.00
26	XCK	-150.00	1065.00
27	FR	-250.00	1065.00
28	LP	-350.00	1065.00
29	VDD	-450.00	1065.00
30	XDISPOFF	-550.00	1065.00
31	PS	-650.00	1065.00
32	VSS	-750.00	1065.00
33	SEG0	-850.00	1065.00
34	SEG1	-950.00	1065.00
35	SEG2	-1050.00	1065.00
36	SEG3	-1150.00	1065.00
37	SEG4	-1250.00	1065.00

Pad.No	Function	X	Y
69	SEG36	-2385.00	-1065.00
70	SEG37	-2265.00	-1065.00
71	SEG38	-2155.00	-1065.00
72	SEG39	-2050.00	-1065.00
73	SEG40	-1950.00	-1065.00
74	SEG41	-1850.00	-1065.00
75	SEG42	-1750.00	-1065.00
76	SEG43	-1650.00	-1065.00
77	SEG44	-1550.00	-1065.00
78	SEG45	-1450.00	-1065.00
79	SEG46	-1350.00	-1065.00
80	SEG47	-1250.00	-1065.00
81	SEG48	-1150.00	-1065.00
82	SEG49	-1050.00	-1065.00
83	SEG50	-950.00	-1065.00
84	SEG51	-850.00	-1065.00
85	SEG52	-750.00	-1065.00
86	SEG53	-650.00	-1065.00
87	SEG54	-550.00	-1065.00
88	SEG55	-450.00	-1065.00
89	SEG56	-350.00	-1065.00
90	SEG57	-250.00	-1065.00
91	SEG58	-150.00	-1065.00
92	SEG59	-50.00	-1065.00
93	SEG60	50.00	-1065.00
94	SEG61	150.00	-1065.00
95	SEG62	250.00	-1065.00
96	SEG63	350.00	-1065.00
97	SEG64	450.00	-1065.00
98	SEG65	550.00	-1065.00
99	SEG66	650.00	-1065.00
100	SEG67	750.00	-1065.00
101	SEG68	850.00	-1065.00
102	SEG69	950.00	-1065.00
103	SEG70	1050.00	-1065.00
104	SEG71	1150.00	-1065.00
105	SEG72	1250.00	-1065.00

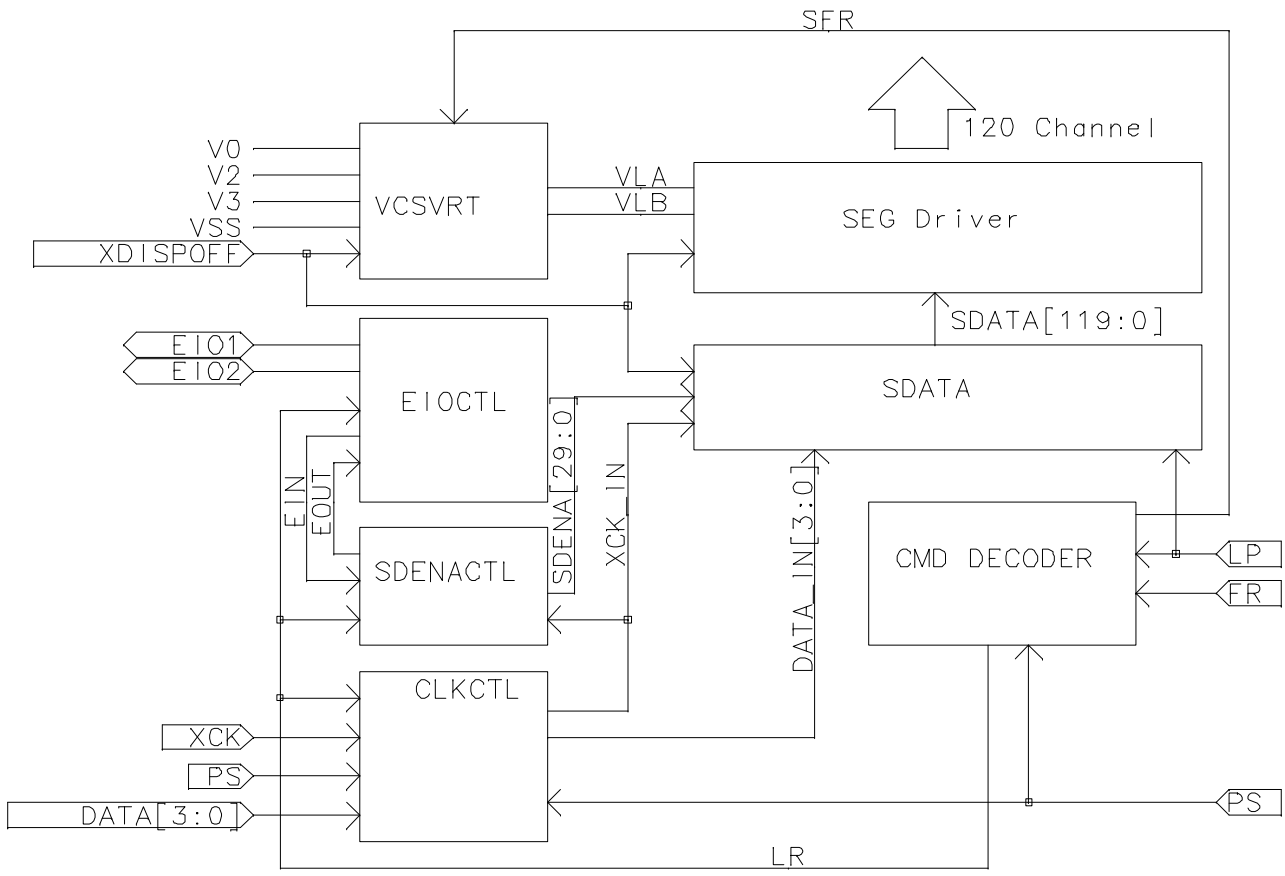
Pad.No	Function	X	Y
38	SEG5	-1350.00	1065.00
39	SEG6	-1450.00	1065.00
40	SEG7	-1550.00	1065.00
41	SEG8	-1650.00	1065.00
42	SEG9	-1750.00	1065.00
43	SEG10	-1850.00	1065.00
44	SEG11	-1950.00	1065.00
45	SEG12	-2050.00	1065.00
46	SEG13	-2155.00	1065.00
47	SEG14	-2265.00	1065.00
48	SEG15	-2385.00	1065.00
49	SEG16	-2385.00	955.00
50	SEG17	-2385.00	850.00
51	SEG18	-2385.00	750.00
52	SEG19	-2385.00	650.00
53	SEG20	-2385.00	550.00
54	SEG21	-2385.00	450.00
55	SEG22	-2385.00	350.00
56	SEG23	-2385.00	250.00
57	SEG24	-2385.00	150.00
58	SEG25	-2385.00	50.00
59	SEG26	-2385.00	-50.00
60	SEG27	-2385.00	-150.00
61	SEG28	-2385.00	-250.00
62	SEG29	-2385.00	-350.00
63	SEG30	-2385.00	-450.00
64	SEG31	-2385.00	-550.00
65	SEG32	-2385.00	-650.00
66	SEG33	-2385.00	-750.00
67	SEG34	-2385.00	-850.00
68	SEG35	-2385.00	-955.00

Pad.No	Function	X	Y
106	SEG73	1350.00	-1065.00
107	SEG74	1450.00	-1065.00
108	SEG75	1550.00	-1065.00
109	SEG76	1650.00	-1065.00
110	SEG77	1750.00	-1065.00
111	SEG78	1850.00	-1065.00
112	SEG79	1950.00	-1065.00
113	SEG80	2050.00	-1065.00
114	SEG81	2155.00	-1065.00
115	SEG82	2265.00	-1065.00
116	SEG83	2385.00	-1065.00
117	SEG84	2385.00	-955.00
118	SEG85	2385.00	-850.00
119	SEG86	2385.00	-750.00
120	SEG87	2385.00	-650.00
121	SEG88	2385.00	-550.00
122	SEG89	2385.00	-450.00
123	SEG90	2385.00	-350.00
124	SEG91	2385.00	-250.00
125	SEG92	2385.00	-150.00
126	SEG93	2385.00	-50.00
127	SEG94	2385.00	50.00
128	SEG95	2385.00	150.00
129	SEG96	2385.00	250.00
130	SEG97	2385.00	350.00
131	SEG98	2385.00	450.00
132	SEG99	2385.00	550.00
133	SEG100	2385.00	650.00
134	SEG101	2385.00	750.00
135	SEG102	2385.00	850.00
136	SEG103	2385.00	955.00

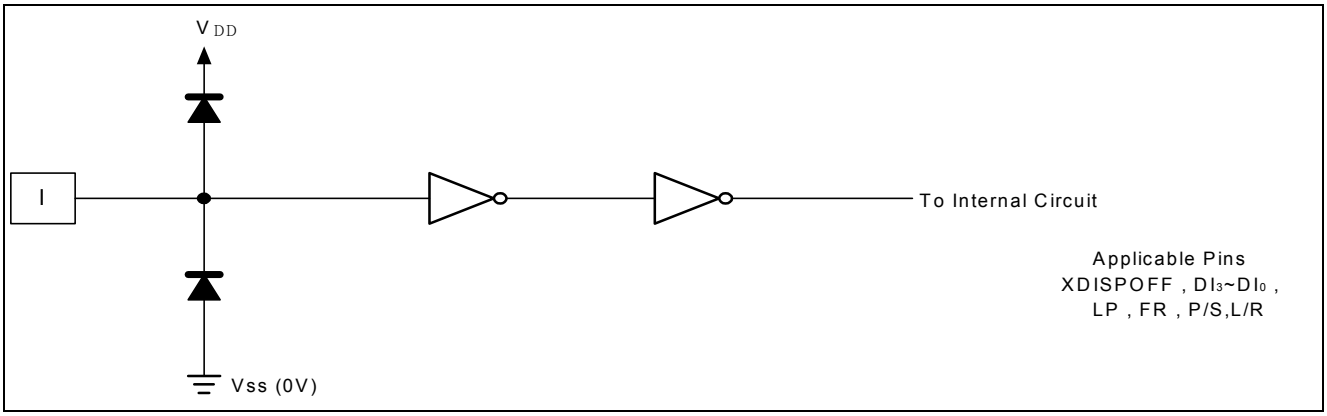
PIN DESCRIPTION

SYMBOL	I/O	DESCRIPTION	No of Num
SEG0-SEG119	O	LCD drive output	120
V0,V2,V3	P	Power supply for LCD drive	3
XDISPOFF	I	Control input for output of non-select level	1
VDD	P	Power supply for logic system (+2.5 to +5.5 V)	1
EIO2, EIO1	I/O	Input/output for chip selection at segment mode and FLM input output function at com/seg mix mode or common mode	2
DI0-DI3	I	Display data input at segment mode	4
XCK	I	Clock input for taking display data at segment mode	1
L/R	I	Display data shift direction selection	
LP	I	Latch pulse input for display data at segment mode/ Shift clock input for shift register at common mode	1
FR	I	AC-converting signal input for LCD drive waveform	1
P/S	I	This is the parallel data input/serial data input switch terminal. P/S="H": Parallel data input. P/S="L": Serial data input.	1
VSS	P	Ground (0 V)	1

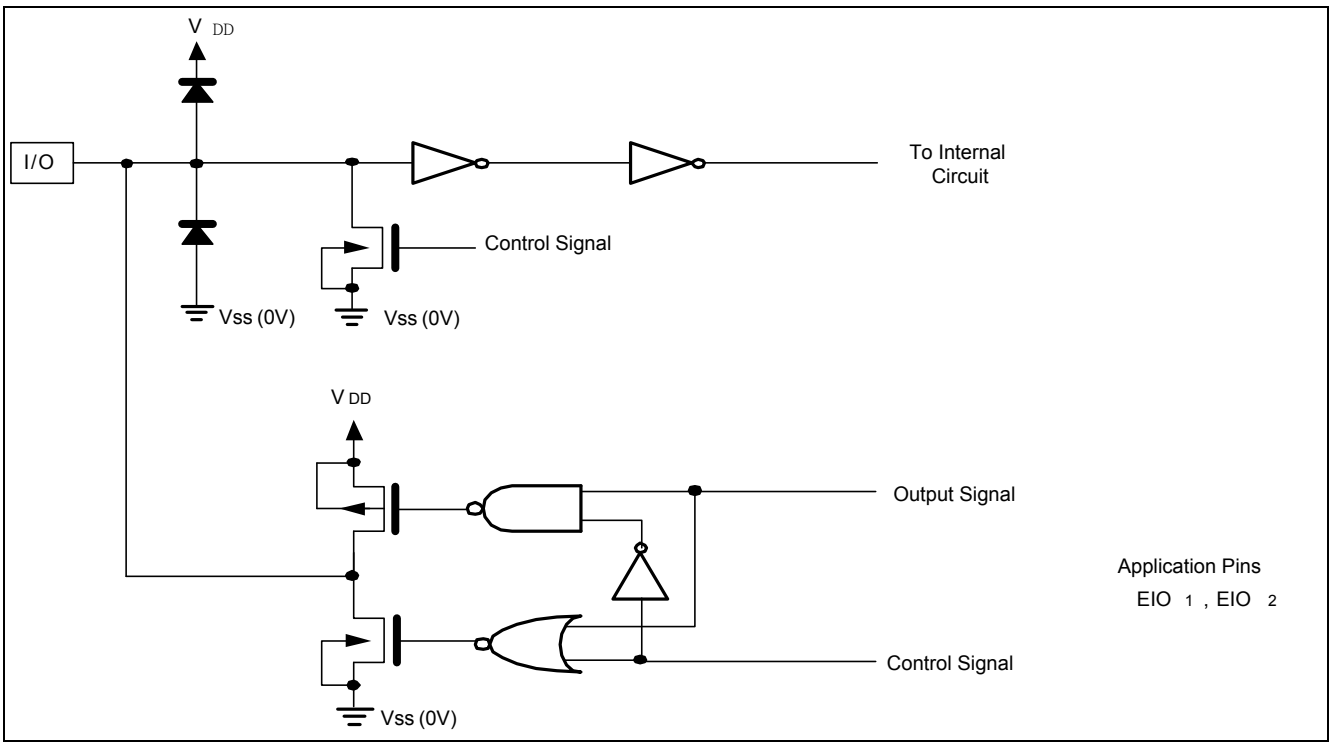
■ BLOCK DIAGRAM



■ INPUT/OUTPUT CIRCUITS



Input Circuit



Input/Output Circuit

■ FUNCTIONAL DESCRIPTION

◆ Pin Functions

SYMBOL	FUNCTION
VDD	Logic system power supply pin, connected to +2.5 to +5.5 V.
VSS	Ground pin, connected to 0 V.
V0 V2 V3	This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on VSS, and must maintain the relative magnitudes shown below. • V0 ≧V2 ≧V3≧Vss
DI3-DI0	Input pins for display data • In 4-bit parallel input mode, input data into the 4 pins, DI3-DI0. • In serial input mode, input data into the 1 pin DI0. Connect DI3-DI1 to VSS or VDD • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
XCK	Clock input pin for taking display data * Data is read at the falling edge of the clock pulse.
LP	Latch pulse input pin for display data • Data is latched at the falling edge of the clock pulse.
XDISPOFF	Control input pin for output of non-select level • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to VSS level "L", the LCD drive output pins (SEG0-SEG119) are set to level Vss. • When set to "L", the contents of the line latch are reset, but the display data are read in the data latch regardless of the condition of /DISPOFF. When the XDISPOFF function is canceled, the driver outputs non-select level (V2 or V3), then outputs the contents of the data latch at the next falling edge of the LP. At that time, if XDISPOFF removal time does not correspond to what is shown in AC characteristics, it cannot output the reading data correctly. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
FR	AC signal input pin for LCD drive waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
P/S	Interface Mode selection pin • When P/S is “H” then parallel data input mode.

	When P/S is “L” the serial data input mode,
L/R	Input pin for selecting the reading direction of display data. **Default value is LOW** • When set to V_{SS} level "L", data is read sequentially from SEG_{119} to SEG_0. • When set to V_{DD} level "H", data is read sequentially from SEG_0 to SEG_{119}. • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
EIO1, EIO2	Input/output pins for chip selection. AT segment mode: • When L/R input is at VSS level "L", EIO1 is set for output, and EIO2 is set for input(connect to Vss). • When L/R input is at VDD level "H", EIO1 is set for input(connect to Vss), and EIO2 is set for output. • During output, set to "H" while LP • XCK is "H" and after 120 bits of data have been read, set to "L” for one cycle (from falling edge to failing edge of XCK), after which it returns to "H". During input, the chip is selected while EI is set to "L" after the LP signal is input. The chip is non-selected after 120 bits of data have been read.
SEG0–SEG119	LCD drive output pins • Corresponding directly to each bit of the data latch, one level (V0, V2, V3, and Vss) is selected and output. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.

◆ Functional Operations

FR	LATCH DATA	/DISPOFF	LCD DRIVE OUTPUT VOLTAGE LEVEL (SEG0-SEG119)
L	L	H	V3
L	H	H	Vss
H	L	H	V2
H	H	H	V0
X	X	L	Vss

TRUTH TABLE

NOTES:

- L : VSS (0 V), H : VDD (+2.5 to +5.5 V),
- "Don't care" should be fixed to "H" or "L", avoiding floating.

There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver. Supply regular voltage that is assigned by specification for each power pin.

◆ RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS

(A) 4-bit Parallel Input Mode

L/R	EIO1	EIO2	DATA INPUT	NUMBER OF CLOCKS						
				30 CLOCK	29 CLOCK	28 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
L	Output	Input	DI0	SEG0	SEG4	SEG8	…	SEG108	SEG112	SEG116
			DI1	SEG1	SEG5	SEG9	…	SEG109	SEG113	SEG117
			DI2	SEG2	SEG6	SEG10	…	SEG110	SEG114	SEG118
			DI3	SEG3	SEG7	SEG11	…	SEG111	SEG115	SEG119
H	Input	Output	DI0	SEG119	SEG115	SEG111	…	SEG11	SEG7	SEG3
			DI1	SEG118	SEG114	SEG110	…	SEG10	SEG6	SEG2
			DI2	SEG117	SEG113	SEG109	…	SEG9	SEG5	SEG1
			DI3	SEG116	SEG112	SEG108	…	SEG8	SEG4	SEG0

(B) Serial Input Mode

L/R	EIO1	EIO2	DATA INPUT	NUMBER OF CLOCKS						
				120 CLOCK	119 CLOCK	118 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
L	Output	Input	DI0	SEG0	SEG1	SEG2	…	SEG117	SEG118	SEG119
			DI1	X	X	X	X	X	X	X
			DI2	X	X	X	X	X	X	X
			DI3	X	X	X	X	X	X	X
H	Input	Output	DI0	SEG119	SEG118	SEG117	…	SEG2	SEG1	SEG0
			DI1	X	X	X	X	X	X	X
			DI2	X	X	X	X	X	X	X
			DI3	X	X	X	X	X	X	X

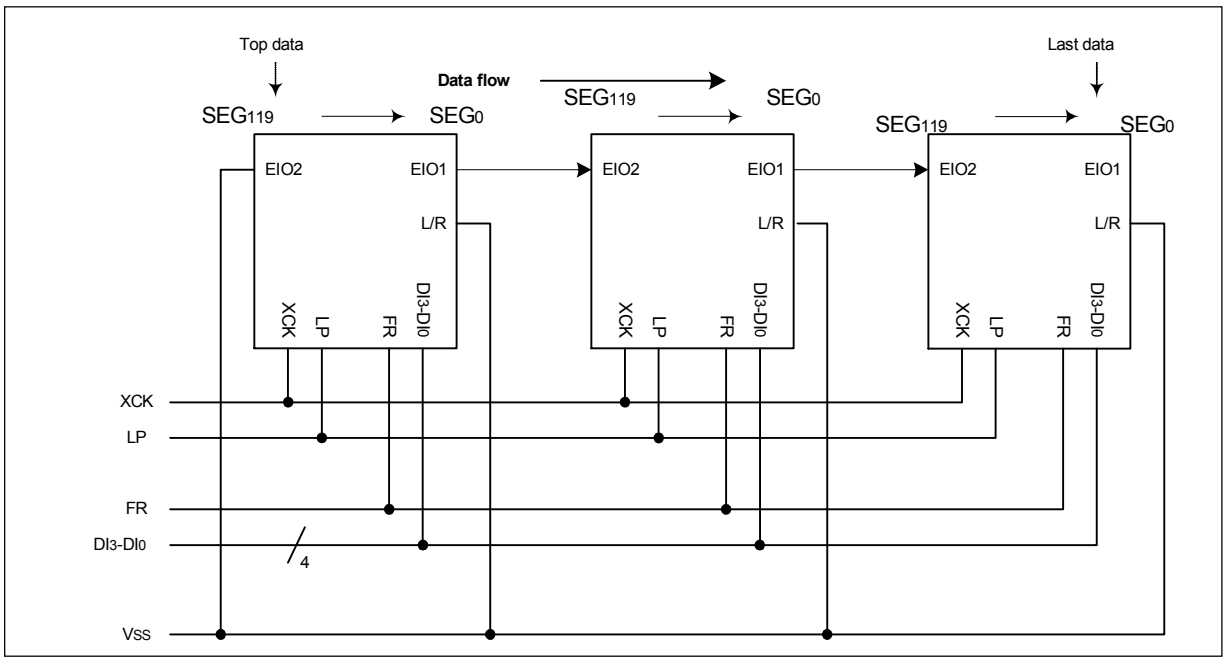
NOTES:

- L : VSS (0 V), H : VDD (+2.5 to +5.5 V), X : Don't care

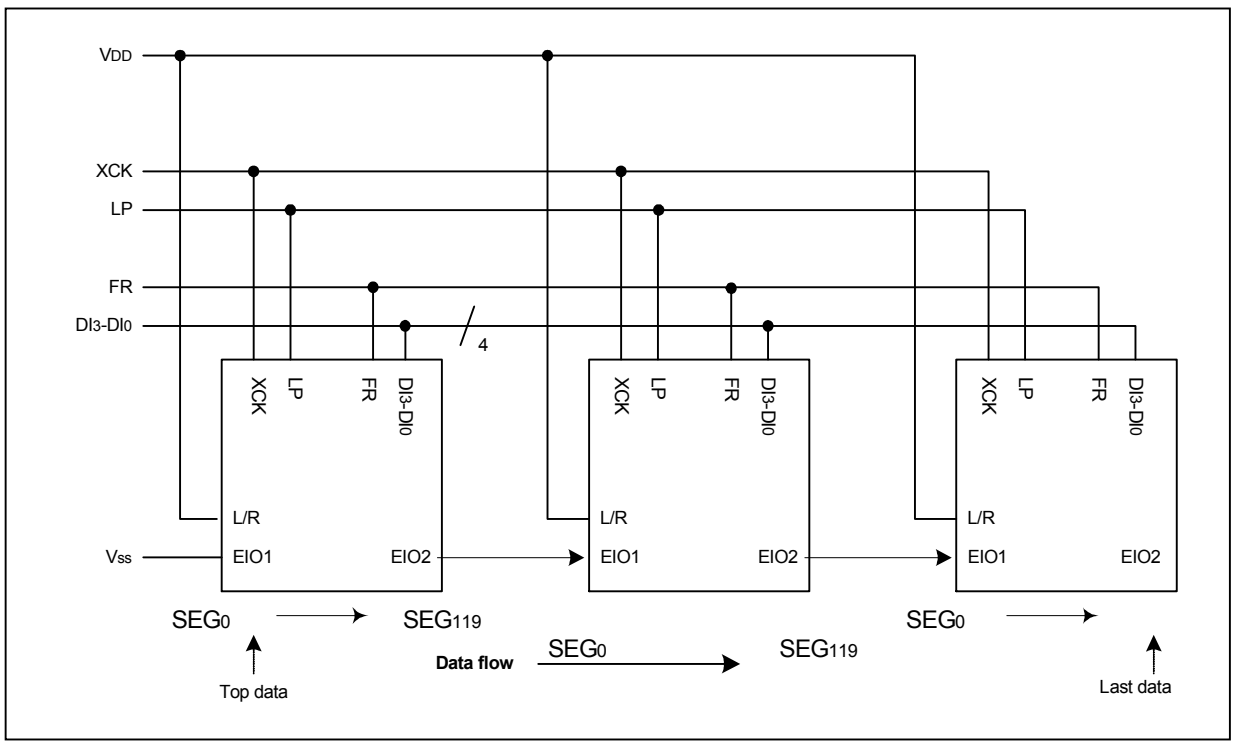
  "Don't care" should be fixed to "H" or "L", avoiding floating.

◆ Connection examples of plural segment drivers

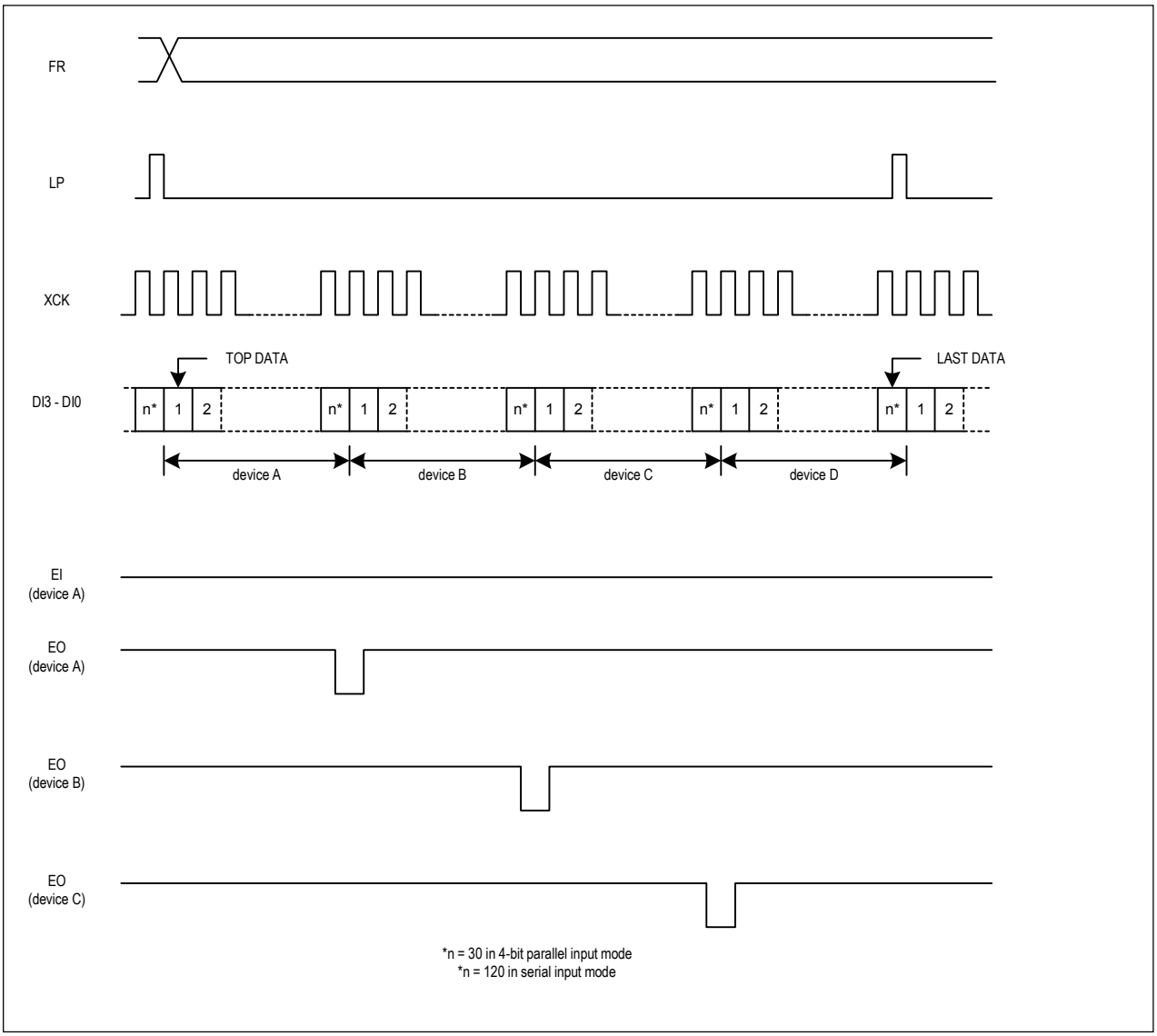
(A) When L/R = "L"



(B) When L/R = "H"



◆ Timing chart of 4-device cascade connection of segment drivers



◆ PRECAUTIONS

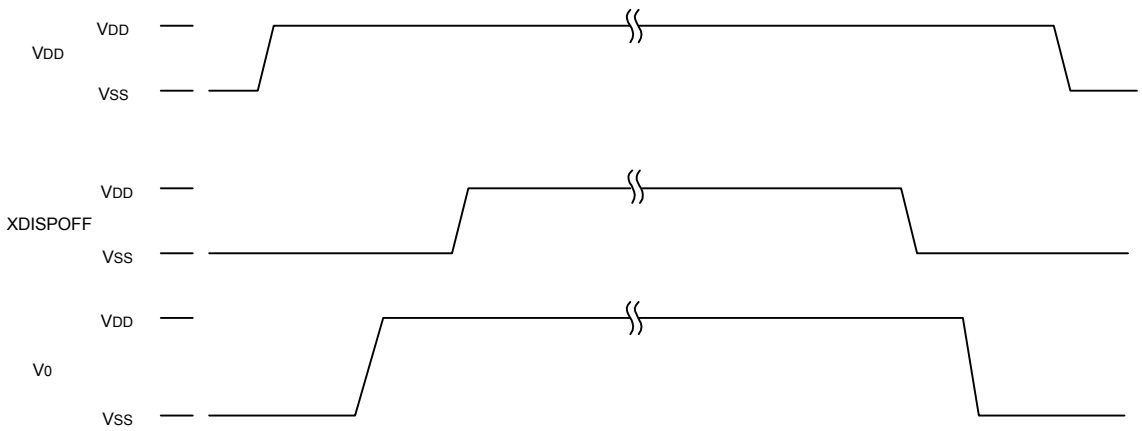
Precautions when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so a high current that may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating may permanently damage it. The details are as follows,

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power

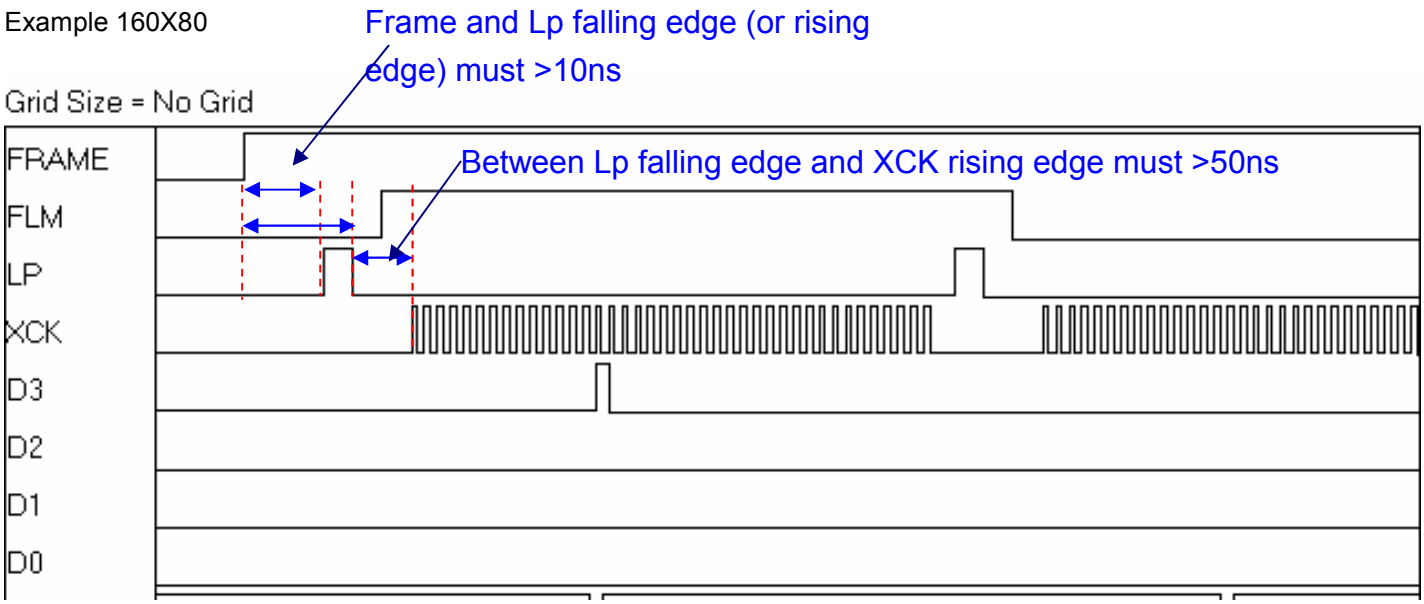
And when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on XDISPOFF function. After that, cancel the XDISPOFF function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level Vss on XDISPOFF function. Then disconnect the logic system power after disconnecting the LCD drive power.

When connecting the power supply, follow the recommended sequence shown here

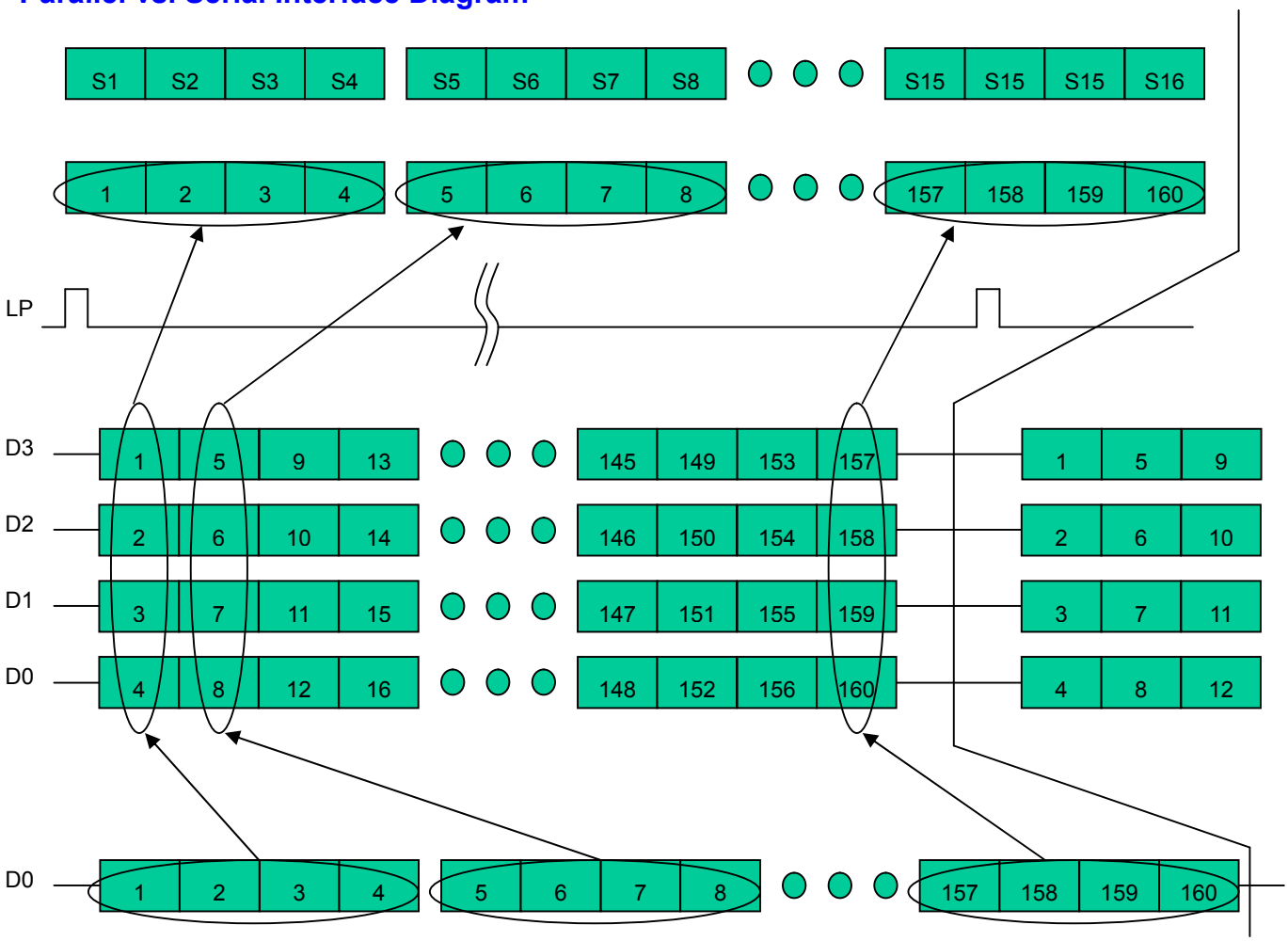


Application Timing Block:

Example 160X80



Parallel vs. Serial Interface Diagram



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	-0.3~+7.0	V	1,2
	V_2	V_2	V_{DD}-10~ V_{DD}+0.3		
	V_3	V_3	-0.3~V_{5S}+10	V	
Input voltage	V_I	$D1_4$-DI_0, XCK, LP, L/R, FR, EIO_1, EIO_2, XDISPOFF	-0.3 to V_{DD}+0.3	V	
Storage temperature	T_{STG}		-45 to +125	°C	

NOTES:

1. TA = +25 °C
2. The maximum applicable voltage on any pin with respect to V_{SS} (0 V).

■ RECOMMENDED OPERATING Conditions

PARAMETER	SYMBOL	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage (1)	VDD	VDD	+2.5		+5.5	V	1, 2
Supply voltage (2)	V0	V0	+6.0		+16.0	V	
Operating temperature	TOPR		-20		+85	°C	

NOTES:

1. The applicable voltage on any pin with respect to V_{SS} (0 V).
2. Ensure that voltages are set such that V2 ≧V3 ≧VSS.

■ ELECTRICAL CHARACTERISTICS

◆ DC Characteristics

(V_{SS} = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = + 6.0 to +15.0 V, T_{OPR} = -20 to +85°C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	VIL		DI3-DI0, XCK, LP, L/R FR, EIO1, EIO2, XDISPOFF			0.2VDD	V	
Input "High" voltage	VIH			0.8VDD			V	
Output "Low" voltage	VOL	IOL = +0.4 mA	EIO1, EIO2			+0.4	V	
Output "High" voltage	VOH	IOH = -0.4 mA		VDD-0.4			V	
Input leakage current	ILIL	VI = VSS	DI3-DI0, XCK, LP, LIR, FR, EIO1, EIO2, XDISPOFF			-10	μA	
	ILIH	VI = VDD				+10	μA	
Output resistance	RON	|ΔVON| =0.5V, V0 = 30 V	SEG0-SEG119		1.5	2.0	kΩ	
Standby current	ISTB		VSS			50	μA	1
Supply current (1) (Non-selection)	ISS		VSS			2.0	mA	2
Supply current (2)	I0		V0			0.9	mA	4

NOTES:

1. V_{DD} = +3.0 V, V_0 = +12.0 V
2. V_{DD} = +3.0 V, V_0 = +12.0 V, f_{XCK} = 8 MHz, no-load, EI = V_{DD}. The input data is turned over by data taking clock (4-bit parallel input mode).
3. V_{DD} = +3.0 V, V_0 = +12.0 V, f_{XCK} = 8 MHz, no-load, EI = V_{SS}. The input data is turned over by data taking clock (4-bit parallel input mode).
4. V_{DD} = +3.0 V, V_0 = +12.0 V, f_{XCK} = 8MHz, f_{LP} = 19.2 kHz, f_{FR} = 80 Hz, no-load. The input data is turned over by data taking clock (4-bit parallel input mode).

◆ AC Characteristics

(V_{SS} = 0 V, V_{DD} = +2.5 to +3.0 V, V_0 = + 6.0 to +15.0 V, T_{OPR} = -20 10+85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R,t_F ≤ 11ns	125			ns	1
Shift clock "H" pulse width	t_{WCKH}		51			ns	
Shift clock "L" pulse width	t_{WCKL}		51			ns	
Data setup time	t_{DS}		30			ns	
Data hold time	t_{DH}		40			ns	
Latch pulse "H" pulse width	t_{WLPH}		51			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		51			ns	
Latch pulse rise to shift clock rise time	t_{LS}		51			ns	
Latch pulse fall to shift clock fall time	t_{LH}		51			ns	
Latch pulse fall to shift clock rise time	t_{LSW}		50			ns	
Enable setup time	t_S		36			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			78	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

NOTES:
1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(V_{SS} = 0 V, V_{DD} = +5.0±0.5 V, V_0 = + 6.0 to +15.0 V, T_{OPR} = -20 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	tR,tF ≤ 10ns	66			ns	1
Shift clock "H" pulse width	t_{WCKH}		23			ns	
Shift clock "L" pulse width	t_{WCKL}		23			ns	
Data setup time	t_{DS}		15			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		50			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Latch pulse fall to shift clock rise time	t_{LSW}		50			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			41	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

NOTES:
1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

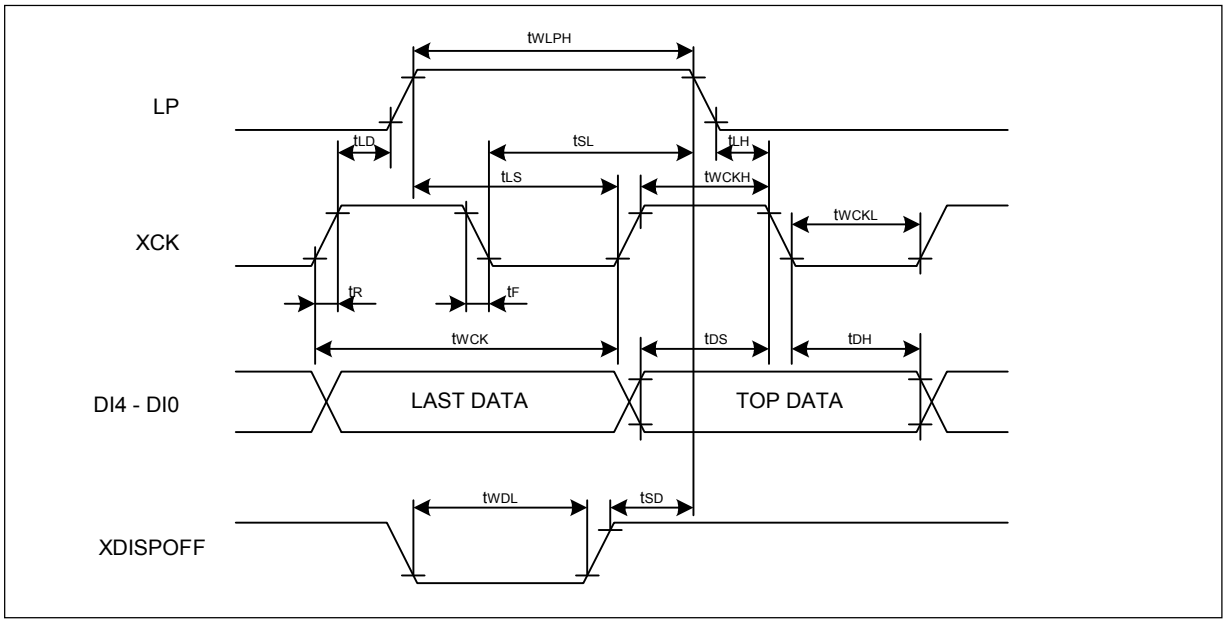
(V_{SS} = 0 V, V_{DD} = +3.0 to +4.5 V, V_0 = + 6.0 to +15.0 V, T_{OPR} = -20 10+85 °C)

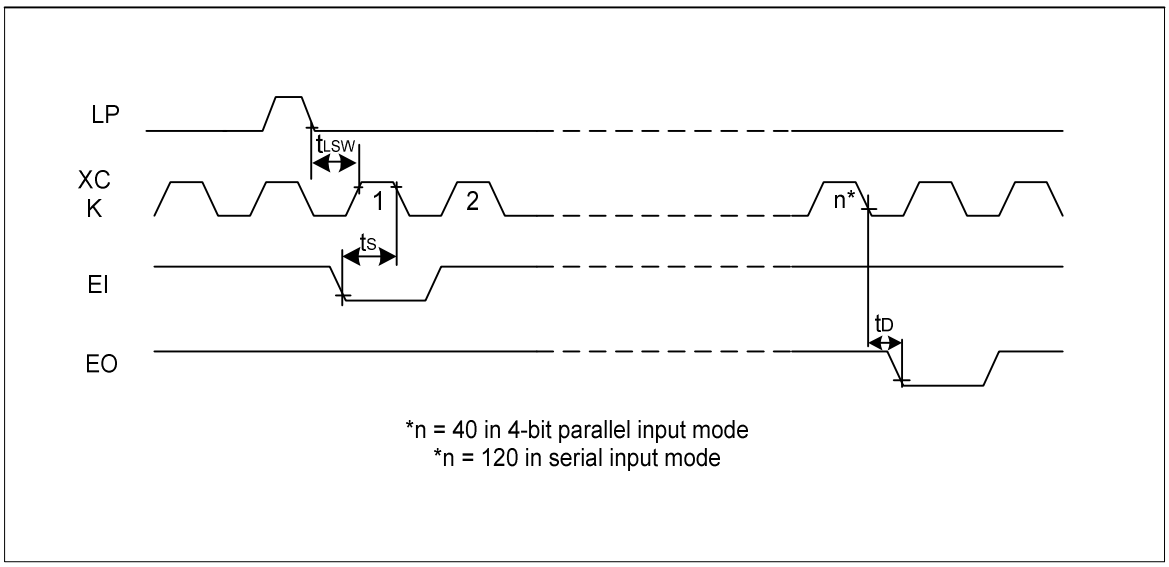
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R,t_F ≤ 10ns	82			ns	1
Shift clock "H" pulse width	t_{WCKH}		28			ns	
Shift clock "L" pulse width	t_{WCKL}		28			ns	
Data setup time	t_{DS}		20			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		51			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Latch pulse fall to shift clock rise time	t_{LSW}		50			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			57	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

NOTES:

1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

◆ Timing Chart of Segment Mode





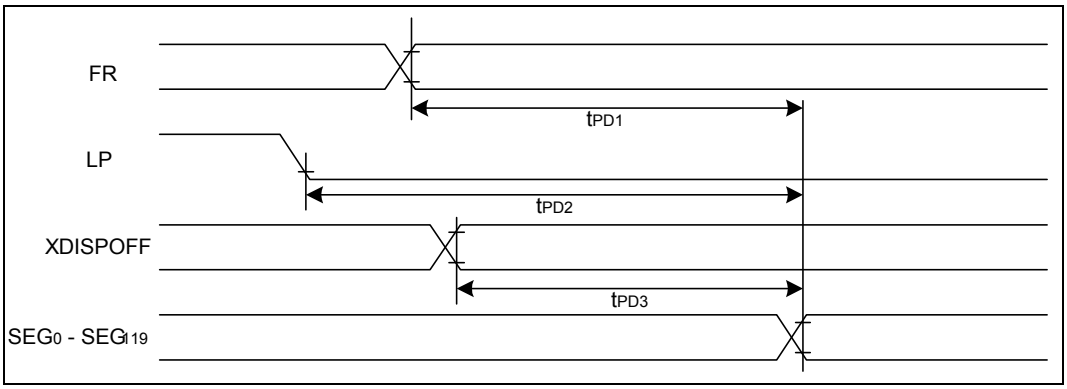


Fig. 8 Timing Characteristics (3)