Sitronix

ST8016

160 Output LCD Common/ Segment Driver IC

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Datasheet

Version 1.9

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Sitronix Technology Corporation

1 FEATURES

- Number of LCD drive outputs: 160
- Supply voltage for LCD drive: +15.0 to +30.0 V
- Supply voltage for the logic system: +2.5 to +5.5 V
- Low power consumption
- Low output impedance

(Segment mode)

- Shift clock frequency
  - 20 MHz (MAX.): V_{DD} = +5.0 ± 0.5 V
  - 12 MHz (MAX.): V_{DD} = +3.0 to + 4.5 V
  - 8 MHz (MAX.): V_{DD} = +2.5 to + 3.0 V
- Adopts a data bus system
- 4-bit/8-bit parallel input modes are selectable with a mode (MD) pin
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 160 bits of input data
- Line latch circuits are reset when /DISPOFF active

(Common mode)

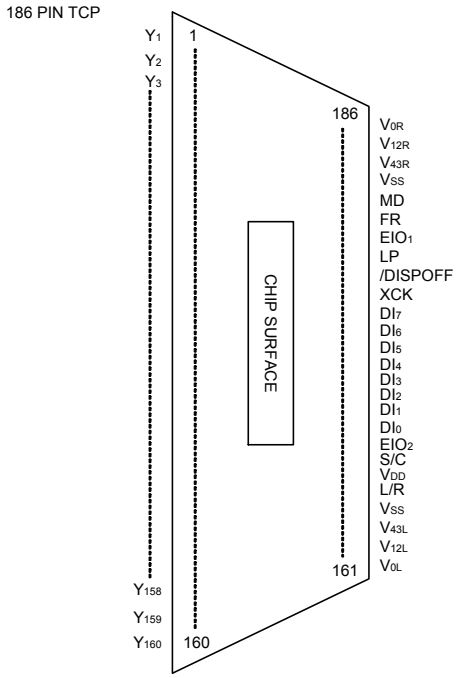
- Shift clock frequency: 4 MHz (MAX.)
- Built-in 160-bit bi-directional shift register (divisible into 80 bits x 2)
- Available in a single mode (160-bit shift register) or in a dual mode (80-bit shift register x 2)
  - Y_1->Y_{160} Single mode
  - Y_{160}->Y_1 Single mode
  - Y_1->Y_{80}, Y_{81}->Y_{160} Dual mode
  - Y_{160}->Y_{81}, Y_{80}->Y_1 Dual mode

  The above 4 shift directions are pin-selectable
- Shift register circuits are reset when /DISPOFF active

2 DESCRIPTION

The ST8016 is a 160-output segment/common driver IC suitable for driving large/medium scale dot matrix LCD panels, and is used in personal computers/work stations. Through the use of SST (Super Slim TCP) technology, it is ideal for substantially decreasing the size of the frame section of the LCD module. The ST8016 is good both as a segment driver and a common driver, and it can create a low power consuming, high-resolution LCD.

3 PIN CONNECTIONS



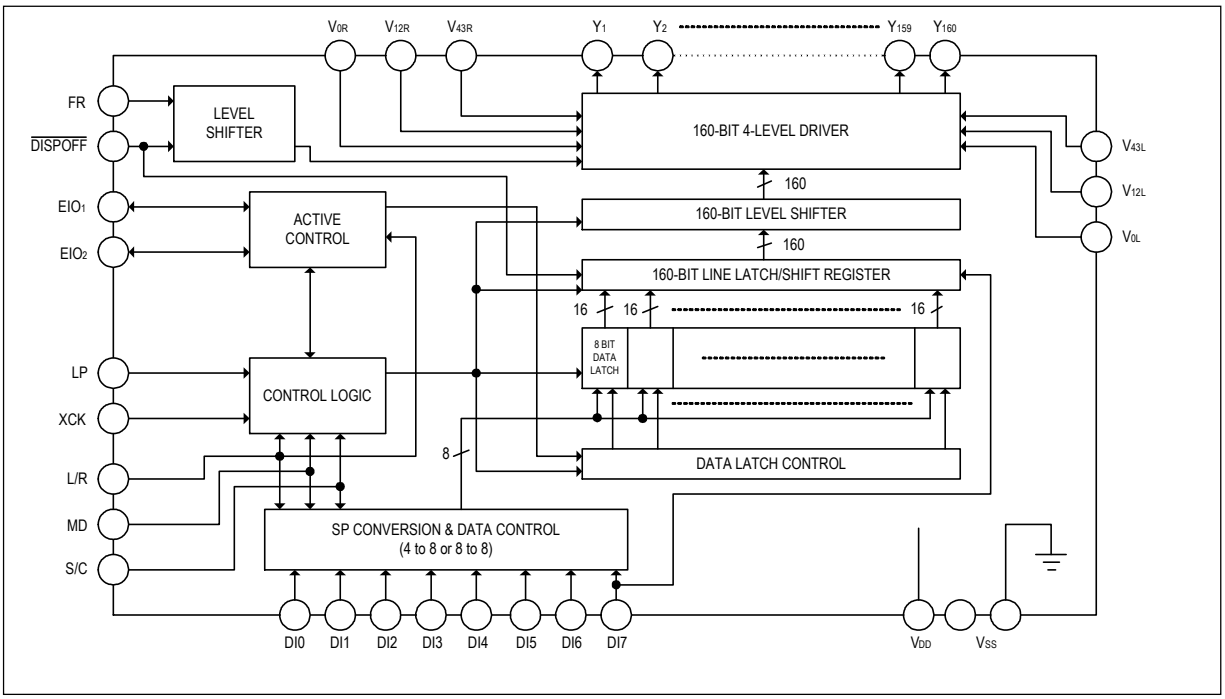
Package: 186-pin TCP (Tape Carrier Package)

4 PIN DESCRIPTION (TCP)

PIN NO.	SYMBOL	I/O	DESCRIPTION
1 ~ 160	Y_1-Y_{160}	O	LCD drive output
161,186	V_{0L}, V_{0R}	P	Power supply for LCD drive
162,185	V_{12L}, V_{12R}	P	Power supply for LCD drive
163,184	V_{43L}, V_{43R}	P	Power supply for LCD drive
165	L/R	I	Display data shift direction selection
166	V_{DD}	P	Power supply for logic system (+2.5 to +5.5 V)
167	S/C	I	Segment mode/common mode selection
168,180	EIO_2, EIO_1	I/O	Input/output for chip selection at segment mode Shift data input/output for shift register at common mode
169 ~ 175	DI_0-DI_6	I	Display data input at segment mode
176	DI_7	I	Display data input at segment mode/Dual mode data input at common mode
177	XCK	I	Clock input for taking display data at segment mode
178	/DISPOFF	I	Control input for output of non-select level
179	LP	I	Latch pulse input for display data at segment mode/ Shift clock input for shift register at common mode
181	FR	I	AC-converting signal input for LCD drive waveform
182	MD	I	Mode selection input
164,183	V_{SS}	P	Ground (0 V)

P: power pin

5 BLOCK DIAGRAM



6 FUNCTIONAL OPERATIONS OF EACH BLOCK

BLOCK	FUNCTION
Active Control	In case of segment mode, controls the selection or non-selection of the chip. Following an LP signal input, and after the chip selection signal is input, a selection signal is generated internally until 160 bits of data have been read in. Once data input has been completed, a selection signal for cascade connection is output, and the chip is non-selected. In case of common mode, controls the input/output data of bi-directional pins.
SP Conversion & Data Control	In case of segment mode, keeps input data which are 2 clocks of XCK at 4-bit parallel input mode in latch circuit, or keeps input data which are 1 clock of XCK at 8-bit parallel input mode in latch circuit; after that they are put on the internal data bus 8 bits at a time.
Data Latch Control	In case of segment mode, selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic. For every 16 bits of data read in, the selection signal shifts one bit based on the state of the control circuit.
Data Latch	In case of segment mode, latches the data on the data bus. The latch state of each LCD drive output pin is controlled by the control logic and the data latch control; 160 bits of data are read in 20 sets of 8 bits.
Line Latch/ Shift Register	In case of segment mode, all 160 bits which have been read into the data latch are simultaneously latched at the falling edge of the LP signal, and are output to the level shifter block. In case of common mode, shifts data from the data input pin at the falling edge of the LP signal.
Level Shifter	The logic voltage signal is level-shifted to the LCD drive voltage level, and is output to the driver block.
4-Level Driver	Drives the LCD drive output pins from the line latch/shift register data, and selects one of 4 levels (V0, V12, V43 or VSS) based on the S/C, FR and /DISPOFF signals.
Control Logic	Controls the operation of each block. In case of segment mode, when an LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission is controlled, 160 bits of data are read in, and the chip is non-selected. In case of common mode, controls the direction of data shift.

7 INPUT/ OUTPUT CIRCUITS

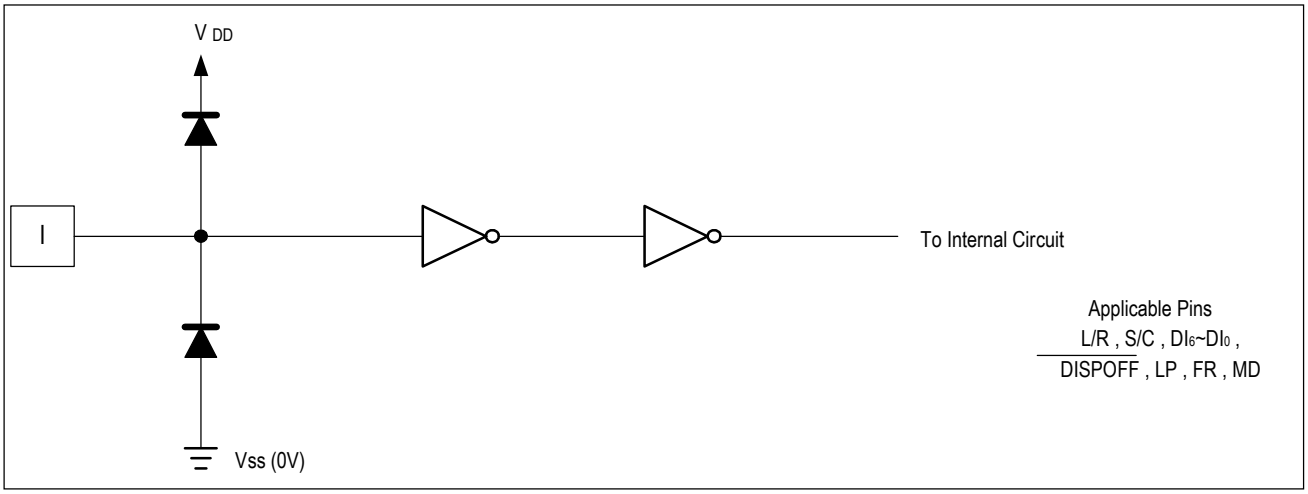


Figure 7-1 Input Circuit (1)

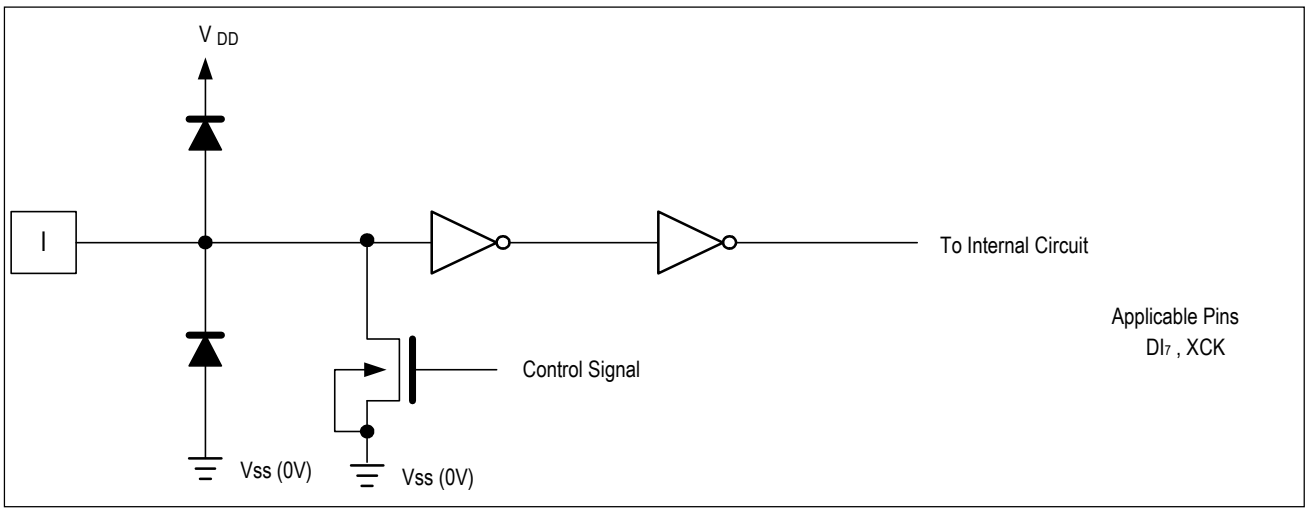


Figure 7-2 Input Circuit (2)

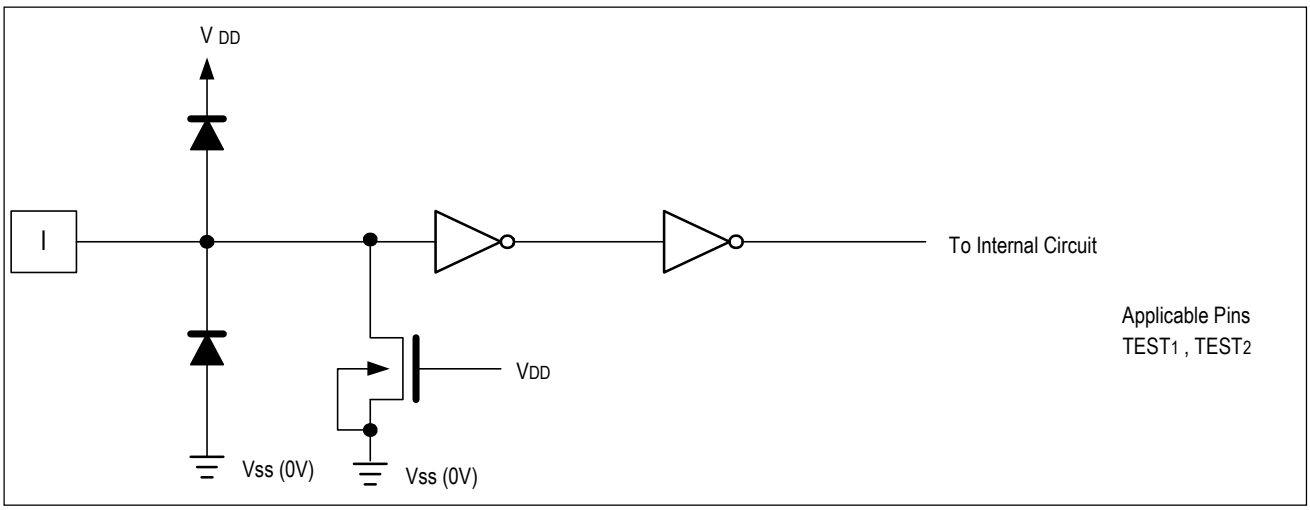


Figure 7-3 Input Circuit (3)

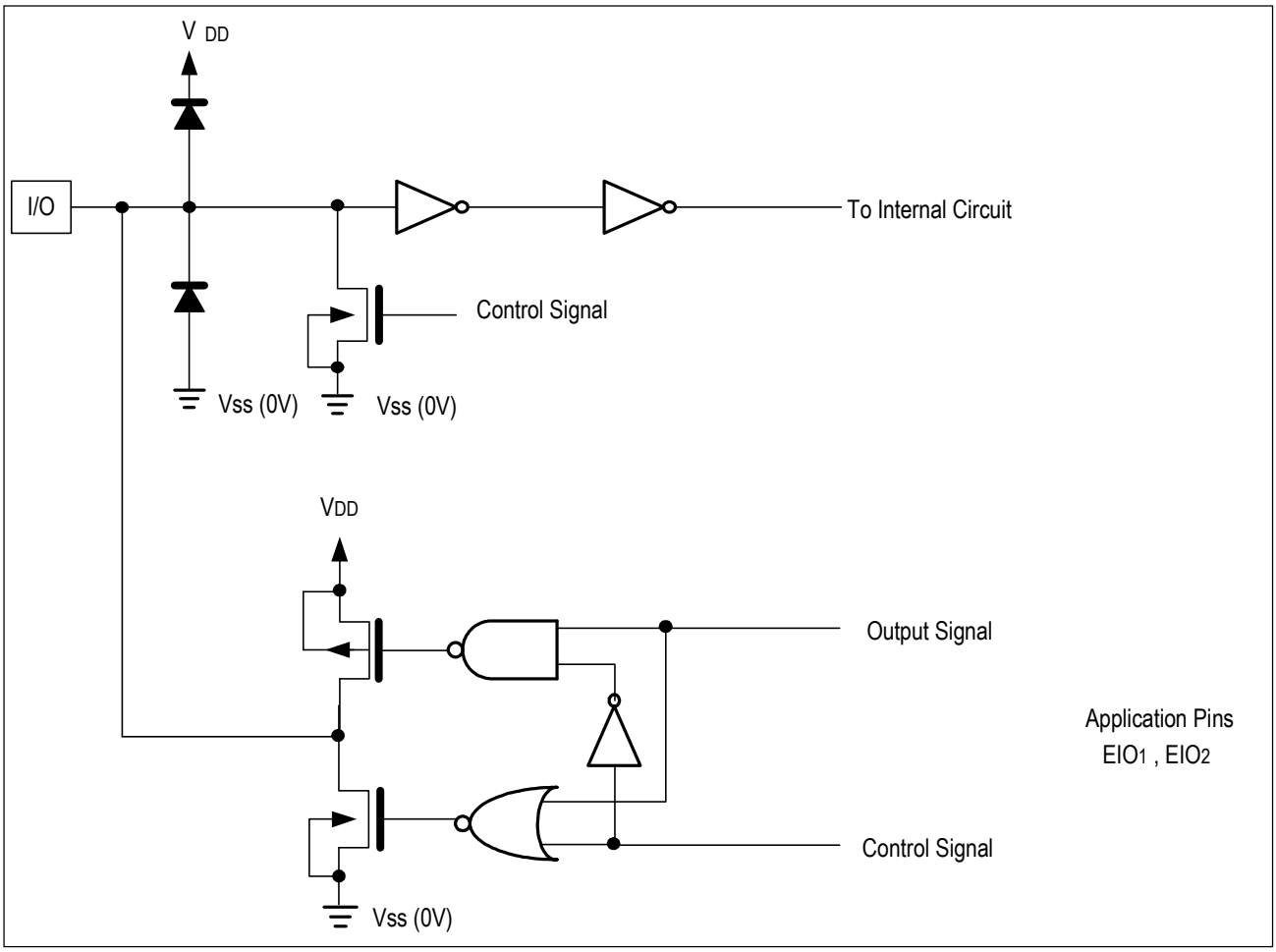


Figure 7-4 Input/Output Circuit

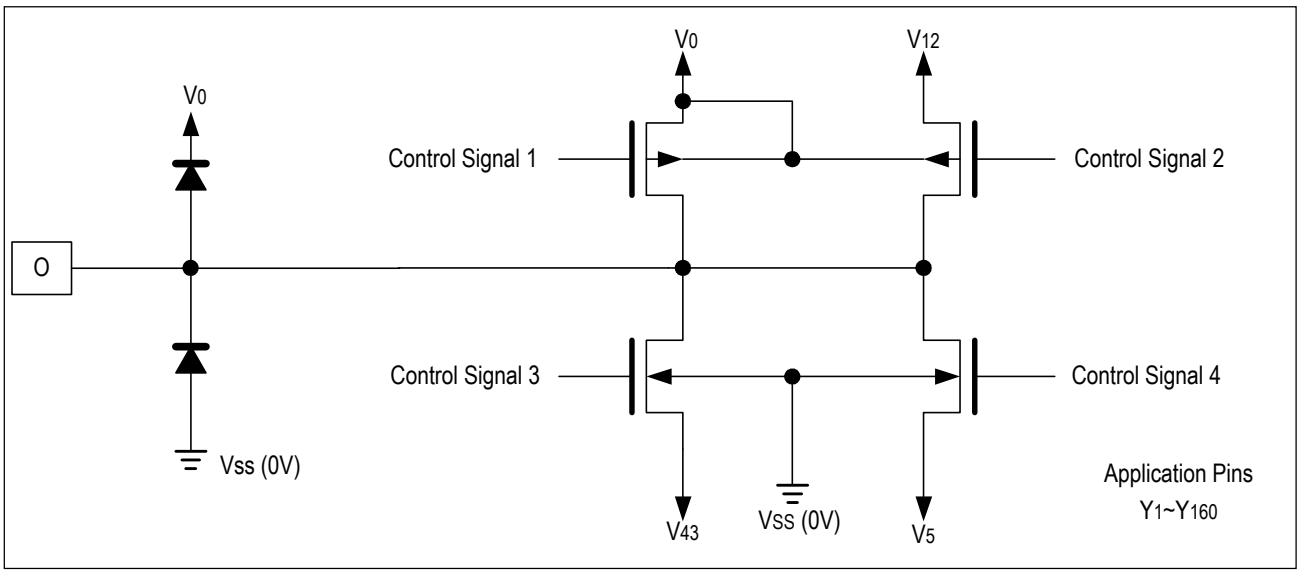


Figure 7-5 LCD Drive Output Circuit

8 FUNCTIONAL DESCRIPTION

8.1 Pin Functions

(Segment mode)

SYMBOL	FUNCTION
V_{DD}	Logic system power supply pin, connected to +2.5 to +5.5 V.
V_{SS}	Ground pin, connected to 0 V.
V_{0L}, V_{0R} V_{12L}, V_{12R} V_{43L}, V_{43R}	Bias power supply pins for LCD drive voltage • Normally use the bias voltages set by a resistor divider • Ensure that voltages are set such that $V_{SS} < V_{43} < V_{12} < V_0$. • V_{iL} and V_{iR} (i = 0,12, 43) must connect to an external power supply, and supply regular voltage which is assigned by specification for each power pin
DI_7-DI_0	Input pins for display data • In 4-bit parallel input mode, input data into the 4 pins, DI_3-DI_0. Connect DI_7-DI_4 to V_{SS} or V_{DD}. • In 8-bit parallel input mode, input data into the 8 pins, DI_7-DI_0. • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
XCK	Clock input pin for taking display data * Data is read at the falling edge of the clock pulse.
LP	Latch pulse input pin for display data • Data is latched at the falling edge of the clock pulse.
L/R	Input pin for selecting the reading direction of display data • When set to V_{SS} level "L", data is read sequentially from Y_{160} to Y_1. • When set to V_{DD} level "H", data is read sequentially from Y_1 to Y_{160}. • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
/DISPOFF	Control input pin for output of non-select level • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to V_{SS} level "L", the LCD drive output pins (Y_1-Y_{160}) are set to level Vss. • When set to "L", the contents of the line latch are reset, but the display data are read in the data latch regardless of the condition of /DISPOFF. When the /DISPOFF function is canceled, the driver outputs non-select level (V_{12} or V_{43}), then outputs the contents of the data latch at the next falling edge of the LP. At that time, if /DISPOFF removal time does not correspond to what is shown in AC characteristics, it cannot output the reading data correctly. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
FR	AC signal input pin for LCD drive waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
MD	Mode selection pin • When set to V_{SS} level "L", 4-bit parallel input mode is set. • When set to V_{DD} level "H", 8-bit parallel input mode is set. • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
S/C	Segment mode/common mode selection pin • When set to V_{DD} level "H", segment mode is set.
EIO_1, EIO_2	Input/output pins for chip selection • When L/R input is at V_{SS} level "L", EIO_1 is set for output, and EIO_2 is set for input. • When L/R input is at V_{DD} level "H", $\overline{EIO_1}$ is set for input, and EIO_2 is set for output. • During output, set to "H" while LP • $\overline{XCK}$ is "H" and after 160 bits of data have been read, set

	to "L" for one cycle (from falling edge to failing edge of XCK), after which it returns to "H". • During input, the chip is selected while EI is set to "L" after the LP signal is input. The chip is non-selected after 160 bits of data have been read.
OPTION_VDD	Option selection pin • For COG layout to reduce interface pins. • Normally let it open
Y_1 -Y_{160}	LCD drive output pins • Corresponding directly to each bit of the data latch, one level (V_0, V_{12} or V_{43}) is selected and output. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.

(Common mode)

SYMBOL	FUNCTION
V_{DD}	Logic system power supply pin, connected to +2.5 to +5.5 V.
V_{SS}	Ground pin, connected to 0 V.
V_{0L}, V_{0R} V_{12L}, V_{12R} V_{43L}, V_{43R}	Bias power supply pins for LCD drive voltage • Normally use the bias voltages set by a resistor divider. • Ensure that voltages are set such that $V_{SS} < V_{43} < V_{12} < V_0$. • V_{iL} and V_{iR} (i = 0,12, 43) must connect to an external power supply, and supply regular voltage that is assigned by specification for each power pin.
EIO_1	Shift data input/output pin for bi-directional shift register • Output pin when L/R is at V_{SS} level "L', input pin when L/R is at V_{DD} level "H". • When L/R = H, EIO_1 is used as input pin, it will be pulled down. • When L/R = L, EIO_1 is used as output pin, it won't be pulled down. • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
EIO_2	Shift data input/output pin for bi-directional shift register • Input pin when L/R is at V_{SS} level "L", output pin when L/R is at V_{DD} level "H". • When L/R = L, EIO_2 is used as input pin, it will be pulled down. • When L/R = H, EIO_2 is used as output pin, it won't be pulled down. • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
LP	Shift clock pulse input pin for bi-directional shift register • * Data is shifted at the falling edge of the clock pulse.
L/R	Input pin for selecting the shift direction of bi-directional shift register • Data is shifted from Y_{160} to Y_1 when set to V_{SS} level "L", and data is shifted from Y_1 to Y_{160} when set to V_{DD} level "H". • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
/DISPOFF	Control input pin for output of non-select level • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to V_{SS} level "L", the LCD drive output pins (Y_1-Y_{160}) are set to level Vss. • When set to "L", the contents of the shift register are reset to not reading data. When the /DISPOFF function is canceled, the driver outputs non-select level (V_{12} or V_{43}), and the shift data is read at the next falling edge of the LP. At that time, if /DISPOFF removal time does not correspond to what is shown in AC characteristics, the shift data is not read correctly. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
FR	AC signal input pin for LCD drive waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the shift register output signal and the FR signal. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
MD	Mode selection pin • When set to V_{SS} level "L", single mode operation is selected; when set to V_{DD} level "H" dual mode operation is selected. • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.

DI_7	Dual mode data input pin • According to the data shift direction of the data shift register, data can be input starting from the 81st bit. When the chip is used in dual mode, DI_7 will be pulled down. When the chip is used in single mode, DI_7 won't be pulled down(Connect to V_{SS} or V_{DD}, avoiding floating.). • Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
S/C	Segment mode/common mode selection pin • When set to V_{SS} level "L", common mode is set.
DI_6-DI_0	Not used • Connect DI_6-DI_0 to V_{SS} or V_{DD}, avoiding floating.
XCK	Not used • XCK is pulled down in common mode, so connect to V_{SS} or open.
OPTION_VDD	Option selection pin • For COG layout to reduce interface pin.
Y_1 -Y_{160}	LCD drive output pins • Corresponding directly to each bit of the shift register, one level (V_0, V_{12}, V_{43}, or V_{SS}) is selected and output. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.

8.2 Functional Operations

8.2.1 Truth Table

(Segment Mode)

FR	LATCH DATA	/DISPOFF	LCD DRIVE OUTPUT VOLTAGE LEVEL (Y1-Y160)
L	L	H	V_{43}
L	H	H	V_{SS}
H	L	H	V_{12}
H	H	H	V_0
X	X	L	V_{SS}

(Common Mode)

FR	LATCH DATA	/DISPOFF	LCD DRIVE OUTPUT VOLTAGE LEVEL (Y1-Y160)
L	L	H	V_{43}
L	H	H	V_0
H	L	H	V_{12}
H	H	H	V_{SS}
X	X	L	V_{SS}

NOTES:

- VSS < V43 < V12 < V0
- L : VSS (0 V), H : VDD (+2.5 to +5.5 V), X : Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.
  There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver.
  Supply regular voltage that is assigned by specification for each power pin.

8.2.2 Relationship between the Display Data and LCD Drive Output Pins

(Segment Mode)

(a) 4-bit Parallel Input Mode

MD	L/R	EIO_1	EIO_2	DATA INPUT	NUMBER OF CLOCKS						
					40 CLOCK	39 CLOCK	38 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
L	L	Output	Input	DI_0	Y_1	Y_5	Y_9	…	Y_{149}	Y_{153}	Y_{157}
				DI_1	Y_2	Y_6	Y_{10}	…	Y_{150}	Y_{154}	Y_{158}
				DI_2	Y_3	Y_7	Y_{11}	…	Y_{151}	Y_{155}	Y_{159}
				DI_3	Y_4	Y_8	Y_{12}	…	Y_{152}	Y_{156}	Y_{160}
L	H	Input	Output	DI_0	Y_{160}	Y_{156}	Y_{152}	…	Y_{12}	Y_8	Y_4
				DI_1	Y_{159}	Y_{155}	Y_{151}	…	Y_{11}	Y_7	Y_3
				DI_2	Y_{158}	Y_{154}	Y_{150}	…	Y_{10}	Y_6	Y_2
				DI_3	Y_{157}	Y_{153}	Y_{149}	…	Y_9	Y_5	Y_1

(b) 8-bit Parallel Input Mode

MD	L/R	EIO_1	EIO_2	DATA INPUT	NUMBER OF CLOCKS						
					20 CLOCK	19 CLOCK	18 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
H	L	Output	Input	DI_0	Y_1	Y_9	Y_{17}	…	Y_{137}	Y_{145}	Y_{153}
				DI_1	Y_2	Y_{10}	Y_{18}	…	Y_{138}	Y_{146}	Y_{154}
				DI_2	Y_3	Y_{11}	Y_{19}	…	Y_{139}	Y_{147}	Y_{155}
				DI_3	Y_4	Y_{12}	Y_{20}	…	Y_{140}	Y_{148}	Y_{156}
				DI_4	Y_5	Y_{13}	Y_{21}		Y_{141}	Y_{149}	Y_{157}
				DI_5	Y_6	Y_{14}	Y_{22}		Y_{142}	Y_{150}	Y_{158}
				DI_6	Y_7	Y_{15}	Y_{23}		Y_{143}	Y_{151}	Y_{159}
				DI_7	Y_8	Y_{16}	Y_{24}		Y_{144}	Y_{152}	Y_{160}
H	H	Input	Output	DI_0	Y_{160}	Y_{152}	Y_{144}	…	Y_{24}	Y_{16}	Y_8
				DI_1	Y_{159}	Y_{151}	Y_{143}	…	Y_{23}	Y_{15}	Y_7
				DI_2	Y_{158}	Y_{150}	Y_{142}	…	Y_{22}	Y_{14}	Y_6
				DI_3	Y_{157}	Y_{149}	Y_{141}	…	Y_{21}	Y_{13}	Y_5
				DI_4	Y_{156}	Y_{148}	Y_{140}	…	Y_{20}	Y_{12}	Y_4
				DI_5	Y_{155}	Y_{147}	Y_{139}	…	Y_{19}	Y_{11}	Y_3
				DI_6	Y_{154}	Y_{146}	Y_{138}	…	Y_{18}	Y_{10}	Y_2
				DI_7	Y_{153}	Y_{145}	Y_{137}	…	Y_{17}	Y_9	Y_1

(Common Mode)

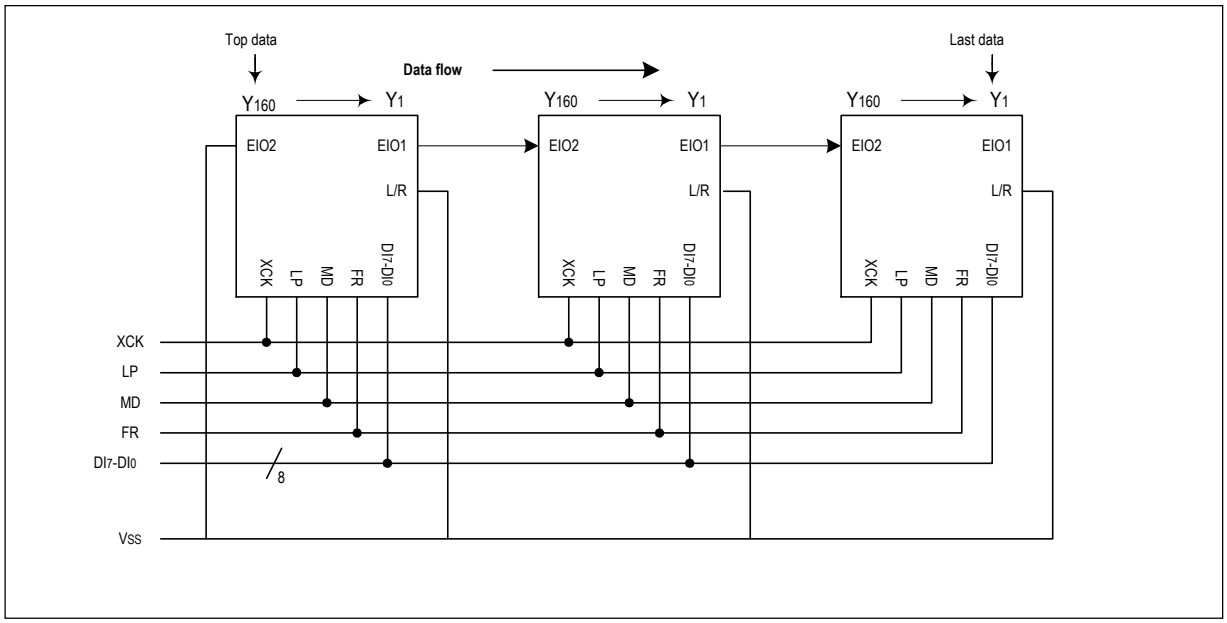
MD	L/R	DATA TRANSFER DIRECTION	EIO_1	EIO_2	DI_7
L (Single)	L	$Y_{160} \rightarrow Y_1$	Output	Input	X
	H	$Y_1 \rightarrow Y_{160}$	Input	Output	X
H (Dual)	L	$Y_{160} \rightarrow Y_{81}$ $Y_{80} \rightarrow Y_1$	Output	Input	Input
	H	$Y_1 \rightarrow Y_{80}$ $Y_{81} \rightarrow Y_{160}$	Input	Output	Input

NOTES:

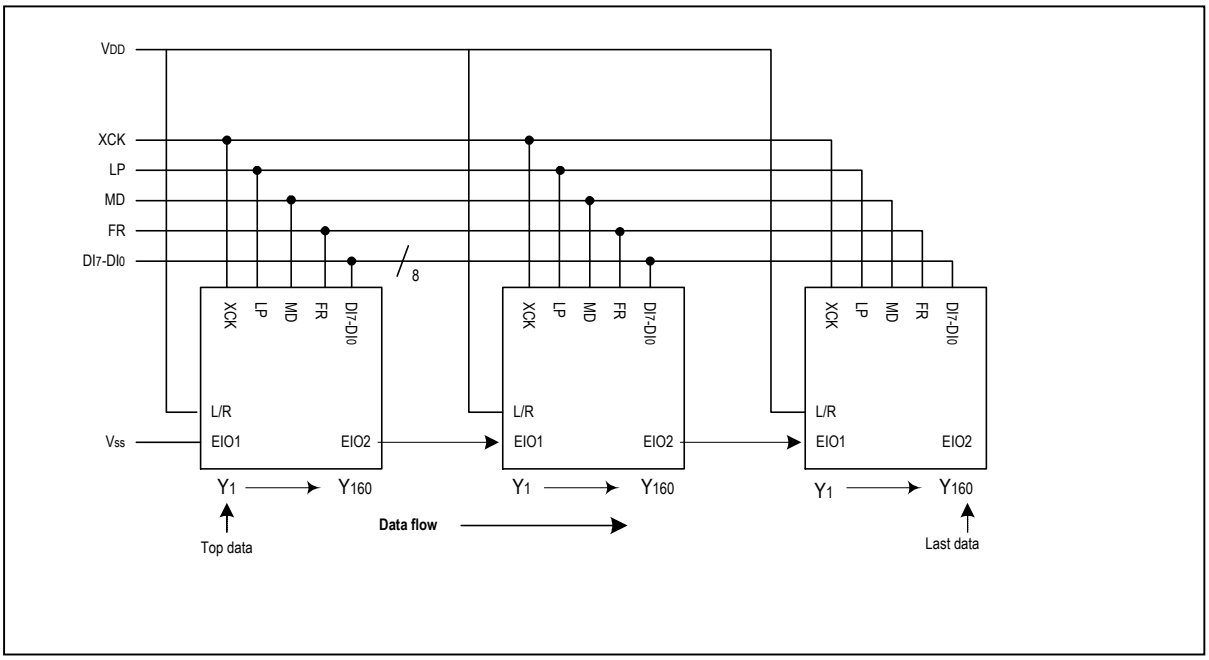
- L : V_{SS} (0 V), H : V_{DD} (+2.5 to +5.5 V), X : Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.

8.2.3 Connection Examples of Plural Segment Drivers

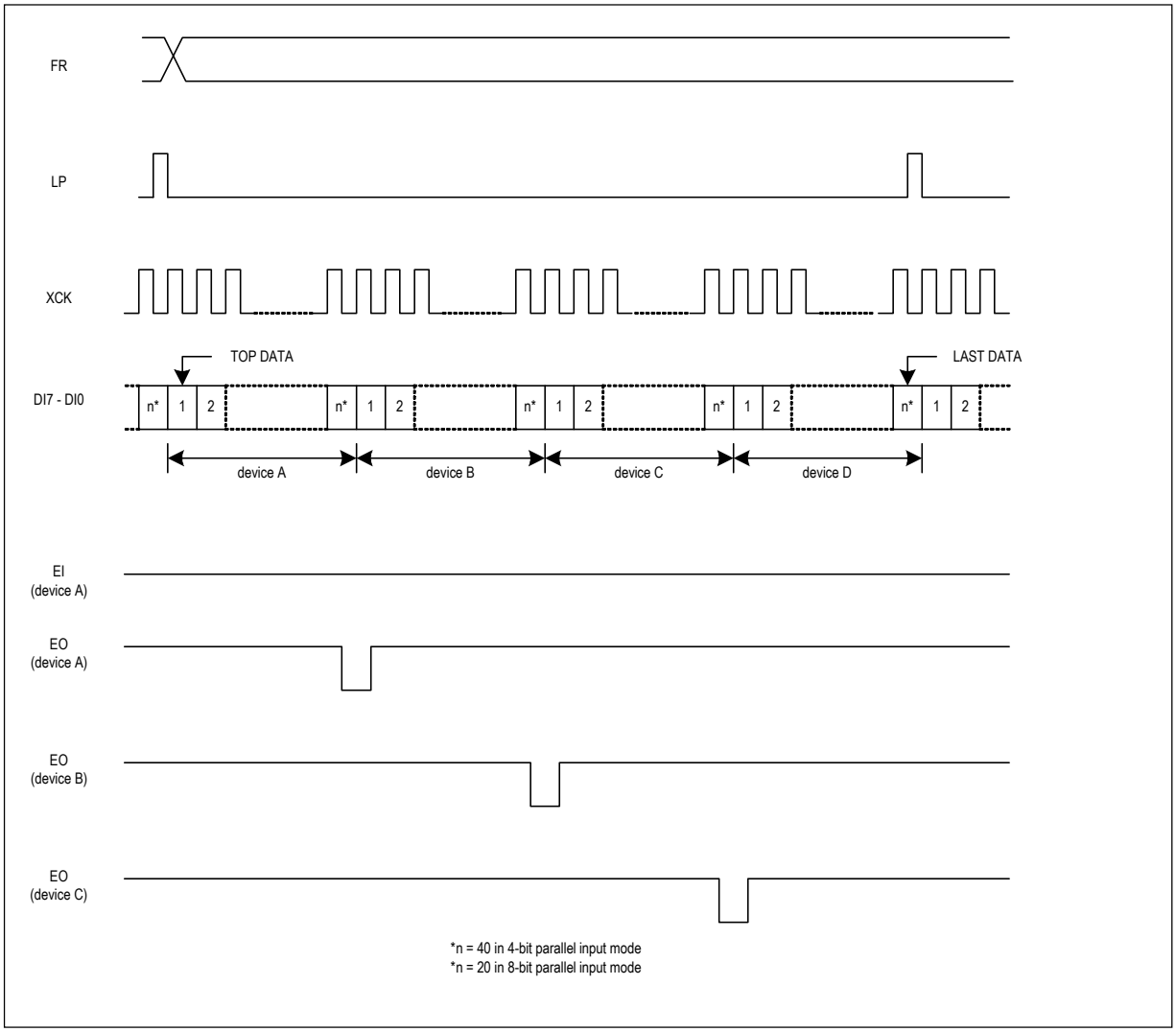
(a) *When L/R = "L"*



(b) When L/R = "H"

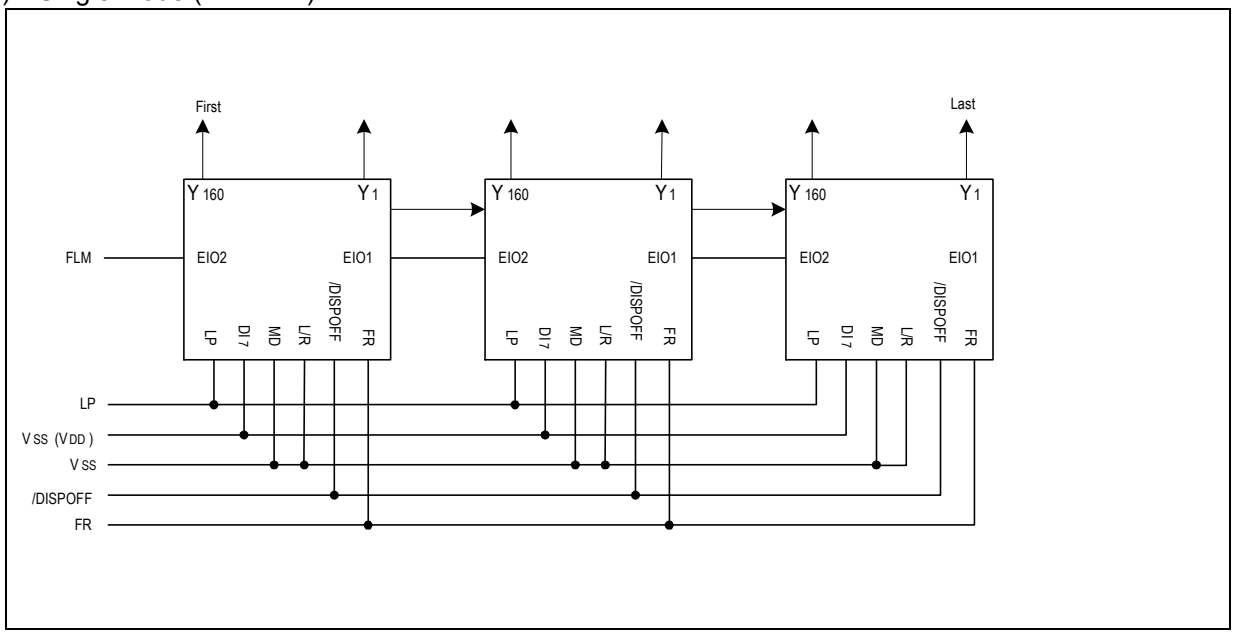


8.2.4 Timing Chart of 4-Device Cascade Connection of Segment Drivers

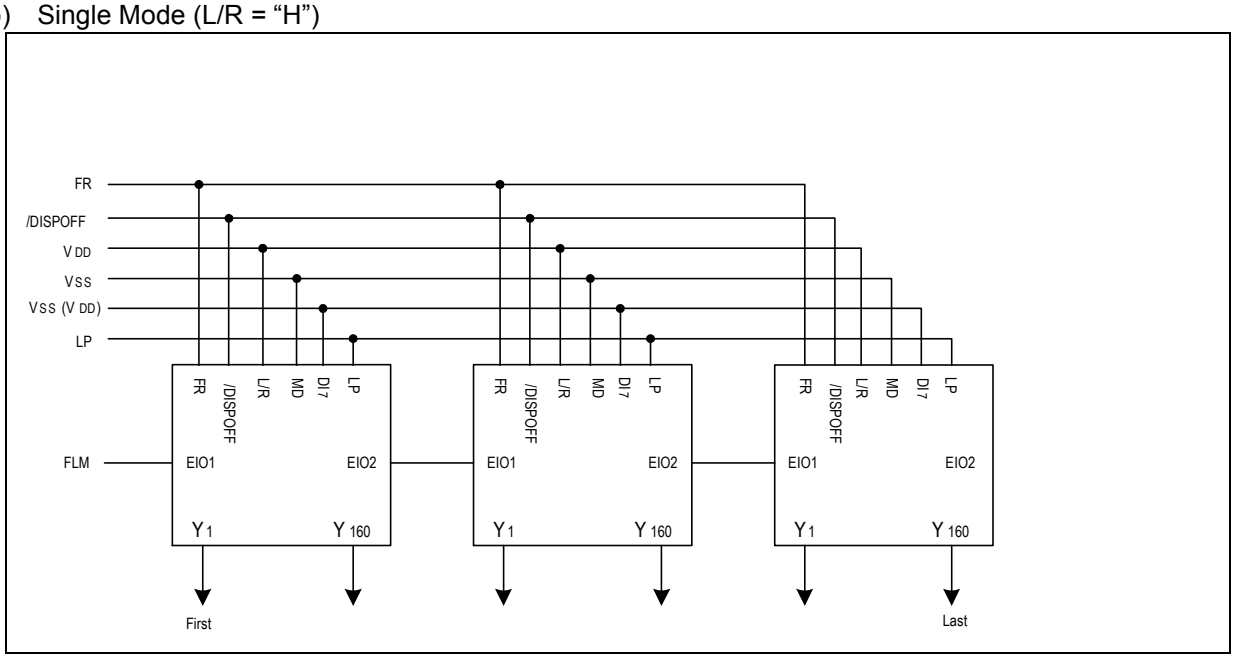


8.2.5 Connection Examples for Plural Common Drivers

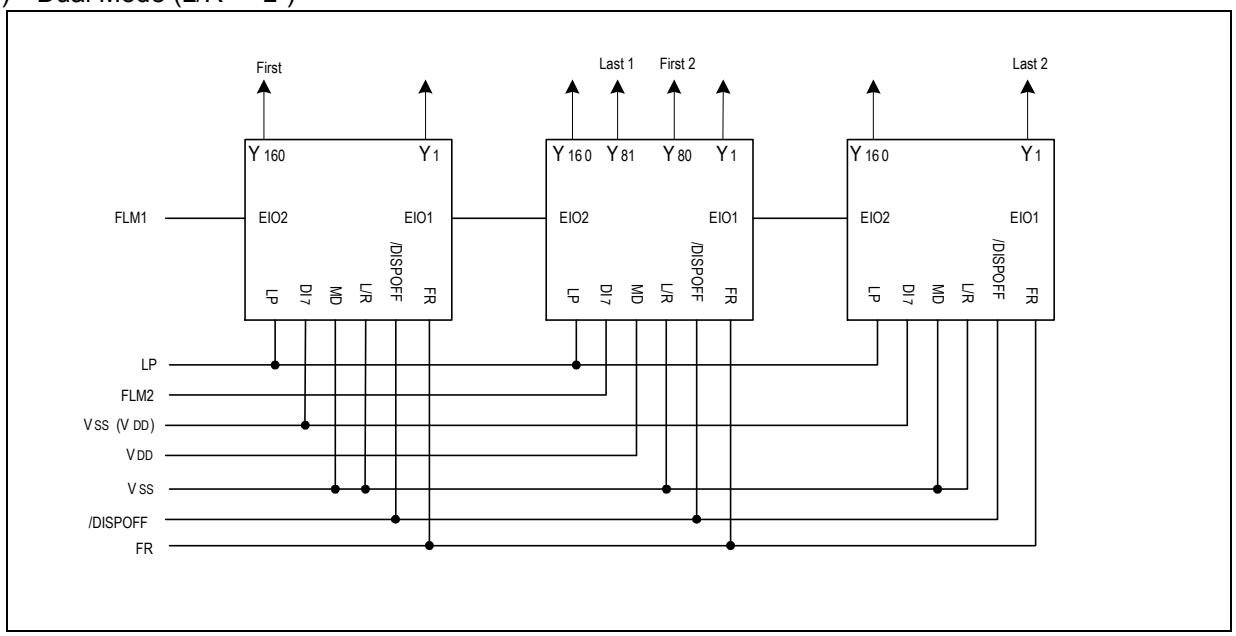
(a) Single Mode (L/R = ”L”)



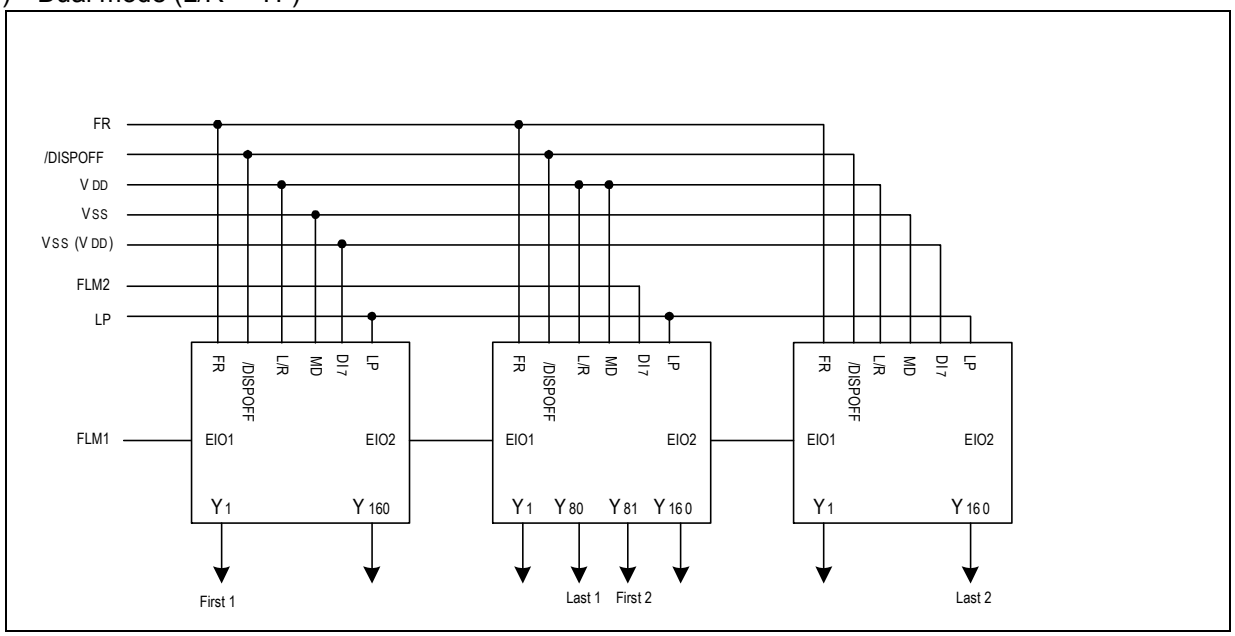
(b) Single Mode (L/R = “H”)



(c) Dual Mode (L/R = “L”)



(d) Dual mode (L/R = “H”)

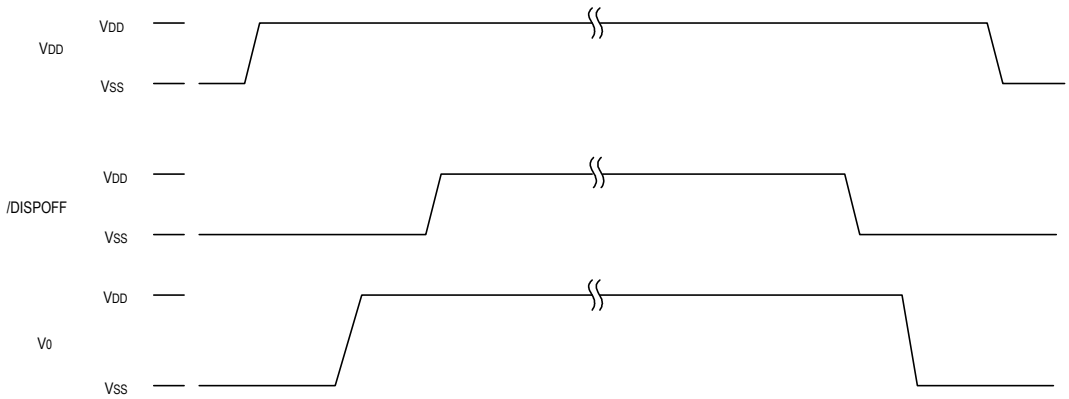


9 PRECAUTIONS

Precautions when connecting or disconnecting the power supply
This IC has a high-voltage LCD driver, so a high current that may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating may permanently damage it. The details are as follows,

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power
- It is advisable to connect the serial resistor (50 to 100 Ω) or fuse to the LCD drive power V0 of the system as a current limiter. Set up a suitable value of the resistor in consideration of the display grade.

And when connecting the logic power supply, the logic condition of this IC inside is insecure.



Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on /DISPOFF function. After that, cancel the /DISPOFF function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level Vss on /DISPOFF function. Then disconnect the logic system power after disconnecting the LCD drive power.
When connecting the power supply, follow the recommended sequence shown here.

10 ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	-0.3~ +7.0	V	1,2
Supply voltage (2)	V_0	V_{0L}, V_{0R}	-0.3 ~ +33.0	V	
	V_{12}	V_{12L}, V_{12R}	V_0 -10~ V_0 + 0.3	V	
	V_{43}	V_{43L}, V_{43R}	-0.3 ~ V_{SS} + 10	V	
Input voltage	V_I	$D1_7$-DI_0, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, /DISPOFF, $TEST_1$	-0.3 to V_{DD} + 0.3	V	
Storage temperature	T_{STG}		-45 to +125	°C	

NOTES:
1. TA = +25 °C
2. The maximum applicable voltage on any pin with respect to V_{SS} (0 V).
3. Stress over the “Absolute Max. Ratings” conditions will damaged the device permanently.

11 RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	+2.5		+5.5	V	1, 2
Supply voltage (2)	V_0	V_{0L}, V_{0R}	+15.0		+30.0	V	
Operating temperature	T_{OPR}		-25		+85	°C	

NOTES:
1. The applicable voltage on any pin with respect to V_{SS} (0 V).
2. Ensure that voltages are set such that $V_{SS} < V_{43} < V_{I2} < V_0$.

12 ELECTRICAL CHARACTERISTICS

12.1 DC Characteristics

(Segment Mode) (V_{SS} = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = + 15.0 to +30.0 V, T_{OPR} = -25 to +85°C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		DI7-DI0, XCK, LP, L/R FR, MD, S/C, EIO_1, EIO_2, /DISPOFF			$0.2V_{DD}$	V	
Input "High" voltage	V_{IH}			$0.8V_{DD}$		V_{DD}+0.7	V	
Output "Low" voltage	V_{OL}	I_{OL} = +0.4 mA	EIO_1, EIO_2			+0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -0.4 mA		V_{DD}-0.4			V	
Input leakage current	I_{LIL}	$V_I = V_{SS}$	DI7-DI0, XCK, LP, LIR, FR, MD, S/C, EIO_1, EIO_2, /DISPOFF			-10	μA	
	I_{LIH}	$V_I = V_{DD}$				+10	μA	
Output resistance	R_{ON}	$\lvert\Delta V_{ON}\rvert$ =0.5V, V_0 = 30 V	Y_1-Y_{160}		1.0	1.5	kΩ	
Standby current	I_{STB}		V_{SS}			50	μA	1
Supply current (1) (Non-selection)	I_{DD1}		V_{DD}			2.0	mA	2
Supply current (2) (Selection)	I_{DD2}		V_{DD}			7.0	mA	3
Supply current (3)	I_0		V_{0L}, V_{0R}			0.9	mA	4

NOTES:

1. V_{DD} = +5.0 V, V_0 = +30.0 V, Vi = V_{SS}.
2. V_{DD} = +5.0 V, V_0 = +30.0 V, f_{XCK} = 8 MHz, no-load, EI = V_{DD}. The input data is turned over by data taking clock (4-bit parallel input mode).
3. V_{DD} = +5.0 V, V_0 = +30.0 V, f_{XCK} = 8 MHz, no-load, EI = V_{SS}. The input data is turned over by data taking clock (4-bit parallel input mode).
4. V_{DD} = +5.0 V, V_0 = +30.0 V, f_{XCK} = 8MHz, f_{LP} = 19.2 kHz, f_{FR} = 80 Hz, no-load. The input data is turned over by data taking clock (4-bit parallel input mode).

(Common Mode) (V_{SS} = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = + 15.0 to +30.0 V, T_{OPR} = -25 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		DI7-DI0, XCK, LP, L/R FR, MD, S/C, EIO_1, EIO_2, /DISPOFF			$0.2V_{DD}$	V	
Input "High" voltage	V_{IH}			$0.8V_{DD}$		V_{DD}+0.7	V	
Output "Low" voltage	V_{OL}	I_{OL} = +0.4 mA	EIO_1, EIO_2			+0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -0.4 mA		V_{DD}-0.4			V	
Input leakage current	I_{LIL}	$V_I = V_{SS}$	DI7-DI0, XCK, LP, L/R FR, MD, S/C, EIO_1, EIO_2, /DISPOFF			-10.0	μA	
	I_{LIH}	$V_I = V_{DD}$	DI6-DI0, LP, L/R, FR, MD, S/C, /DISPOFF			+10.0	μA	
Input pull-down current	I_{PD}	$V_I = V_{DD}$	DI7, XCK, EIO_1, EIO_2			100	μA	
Output resistance	R_{ON}	$\lvert\Delta V_{ON}\rvert$ =0.5V, V_0 = 30 V	Y_1-Y_{160}		1.0	1.5	kΩ	
Standby current	I_{SPD}		V_{SS}			50	μA	1
Supply current (1)	I_{DD}		V_{DD}			80	μA	2
Supply current (2)	I_0		V_{OL}, V_{OR}			130	μA	2

NOTES:

1. VDD = +5.0 V, V0 = +30.0 V, VI = VSS
2. VDD = +5.0 V, V0 = +30.0 V, fLP =19.2 kHz, fFR = 80 Hz, 1/240 duty operation, no-load.

12.2 AC Characteristics

(Segment Mode 1) (V_{SS} = 0 V, V_{DD} = +2.5 to +3.0 V, V_0 = + 15.0 to +30.0 V, T_{OPR} = -25 10+85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R,t_F ≤ 10ns	125			ns	1
Shift clock "H" pulse width	t_{WCKH}		51			ns	
Shift clock "L" pulse width	t_{WCKL}		51			ns	
Data setup time	t_{DS}		30			ns	
Data hold time	t_{DH}		40			ns	
Latch pulse "H" pulse width	t_{WLPH}		51			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		51			ns	
Latch pulse rise to shift clock rise time	t_{LS}		51			ns	
Latch pulse fall to shift clock fall time	t_{LH}		51			ns	
Enable setup time	t_S		36			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
/DISPOFF removal time	t_{SD}		100			ns	
/DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			78	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

NOTES:

1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Segment Mode 2) (V_{SS} = 0 V, V_{DD} = +3.0 to +4.5 V, V_0 = + 15.0 to +30.0 V, T_{OPR} = -25 10+85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R,t_F ≤ 10ns	82			ns	1
Shift clock "H" pulse width	t_{WCKH}		28			ns	
Shift clock "L" pulse width	t_{WCKL}		28			ns	
Data setup time	t_{DS}		20			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		51			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
/DISPOFF removal time	t_{SD}		100			ns	
/DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			57	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

NOTES:

1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Segment Mode 3) (V_{SS} = 0 V, V_{DD} = +5.0±0.5 V, V_0 = + 15.0 to +30.0 V, T_{OPR} = -25 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R,t_F ≤ 10ns	50			ns	1
Shift clock "H" pulse width	t_{WCKH}		15			ns	
Shift clock "L" pulse width	t_{WCKL}		15			ns	
Data setup time	t_{DS}		10			ns	
Data hold time	t_{DH}		12			ns	
Latch pulse "H" pulse width	t_{WLPH}		15			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		25			ns	
Latch pulse rise to shift clock rise time	t_{LS}		25			ns	
Latch pulse fall to shift clock fall time	t_{LH}		25			ns	
Enable setup time	t_S		10			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			30	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			400	ns	
Output delay time (3)	t_{PD3}	CL = 15 pF			400	ns	

NOTES:

1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Common Mode) (V_{SS} = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = + 15.0 to +30.0 V, T_{OPR} = -25 10+85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Shift clock period	t_{WLP}	t_R, t_F 20ns	250			ns
Shift clock “H” pulse width	t_{WLPH}	VDD=5± 0.5V VDD=2.5~4.5V	15 30			ns
Data setup time	t_{SU}		30			ns
Data hold time	t_H		50			ns
Input signal rise time	t_R				50	ns
Input signal fall time	t_F				50	ns
DISPOFF removal time	t_{SD}		100			ns
DISPOFF “L” pulse width	t_{WDL}		1.2			us
Output delay time (1)	t_{DL}	CL=10pF			200	ns
Output delay time (2)	t_{PD1},t_{PD2}	CL=10pF			1.2	us
Output delay time (3)	t_{PD3}	CL=10pF			1.2	us

12.3 Timing Chart of Segment Mode

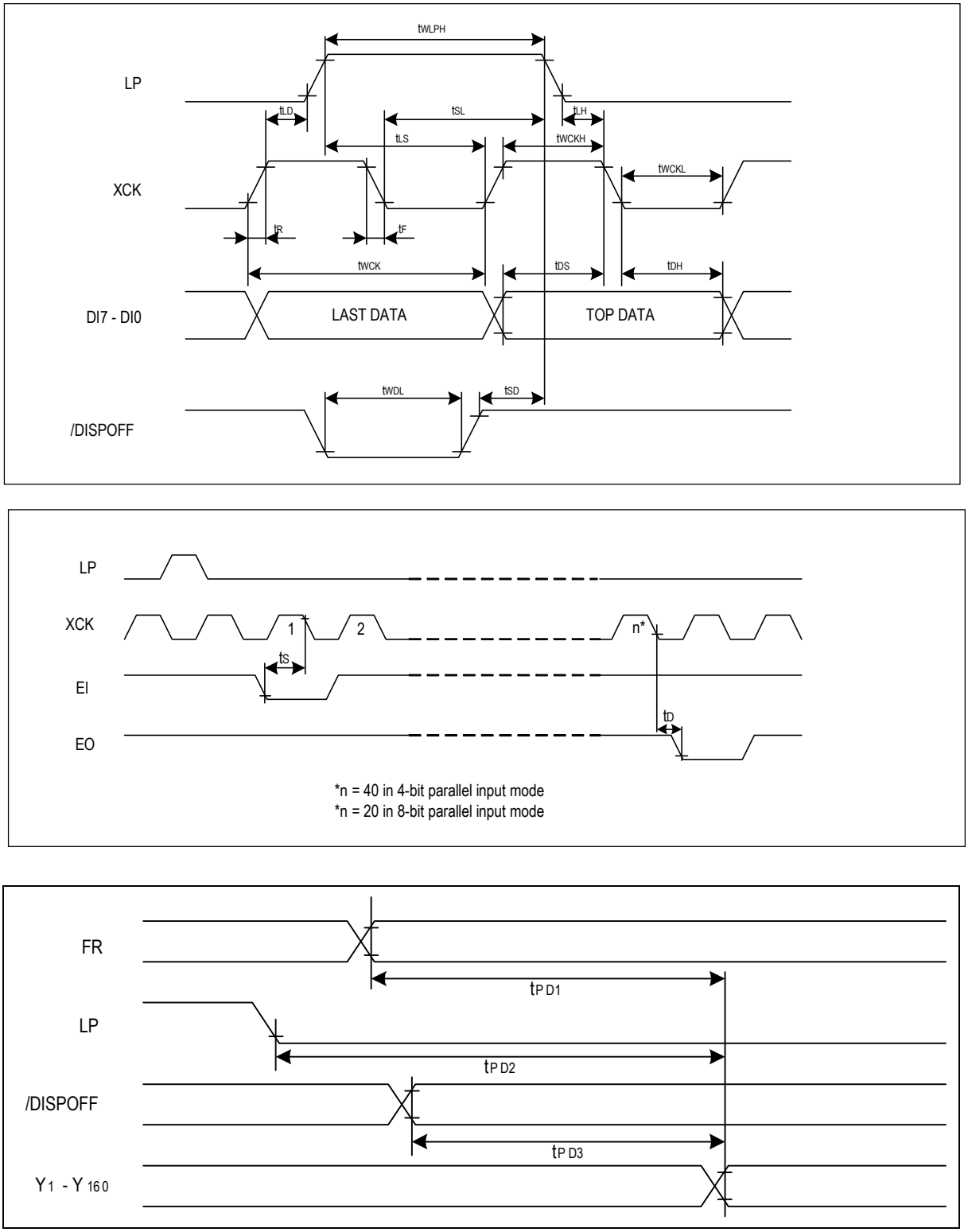
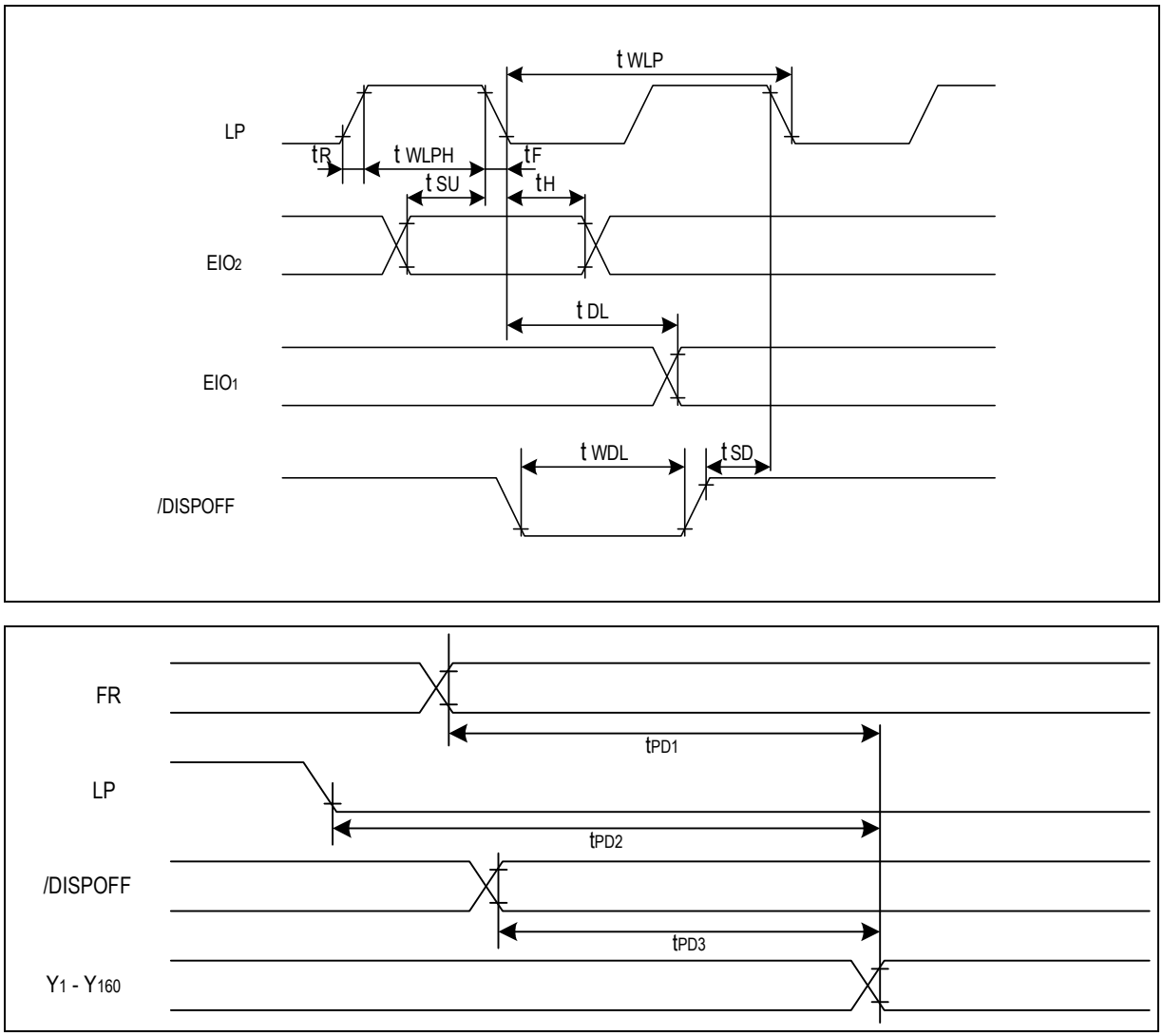


Figure 12-1 Timing Characteristics (3)

12.4 Timing Chart of Common Mode

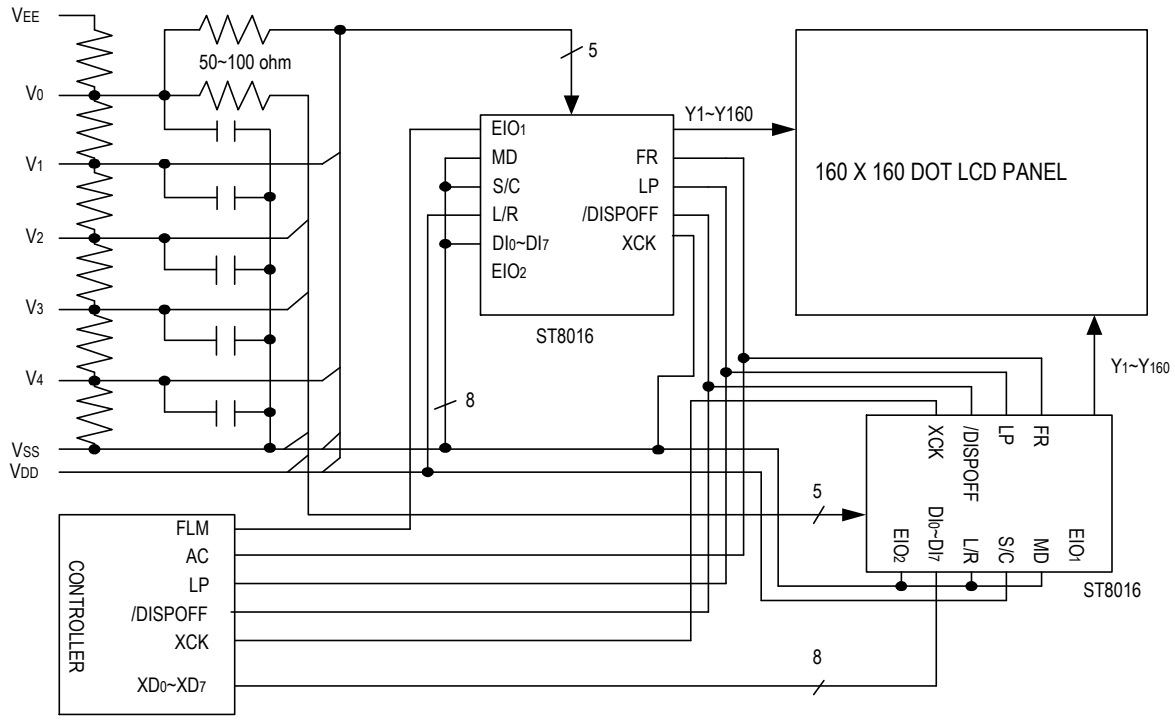


(Common Mode) (V_{SS} = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = + 15.0 to +30.0 V, T_{OPR} = -25 10+85 °C)

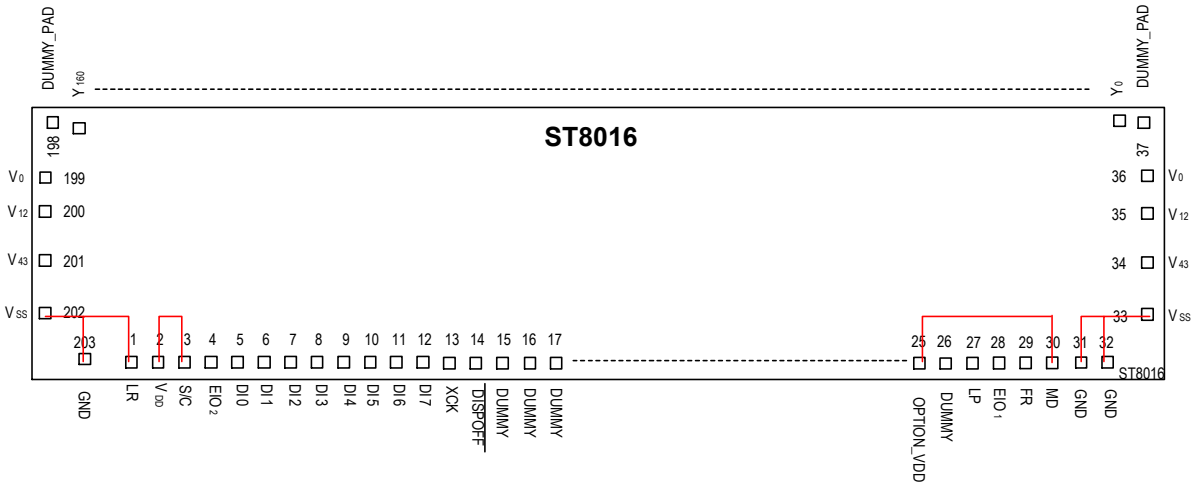
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Shift clock period	t_{WLP}	t_R, t_F 20ns	250			ns
Shift clock "H" pulse width	t_{WLPH}	V_{DD}=5± 0.5V V_{DD}=2.5~4.5V	15 30			ns
Data setup time	t_{SU}		30			ns
Data hold time	t_H		50			ns
Input signal rise time	t_R				50	ns
Input signal fall time	t_F				50	ns
DISPOFF removal time	t_{SD}		100			ns
DISPOFF "L" pulse width	t_{WDL}		1.2			us
Output delay time (1)	t_{DL}	CL=10pF			200	ns
Output delay time (2)	t_{PD1},t_{PD2}	CL=10pF			1.2	us
Output delay time (3)	t_{PD3}	CL=10pF			1.2	us

13 APPLICATION CIRCUIT

13.1 Application Circuit for Module



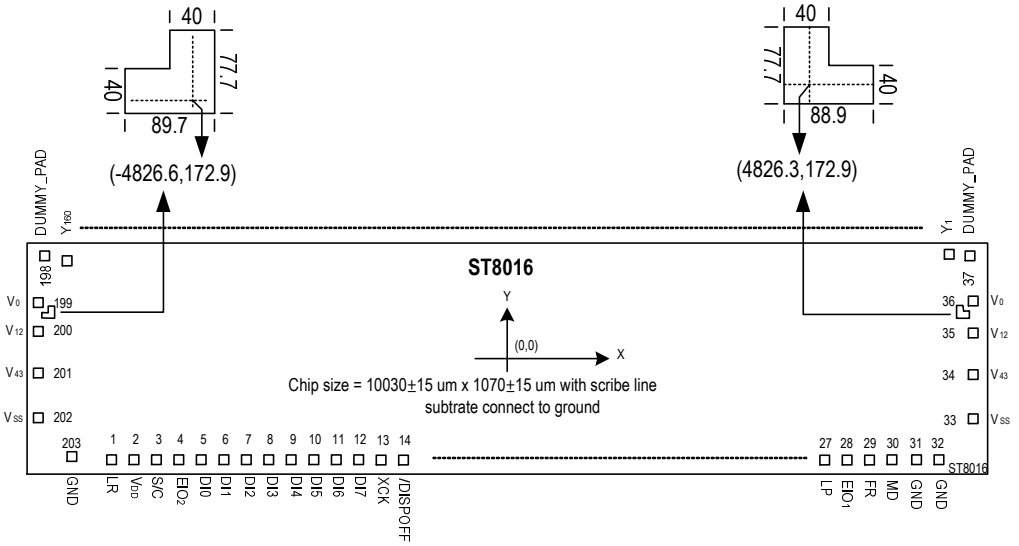
13.2 Application Circuit for COG Layout (Example)



PCB layout notice:

1. When V_{DD} < 2.7V, the resistance of (V_{DD} PCB path + VDD ITO path + GND ITO path + GND PCB path) must be less than 75 Ohm.
2. When V_{DD} >= 2.7V, the resistance of (V_{DD} PCB path + VDD ITO path + GND ITO path + GND PCB path) must be less than 130 Ohm.

14 PAD DIAGRAM



Unit: um

PIN#	Name	X	Y	PIN#	Name	X	Y
1	L/R	-4538.6	-406.9	32	GND	4720.4	-404.3
2	VDD	-4227.0	-409.7	33	VSS	4904.5	-344.1
3	S/C	-4074.5	-406.9	34	V43	4904.5	-125.7
4	EIO2	-3607.4	-406.9	35	V12	4904.5	90.7
5	DI0	-3413.4	-406.9	36	V0	4904.5	265.9
6	DI1	-3056.4	-406.9	37	DUMMY_PAD	4890.0	438.3
7	DI2	-2862.4	-406.9	38	Y1	4770.0	383.8
8	DI3	-2505.9	-406.9	39	Y2	4710.0	383.8
9	DI4	-2311.9	-406.9	40	Y3	4650.0	383.8
10	DI5	-1955.6	-406.9	41	Y4	4590.0	383.8
11	DI6	-1761.6	-406.9	42	Y5	4530.0	383.8
12	DI7	-1355.9	-406.9	43	Y6	4470.0	383.8
13	XCK	-1161.9	-406.9	44	Y7	4410.0	383.8
14	DISPOFFB	-741.5	-406.9	45	Y8	4350.0	383.8
15	DUMMY_PAD	-586.0	-419.2	46	Y9	4290.0	383.8
16	DUMMY_PAD	-70.4	-421.5	47	Y10	4230.0	383.8
17	DUMMY_PAD	152.5	-398.3	48	Y11	4170.0	383.8
18	DUMMY_PAD	400.6	-394.3	49	Y12	4110.0	383.8
19	DUMMY_PAD	768.3	-398.7	50	Y13	4050.0	383.8
20	DUMMY_PAD	1183.9	-398.7	51	Y14	3990.0	383.8
21	DUMMY_PAD	1474.6	-395.3	52	Y15	3930.0	383.8
22	DUMMY_PAD	1595.8	-411.9	53	Y16	3870.0	383.8
23	DUMMY_PAD	2092.5	-412.6	54	Y17	3810.0	383.8
24	DUMMY_PAD	2318.2	-404.5	55	Y18	3750.0	383.8
25	OPTION_VDD	2744.0	-407.1	56	Y19	3690.0	383.8
26	DUMMY_PAD	3082.8	-407.1	57	Y20	3630.0	383.8
27	LP	3220.8	-406.9	58	Y21	3570.0	383.8
28	EIO1	3701.6	-406.9	59	Y22	3510.0	383.8
29	FR	3895.6	-406.9	60	Y23	3450.0	383.8
30	MD	4313.0	-406.9	61	Y24	3390.0	383.8
31	GND	4525.0	-406.9	62	Y25	3330.0	383.8

63	Y26	3270.0	383.8	113	Y76	270.0	383.8
64	Y27	3210.0	383.8	114	Y77	210.0	383.8
65	Y28	3150.0	383.8	115	Y78	150.0	383.8
66	Y29	3090.0	383.8	116	Y79	90.0	383.8
67	Y30	3030.0	383.8	117	Y80	30.0	383.8
68	Y31	2970.0	383.8	118	Y81	-30.0	383.8
69	Y32	2910.0	383.8	119	Y82	-90.0	383.8
70	Y33	2850.0	383.8	120	Y83	-150.0	383.8
71	Y34	2790.0	383.8	121	Y84	-210.0	383.8
72	Y35	2730.0	383.8	122	Y85	-270.0	383.8
73	Y36	2670.0	383.8	123	Y86	-330.0	383.8
74	Y37	2610.0	383.8	124	Y87	-390.0	383.8
75	Y38	2550.0	383.8	125	Y88	-450.0	383.8
76	Y39	2490.0	383.8	126	Y89	-510.0	383.8
77	Y40	2430.0	383.8	127	Y90	-570.0	383.8
78	Y41	2370.0	383.8	128	Y91	-630.0	383.8
79	Y42	2310.0	383.8	129	Y92	-690.0	383.8
80	Y43	2250.0	383.8	130	Y93	-750.0	383.8
81	Y44	2190.0	383.8	131	Y94	-810.0	383.8
82	Y45	2130.0	383.8	132	Y95	-870.0	383.8
83	Y46	2070.0	383.8	133	Y96	-930.0	383.8
84	Y47	2010.0	383.8	134	Y97	-990.0	383.8
85	Y48	1950.0	383.8	135	Y98	-1050.0	383.8
86	Y49	1890.0	383.8	136	Y99	-1110.0	383.8
87	Y50	1830.0	383.8	137	Y100	-1170.0	383.8
88	Y51	1770.0	383.8	138	Y101	-1230.0	383.8
89	Y52	1710.0	383.8	139	Y102	-1290.0	383.8
90	Y53	1650.0	383.8	140	Y103	-1350.0	383.8
91	Y54	1590.0	383.8	141	Y104	-1410.0	383.8
92	Y55	1530.0	383.8	142	Y105	-1470.0	383.8
93	Y56	1470.0	383.8	143	Y106	-1530.0	383.8
94	Y57	1410.0	383.8	144	Y107	-1590.0	383.8
95	Y58	1350.0	383.8	145	Y108	-1650.0	383.8
96	Y59	1290.0	383.8	146	Y109	-1710.0	383.8
97	Y60	1230.0	383.8	147	Y110	-1770.0	383.8
98	Y61	1170.0	383.8	148	Y111	-1830.0	383.8
99	Y62	1110.0	383.8	149	Y112	-1890.0	383.8
100	Y63	1050.0	383.8	150	Y113	-1950.0	383.8
101	Y64	990.0	383.8	151	Y114	-2010.0	383.8
102	Y65	930.0	383.8	152	Y115	-2070.0	383.8
103	Y66	870.0	383.8	153	Y116	-2130.0	383.8
104	Y67	810.0	383.8	154	Y117	-2190.0	383.8
105	Y68	750.0	383.8	155	Y118	-2250.0	383.8
106	Y69	690.0	383.8	156	Y119	-2310.0	383.8
107	Y70	630.0	383.8	157	Y120	-2370.0	383.8
108	Y71	570.0	383.8	158	Y121	-2430.0	383.8
109	Y72	510.0	383.8	159	Y122	-2490.0	383.8
110	Y73	450.0	383.8	160	Y123	-2550.0	383.8
111	Y74	390.0	383.8	161	Y124	-2610.0	383.8
112	Y75	330.0	383.8	162	Y125	-2670.0	383.8

163	Y126	-2730.0	383.8	184	Y147	-3990.0	383.8
164	Y127	-2790.0	383.8	185	Y148	-4050.0	383.8
165	Y128	-2850.0	383.8	186	Y149	-4110.0	383.8
166	Y129	-2910.0	383.8	187	Y150	-4170.0	383.8
167	Y130	-2970.0	383.8	188	Y151	-4230.0	383.8
168	Y131	-3030.0	383.8	189	Y152	-4290.0	383.8
169	Y132	-3090.0	383.8	190	Y153	-4350.0	383.8
170	Y133	-3150.0	383.8	191	Y154	-4410.0	383.8
171	Y134	-3210.0	383.8	192	Y155	-4470.0	383.8
172	Y135	-3270.0	383.8	193	Y156	-4530.0	383.8
173	Y136	-3330.0	383.8	194	Y157	-4590.0	383.8
174	Y137	-3390.0	383.8	195	Y158	-4650.0	383.8
175	Y138	-3450.0	383.8	196	Y159	-4710.0	383.8
176	Y139	-3510.0	383.8	197	Y160	-4770.0	383.8
177	Y140	-3570.0	383.8	198	DUMMY_PAD	-4890.0	438.3
178	Y141	-3630.0	383.8	199	V0	-4904.5	265.9
179	Y142	-3690.0	383.8	200	V12	-4904.5	90.7
180	Y143	-3750.0	383.8	201	V43	-4904.5	-125.7
181	Y144	-3810.0	383.8	202	VSS	-4904.5	-344.1
182	Y145	-3870.0	383.8	203	GND	-4781.8	-404.9
183	Y146	-3930.0	383.8				

14.1 Gold Bump Size (unit: um)

Pad No.	X	Y	Area (um^2)
38~197	45	72	3240
1~14,17,27~32,203	62	58	3596
33~36,199~202	58	62	3596
15,16,18,21~26	38	60	2280
19,20	60	38	2280
37,198	85	60	5100

Wafer Thickness = 675±20um, Bump pad height (pad 1~198) = 18um, strength=30g

15 REVISION

REVISION	DESCRIPTION	PAGE	DATE
	Page1, modify pin configuration		2000/05/16
	Application circuit		2000/07/25
	Pad allocation, Bump size		2000/08/01
0.14	change pad name V5 as Vss		2000/08/09
0.143	add pad 203 gold bump data		2000/08/17
0.152	add some bump information		2000/10/09
0.153	correct pad name		2000/11/02
0.16	update TCP(F18) information		2000/12/04
0.17	correct all V5 as Vss		2000/12/19
0.2	AC/DC data revise		2000/12/26
0.23	correct segment mode MD=L/H=4/8 bit (section 7.2.2)		2001/02/08
0.24	gold bump strength=30g		2001/03/01
0.30	Dual mode describe correct and COG application circuit (section 12.2)		2001/05/22
0.31	Correct some wrong word mistake		2001/06/11
0.32	add Input/Output circuit		2001/08/29
0.33	t_{SL} MIN change to 51 , and change parameter name		2001/09/28
0.34	Correct AC characteristics column		2001/10/04
0.35	Change operating temperature from -20°C~85°C to -25°C~85°C		2002/06/07
1.2	Modify V5 to Vss in Pad Diagram Table , and DI_7 pin description for com mode		2005/01/31
1.3	Modify AC Characteristics		2005/09/23
1.4	Add alignment mark		2005/10/19
1.5	Add max value for input high voltage		2006/09/04
1.6	Modify chip size and thickness with scribe line		2006/10/26
1.7	Modify Wafer Thickness	25	2006/12/22
1.8	Add PCB layout notice: resistance limitation between Vdd and GND	23	2007/2/6
1.9	Modify all the data about absolute max voltage and recommend max voltage	2,16	2007/5/25