Sitronix

ST8016T

COM/SEG LCD Driver

P r e l i m i n a r y

Note: Sitronix Technology Corp. reserves the right to change the contents in this document without prior notice. This is not a final specification. Some parameters are subject to change.

Datasheet

Version 0.12

2007/10/29

Sitronix Technology Corporation

1 FEATURES

- Number of LCD drive outputs: 160
- Supply voltage for LCD drive: +15.0 to +30.0 V
- Supply voltage for the logic system: +2.5 to +5.5 V
- Low power consumption
- Low output impedance

(Segment mode)

- Shift clock frequency
  - 20 MHz (MAX.): V_{DD} = +5.0 ± 0.5 V
  - 15 MHz (MAX.): V_{DD} = +3.0 to + 4.5 V
  - 12 MHz (MAX.): V_{DD} = +2.5 to + 3.0 V
- 4-bit/8-bit parallel input modes are selectable with a mode (MD) pin
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 160 bits of input data
- Line latch circuits are reset when /DISPOFF active

(Common mode)

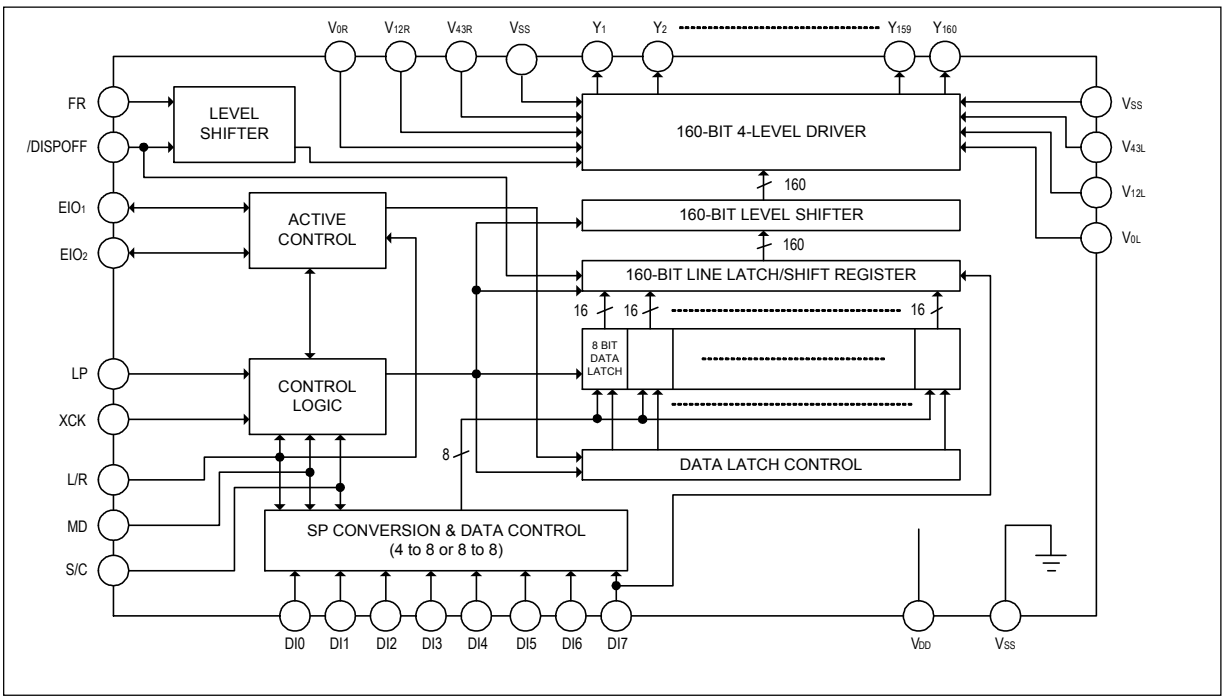
- Shift clock frequency: 4 MHz (MAX.)
- Built-in 160-bit bi-directional shift register (divisible into 80 bits x 2)
- Available in a single mode (160-bit shift register) or in a dual mode (80-bit shift register x 2)
  - Y_1->Y_{160} Single mode
  - Y_{160}->Y_1 Single mode
  - Y_1->Y_{80}, Y_{81}->Y_{160} Dual mode
  - Y_{160}->Y_{81}, Y_{80}->Y_1 Dual mode

  The above 4 shift directions are pin-selectable
- Shift register circuits are reset when /DISPOFF active

2 DESCRIPTION

The ST8016T is a 160-output segment/common driver IC suitable for driving large/medium scale dot matrix LCD panels, and is used in personal computers/work stations. The ST8016T is good both as a segment driver and a common driver, and it can create a low power consuming, high-resolution LCD.

3 BLOCK DIAGRAM



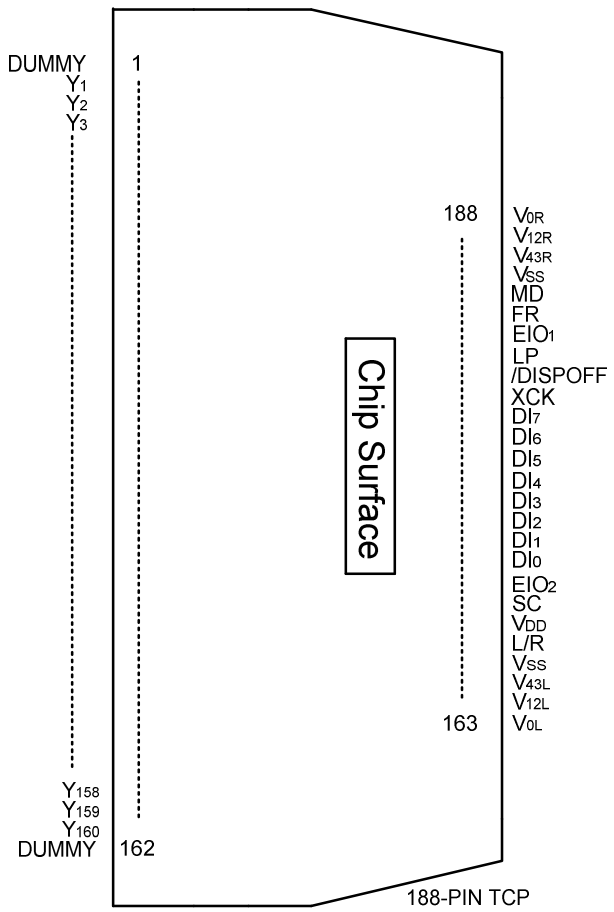
4 FUNCTIONAL OPERATIONS OF EACH BLOCK

BLOCK	FUNCTION
Active Control	In case of segment mode, controls the selection or non-selection of the chip. Following an LP signal input, and after the chip selection signal is input, a selection signal is generated internally until 160 bits of data have been read in. Once data input has been completed, a selection signal for cascade connection is output, and the chip is non-selected. In case of common mode, controls the input/output data of bi-directional pins.
SP Conversion & Data Control	In case of segment mode, keeps input data which are 2 clocks of XCK at 4-bit parallel input mode in latch circuit, or keeps input data which are 1 clock of XCK at 8-bit parallel input mode in latch circuit; after that they are put on the internal data bus 8 bits at a time.
Data Latch Control	In case of segment mode, selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic. For every 16 bits of data read in, the selection signal shifts one bit based on the state of the control circuit.
Data Latch	In case of segment mode, latches the data on the data bus. The latch state of each LCD drive output pin is controlled by the control logic and the data latch control; 160 bits of data are read in 20 sets of 8 bits.
Line Latch/ Shift Register	In case of segment mode, all 160 bits which have been read into the data latch are simultaneously latched at the falling edge of the LP signal, and are output to the level shifter block. In case of common mode, shifts data from the data input pin at the falling edge of the LP signal.
Level Shifter	The logic voltage signal is level-shifted to the LCD drive voltage level, and is output to the driver block.
4-Level Driver	Drives the LCD drive output pins from the line latch/shift register data, and selects one of 4 levels (V_0, V_{12}, V_{43} or V_{SS}) based on the S/C, FR and /DISPOFF signals.
Control Logic	Controls the operation of each block. In case of segment mode, when an LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission is controlled, 160 bits of data are read in, and the chip is non-selected. In case of common mode, controls the direction of data shift.

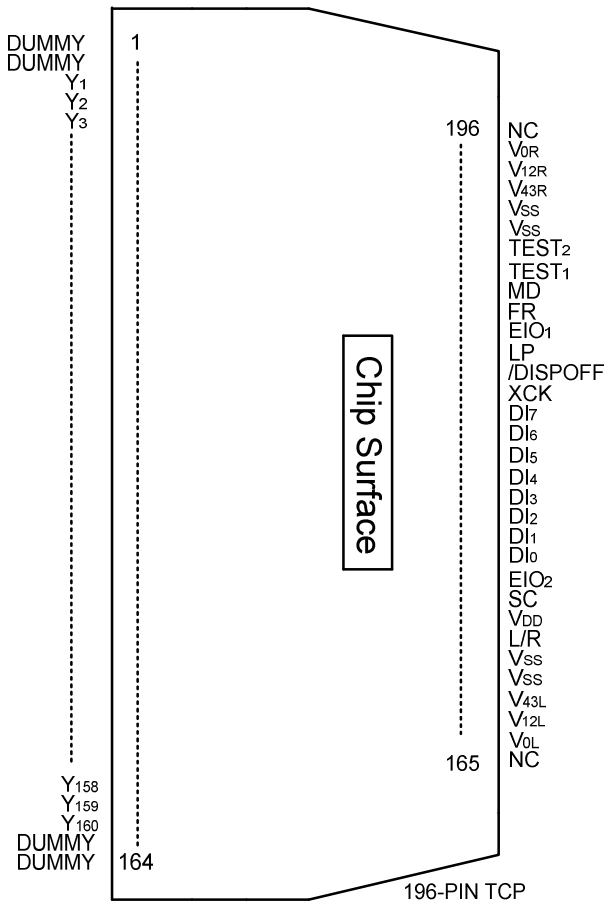
5 PIN DESCRIPTION (TCP TYPE)

SYMBOL	I/O	DESCRIPTION
Y_1-Y_{160}	O	LCD drive output
V_{0L}, V_{0R}	P	Power supply for LCD drive
V_{12L}, V_{12R}	P	Power supply for LCD drive
V_{43L}, V_{43R}	P	Power supply for LCD drive
L/R	I	Display data shift direction selection
V_{DD}	P	Power supply for logic system (+2.5 to +5.5 V)
S/C	I	Segment mode/common mode selection
EIO_2, EIO_1	I/O	Input/output for chip selection at segment mode Shift data input/output for shift register at common mode
DI_0-DI_6	I	Display data input at segment mode
DI_7	I	Display data input at segment mode/Dual mode data input at common mode
XCK	I	Clock input for taking display data at segment mode
/DISPOFF	I	Control input for output of non-select level
LP	I	Latch pulse input for display data at segment mode/ Shift clock input for shift register at common mode
FR	I	AC-converting signal input for LCD drive waveform
MD	I	4 or 8 bits mode selection input
V_{SS}	P	Ground (0 V)
TEST1,TEST2	I	Connect to GND or floating

PS : Detail size see TCP drawing data



ST8016 F2 TCP



ST8016 F3 TCP

6 INPUT/OUTPUT CIRCUITS

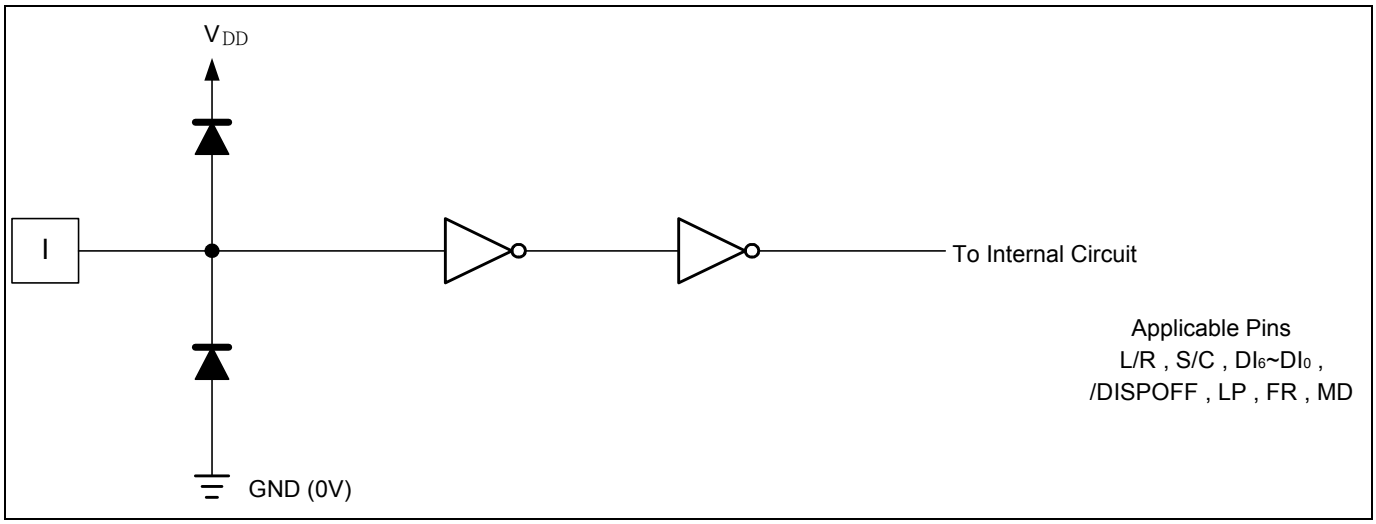


Figure 1 Input Circuit (1)

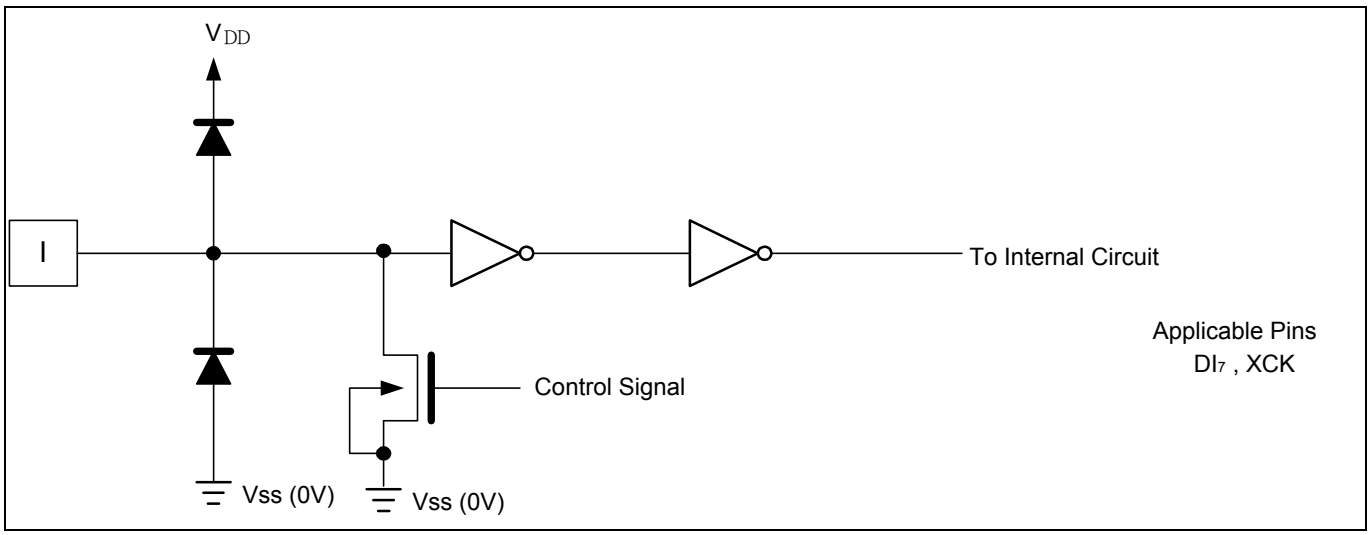


Figure 2 Input Circuit (2)

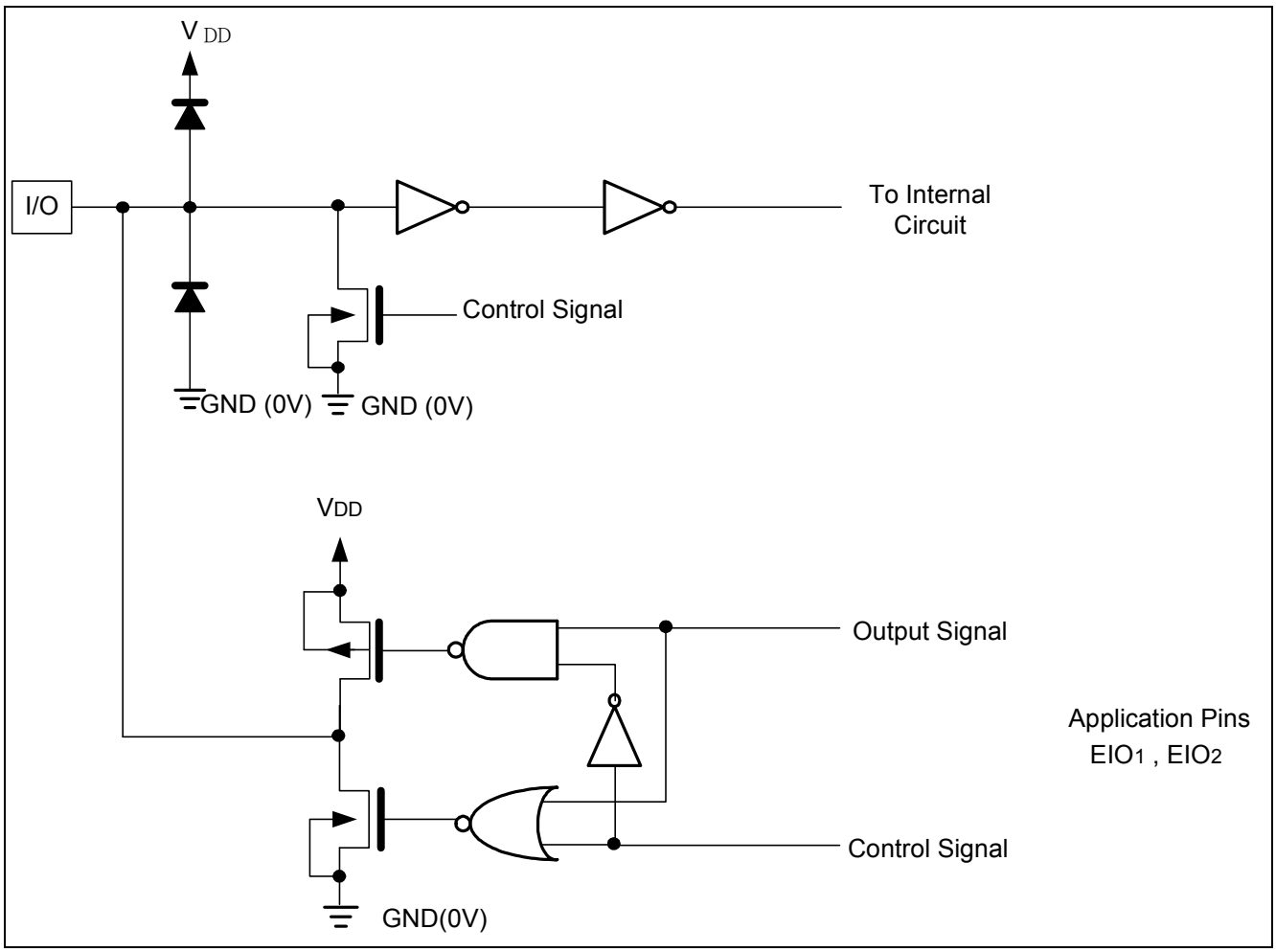


Figure 3 Input/Output Circuit

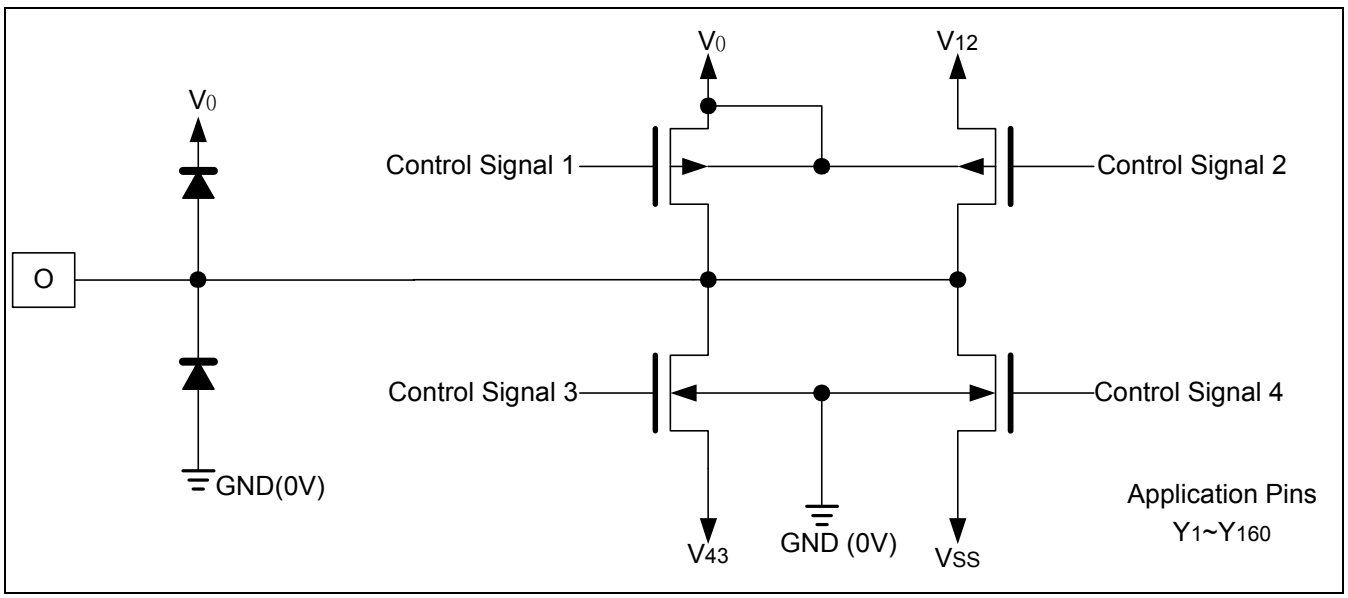


Figure 4 LCD Drive Output Circuit

7 FUNCTIONAL DESCRIPTION

7.1 Pin Functions

(Segment mode)

SYMBOL	FUNCTION
V_{DD}	Logic system power supply pin • Connected to +2.5 to +5.5 V.
GND	Ground pin
LGND	Logic system power ground pin • Do not short LGND with GND and Vss by ITO on LCD panel • Connect it to GND on PCB or FPC.
V_{SS}	Connect to GND by ITO on LCD panel.
V_{0L}, V_{0R} V_{12L}, V_{12R} V_{43L}, V_{43R}	Bias power supply pins for LCD drive voltage • Normally use the bias voltages set by a resistor divider • Ensure that voltages are set such that $V_{SS} < V_{43} < V_{12} < V_0$. • V_{iL} and V_{iR} (i = 0,12, 43) must connect to an external power supply, and supply regular voltage which is assigned by specification for each power pin
DI_7-DI_0	Input pins for display data • In 4-bit parallel mode, DI_3-DI_0 are the display data input pins, and DI_7-DI_4 must be connected to LGND or V_{DD}. • In 8-bit parallel mode, All DI_7-DI_0 pins are the display data input pins. • Refer to section 7.2.2.
XCK	Clock input pin for taking display data • Data is read at the falling edge of the clock pulse.
LP	Latch pulse input pin for display data • Data is latched at the falling edge of the clock pulse.
L/R	Input pin for selecting the reading direction of display data • When set to LGND level "L", data is read sequentially from Y_{160} to Y_1. • When set to V_{DD} level "H", data is read sequentially from Y_1 to Y_{160}. • Refer to section 7.2.2.
/DISPOFF	Control input pin for output of non-select level • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to LGND level "L", the LCD drive output pins (Y_1-Y_{160}) are set to level Vss. • When set to "L", the contents of the line latch are reset, but the display data are read in the data latch regardless of the condition of /DISPOFF. When the /DISPOFF function is canceled the driver outputs non-select level (V_{12} or V_{43}), then outputs the contents of the data latch at the next falling edge of the LP. At that time, if /DISPOFF removal time does not correspond to what is shown in AC characteristics, it cannot output the reading data correctly. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
FR	AC signal input pin for LCD drive waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
MD	Mode selection pin • When set to LGND level "L", 4-bit parallel input mode is set. • When set to VDD level "H", 8-bit parallel input mode is set. • Refer to section 7.2.2.
S/C	Segment mode/common mode selection pin • When set to VDD level "H", segment mode is set.
EIO_1, EIO_2	Input/output pins for chip selection • When L/R input is at LGND level "L", EIO_1 is set for output, and EIO_2 is set for input. • When L/R input is at V_{DD} level "H", $\overline{EIO_1}$ is set for input, and EIO_2 is set for output. • During output, set to "H" while LP • XCK is "H" and after 160 bits of data have been read, set to "L" for one cycle (from falling edge to failing edge of XCK), after which it returns to "H". • During input, the chip is selected while EI is set to "L" after the LP signal is input. The chip is

	non-selected after 160 bits of data have been read.
Y_1 -Y_{160}	LCD drive output pins • Corresponding directly to each bit of the data latch, one level (V_0, V_{12} or V_{43}) is selected and output. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.

(Common mode)

SYMBOL	FUNCTION
V_{DD}	Logic system power supply pin • Connected to +2.5 to +5.5 V.
GND	Ground pin
LGND	Logic system power ground pin • Do not short LGND with GND and Vss by ITO on LCD panel • Connect it to GND on PCB or FPC.
V_{SS}	Connect to GND by ITO on LCD panel.
V_{0L}, V_{0R} V_{12L}, V_{12R} V_{43L}, V_{43R}	Bias power supply pins for LCD drive voltage • Normally use the bias voltages set by a resistor divider. • Ensure that voltages are set such that $V_{SS} < V_{43} < V_{12} < V_0$. • V_{iL} and V_{iR} (i = 0,12, 43) must connect to an external power supply, and supply regular voltage that is assigned by specification for each power pin.
EIO_1	Shift data input/output pin for bi-directional shift register • Output pin when L/R is at LGND level "L', input pin when L/R is at V_{DD} level "H". • When L/R = H, EIO_1 is used as input pin, it will be pulled down. • When L/R = L, EIO_1 is used as output pin, it won't be pulled down. • Refer to section 7.2.2.
EIO_2	Shift data input/output pin for bi-directional shift register • Input pin when L/R is at LGND level "L", output pin when L/R is at V_{DD} level "H". • When L/R = L, EIO_2 is used as input pin, it will be pulled down. • When L/R = H, EIO_2 is used as output pin, it won't be pulled down. • Refer to section 7.2.2.
LP	Shift clock pulse input pin for bi-directional shift register • * Data is shifted at the falling edge of the clock pulse.
L/R	Input pin for selecting the shift direction of bi-directional shift register • Data is shifted from Y_{160} to Y_1 when set to LGND level "L", and data is shifted from Y_1 to Y_{160} when set to V_{DD} level "H". • Refer to section 7.2.2.
/DISPOFF	Control input pin for output of non-select level • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to LGND level "L", the LCD drive output pins (Y_1-Y_{160}) are set to level Vss. • When set to "L", the contents of the shift register are reset to not reading data. When the /DISPOFF function is canceled, the driver outputs non-select level (V_{12} or V_{43}), and the shift data is read at the next falling edge of the LP. At that time, if /DISPOFF removal time does not correspond to what is shown in AC characteristics, the shift data is not read correctly. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
FR	AC signal input pin for LCD drive waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the shift register output signal and the FR signal. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
MD	Mode selection pin • When set to LGND level "L", single mode operation is selected; when set to V_{DD} level "H" dual mode operation is selected. • Refer to section 7.2.2.
DI_7	Dual mode data input pin • According to the data shift direction of the data shift register, data can be input starting from the 81st bit.

	When the chip is used in dual mode, DI_7 will be pulled down. When the chip is used in single mode, DI_7 won't be pulled down(Connect to LGND or V_{DD}, avoiding floating.). • Refer to section 7.2.2.
S/C	Segment mode/common mode selection pin • When set to LGND level "L", common mode is set.
DI_6-DI_0	Not used • Connect DI_6-DI_0 to LGND or V_{DD}, avoiding floating.
XCK	Not used • XCK is pulled down in common mode, so connect to LGND or open.
Y_1 -Y_{160}	LCD drive output pins • Corresponding directly to each bit of the shift register, one level (V_0, V_{12}, V_{43}, or V_{SS}) is selected and output. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.

7.2 Functional Operations

7.2.1 Truth table

(Segment Mode)

FR	LATCH DATA	/DISPOFF	LCD DRIVE OUTPUT VOLTAGE LEVEL (Y1-Y160)
L	L	H	V_{43}
L	H	H	V_{SS}
H	L	H	V_{12}
H	H	H	V_0
X	X	L	V_{SS}

(Common Mode)

FR	LATCH DATA	/DISPOFF	LCD DRIVE OUTPUT VOLTAGE LEVEL (Y1-Y160)
L	L	H	V_{43}
L	H	H	V_0
H	L	H	V_{12}
H	H	H	V_{SS}
X	X	L	V_{SS}

NOTES:

1. $V_{SS} < V_{43} < V_{12} < V_0$
2. L : LGND (0 V), H : V_{DD} (+2.5 to +5.5 V), X : Don't care
3. "Don't care" should be fixed to "H" or "L", avoiding floating.
4. There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver.
5. Supply regular voltage that is assigned by specification for each power pin.

7.2.2 Relationship between the display data and LCD drive output Pins

(Segment Mode)

(a) 4-bit Parallel Input Mode

MD	L/R	EIO_1	EIO_2	DATA INPUT	NUMBER OF CLOCKS						
					40 CLOCK	39 CLOCK	38 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
L	L	Output	Input	DI_0	Y_1	Y_5	Y_9	…	Y_{149}	Y_{153}	Y_{157}
				DI_1	Y_2	Y_6	Y_{10}	…	Y_{150}	Y_{154}	Y_{158}
				DI_2	Y_3	Y_7	Y_{11}	…	Y_{151}	Y_{155}	Y_{159}
				DI_3	Y_4	Y_8	Y_{12}	…	Y_{152}	Y_{156}	Y_{160}
L	H	Input	Output	DI_0	Y_{160}	Y_{156}	Y_{152}	…	Y_{12}	Y_8	Y_4
				DI_1	Y_{159}	Y_{155}	Y_{151}	…	Y_{11}	Y_7	Y_3
				DI_2	Y_{158}	Y_{154}	Y_{150}	…	Y_{10}	Y_6	Y_2
				DI_3	Y_{157}	Y_{153}	Y_{149}	…	Y_9	Y_5	Y_1

(b) 8-bit Parallel Input Mode

MD	L/R	EIO_1	EIO_2	DATA INPUT	NUMBER OF CLOCKS						
					20 CLOCK	19 CLOCK	18 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
H	L	Output	Input	DI_0	Y_1	Y_9	Y_{17}	…	Y_{137}	Y_{145}	Y_{153}
				DI_1	Y_2	Y_{10}	Y_{18}	…	Y_{138}	Y_{146}	Y_{154}
				DI_2	Y_3	Y_{11}	Y_{19}	…	Y_{139}	Y_{147}	Y_{155}
				DI_3	Y_4	Y_{12}	Y_{20}	…	Y_{140}	Y_{148}	Y_{156}
				DI_4	Y_5	Y_{13}	Y_{21}		Y_{141}	Y_{149}	Y_{157}
				DI_5	Y_6	Y_{14}	Y_{22}		Y_{142}	Y_{150}	Y_{158}
				DI_6	Y_7	Y_{15}	Y_{23}		Y_{143}	Y_{151}	Y_{159}
				DI_7	Y_8	Y_{16}	Y_{24}		Y_{144}	Y_{152}	Y_{160}
H	H	Input	Output	DI_0	Y_{160}	Y_{152}	Y_{144}	…	Y_{24}	Y_{16}	Y_8
				DI_1	Y_{159}	Y_{151}	Y_{143}	…	Y_{23}	Y_{15}	Y_7
				DI_2	Y_{158}	Y_{150}	Y_{142}	…	Y_{22}	Y_{14}	Y_6
				DI_3	Y_{157}	Y_{149}	Y_{141}	…	Y_{21}	Y_{13}	Y_5
				DI_4	Y_{156}	Y_{148}	Y_{140}	…	Y_{20}	Y_{12}	Y_4
				DI_5	Y_{155}	Y_{147}	Y_{139}	…	Y_{19}	Y_{11}	Y_3
				DI_6	Y_{154}	Y_{146}	Y_{138}	…	Y_{18}	Y_{10}	Y_2
				DI_7	Y_{153}	Y_{145}	Y_{137}	…	Y_{17}	Y_9	Y_1

(Common Mode)

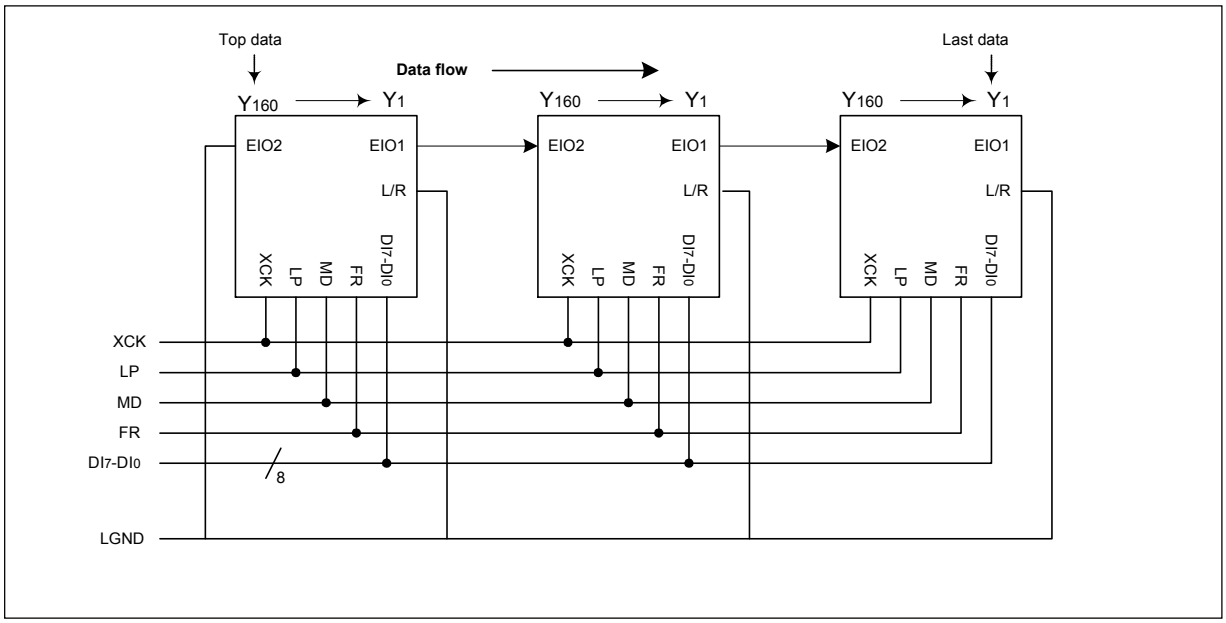
MD	L/R	DATA TRANSFER DIRECTION	EIO_1	EIO_2	DI_7
L (Single)	L	$Y_{160} \rightarrow Y_1$	Output	Input	X
	H	$Y_1 \rightarrow Y_{160}$	Input	Output	X
H (Dual)	L	$Y_{160} \rightarrow Y_{81}$ $Y_{80} \rightarrow Y_1$	Output	Input	Input
	H	$Y_1 \rightarrow Y_{80}$ $Y_{81} \rightarrow Y_{160}$	Input	Output	Input

NOTES:

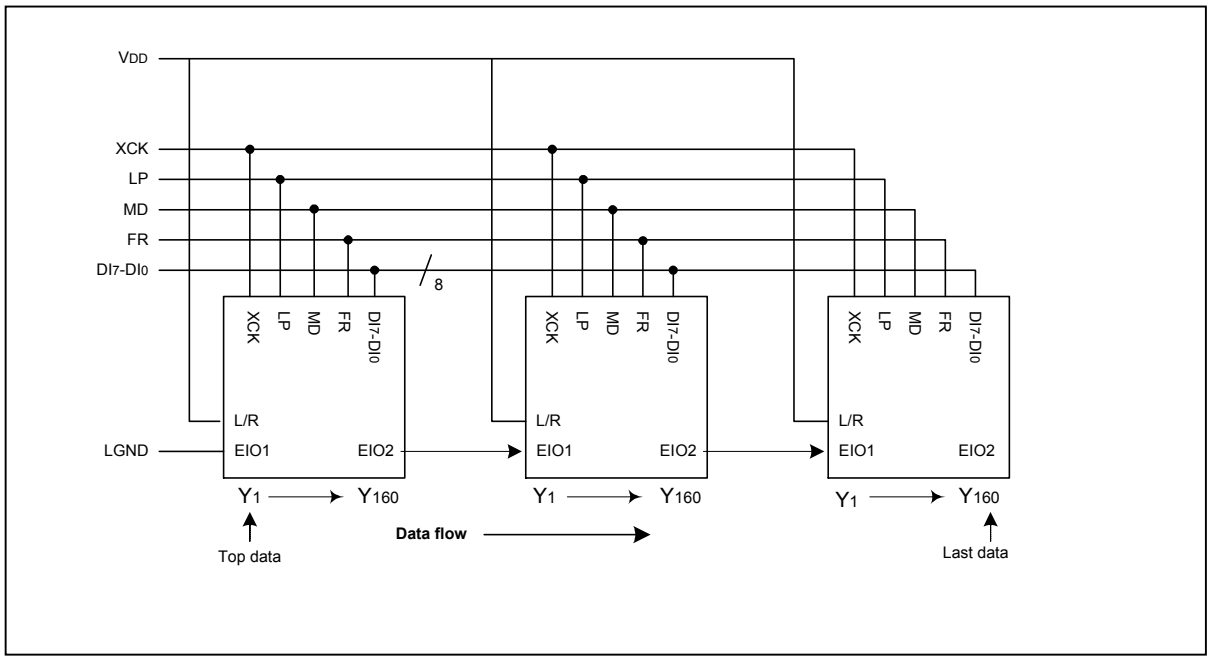
1. L : LGND (0 V), H : V_{DD} (+2.5 to +5.5 V), X : Don't care
2. "Don't care" should be fixed to "H" or "L", avoiding floating.

7.2.3 Connection examples of plural segment drivers

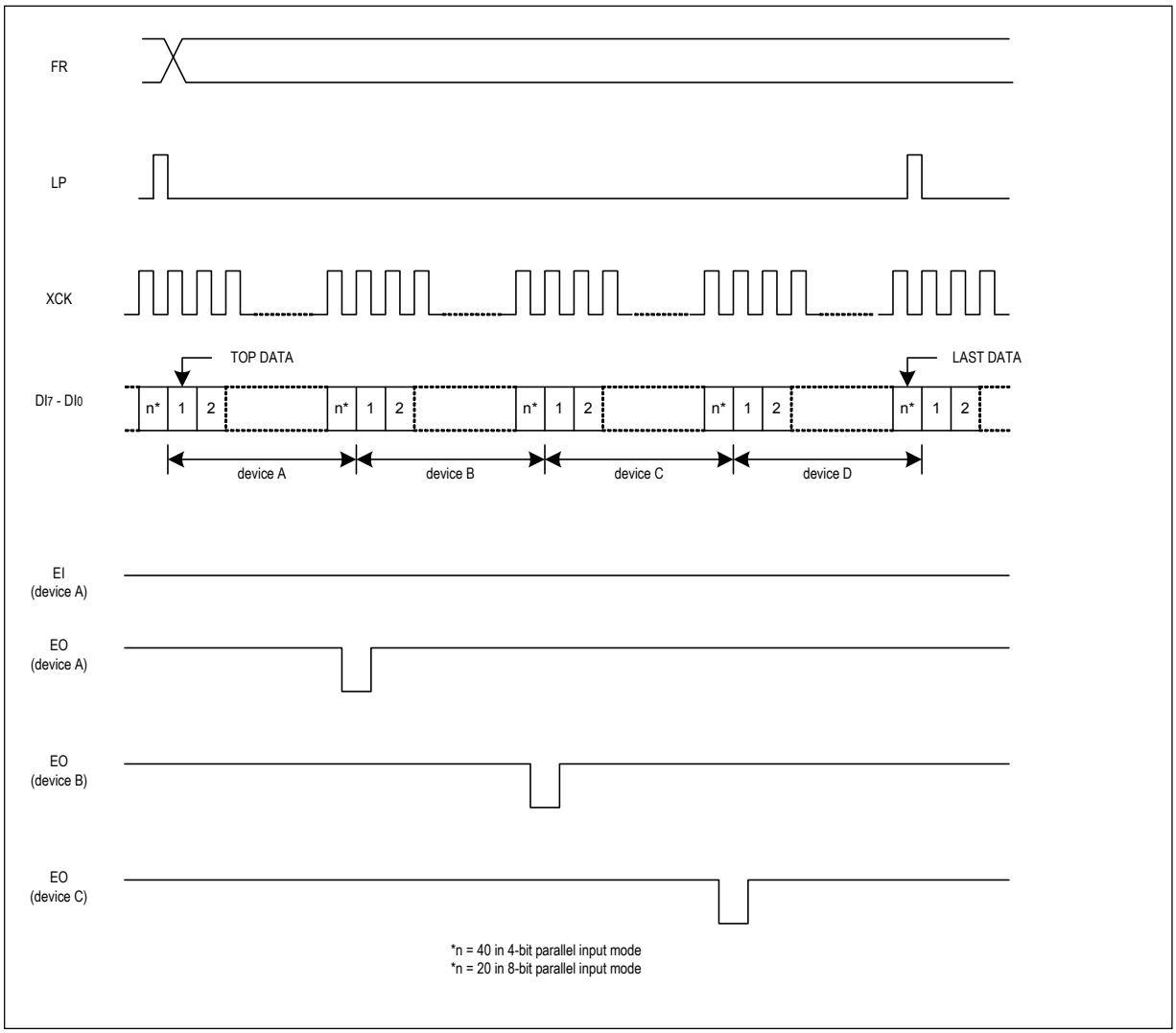
(a) When L/R = "L"



(b) When L/R = "H"

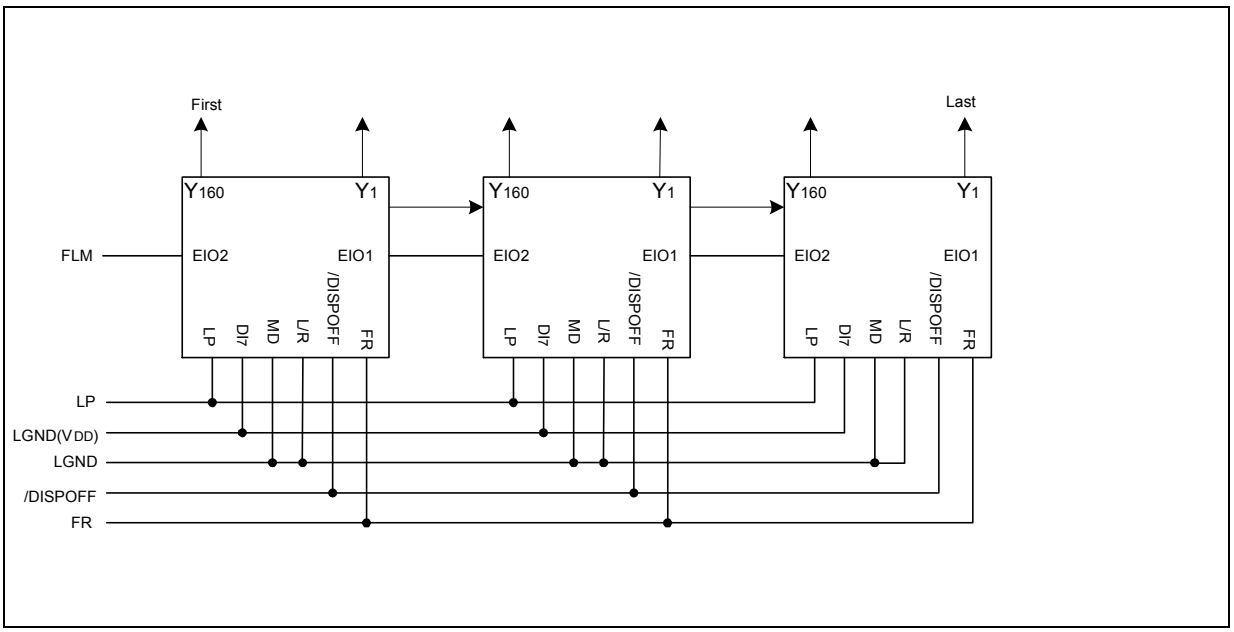


7.2.4 Timing chart of 4-device cascade connection of segment drivers

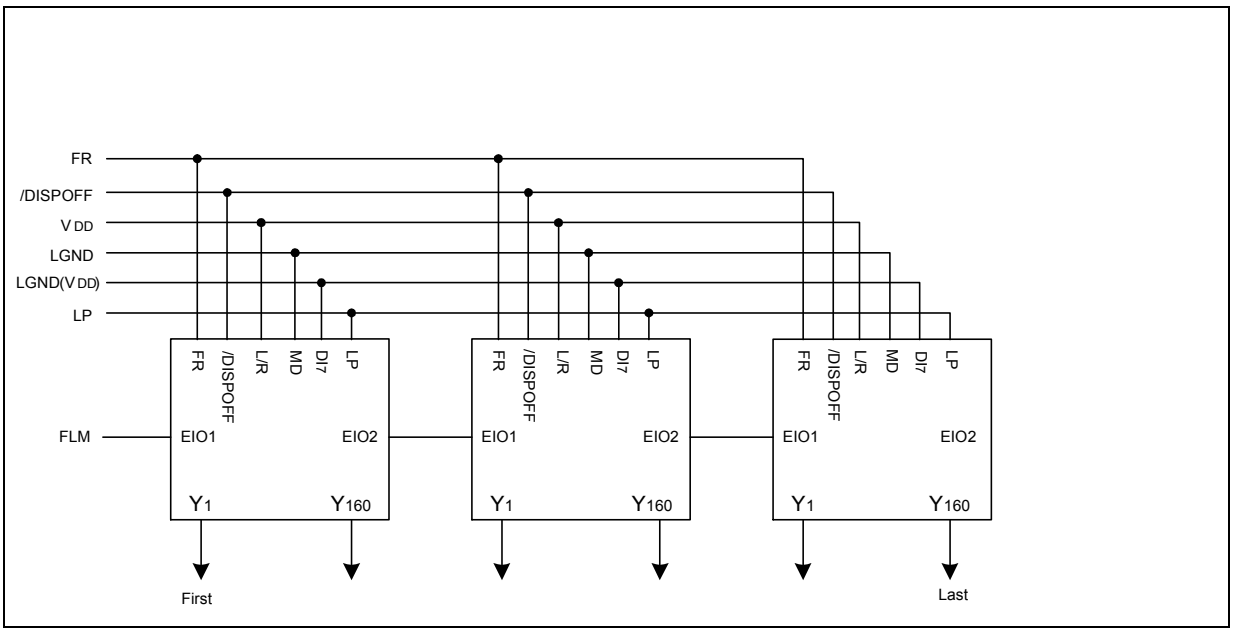


7.2.5 Connection examples for plural common drivers

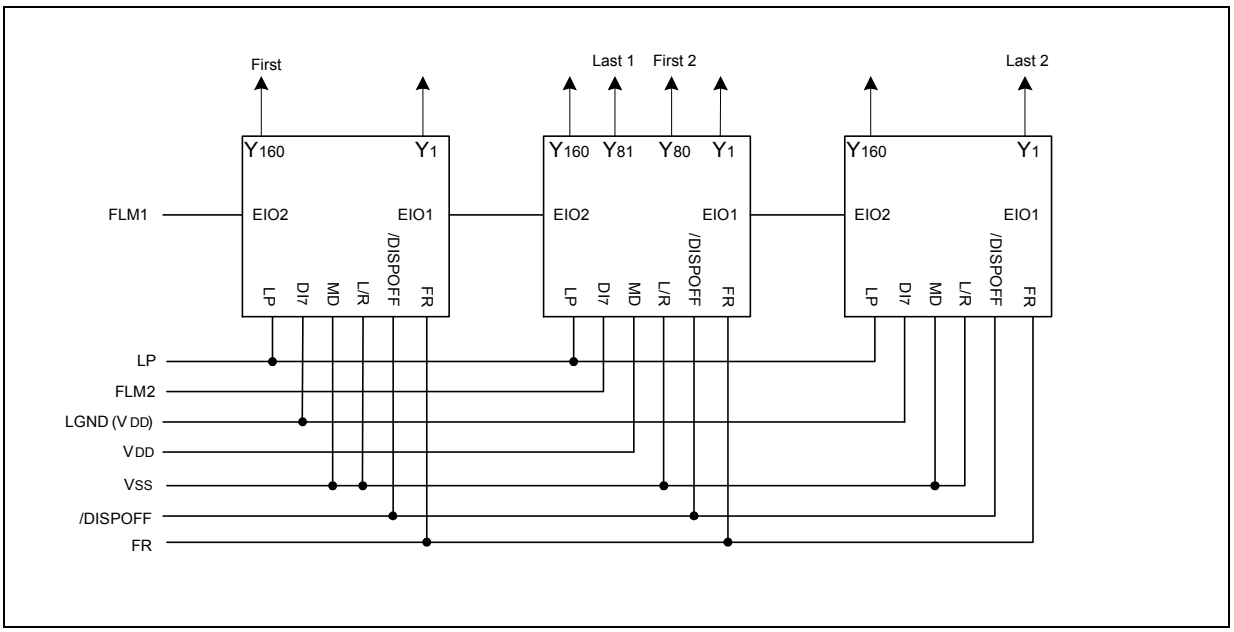
(a) Single Mode (L/R = "L")



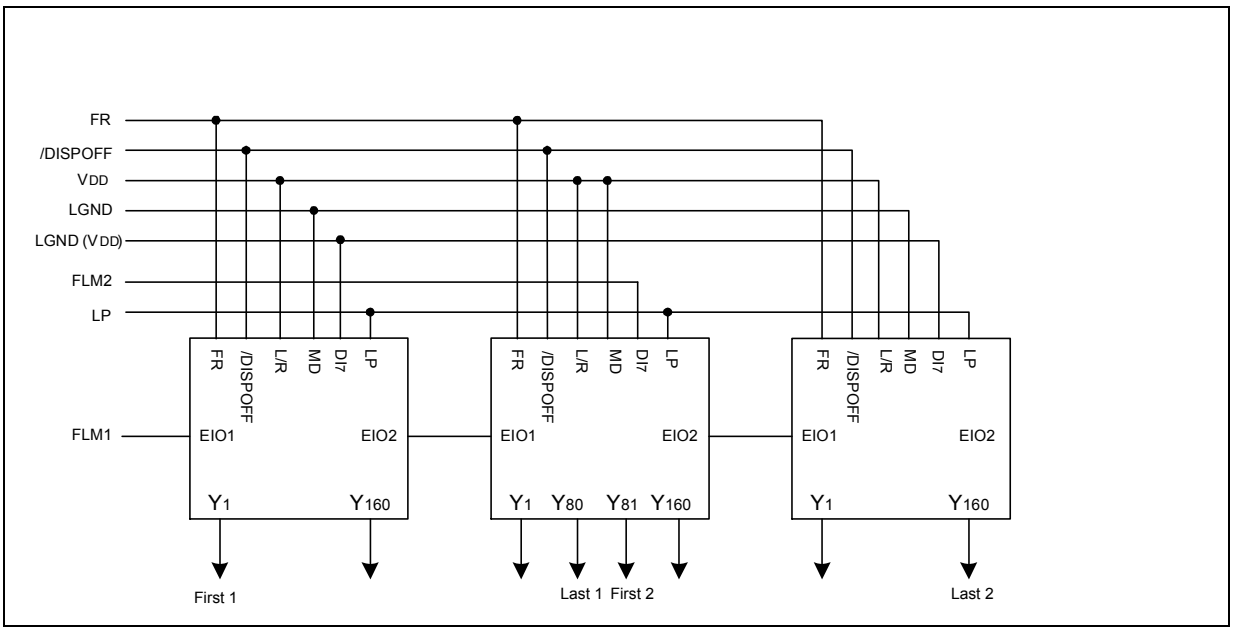
(b) Single Mode (L/R = "H")



(c) Dual Mode (L/R = "L")



(d) Dual mode (L/R = "H")



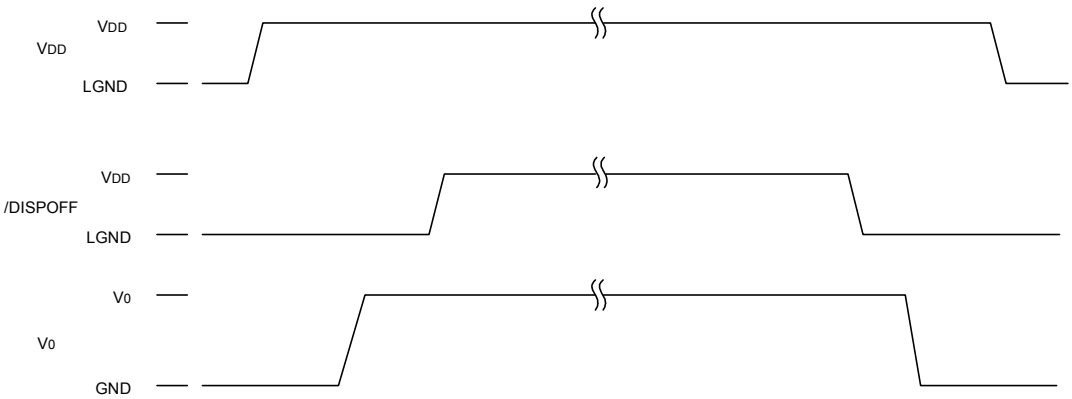
8 PRECAUTIONS

Precautions when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so a high current that may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating may permanently damage it. The details are as follows,

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power
- It is advisable to connect the serial resistor (4.7Ω to 50Ω) or fuse to the LCD drive power V_0 of the system as a current limiter. Set up a suitable value of the resistor in consideration of the display grade.

And when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on /DISPOFF function. After that, cancel the /DISPOFF function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level LGND on /DISPOFF function. Then disconnect the logic system power after disconnecting the LCD drive power.
When connecting the power supply, follow the recommended sequence shown here



.

9 ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	-0.3~ +7.0	V	1,2
Supply voltage (2)	V_0	V_{0L}, V_{0R}	-0.3 ~ +33.0	V	
	V_{12}	V_{12L}, V_{12R}	V_0 -10~ V_0 + 0.3	V	
	V_{43}	V_{43L}, V_{43R}	-0.3 ~ V_{SS} + 10	V	
Input voltage	V_I	DI_7-DI_0, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, /DISPOFF	-0.3 to V_{DD} + 0.3	V	
Storage temperature	T_{STG}		-45 to +125	°C	

NOTES:
1. TA = +25 °C
2. The applicable voltage on logic pins with respect to LGND, high voltage pins with V_{SS} (0 V).

10 RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	+2.5		+5.5	V	1, 2
Supply voltage (2)	V_0	V_{0L}, V_{0R}	+15.0		+30.0	V	
Operating temperature	T_{OPR}		-25		+70	°C	

NOTES:
1. The applicable voltage on logic pins with respect to LGND, high voltage pins with V_{SS} (0 V).
2. Ensure that voltages are set such that $V_{SS} < V_{43} < V_{I2} < V_0$.

11 ELECTRICAL CHARACTERISTICS

11.1 DC Characteristics

(Segment Mode) (LGND =V_{SS} = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = + 15.0 to +30.0 V, T_{OPR} = -25 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		DI_7-DI_0, XCK, LP, L/R FR, MD, S/C, EIO_1, EIO_2, /DISPOFF			$0.2V_{DD}$	V	
Input "High" voltage	V_{IH}			$0.8V_{DD}$			V	
Output "Low" voltage	V_{0L}	I_{OL} = +0.4 mA	EIO_1, EIO_2			+0.4	V	
Output "High" voltage	V_{0H}	I_{OH} = -0.4 mA		V_{DD}-0.4			V	
Input leakage current	I_{LIL}	V_I = LGND	DI_7-DI_0, XCK, LP, L/R FR, MD, S/C, EIO_1, EIO_2, /DISPOFF			-10	µA	
	I_{LIH}	V_I = V_{DD}				+10	µA	
Output resistance	R_{ON}	$\lvert\Delta V_{ON}\rvert$ =0.5V, V_0 = 30 V	Y_1-Y_{160}		1.0	1.5	kΩ	
Standby current	I_{STB}		LGND+GND+VSS			50	µA	1
Supply current (1) (Non-selection)	I_{DD1}		V_{DD}			2.0	mA	2
Supply current (2) (Selection)	I_{DD2}		V_{DD}			7.0	mA	3
Supply current (3)	I_0		V_{0L}, V_{0R}			0.9	mA	4

NOTES:

1. V_{DD} = +5.0 V, V_0 = +30.0 V, Vi = LGND.
2. V_{DD} = +5.0 V, V_0 = +30.0 V, f_{XCK} = 20 MHz, no-load, EI = V_{DD}. The input data is turned over by data taking clock (4-bit parallel input mode).
3. V_{DD} = +5.0 V, V_0 = +30.0 V, f_{XCK} = 20 MHz, no-load, EI = LGND. The input data is turned over by data taking clock (4-bit parallel input mode).
4. V_{DD} = +5.0 V, V_0 = +30.0 V, f_{XCK} = 20MHz, f_{LP} = 20.8 kHz, f_{FR} = 80 Hz, no-load. The input data is turned over by data taking clock (4-bit parallel input mode).

(Common Mode) (LGND =V_{SS} = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = + 15.0 to +30.0 V, T_{OPR} = -25 to +70 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABL E PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		DI_7-DI_0, XCK, LP, L/R FR, MD, S/C, EIO_1, EIO_2, /DISPOFF			$0.2V_{DD}$	V	
Input "High" voltage	V_{IH}			$0.8V_{DD}$			V	
Output "Low" voltage	V_{0L}	I_{OL} = +0.4 mA	EIO_1, EIO_2			+0.4	V	
Output "High" voltage	V_{0H}	I_{OH} = -0.4 mA		V_{DD}-0.4			V	
Input leakage current	I_{LIL}	V_I = LGND	DI_7-DI_0, XCK, LP, L/R FR, MD, S/C, EIO_1, EIO_2, /DISPOFF			-10.0	µA	
	I_{LIH}	V_I = V_{DD}	DI_6-DI_0, LP, L/R, FR, MD, S/C, /DISPOFF			+10.0	µA	
Input pull-down current	I_{PD}	V_I = V_{DD}	DI_7, XCK, EIO_1, EIO_2			100	µA	
Output resistance	R_{ON}	$\lvert\Delta V_{ON}\rvert$ =0.5V, V_0 = 30 V	Y_1-Y_{160}		1.0	1.5	kΩ	
Standby current	I_{SPD}		LGND+GND+VSS			50	µA	1
Supply current (1)	I_{DD}		V_{DD}			80	µA	2
Supply current (2)	I_0		V_{0L}, V_{0R}			130	µA	2

NOTES:

1. V_{DD} = +5.0 V, V_0 = +30.0 V, V_I = LGND
2. V_{DD} = +5.0 V, V_0 = +30.0 V, f_{LP} =20.8 kHz, f_{FR} = 80 Hz, 1/320 duty operation, no-load.

11.2 AC Characteristics

(Segment Mode 1) (LGND =V_{SS} = 0 V, V_{DD} = +2.5 to +3.0 V, V_0 = + 15.0 to +30.0 V, T_{OPR} = -25 10+70 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R,t_F ≤ 11ns	125			ns	1
Shift clock "H" pulse width	t_{WCKH}		51			ns	
Shift clock "L" pulse width	t_{WCKL}		51			ns	
Data setup time	t_{DS}		30			ns	
Data hold time	t_{DH}		40			ns	
Latch pulse "H" pulse width	t_{WLPH}		51			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		51			ns	
Latch pulse rise to shift clock rise time	t_{LS}		51			ns	
Latch pulse fall to shift clock fall time	t_{LH}		51			ns	
Enable setup time	t_S		36			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			78	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

NOTES:
1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Segment Mode 2) (LGND =V_{SS} = 0 V, V_{DD} = +5.0±0.5 V, V_0 = + 15.0 to +30.0 V, T_{OPR} = -25 to +70 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R,t_F ≤ 10ns	66			ns	1
Shift clock "H" pulse width	t_{WCKH}		23			ns	
Shift clock "L" pulse width	t_{WCKL}		23			ns	
Data setup time	t_{DS}		15			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		50			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			41	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

NOTES:
1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Segment Mode 3) (LGND =V_{SS} = 0 V, V_{DD} = +3.0 to +4.5 V, V_0 = + 15.0 to +30.0 V, T_{OPR} = -25 10+70 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R,t_F ≤ 10ns	82			ns	1
Shift clock "H" pulse width	t_{WCKH}		28			ns	
Shift clock "L" pulse width	t_{WCKL}		28			ns	
Data setup time	t_{DS}		20			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		51			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			57	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

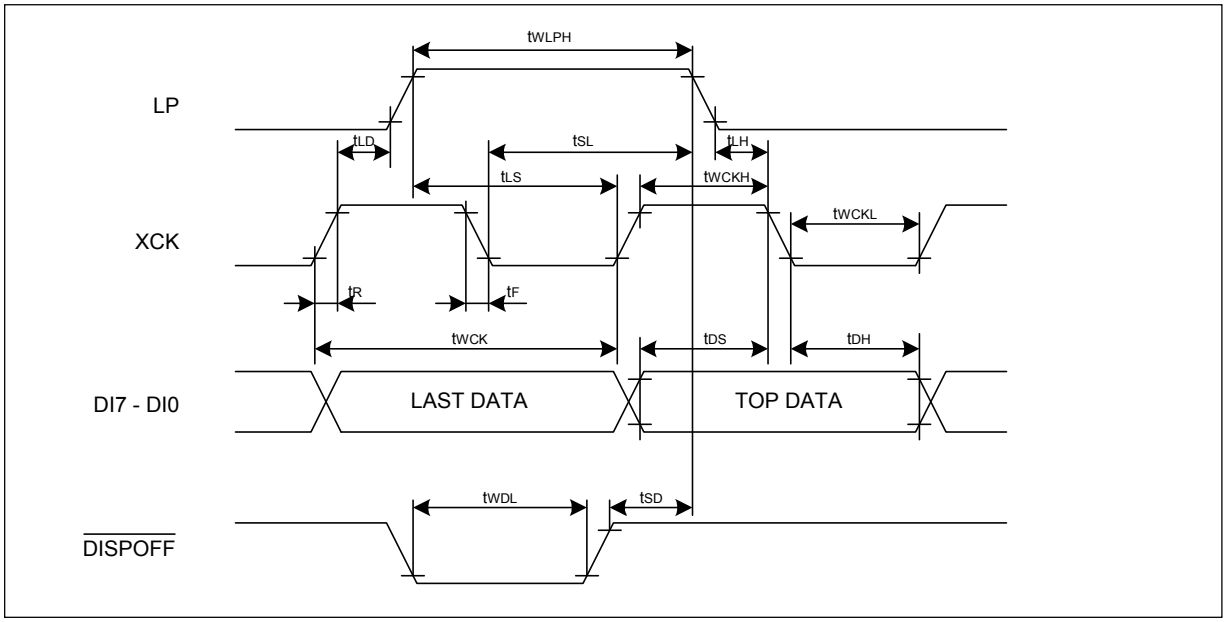
NOTES:

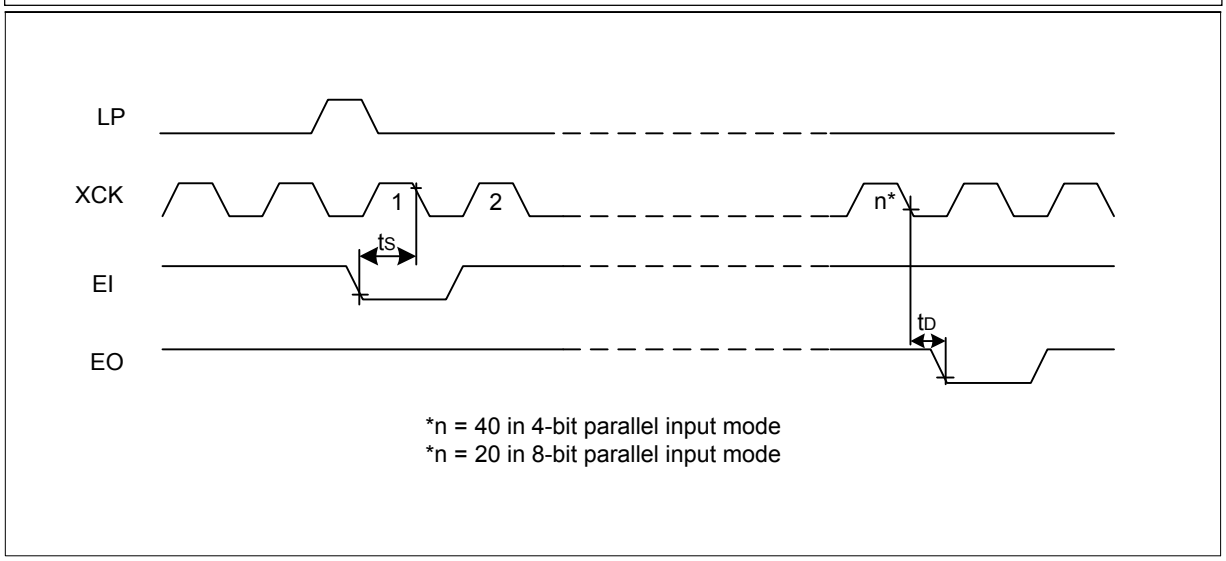
1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Common Mode) (LGND =V_{SS} = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = +15.0 to +30.0 V, T_{OPR} = -25 to +70° C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Shift clock period	t_{WLP}	t_R,t_F ≤ 20ns	250			ns
Shift clock "H" pulse width	t_{WLPH}	V_{DD} = +5.0± 0.5V	15			ns
		V_{DD} = +2.5+ 4.5V	30			ns
Data setup time	t_{SU}		30			ns
Data hold time	t_H		50			ns
Input signal rise time	t_R				50	ns
Input signal fall time	t_F				50	ns
DISPOFF removal time	t_{SD}		100			ns
DISPOFF "L" pulse width	t_{WDL}		1.2			µs
Output delay time (1)	t_{DL}	CL = 15 pF			200	ns
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs

11.3 Timing Chart of Segment Mode





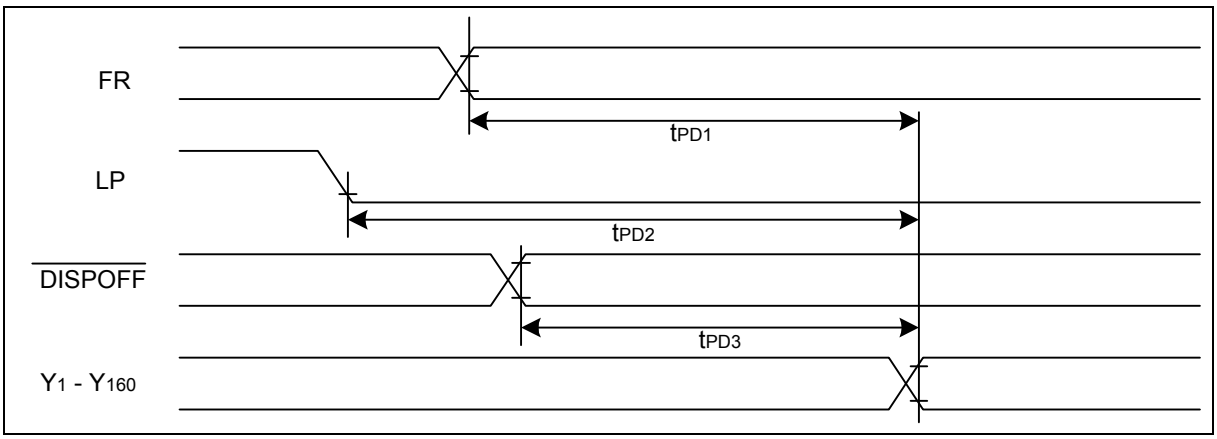
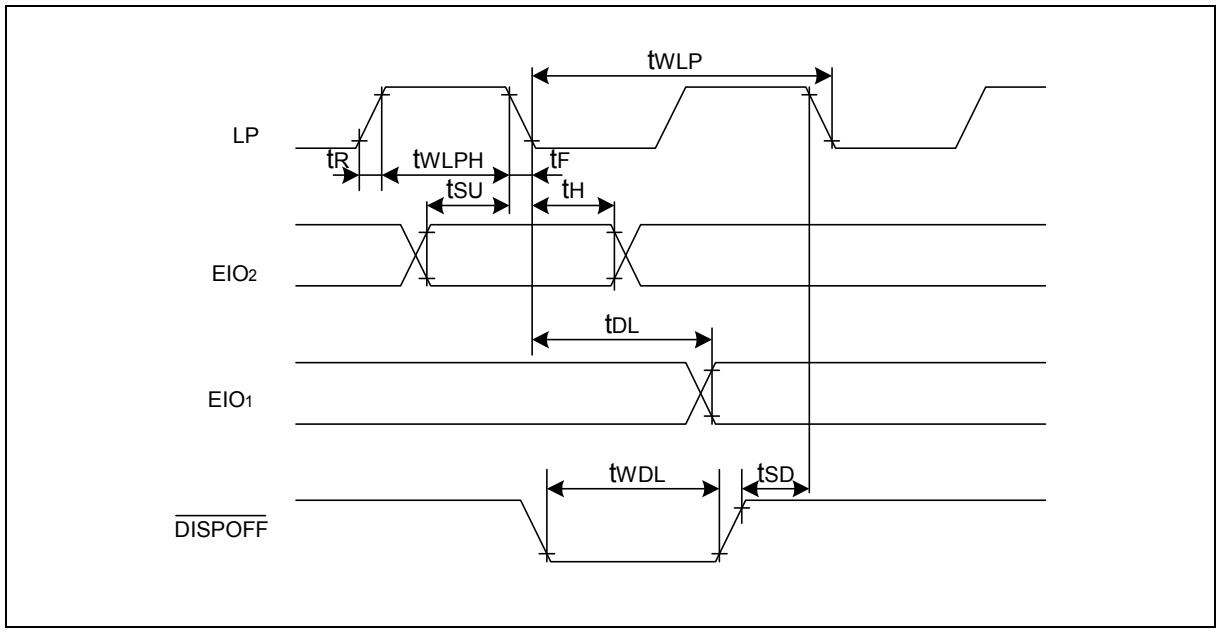
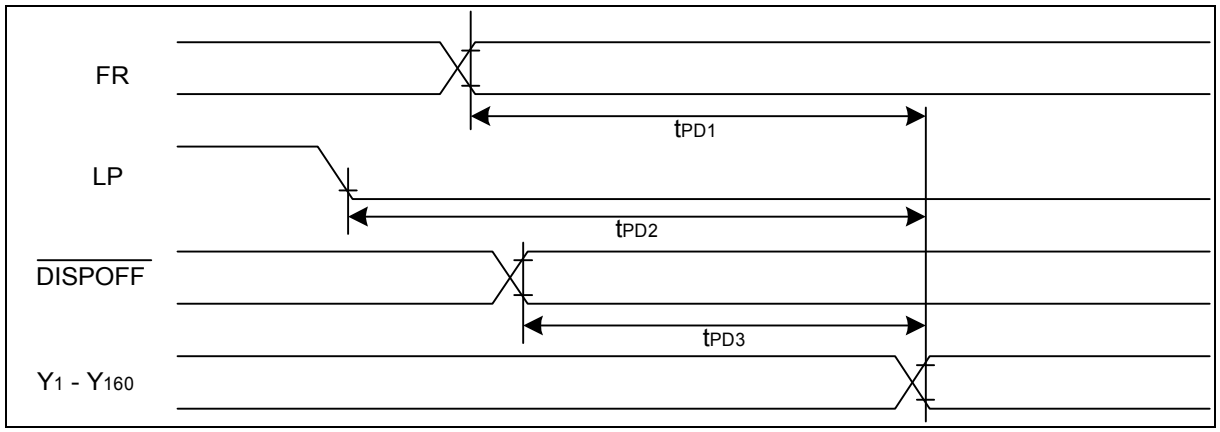


Fig. 8 Timing Characteristics (3)

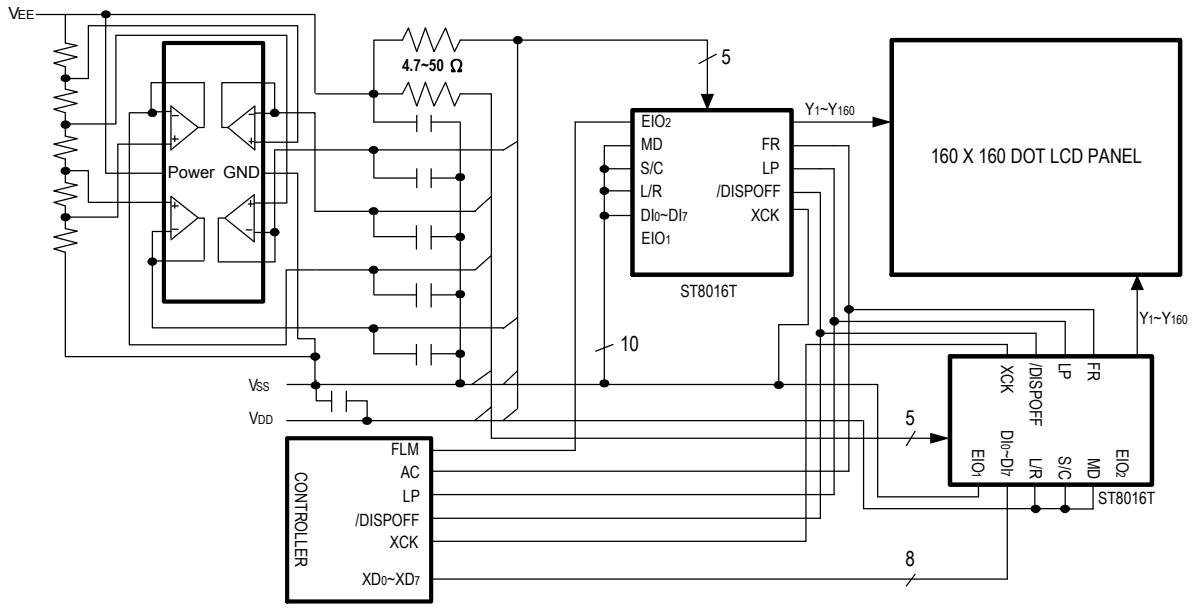
11.4 Timing Chart of Common Mode



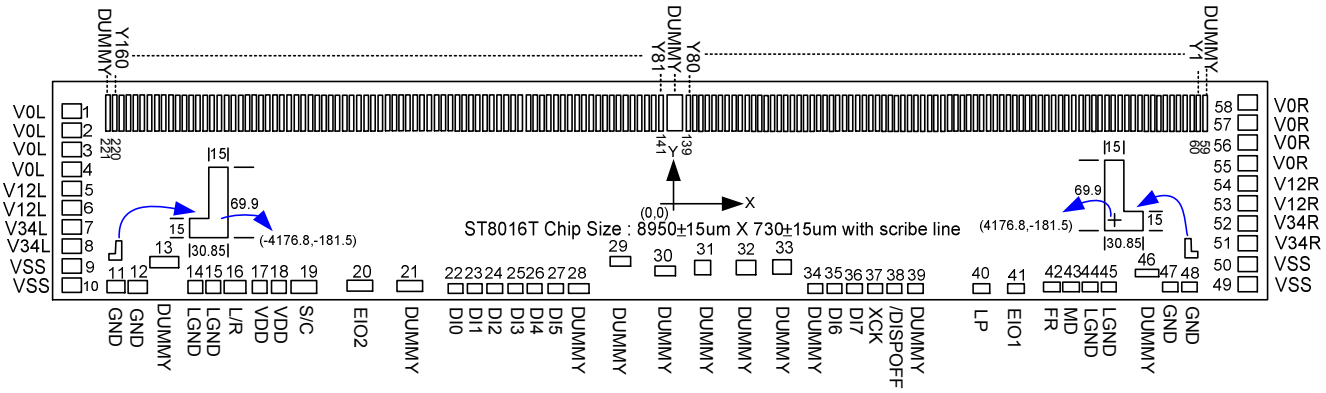


12 APPLICATION CIRCUIT

12.1 Application Circuit for Module



13 PAD DIAGRAM



Unit: um

PIN#	Name	X	Y	PIN#	Name	X	Y
1	V0L	-4357.250	266.850	32	DUMMY	614.425	-217.725
2	V0L	-4357.250	207.550	33	DUMMY	878.050	-220.475
3	V0L	-4357.250	148.250	34	DUMMY	1264.175	-263.100
4	V0L	-4357.250	88.950	35	DI6	1425.350	-263.100
5	V12L	-4357.250	29.650	36	DI7	1586.650	-263.100
6	V12L	-4357.250	-29.650	37	XCK	1751.250	-263.100
7	V34L	-4357.250	-88.950	38	/DISPOFF	1912.550	-263.100
8	V34L	-4357.250	-148.250	39	DUMMY	2116.875	-263.100
9	VSS	-4357.250	-207.550	40	LP	2509.450	-263.100
10	VSS	-4357.250	-266.850	41	EIO1	2845.600	-263.100
11	GND	-4190.000	-263.150	42	FR	3195.300	-263.100
12	GND	-4065.200	-263.150	43	MD	3356.600	-263.100
13	DUMMY	-3906.700	-209.050	44	LGND	3493.050	-263.150
14	LGND	-3600.500	-263.150	45	LGND	3600.500	-263.150
15	LGND	-3493.050	-263.150	46	DUMMY	3906.700	-209.050
16	L/R	-3357.200	-263.100	47	GND	4065.200	-263.150
17	VDD	-3223.550	-263.150	48	GND	4190.000	-263.150
18	VDD	-3116.100	-263.150	49	VSS	4357.250	-266.850
19	S/C	-2978.650	-263.100	50	VSS	4357.250	-207.550
20	EIO2	-2635.050	-263.100	51	V34R	4357.250	-148.250
21	DUMMY	-2264.675	-263.100	52	V34R	4357.250	-88.950
22	DI0	-1872.100	-263.100	53	V12R	4357.250	-29.650
23	DI1	-1710.800	-263.100	54	V12R	4357.250	29.650
24	DI2	-1546.200	-263.100	55	V0R	4357.250	88.950
25	DI3	-1384.900	-263.100	56	V0R	4357.250	148.250
26	DI4	-1220.300	-263.100	57	V0R	4357.250	207.550
27	DI5	-1059.000	-263.100	58	V0R	4357.250	266.850
28	DUMMY	-883.300	-263.100	59	DUMMY	4237.000	250.100
29	DUMMY	-527.800	-224.400	60	Y1	4187.000	250.100
30	DUMMY	-161.075	-227.675	61	Y2	4135.000	250.100
31	DUMMY	228.825	-217.725	62	Y3	4083.000	250.100

63	Y4	4031.000	250.100	111	Y52	1535.000	250.100
64	Y5	3979.000	250.100	112	Y53	1483.000	250.100
65	Y6	3927.000	250.100	113	Y54	1431.000	250.100
66	Y7	3875.000	250.100	114	Y55	1379.000	250.100
67	Y8	3823.000	250.100	115	Y56	1327.000	250.100
68	Y9	3771.000	250.100	116	Y57	1275.000	250.100
69	Y10	3719.000	250.100	117	Y58	1223.000	250.100
70	Y11	3667.000	250.100	118	Y59	1171.000	250.100
71	Y12	3615.000	250.100	119	Y60	1119.000	250.100
72	Y13	3563.000	250.100	120	Y61	1067.000	250.100
73	Y14	3511.000	250.100	121	Y62	1015.000	250.100
74	Y15	3459.000	250.100	122	Y63	963.000	250.100
75	Y16	3407.000	250.100	123	Y64	911.000	250.100
76	Y17	3355.000	250.100	124	Y65	859.000	250.100
77	Y18	3303.000	250.100	125	Y66	807.000	250.100
78	Y19	3251.000	250.100	126	Y67	755.000	250.100
79	Y20	3199.000	250.100	127	Y68	703.000	250.100
80	Y21	3147.000	250.100	128	Y69	651.000	250.100
81	Y22	3095.000	250.100	129	Y70	599.000	250.100
82	Y23	3043.000	250.100	130	Y71	547.000	250.100
83	Y24	2991.000	250.100	131	Y72	495.000	250.100
84	Y25	2939.000	250.100	132	Y73	443.000	250.100
85	Y26	2887.000	250.100	133	Y74	391.000	250.100
86	Y27	2835.000	250.100	134	Y75	339.000	250.100
87	Y28	2783.000	250.100	135	Y76	287.000	250.100
88	Y29	2731.000	250.100	136	Y77	235.000	250.100
89	Y30	2679.000	250.100	137	Y78	183.000	250.100
90	Y31	2627.000	250.100	138	Y79	131.000	250.100
91	Y32	2575.000	250.100	139	Y80	79.000	250.100
92	Y33	2523.000	250.100	140	DUMMY	0.000	250.100
93	Y34	2471.000	250.100	141	Y81	-79.000	250.100
94	Y35	2419.000	250.100	142	Y82	-131.000	250.100
95	Y36	2367.000	250.100	143	Y83	-183.000	250.100
96	Y37	2315.000	250.100	144	Y84	-235.000	250.100
97	Y38	2263.000	250.100	145	Y85	-287.000	250.100
98	Y39	2211.000	250.100	146	Y86	-339.000	250.100
99	Y40	2159.000	250.100	147	Y87	-391.000	250.100
100	Y41	2107.000	250.100	148	Y88	-443.000	250.100
101	Y42	2055.000	250.100	149	Y89	-495.000	250.100
102	Y43	2003.000	250.100	150	Y90	-547.000	250.100
103	Y44	1951.000	250.100	151	Y91	-599.000	250.100
104	Y45	1899.000	250.100	152	Y92	-651.000	250.100
105	Y46	1847.000	250.100	153	Y93	-703.000	250.100
106	Y47	1795.000	250.100	154	Y94	-755.000	250.100
107	Y48	1743.000	250.100	155	Y95	-807.000	250.100
108	Y49	1691.000	250.100	156	Y96	-859.000	250.100
109	Y50	1639.000	250.100	157	Y97	-911.000	250.100
110	Y51	1587.000	250.100	158	Y98	-963.000	250.100

159	Y99	-1015.000	250.100	191	Y131	-2679.000	250.100
160	Y100	-1067.000	250.100	192	Y132	-2731.000	250.100
161	Y101	-1119.000	250.100	193	Y133	-2783.000	250.100
162	Y102	-1171.000	250.100	194	Y134	-2835.000	250.100
163	Y103	-1223.000	250.100	195	Y135	-2887.000	250.100
164	Y104	-1275.000	250.100	196	Y136	-2939.000	250.100
165	Y105	-1327.000	250.100	197	Y137	-2991.000	250.100
166	Y106	-1379.000	250.100	198	Y138	-3043.000	250.100
167	Y107	-1431.000	250.100	199	Y139	-3095.000	250.100
168	Y108	-1483.000	250.100	200	Y140	-3147.000	250.100
169	Y109	-1535.000	250.100	201	Y141	-3199.000	250.100
170	Y110	-1587.000	250.100	202	Y142	-3251.000	250.100
171	Y111	-1639.000	250.100	203	Y143	-3303.000	250.100
172	Y112	-1691.000	250.100	204	Y144	-3355.000	250.100
173	Y113	-1743.000	250.100	205	Y145	-3407.000	250.100
174	Y114	-1795.000	250.100	206	Y146	-3459.000	250.100
175	Y115	-1847.000	250.100	207	Y147	-3511.000	250.100
176	Y116	-1899.000	250.100	208	Y148	-3563.000	250.100
177	Y117	-1951.000	250.100	209	Y149	-3615.000	250.100
178	Y118	-2003.000	250.100	210	Y150	-3667.000	250.100
179	Y119	-2055.000	250.100	211	Y151	-3719.000	250.100
180	Y120	-2107.000	250.100	212	Y152	-3771.000	250.100
181	Y121	-2159.000	250.100	213	Y153	-3823.000	250.100
182	Y122	-2211.000	250.100	214	Y154	-3875.000	250.100
183	Y123	-2263.000	250.100	215	Y155	-3927.000	250.100
184	Y124	-2315.000	250.100	216	Y156	-3979.000	250.100
185	Y125	-2367.000	250.100	217	Y157	-4031.000	250.100
186	Y126	-2419.000	250.100	218	Y158	-4083.000	250.100
187	Y127	-2471.000	250.100	219	Y159	-4135.000	250.100
188	Y128	-2523.000	250.100	220	Y160	-4187.000	250.100
189	Y129	-2575.000	250.100	221	DUMMY	-4237.000	250.100
190	Y130	-2627.000	250.100				

13.1 Gold Bump size (unit: um)

Pad No.	X	Y	Area (um^2)
1~10,49~58	87.50	44.30	3876.2500
11,12,47,48	109.80	42.30	4644.5400
13,46	160.20	33.30	5334.6600
1415,17,18,44,45	92.50	42.30	3912.7500
16,19,20,22~27,35~38,40~43	131.30	42.40	5567.1200
21,39	152.35	42.40	6459.6400
28	165.80	42.40	7029.9200
29	94.30	44.40	4186.9200
30	103.85	37.85	3930.7225
31,32	85.65	57.75	4946.2875
33	117.20	52.25	6123.7000
34	136.75	42.40	5798.2000
59,221	33.00	81.00	2673.0000
60~139,141~220	37.00	81.00	2997.0000
140	91.00	81.00	7371.0000

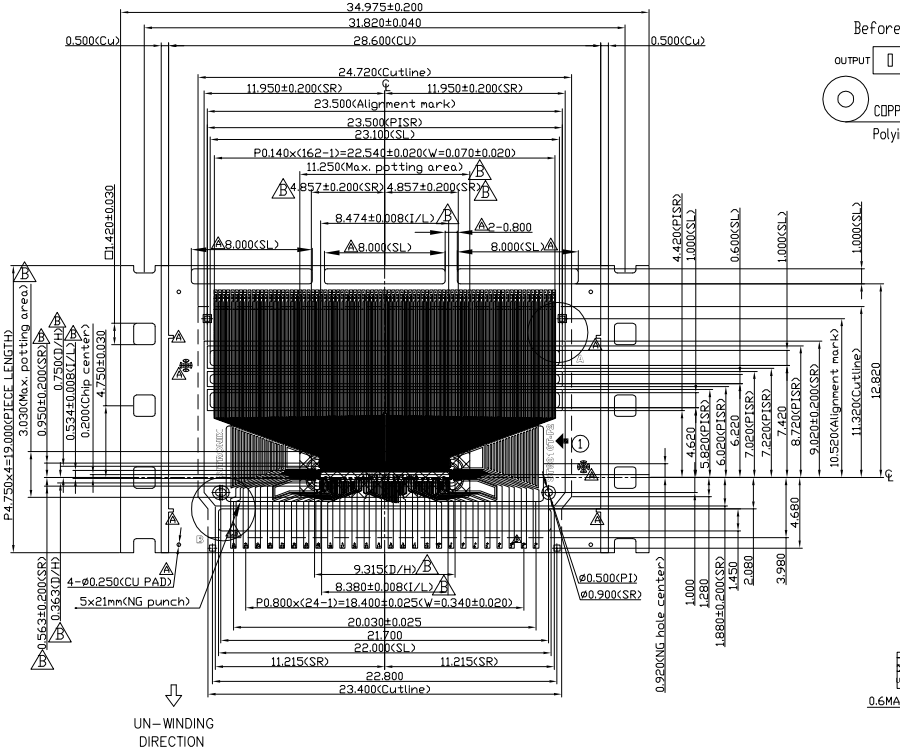
Wafer thickness = 480±20um, Bump pad height (pad 1~215) = 15um, strength=30g

14 REVISION

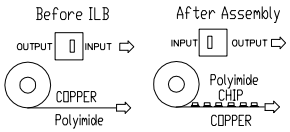
REVISION	DESCRIPTION	PAGE	DATE
0.10	First release	1-27	2006/12/11
0.11	Change Max. operating voltage to +30.0V Change Standby Current Application Pin to LGND+GND+VSS	1-27	2007/04/20
0.12	Modify operating temperature to 70°C	16-19	2007/10/29

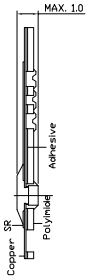
RevNo.	Revision note.	Date
△		

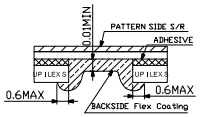
COPPER VIEW

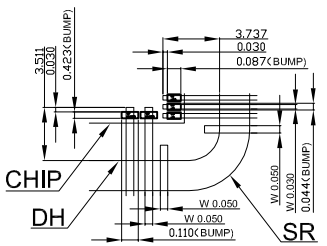


UN-WINDING DIRECTION

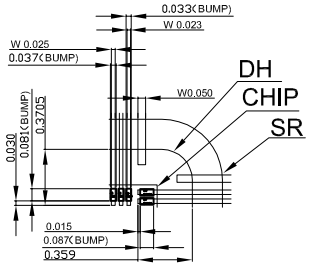




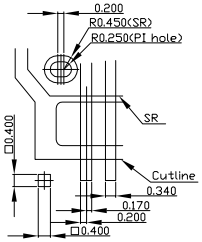




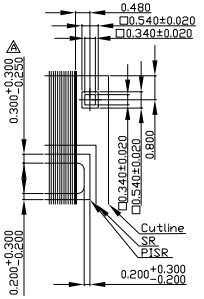
Detail of inner lead(input) Ⓑ
Scale 10:1



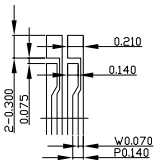
Detail of inner lead(output) Ⓑ
Scale 10:1



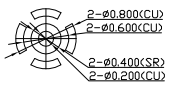
Detail B
Scale 2:1



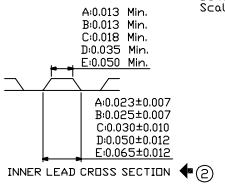
Detail A
Scale 2:1



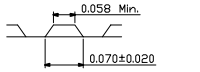
Detail of testpad
Scale 5:1



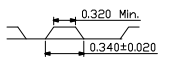
Detail of SR Alignment mark
Scale 5:1



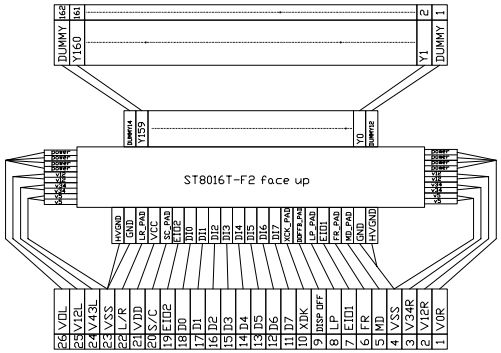
INNER LEAD CROSS SECTION ②



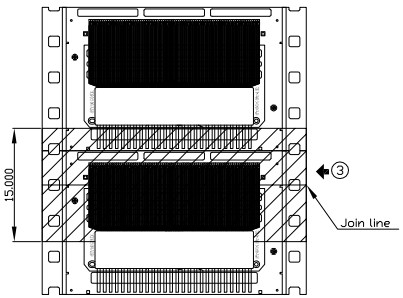
OUTPUT SIDE OUTER LEAD SECTION



INPUT SIDE OUTER LEAD SECTION



PIN ASSIGNMENT Ⓑ



③

Material Description

1. Spacer Tape Material	Polyester(PET)		ATECT
Leader Tape Material	Polyetherimide (PEI)		UBE Ⓐ
PKG Reel Size	405mm		Daiichi
Polyimide	UPILEX-S	75±6 um	UBE
Adhesive	#7100	12±3 um	Toray
Copper	FQ-VLP	18±5 um	
Pre-plating	Sn	0.21±0.05 um	
Solder Resist	AE-70-M11	26±14 um	Ajinomoto
Solder Resist Tolerance: ±0.200mm			
Flex coat	FS-100L	MIN.10um	

2. Flex coating is SUPER-U(U-FLEX).
3. ALL CHAMFER IS R0.200mm.
4. ALL OTHER DIMENSIONAL TOLERANCES ARE 0.05mm, UNLESS OTHERWISE NOTED.
5. 4 SPROCKET HOLES (35SW) FOR 1TAPESITE.
6. IL Min. Pitch 49um Min Space 26um ; Pattern Min. Pitch 50um Min Space 25um Ⓑ
7. Tape vendor & Assembly defect punch size 5x21mm.
8. INNER LEAD WIDTH MEASURE LOCTION: BUMP CENTER.
9. GENERAL TOLERANCE = ±0.050 mm Ⓐ

L1_Copper ■ L2_SOLDER RESIST ■ L3_PUNCH ■ L31_SECOND PUNCH ■ OTHER:FOLLOW CUSTOMER LAYER | Change Ⓑ | Date 95.12.05

DWG NO:	C/P/N: ST8016T-F2	SIMPAL DWG NO:	ST018A-03
Designed by-date: ﾒｲﾅﾘ 95.12.05	Checked by-date:	Approved by date:	TOLERANCE: x ± x.xx ± x.x x.xxx±

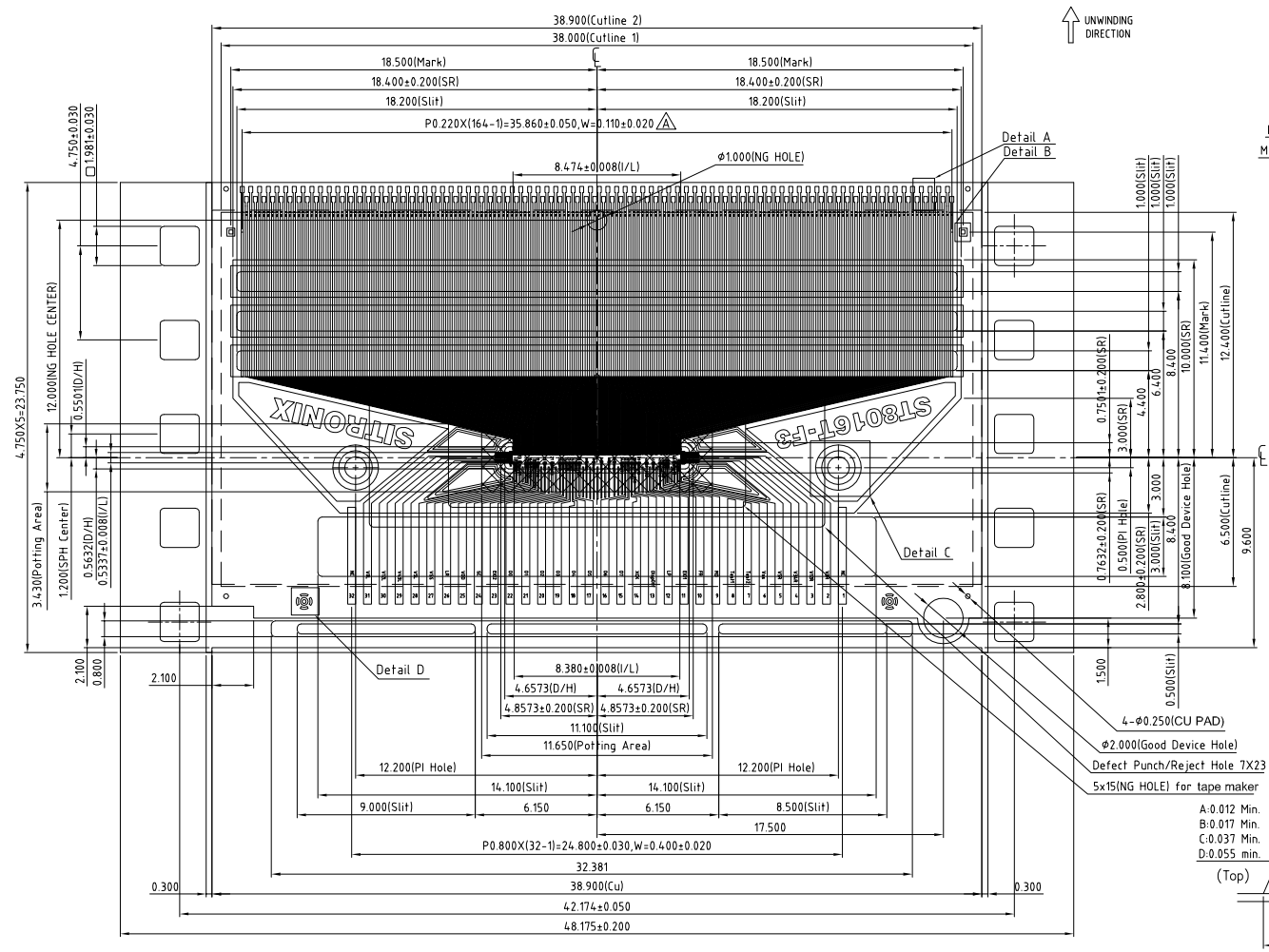
SIMPAL ELECTRONICS CO.,LTD

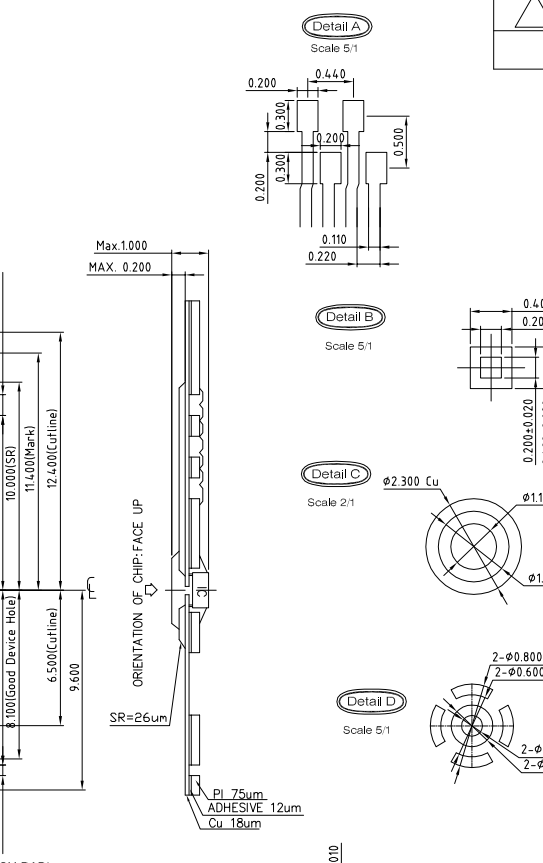
Drawing Name: PATTERN MEASURE DRAWING

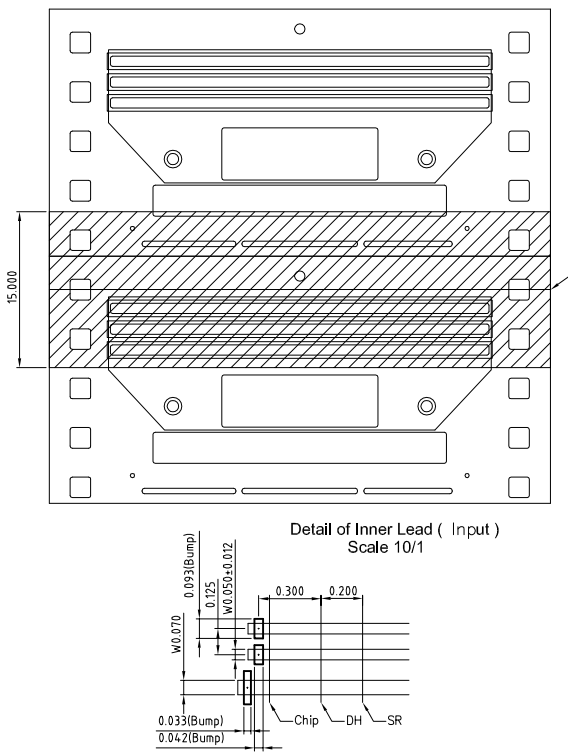
Edition:	Sheet:	Drawing Scale:	Drawing Unit:
A	1/2	1/1	mm

Time:

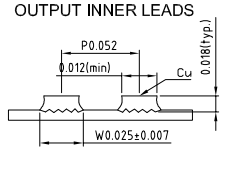
RevNo.	Revision note.	Date
△		



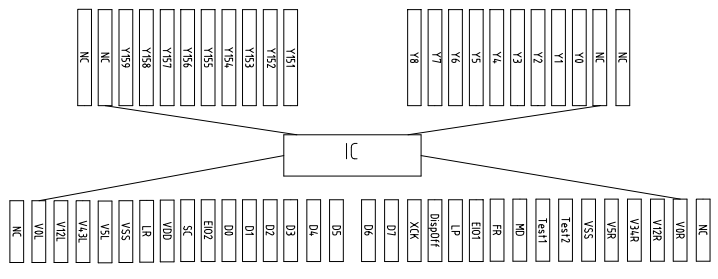


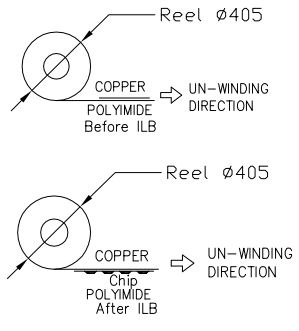


CROSS SECTION OF OUTPUT INNER LEADS



Leads Assignment





Material Description

1.Space Tape Material	Polyester(PET)		ATECT
Leader Tape Material	Polyetherimide (PEI)		
PKG Reel Size	405mm		DAICHI
Polymide	UPILEX-S	75±6 um	UBE
Adhesive	#7100	12±3 um	Toray
Cupper	FQ-VLP	18±5 um	Mitsui
Plating	Sn	0.21±0.05 um	
Flex Coating	FS-100L	Min10 um	UBE
Solder Resist	AE-70-M11	26 ±14 um	Ajinomoto

Solder Mask Tolerance:±0.200mm
2.ALL CHAMFER IS R0.200mm.
3.5 SPROCKET HOLES (48W) FOR 1TAPESITE.
4.Etchingfactor >2.5 for all pattern.
5.Min pitch:50um /spcae:25um
6.Inner Lead Width Measure Location:Bump Center
7.GENERAL TOLERANCE = ± 0.050 mm

L1_Copper ■ L2_SOLDER RESIST ■ L3_PUNCH ■ L31_SECOND PUNCH ■ OTHER:FOLLOW CUSTOMER LAYER

Change	△	Date	96.04.30

DWG NO:	SX022	C/P/N:	➔① ST8016T-F3C	SIMPAL DWG NO:	ST043A-02

Designed by-date:	Checked by-date:	Approved by date:	TOLERANCE: x ± x.xx ± x.x x.xxx±
96.04.30			

Sitronix

Drawing Name: PATTERN MEASURE DRAWING

Edition:	Sheet:	Drawing Scale:	Drawing Unit:
A	1/2	1/1	mm

Time: