# SSD7317

*Product Preview*

## 128 x 96 Dot Matrix OLED/PLED Segment/Common Driver with Integrated Touch Controller

**Appendix: IC Revision history of SSD7317 Specification**

| Version | Change Items | Effective Date |
|---|---|---|
| 0.10 | 1st Release | 21-Mar-18 |
| 0.11 | Update Product Features<br>Update Pin Description for BS[3:0], D[7:4] and revise typo in TD[2:0]<br>Update Figure 1-1: Application Example | 23-Nov-18 |

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# 1 GENERAL DESCRIPTION

SSD7317 is a single-chip CMOS OLED/PLED driver with Integrated Touch Controller for organic/polymer light emitting diode dot-matrix graphic display system. It consists of 128 segments and 96 commons, and supports In-cell capacitive touch detection on conventional panel structure for 4-key application with plastic or glass cover lens. This IC is designed for Common Cathode type OLED/PLED panel with 4-key touch and 1D slide sensing.

SSD7317 displays data directly from its internal 128 x 96 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from general MCU through the hardware selectable $I^2C$ Interface, 6800-/8080-series compatible Parallel Interface or Serial Peripheral Interface. The 256 steps contrast control and oscillator embedded in SSD7317 reduces the number of external components. SSD7317 is designed to support high brightness panel, with maximum source current reaching 600uA, making it suitable for many compact size applications which require high output brightness, such as wearable electronics, smart home device etc.

# 2 FEATURES

**Power Supply**

- $V_{DD}$ = 1.65V – 3.5V (for IC logic)
- $V_{CI}$ = 3V – 3.5V (for Touch analog driving, must be greater than or equal to $V_{DD}$)
- $V_{CC}$ = 8V – 18V (for Display panel driving)

**Display**

- Resolution: 128 x 96 dot matrix panel
- Segment maximum source current: 600uA
- Common maximum sink current: 76.8mA
- Embedded 128 x 96 bit SRAM display buffer
- Screen saving continuous scrolling function in both horizontal and vertical direction
- Screen saving infinite content scrolling function
- Internal or external $I_{REF}$ selection
- RAM write synchronization signal
- Programmable Frame Rate and Multiplexing Ratio
- Row Re-mapping and Column Re-mapping
- Power On Reset (POR)
- On-Chip Oscillator
- Dynamic Grayscale

**Touch**

- Supports In-cell capacitive touch detection on conventional panel structure for 4-key and 1-D slide application
- 16kB firmware-based system operation by host
- Works with all proprietary sensor patterns recommended by SSL for On-cell structure
- Water and moisture immunity:
    - No false touch with condensation or water drop up to 5 mm diameter
    - One-finger tracking with condensation or water drop up to 5 mm diameter
- Large object report flag
- Supports single tap, double taps, long tap, slide gestures
- Supports 4-key touch gloved operation with plastic materials up to 0.2mm thickness
- Scan Speed:
    - Display mode: typical 105Hz
    - Low power mode (LPM): configurable to allow power and speed optimization

- Programmable timeout for automatic transition from active to idle mode
- Auto calibration

**System Interfaces**

- Pin selectable for display communication Interfaces:
  - 8 bits 6800/8080-series
  - SPI
  - $I^2C$
- Pin selectable for touch communication Interfaces:
  - SPI
  - $I^2C$

**Package**

- Chip layout for COG
- Wide range of operating temperature: -40°C to 85°C

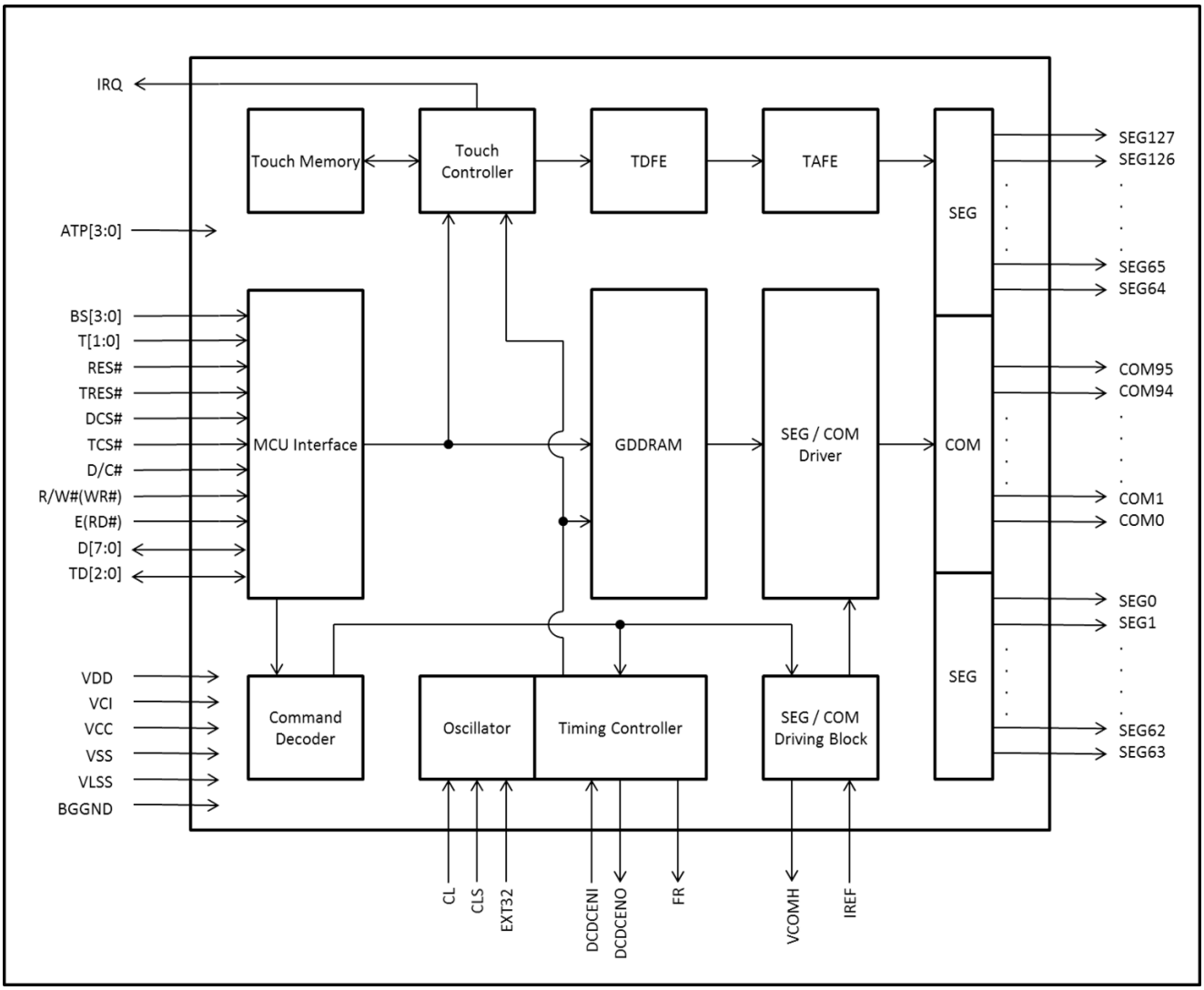
# 3 ORDERING INFORMATION

**Table 3-1: Ordering Information**

| Ordering Part Number | SEG | COM | Package Form | Remark |
|---|---|---|---|---|
| SSD7317Z | 128 | 96 | COG | ○ Min SEG pad pitch : 29um<br>○ Min COM pad pitch : 35um<br>○ Min I/O pad pitch : 55um<br>○ Die thickness: 250um<br>○ Bump height: nominal 9um |

# 4 BLOCK DIAGRAM

**Figure 4-1: SSD7317 Block Diagram**



# 5 PIN DESCRIPTION

**Key:**

| | |
|---|---|
| I = Input | NC = Not Connected |
| O =Output | Pull LOW= connect to Ground |
| I/O = Bi-directional (input/output) | Pull HIGH= connect to $V_{DD}$ |
| P = Power pin | |

**Table 5-1: Pin Description**

| Pin Name | Pin Type | Description |
|---|---|---|
| $V_{DD}$ | P | Power supply pin for core logic operation. |
| $V_{CI}$ | P | Power supply pin for touch analog driving. $V_{CI}$ must be greater than or equal to $V_{DD}$. |
| $V_{CC}$ | P | Power supply for panel driving voltage. This is also the most positive power voltage supply pin. |
| $V_{SS}$ | P | Ground pin. It must be connected to external ground. |
| $V_{LSS}$ | P | Analog system ground pin. It must be connected to external ground. |
| BGGND | P | Reserved pin. It must be connected to ground. |
| VSL | P | This is segment voltage (output low level) reference pin.<br><br>When external VSL is not used, this pin must be connected to $V_{LSS}$ externally.<br>When external VSL is used, connect with resistor and diode to ground (depends on application). |
| $V_{LH}$ | P | Logic high (same voltage level as $V_{DD}$) for internal connection of input and I/O pins.<br>No need to connect to external power source. |
| $V_{LL}$ | P | Logic low (same voltage level as $V_{SS}$) for internal connection of input and I/O pins.<br>No need to connect to external ground. |
| $V_{COMH}$ | P | COM signal deselected voltage level.<br>A capacitor should be connected between this pin and $V_{SS}$. |
| VBREF | O | This is a reserved pin. It should be kept NC. |
| BS[3:0] | I | MCU bus interface selection pins. Select appropriate logic setting as described in Table 5-2: Bus Interface selection. BS3, BS2, BS1and BS0 are pin select. |

**Table 5-2: Bus Interface selection**

| BS[3:0] | Display Interface | Touch Interface |
|---|---|---|
| 0000 | 4 line SPI | SPI |
| 0001 | 3 line SPI | |
| 0010 | $I^2C$ | |
| 0100 | 8-bit 6800 parallel | |
| 0110 | 8-bit 8080 parallel | |
| 1000 | 4 line SPI | $I^2C$ |
| 1001 | 3 line SPI | |
| 1010 | $I^2C$ | |
| 1100 | 8-bit 6800 parallel | |
| 1110 | 8-bit 8080 parallel | |

**Note**

(1) 0 is connected to $V_{SS}$

(2) 1 is connected to $V_{DD}$

| Pin Name | Pin Type | Description |
|---|---|---|
| $I_{REF}$ | I | This pin is the segment output current reference pin.<br><br>When $I_{REF}$ is supplied externally, a resistor should be connected between this pin and $V_{SS}$ to maintain the current around 18.75uA. Please refer to Figure 6-16 for the details of resistor value.<br>When internal $I_{REF}$ is used, this pin should be kept NC. |
| CL | I | This is external clock input pin for display interface.<br><br>When internal clock is enabled (i.e. HIGH in CLS pin), this pin is not used and should be connected to $V_{SS}$. When internal clock is disabled (i.e. LOW in CLS pin), this pin is the external clock source input pin. |
| CLS | I | This is internal clock enable pin for display interface.<br><br>When it is pulled HIGH (i.e. connect to $V_{DD}$), internal clock is enabled. When it is pulled LOW, the internal clock is disabled; an external clock source must be connected to the CL pin for normal operation. |
| DCS# | I | This pin is the chip select input connecting to the MCU for display interface.<br>The display is enabled for MCU communication only when DCS# is pulled LOW (active LOW). |
| RES# | I | This pin is the master reset signal input.<br><br>When the pin is pulled LOW, initialization of the chip is executed.<br>Keep this pin pull HIGH during normal operation. |
| D/C# | I | This pin is Data/Command control pin connecting to the MCU.<br><br>When the pin is pulled HIGH, the data at D[7:0] will be interpreted as data.<br>When the pin is pulled LOW, the data at D[7:0] will be transferred to a command register.<br>In $I^2C$ mode, this pin acts as SA0 for slave address selection.<br>When 3-wire serial interface is selected, this pin must be connected to $V_{SS}$.<br><br>For detail relationship to MCU interface signals, refer to Timing Characteristics Diagrams Figure 10-1 to Figure 10-3. |
| R/W# (WR#) | I | This pin is Read/Write control input pin connecting to the MCU interface.<br><br>When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW.<br>When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected.<br><br>When serial or $I^2C$ interface is selected, this pin must be connected to $V_{SS}$. |
| E (RD#) | I | This pin is MCU interface input.<br><br>When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected.<br>When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected.<br><br>When serial interface is selected, this pin must be connected to $V_{SS}$.<br>In $I^2C$ mode, this pin acts as SA1 for slave address selection. |

| Pin Name | Pin Type | Description |
|---|---|---|
| D[7:0] | I/O | These pins are bi-directional data bus connecting to the MCU data bus for display interface.<br>Unused pins are recommended to tie LOW.<br><br>When serial interface mode is selected, D2, D1 should be tied together and serves as serial data input: SDIN and D0 is the serial clock input: SCLK;<br>When $I^2C$ mode is selected, D2, D1 should be tied together and serve as $SDA_{out}$, $SDA_{in}$ in application and D0 is the serial clock input, SCL. |
| FR | O | This pin outputs RAM write synchronization signal. Proper timing between MCU data writing and frame display timing can be achieved to prevent tearing effect.<br>It should be kept NC if it is not used. |
| EXT32 | I | This is external clock input pin for touch.<br>It should be connected to $V_{SS}$ if it is not used. |
| TCS# | I | This pin is the chip select input connecting to the MCU for touch.<br>The touch interface is enabled for MCU communication only when TCS# is pulled LOW (active LOW). |
| TRES# | I | This pin is the reset signal input for touch.<br><br>When the pin is pulled LOW, initialization of the touch is executed.<br>Keep this pin pull HIGH during normal operation. |
| TD[2:0] | I/O | These pins are bi-directional data bus connecting to the MCU data bus for touch interface.<br>Unused pins are recommended to tie LOW.<br><br>When serial interface mode is selected, TD2 serves as serial data output: SDOUT, TD1 serves as serial data input: SDIN and TD0 is the serial clock input: SCLK;<br>When $I^2C$ mode is selected, TD2, TD1 should be tied together and serve as $SDA_{out}$, $SDA_{in}$ in application and TD0 is the serial clock input, SCL. |
| IRQ | O | Interrupt signal for touch reporting. |
| TEST | I/O | It should be connected to $V_{LL}$ |
| DCDCENI | I | Enable input pin for external DCDC circuit.<br>It must be connected to external ground if it is not used. |
| DCDCENO | O | Enable output pin for external DCDC circuit.<br>It should be kept NC if it is not used. |
| T0, T1 | I/O | Reserved pin. It should be kept NC. |
| SEG0 ~ SEG127 | O | These pins provide the OLED segment driving signals. These pins are $V_{SS}$ state when display is OFF. |
| COM0 ~ COM95 | O | These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is OFF. |
| DR[3:0] | - | Reserved pins, it should be kept NC if it is not used. |
| ATP[3:0] | - | Reserved pins, it must be connected to external ground if it is not used. |
| RX[3:0] | - | Reserved pins, it should be kept NC if it is not used. |

| Pin Name | Pin Type | Description |
|---|---|---|
| RXT[3:0] | - | Reserved pins, it should be kept NC if it is not used. |
| SHA ~ SHN | - | Reserved pins, it should be kept NC if it is not used. |
| V33 | P | Same voltage level as VCC. No need to connect to external power source. |
| V38 | P | Same voltage level as VCOMH. No need to connect to external power source. |
| TR[19:0] | - | Reserved pin. It should be kept NC. |
| NC | - | This is dummy pin. It should be kept NC. |

# 6 FUNCTIONAL BLOCK DESCRIPTIONS

## 6.1 Display Interface Selection

SSD7317 display interface consist of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 6-1. Different display interface mode can be set by hardware selection on BS[3:0] pins.

**Table 6-1: Display interface assignment under different bus interface mode**

| Pin Name / Bus Interface | Data/Command Interface | | | | | | | | Control Signal | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **E** | **R/W#** | **DCS#** | **D/C#** | **RES#** |
| 8-bit 8080 | D[7:0] | | | | | | | | RD# | WR# | DCS# | D/C# | RES# |
| 8-bit 6800 | D[7:0] | | | | | | | | E | R/W# | DCS# | D/C# | RES# |
| 3-wire SPI | Tie LOW | | | | | SDIN | | SCLK | Tie LOW | | DCS# | Tie LOW | RES# |
| 4-wire SPI | Tie LOW | | | | | SDIN | | SCLK | Tie LOW | | DCS# | D/C# | RES# |
| $I^2C$ | Tie LOW | | | | | $SDA_{OUT}$ | $SDA_{IN}$ | SCL | SA1 | Tie LOW | | SA0 | RES# |

### 6.1.1 Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and DCS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.
A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
The E input serves as data latch signal while DCS# is LOW. Data is latched at the falling edge of E signal.

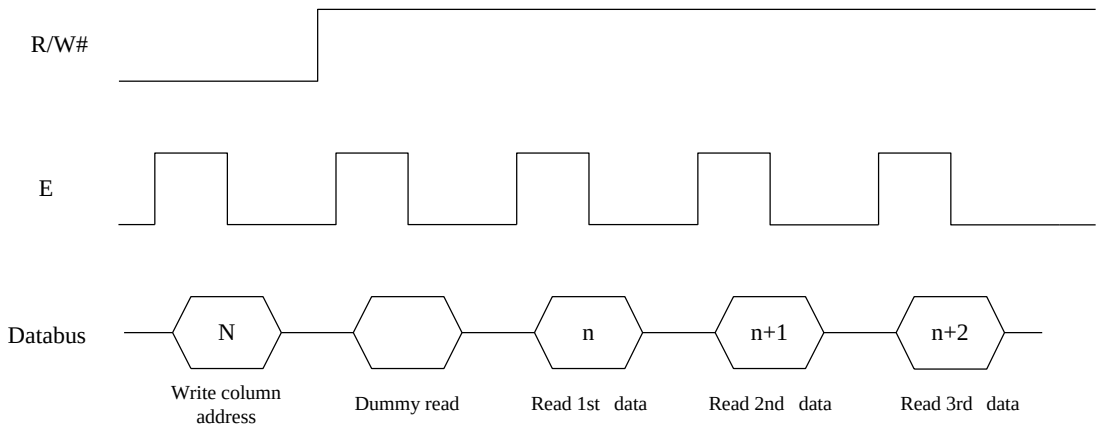
**Table 6-2: Control pins of 6800 interface**

| **Function** | **E** | **R/W#** | **DCS#** | **D/C#** |
|---|---|---|---|---|
| Write command | ↓ | L | L | L |
| Read status | ↓ | H | L | L |
| Write data | ↓ | L | L | H |
| Read data | ↓ | H | L | H |

**Note**
(1) ↓ stands for falling edge of signal
H stands for HIGH in signal
L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 6-1.

**Figure 6-1: Data read back procedure - insertion of dummy read**




### 6.1.2 Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and DCS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
A rising edge of RD# input serves as a data READ latch signal while DCS# is kept LOW.
A rising edge of WR# input serves as a data/command WRITE latch signal while DCS# is kept LOW.

**Figure 6-2: Example of Write procedure in 8080 parallel interface mode**

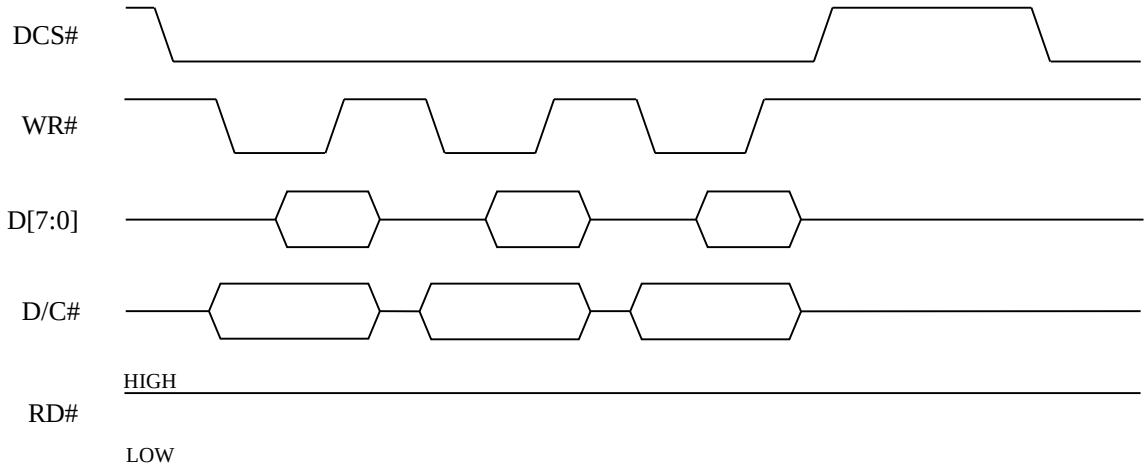



**Figure 6-3: Example of Read procedure in 8080 parallel interface mode**

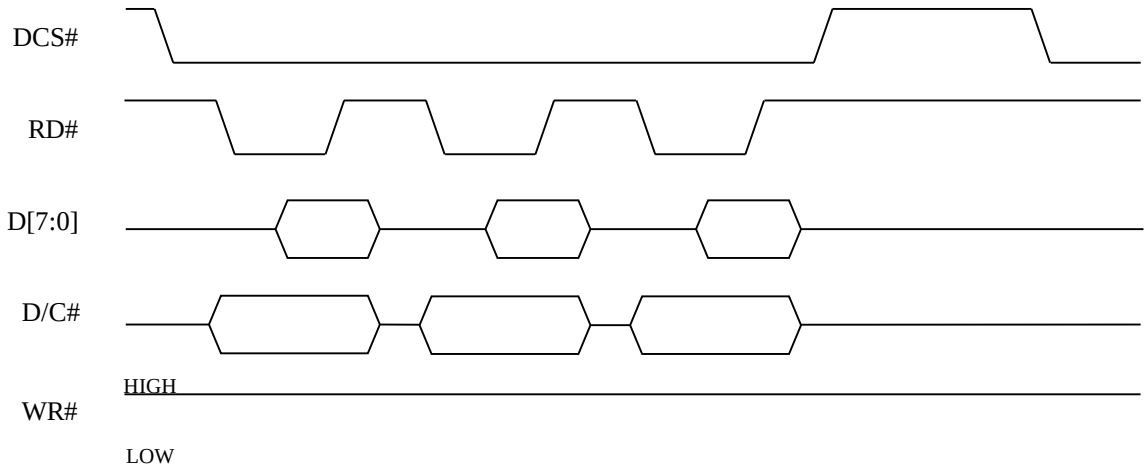


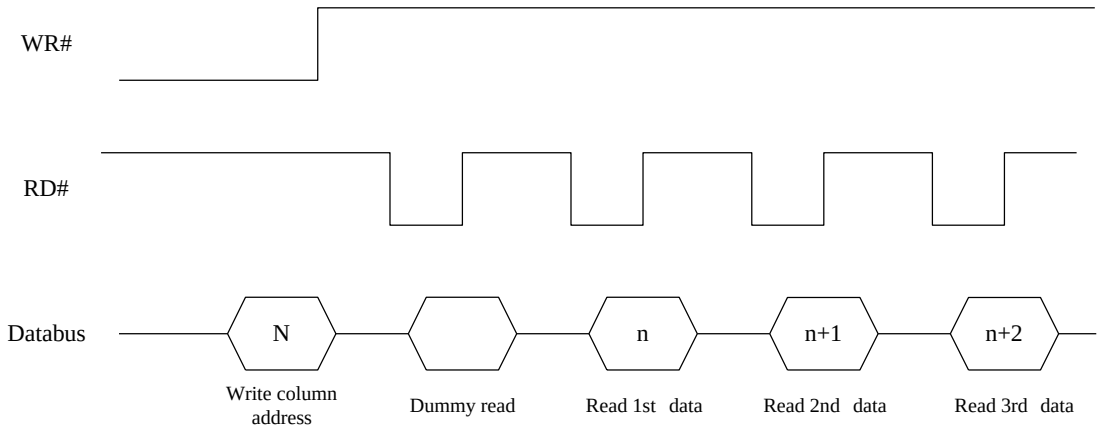
**Table 6-3: Control pins of 8080 interface**

| Function | RD# | WR# | DCS# | D/C# |
|---|---|---|---|---|
| Write command | H | ↑ | L | L |
| Read status | ↑ | H | L | L |
| Write data | H | ↑ | L | H |
| Read data | ↑ | H | L | H |

**Note**
(1) ↑ stands for rising edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 6-4.

**Figure 6-4: Display data read back procedure - insertion of dummy read**




### 6.1.3 Serial Interface (4-wire SPI)

The 4-wire serial interface consists of serial clock: SCLK, serial data: SDIN, D/C#, DCS#. In 4-wire SPI mode, D0 acts as SCLK, D1, D2 are tied together to act as SDIN. For the unused data pins from D3 to D7, E(RD#) and R/W#(WR#) can be connected to an external ground.

**Table 6-4: Control pins of 4-wire Serial interface**

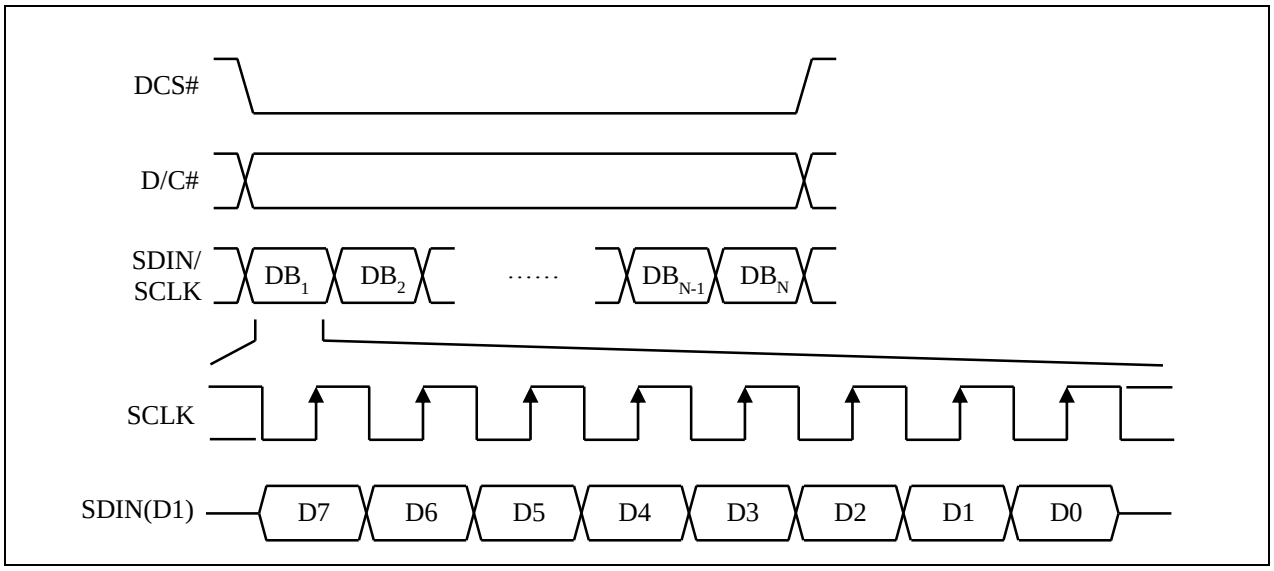
| Function | E | R/W# | DCS# | D/C# | D0 |
|---|---|---|---|---|---|
| Write command | Tie LOW | Tie LOW | L | L | ↑ |
| Write data | Tie LOW | Tie LOW | L | H | ↑ |

**Note**
(1) H stands for HIGH in signal
(2) L stands for LOW in signal
(3) ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... , D0. D/C# is sampled on every eighth clock and D/C# should be kept stable throughout eight clock period. The data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

**Figure 6-5: Write procedure in 4-wire Serial interface mode**




### 6.1.4 Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and DCS#.
In 3-wire SPI mode, D0 acts as SCLK, D1, D2 are tied together to act as SDIN. For the unused data pins from D3 to D7, R/W# (WR#), E(RD#) and D/C# can be connected to an external ground.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

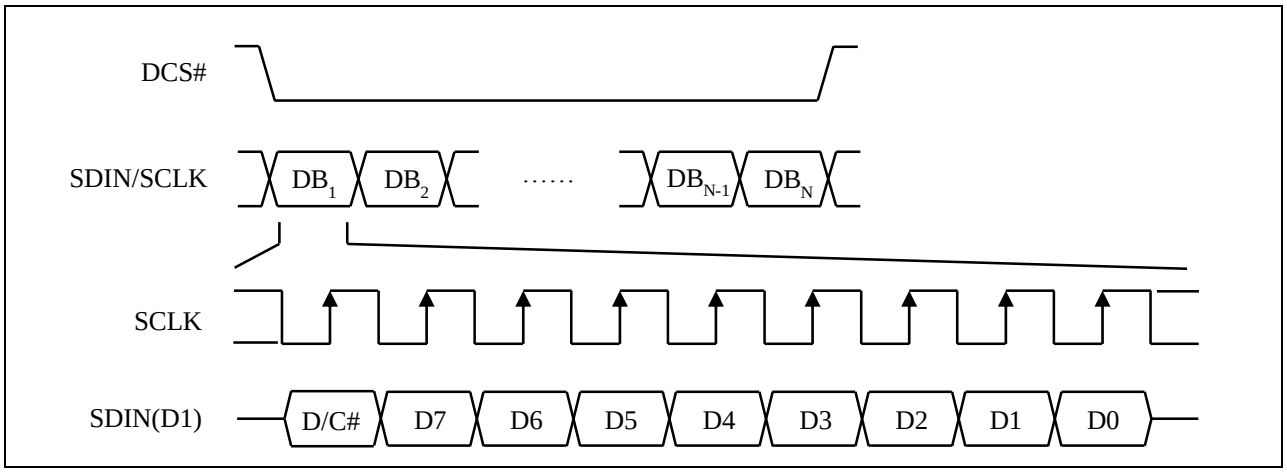
Under serial mode, only write operations are allowed.

**Table 6-5: Control pins of 3-wire Serial interface**

| Function | E(RD#) | R/W#(WR#) | DCS# | D/C# | D0 |
|---|---|---|---|---|---|
| Write command | Tie LOW | Tie LOW | L | Tie LOW | ↑ |
| Write data | Tie LOW | Tie LOW | L | Tie LOW | ↑ |

**Note**
(1) L stands for LOW in signal
(2) ↑ stands for rising edge of signal

**Figure 6-6: Write procedure in 3-wire Serial interface mode**



### 6.1.5 $I^2C$ Interface

The $I^2C$ communication interface consists of slave address bits SA[1:0], $I^2C$-bus data signal SDA ($SDA_{OUT}/D_2$ for output and $SDA_{IN}/D_1$ for input) and $I^2C$-bus clock signal SCL ($D_0$). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bits (SA[1:0])
SSD7317 has to recognize the slave address before transmitting or receiving any information by the $I^2C$-bus. The device will respond to the slave address following by the slave address bits (SA[1:0]) and the read/write select bit ("R/W#" bit) with the following byte format:

| $b_7$ | $b_6$ | $b_5$ | $b_4$ | $b_3$ | $b_2$ | $b_1$ | $b_0$ |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 | SA1 | SA0 | R/W# |

SA[1:0] bits provide extension bits for the slave address. "b0111100" or "b0111101" or "b0111110" or "b0111111", can be selected as the slave address of SSD7317. E pin acts as SA1 and D/C# pin acts as SA0 for slave address selection.
"R/W#" bit is used to determine the operation mode of the $I^2C$-bus interface. R/W# = 1, it is in read mode. R/W# = 0, it is in write mode.

b) $I^2C$-bus data signal (SDA)
SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.

It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".

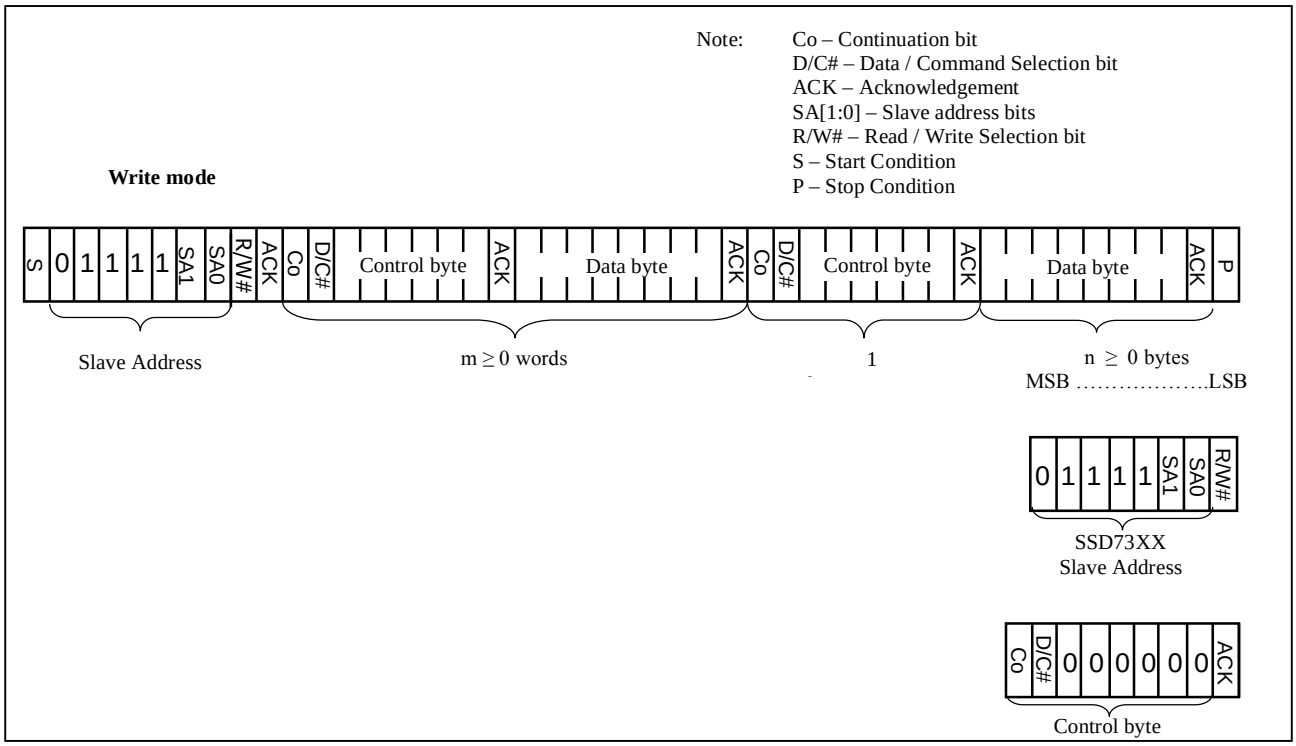
"$SDA_{IN}$" and "$SDA_{OUT}$" are tied together and serve as SDA. The "$SDA_{IN}$" pin must be connected to act as SDA. The "$SDA_{OUT}$" pin may be disconnected. When "$SDA_{OUT}$" pin is disconnected, the acknowledgement signal will be ignored in the $I^2C$-bus.

c) $I^2C$-bus clock signal (SCL)
The transmission of information in the $I^2C$-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

### 6.1.5.1 I²C-bus Write Data

The I²C-bus interface gives access to write data and command into the device. Please refer to for the write mode of I²C-bus in chronological order.

**Figure 6-7: I²C-bus data format**




### 6.1.5.2 Write mode for I²C

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 6-8. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
2) The slave address is following the start condition for recognition use. For the SSD7317, the slave address is "b0111100" or "b0111101" or "b0111110" or "b0111111" by changing the SA[1:0] to LOW or HIGH (E pin acts as SA1 and D/C pin acts as SA0).
3) The write mode is established by setting the R/W# bit to logic "0".
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 6-9 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six "0" 's.
    a. If the Co bit is set as logic "0", the transmission of the following information will contain data bytes only.
    b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic "0", it defines the following data byte as a command. If the D/C# bit is set to logic "1", it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
6) Acknowledge bit will be generated after receiving each control byte or data byte.
7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 6-8. The stop condition is established by pulling the "SDA in" from LOW to HIGH while the "SCL" stays HIGH.

**Figure 6-8: Definition of the Start and Stop Condition**

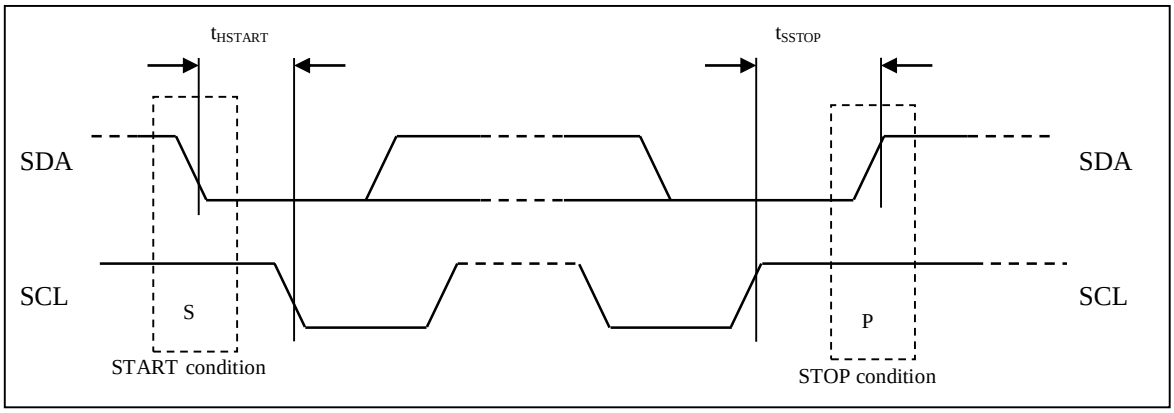
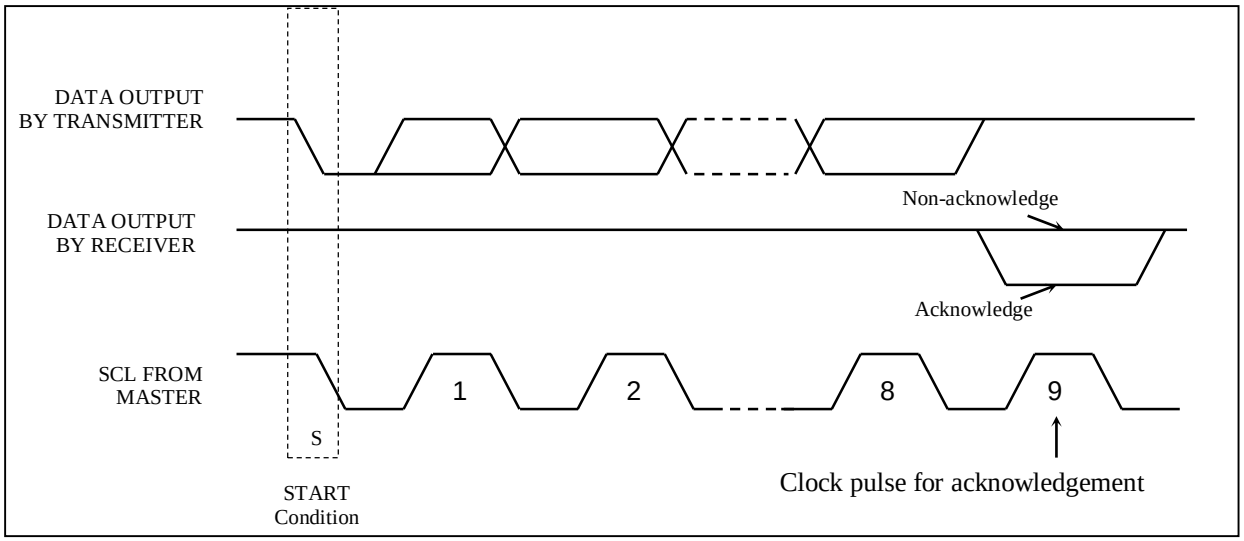


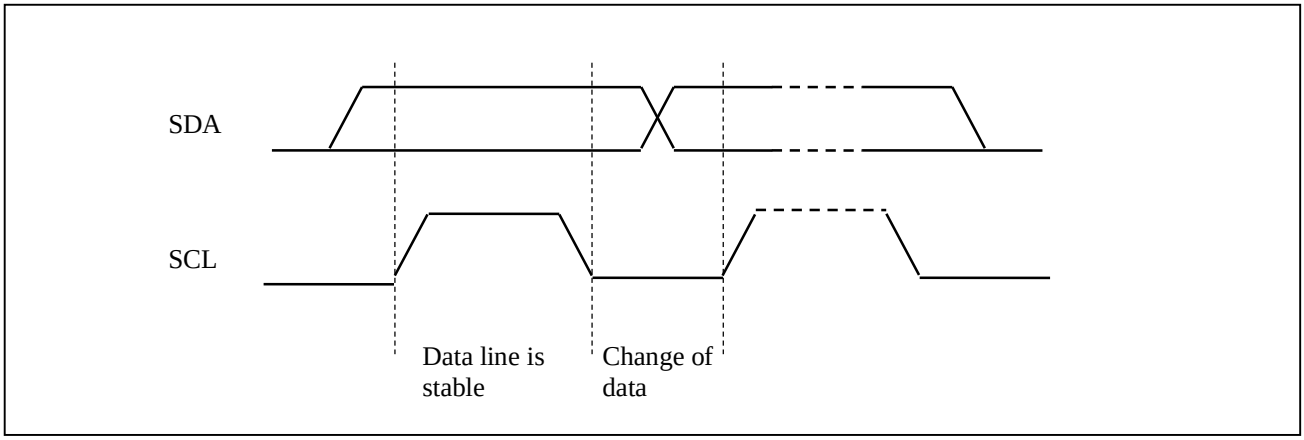

**Figure 6-9: Definition of the acknowledgement condition**




Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Please refer to the Figure 6-10 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

**Figure 6-10: Definition of the data transfer condition**



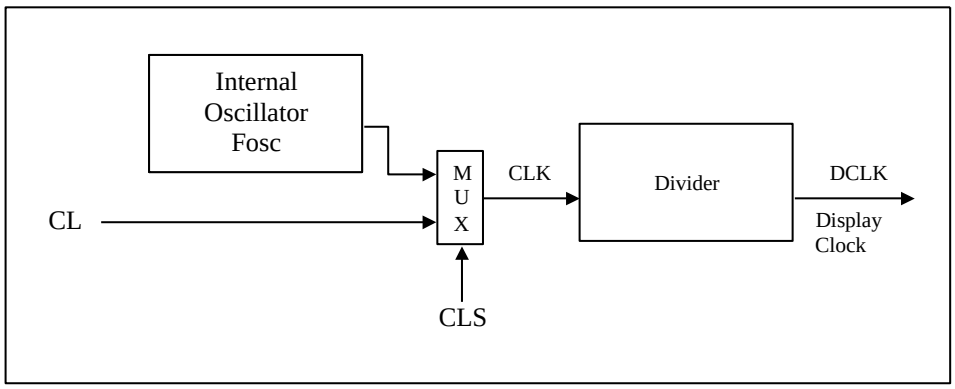
## 6.2 Command Decoder

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is HIGH, D[7:0] is interpreted as display data written to Graphic Display Data RAM (GDDRAM). If it is LOW, the input at D[7:0] is interpreted as a command. Then data input will be decoded and written to the corresponding command register.

## 6.3 Oscillator Circuit and Display Time Generator

**Figure 6-11: Oscillator Circuit and Display Time Generator**




This module is an on-chip LOW power RC oscillator circuitry. The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is pulled HIGH, internal oscillator is chosen and CL should be connected to $V_{SS}$. Pulling CLS pin LOW disables internal oscillator and external clock must be connected to CL pins for proper operation. When the internal oscillator is selected, its output frequency $F_{OSC}$ can be changed by commands D5h A[7:4].

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor "D" can be programmed from 1 to 16 by command D5h.

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula:

$$F_{FRM} = \frac{F_{osc}}{D \times K \times No.\,of\ Mux}$$

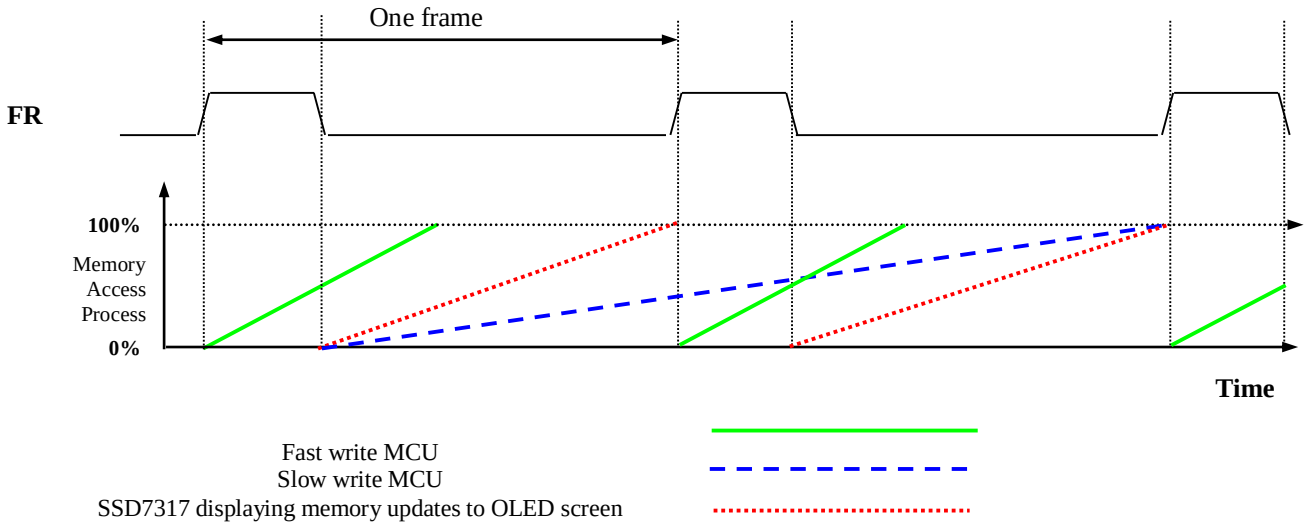
where

- D stands for clock divide ratio. It is set by command D5h A[3:0]. The divide ratio has the range from 1 to 16.
- K is the number of display clocks per row. The value TBD.
  Please refer to **Section 6.6** for the details of the "Phase".
- Number of multiplex ratio is set by command A8h. The power on reset value is 95 (i.e. 96MUX).
- $F_{OSC}$ is the oscillator frequency. It can be changed by commands D5h A[7:4]. The higher the register setting results in higher frequency.

## 6.4 FR Synchronization

FR synchronization signal can be used to prevent tearing effect.

**Figure 6-12: FR Synchronization**




The starting time to write a new image to OLED driver is depended on the MCU writing speed. If MCU can finish writing a frame image within one frame period, it is classified as fast write MCU. For MCU needs longer writing time to complete (more than one frame but within two frames), it is a slow write one.

**For fast write MCU:** MCU should start to write new frame of ram data just after rising edge of FR pulse and should be finished well before the rising edge of the next FR pulse.

**For slow write MCU**: MCU should start to write new frame ram data after the falling edge of the 1st FR pulse and must be finished before the rising edge of the 3rd FR pulse.

## 6.5 Reset Circuit

When RES# input is LOW, the chip will be initialized with the following status:

1. Display is OFF
2. 128 x 96 Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

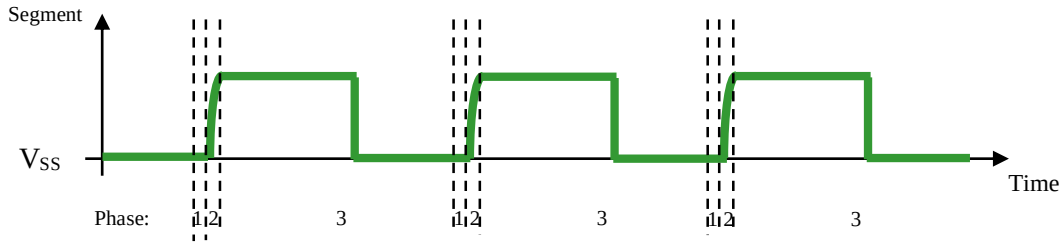
## 6.6 Segment Drivers / Common Drivers

Segment drivers deliver 128 current sources to drive the OLED panel. The driving current can be adjusted by altering the registers of the contrast setting command (81h). Common drivers generate voltage-scanning pulses.

The segment driving waveform is divided into three phases:

1. In phase 1, the OLED pixel charges of previous image are discharged in order to prepare for next image content display.
2. In phase 2, the OLED pixel is driven to the targeted voltage. The pixel is driven to attain the corresponding voltage level from $V_{SS}$. The period of phase 2 can be programmed in length from 2 to 30 DCLKs. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.
3. In phase 3, the OLED driver switches to use current source to drive the OLED pixels and this is the current drive stage.

**Figure 6-13: Segment Output Waveform in three phases**




After finishing phase 3, the driver IC will go back to phase 1 to display the next row image data. This three-step cycle is run continuously to refresh image display on OLED panel.

In phase 3, if the length of current drive pulse width is set to N, after finishing N DCLKs in current drive phase, the driver IC will go back to phase 1 for next row display.

## 6.7 Graphic Display Data RAM (GDDRAM)

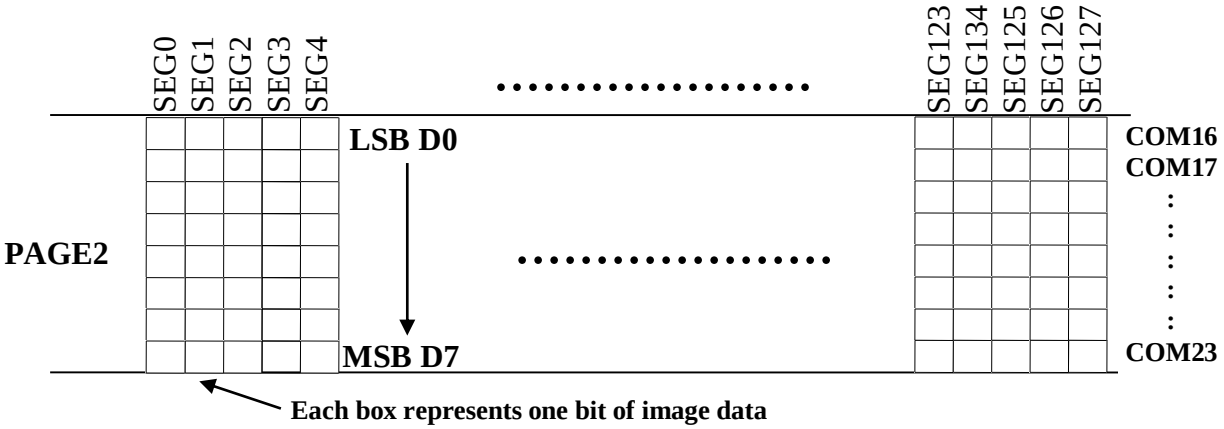
The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 x 96 bits and the RAM is divided into eight pages, from PAGE0 to PAGE11, which are used for monochrome 128x96 dot matrix display, as shown in Figure 6-14.

**Figure 6-14: GDDRAM pages structure**

| | | Row re-mapping |
|---|---|---|
| PAGE0 (COM0-COM7) | Page 0 | PAGE0 (COM95-COM88) |
| PAGE1 (COM8-COM15) | Page 1 | PAGE1 (COM87-COM80) |
| PAGE2 (COM16-COM23) | Page 2 | PAGE2 (COM79-COM72) |
| PAGE3 (COM24-COM31) | Page 3 | PAGE3 (COM71-COM64) |
| PAGE4 (COM32-COM39) | Page 4 | PAGE4 (COM63-COM56) |
| PAGE5 (COM40-COM47) | Page 5 | PAGE5 (COM55-COM48) |
| PAGE6 (COM48–COM55) | Page 6 | PAGE6 (COM47-COM40) |
| PAGE7 (COM56-COM63) | Page 7 | PAGE7 (COM39-COM32) |
| PAGE8 (COM64-COM71) | Page 8 | PAGE8 (COM31-COM24) |
| PAGE9 (COM72-COM79) | Page 9 | PAGE9 (COM23-COM16) |
| PAGE10 (COM80–COM87) | Page 10 | PAGE10 (COM15-COM8) |
| PAGE11 (COM88-COM95) | Page 11 | PAGE11 (COM 7-COM0) |
| | SEG0 ----------SEG127 | |
| Column re-mapping | SEG127 ----------SEG0 | |

When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row as shown in Figure 6-15.

**Figure 6-15: Enlargement of GDDRAM (No row re-mapping and column-remapping)**




For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software as shown in Figure 6-14.

For vertical shifting of the display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display (command D3h).

## 6.8 SEG/COM Driving block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

- $V_{CC}$ is the most positive voltage supply.
- $V_{COMH}$ is the Common deselected level. It is internally regulated.
- $V_{LSS}$ is the ground path of the analog and panel current.
- $I_{REF}$ is a reference current source for segment current drivers $I_{SEG}$. The relationship between reference current and segment current of a color is:

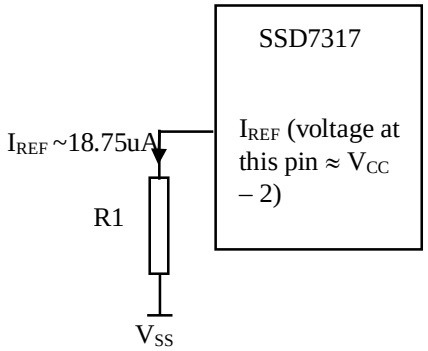
  $I_{SEG}$ = Contrast / 8 x $I_{REF}$

  in which the contrast (1~255) is set by Set Contrast command 81h

  When internal $I_{REF}$ is used, the $I_{REF}$ pin should be kept NC.
  Bit A[4] of command ADh is used to select external or internal $I_{REF}$ :
  A[4] = '0' Select external $I_{REF}$ [Reset]
  A[4] = '1' Enable internal $I_{REF}$ during display ON

When external $I_{REF}$ is used, the magnitude of $I_{REF}$ is controlled by the value of resistor, which is connected between $I_{REF}$ pin and $V_{SS}$ as shown in Figure 6-16. It is recommended to set $I_{REF}$ to 18.75 ± 2uA so as to achieve $I_{SEG}$ = 600uA at maximum contrast 255.

**Figure 6-16: $I_{REF}$ Current Setting by Resistor Value**




Since the voltage at $I_{REF}$ pin is $V_{CC}$ – 2V, the value of resistor R1 can be found as below:

For $I_{REF}$ = 18.75uA, $V_{CC}$ =12V:

R1 = (Voltage at $I_{REF}$ – $V_{SS}$) / $I_{REF}$
≈ (12 – 2) / 18.75uA
= 530kΩ

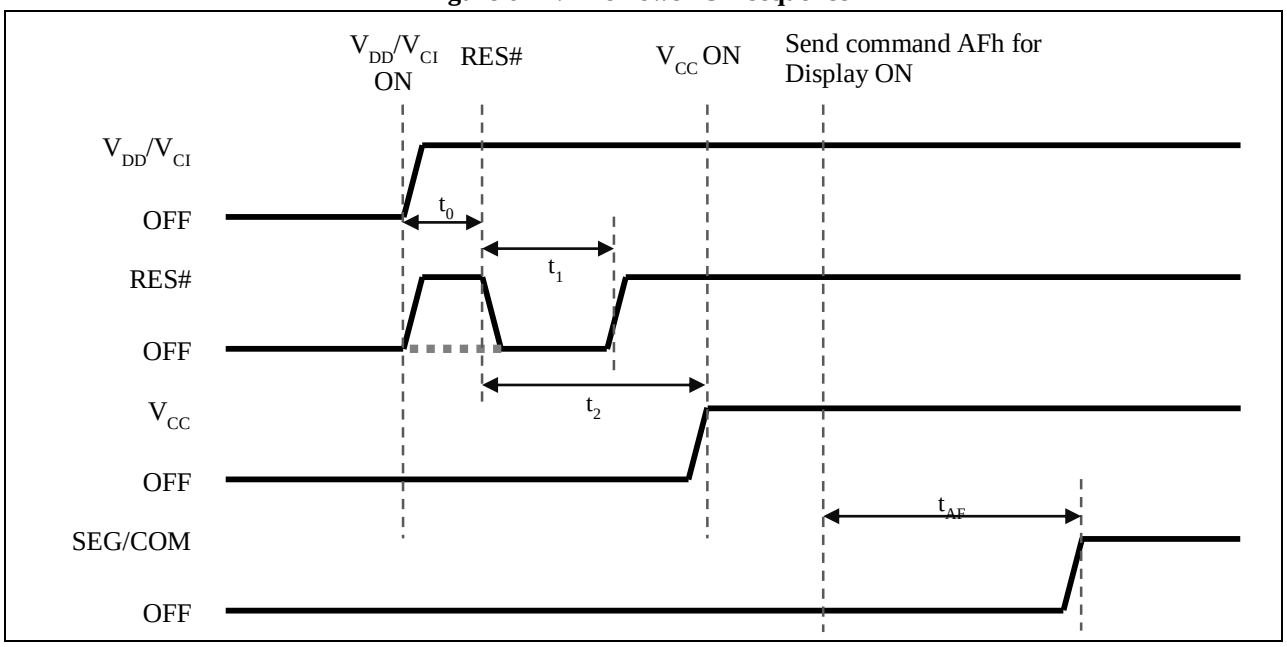
## 6.9 Power ON and OFF sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD7317.

*Power ON sequence*:

1. Power ON $V_{DD}$ and $V_{CI}$. ($V_{CI}$ must be greater than or equal to $V_{DD}$)
2. After $V_{DD}$ and $V_{CI}$ become stable, wait at least 20ms ($t_0$), set RES# pin LOW (logic low) for at least 3us ($t_1$) [4] and then HIGH (logic high).
3. After setting RES# pin LOW (logic low), wait for at least 3us ($t_2$). Then Power ON $V_{CC}$.[1]
4. After $V_{CC}$ becomes stable, send command AFh for display ON. SEG/COM will be ON after 40ms ($t_{AF}$).

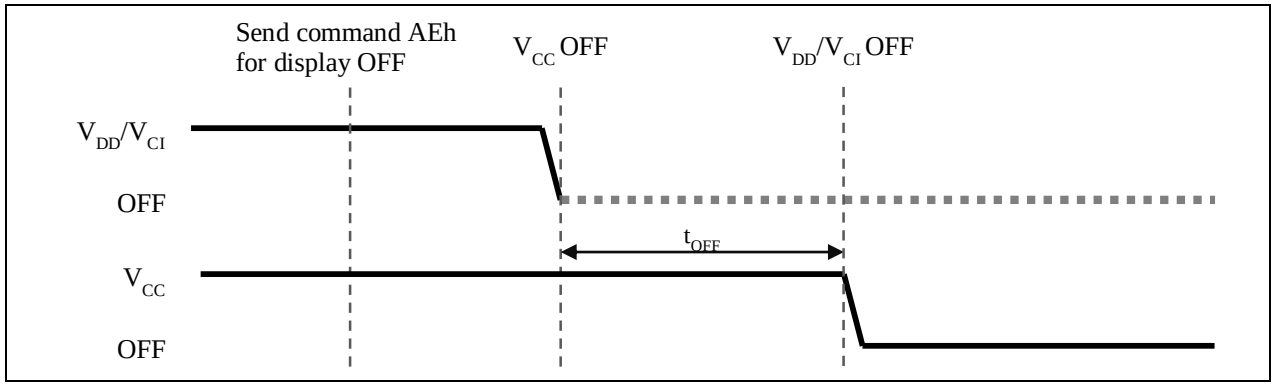
**Figure 6-17: The Power ON sequence**




*Power OFF sequence*:

1. Send command AEh for display OFF.
2. Power OFF $V_{CC}$.[1], [2]
3. Power OFF $V_{DD}$ and $V_{CI}$ after $t_{OFF}$. [4] (where Minimum $t_{OFF}$=0ms, typical $t_{OFF}$=100ms)

**Figure 6-18: The Power OFF sequence**




**Note:**

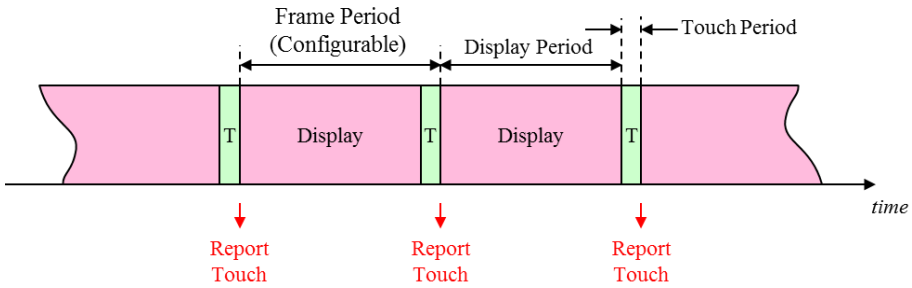
[1] $V_{CC}$ should be kept float (i.e. disable) when it is OFF.
[2] Power Pins ($V_{DD}$, $V_{CI}$, $V_{CC}$) can never be pulled to ground under any circumstance.
[3] The register values are reset after $t_1$.
[4] $V_{DD}$, $V_{CI}$ should not be Power OFF before $V_{CC}$ Power OFF.

## 6.10 Touch Analog Front-end (TAFE)

Touch Analog Front-end is used to detect touch on the panel.

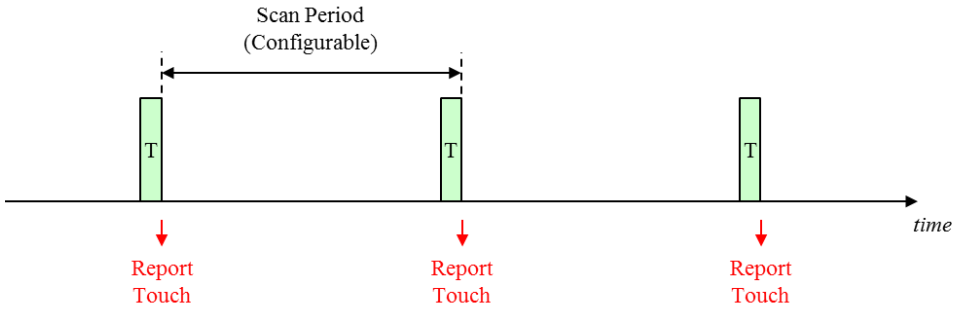
When display is on, segment driving are multiplexed in time slots for display and touch sensing. Touch status is reported at the end of every touch time slot.

**Figure 6-19: Frame Scan during display ON (Active Mode)**




When display is off, only touch sensing takes place at a lower scan rate (which is configurable to allow power and speed optimization). Touch status is reported at the end of every touch time slot.

**Figure 6-20: Frame Scan during display OFF (Low Power Mode)**




## 6.11 Touch Digital Front-end (TDFE)

Digital data of the sensing signal from ADC is processed to generate touch data (Reference, Raw, Delta) and touch status of the touch key. If Delta data is greater than the minimum finger level, "Touch Key Status" will report "1". The touch data and touch status are then passed to Command Decoder for read back through the touch interface.

## 6.12 Touch Memory

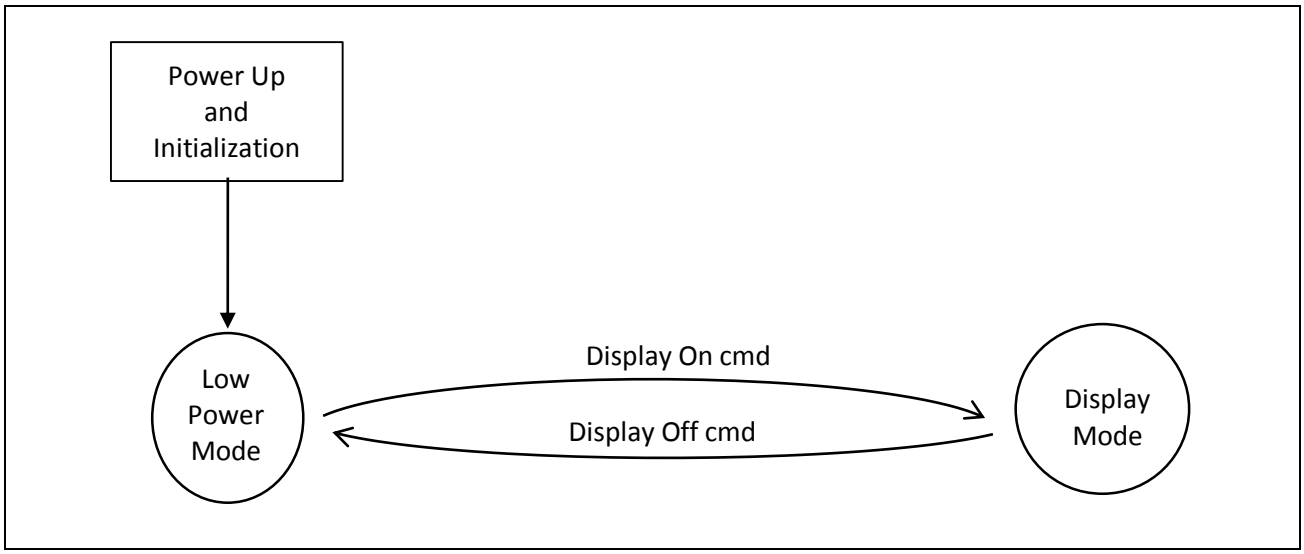
SSD7317 has integrated with 16-bit CPU, 16kB program and data memory. It is able to process all the raw touch data and generate the final touch location and communicate with the MCU host.

## 6.13 Touch Controller

Both TDFE and TAFE Controller is responsible for periodically generate the touch sensing period to perform touch sensing.

# 7 SYSTEM FLOW

**Figure 7-1: Integrated Touch Controller System Flow**



# 8 MAXIMUM RATINGS

**Table 8-1: Maximum Ratings**

(Voltage Reference to $V_{SS}$)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage | -0.3 to +4 | V |
| $V_{CI}$ | | -0.3 to +4 | V |
| $V_{CC}$ | | 0 to 19 | V |
| $V_{SEG}$ | SEG output voltage | 0 to $V_{CC}$ | V |
| $V_{COM}$ | COM output voltage | 0 to 0.9*$V_{CC}$ | V |
| $V_{in}$ | Input voltage | $V_{SS}$-0.3 to $V_{DD}$+0.3 | V |
| $T_A$ | Operating Temperature | -40 to +85 | ℃ |
| $T_{stg}$ | Storage Temperature Range | -65 to +150 | ℃ |

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

*This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

# 9 DC CHARACTERISTICS

**Condition (Unless otherwise specified):**

Voltage referenced to $V_{SS}$
$V_{DD}$ = 1.65V to 3.5V
$V_{CI}$ = 3V to 3.5V ($V_{CI}$ must be greater than or equal to $V_{DD}$)
$T_A$ = 25°C

**Table 9-1: DC Characteristics**

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Operating Voltage | - | 8 | - | 18 | V |
| $V_{DD}$ | Logic Supply Voltage | - | 1.65 | - | 3.5 | V |
| $V_{CI}$ | Touch controller Supply Voltage | - | 3.0 | - | 3.5 | V |
| $V_{OH}$ | High Logic Output Level | $I_{OUT}$ = 100uA, 3.3MHz | 0.9 x $V_{DD}$ | - | - | V |
| $V_{OL}$ | Low Logic Output Level | $I_{OUT}$ = 100uA, 3.3MHz | - | - | 0.1 x $V_{DD}$ | V |
| $V_{IH}$ | High Logic Input Level | - | 0.8 x $V_{DD}$ | - | - | V |
| $V_{IL}$ | Low Logic Input Level | - | - | - | 0.2 x $V_{DD}$ | V |
| $I_{CC, SLEEP}$ | $I_{CC,}$ Sleep mode Current | $V_{DD}$ = 1.65V~3.5V, $V_{CI}$ = 3V~3.5V, $V_{CC}$ = 8V~18V Display OFF, No panel attached | - | - | 10 | uA |
| $I_{DD, SLEEP}$ | $I_{DD,}$ Sleep mode Current | $V_{DD}$ = 1.65V~3.5V, $V_{CI}$ = 3V~3.5V, $V_{CC}$ = 8V~18V Display OFF, No panel attached | - | - | 10 | uA |
| $I_{CI, SLEEP}$ | $I_{CI,}$ Sleep mode Current | $V_{DD}$ = 1.65V~3.5V, $V_{CI}$ = 3V~3.5V, $V_{CC}$ = 8V~18V Display OFF, No panel attached | - | - | 10 | uA |
| $I_{CC}$ | $V_{CC}$ Supply Current $V_{DD}$ = 1.8V, $V_{CI}$ = 3.3V, $V_{CC}$ = 12V, $I_{REF}$ = 18.75uA No loading, Display ON, All ON | Contrast=FFh | - | TBD | TBD | uA |
| $I_{CI}$ | $V_{CI}$ Supply Current $V_{DD}$ = 1.8V, $V_{CI}$ = 3.3V, $V_{CC}$ = 12V, $I_{REF}$ = 18.75uA No loading, Display ON, All ON | | - | TBD | TBD | uA |
| $I_{DD}$ | $V_{DD}$ Supply Current $V_{DD}$ = 1.8V, $V_{CI}$ = 3.3V, $V_{CC}$ = 12V, $I_{REF}$ = 18.75uA No loading, Display ON, All ON | | - | TBD | TBD | uA |
| $I_{SEG}$ | Segment Output Current $V_{DD}$=1.8V, $V_{CI}$ = 3.3V, $V_{CC}$=12V, $I_{REF}$=TBD, Display ON | Contrast=FFh | - | 600 | - | uA |
| | | Contrast=AFh | - | TBD | - | |
| | | Contrast=3Fh | - | TBD | - | |
| Dev | Segment output current uniformity | Dev = ($I_{SEG}$ – $I_{MID}$)/$I_{MID}$ $I_{MID}$ = ($I_{MAX}$ + $I_{MIN}$)/2 $I_{SEG}$[0:127] = Segment current at contrast = FFh | -3 | - | +3 | % |
| Adj. Dev | Adjacent pin output current uniformity (contrast = FF) | Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1]) | -2 | - | +2 | % |
| $I_{Touch}$ | Current for touch sensing (LPM) | $V_{DD}$ = 1.8V, $V_{CI}$ = 3.3V, $V_{CC}$ = 12V, $I_{REF}$ = 18.75uA No loading, Display OFF | - | TBD | TBD | uA |
| | Current for touch sensing (Display mode) | $V_{DD}$ = 1.8V, $V_{CI}$ = 3.3V, $V_{CC}$ = 12V, $I_{REF}$ = 18.75uA No loading, Display OFF | - | TBD | TBD | mA |

# 10 AC CHARACTERISTICS

**Conditions:**

Voltage referenced to $V_{SS}$
$V_{DD}$ =1.65 to 3.5V
$V_{CI}$ = 3V to 3.5V ($V_{CI}$ must be greater than or equal to $V_{DD}$)
$T_A$ = 25°C

**Table 10-1: AC Characteristics**

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $F_{OSC}$ | Oscillation Frequency of Display Timing Generator | $V_{DD}$ = 1.8V | TBD | TBD | TBD | kHz |
| $F_{FRM}$ | Frame Frequency | 128x96 Graphic Display Mode, Display ON, Internal Oscillator Enabled | - | 105 | - | Hz |
| RES# | Reset low pulse width | | 3 | - | - | us |

**Table 10-2: 6800-Series Parallel Interface Timing Characteristics**

($V_{DD}$ - $V_{SS}$ = 1.65V to 3.5V, $T_A$ = 25℃)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{cycle}$ | Clock Cycle Time | 300 | - | - | ns |
| $t_{AS}$ | Address Setup Time | TBD | - | - | ns |
| $t_{AH}$ | Address Hold Time | TBD | - | - | ns |
| $t_{DSW}$ | Write Data Setup Time | TBD | - | - | ns |
| $t_{DHW}$ | Write Data Hold Time | TBD | - | - | ns |
| $t_{DHR}$ | Read Data Hold Time | TBD | - | - | ns |
| $t_{OH}$ | Output Disable Time | - | - | TBD | ns |
| $t_{ACC}$ | Access Time | - | - | TBD | ns |
| $PW_{CSL}$ | Chip Select Low Pulse Width (read)<br>Chip Select Low Pulse Width (write) | TBD<br>TBD | - | - | ns |
| $PW_{CSH}$ | Chip Select High Pulse Width (read)<br>Chip Select High Pulse Width (write) | TBD<br>TBD | - | - | ns |
| $t_R$ | Rise Time | - | - | 15 | ns |
| $t_F$ | Fall Time | - | - | 15 | ns |

**Figure 10-1: 6800-series parallel interface characteristics**

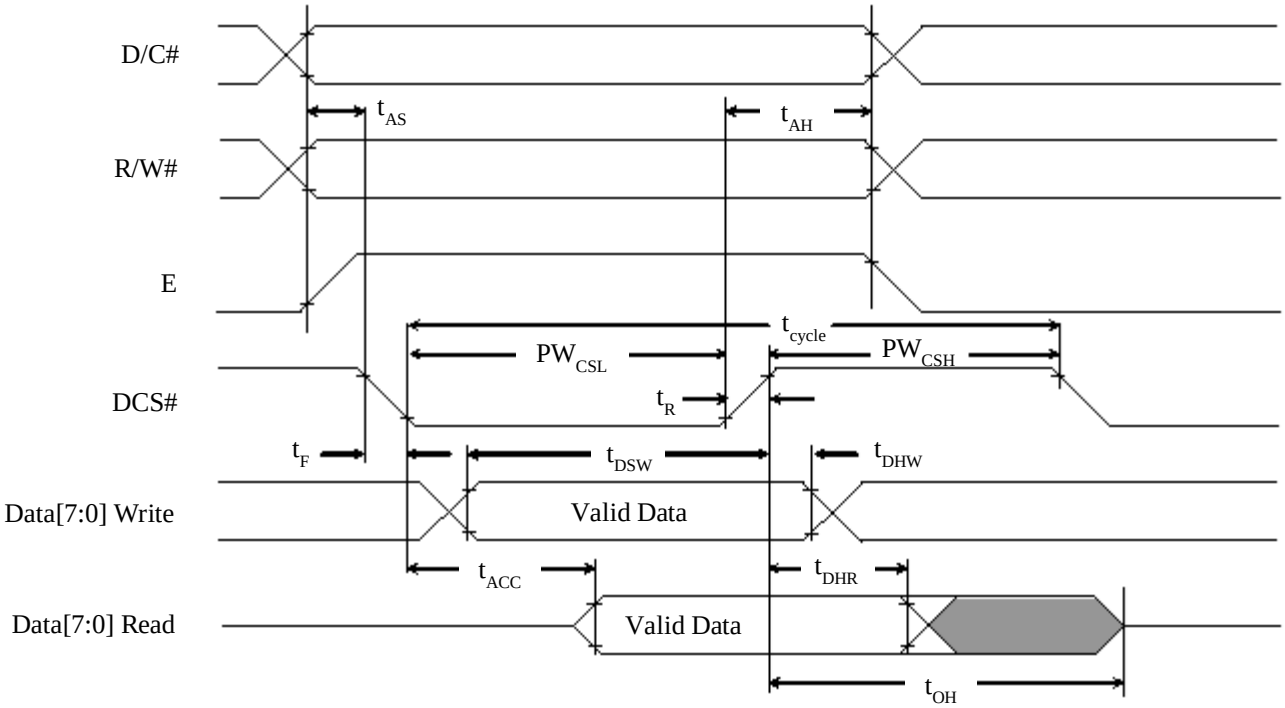
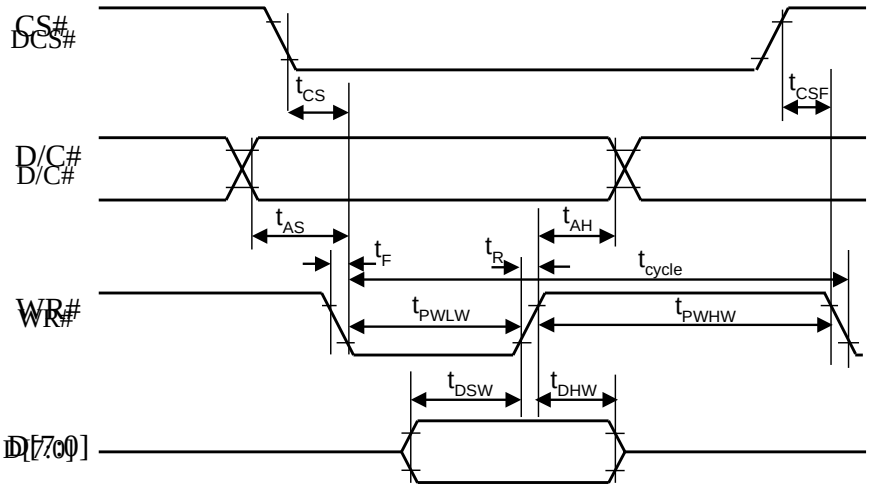


**Table 10-3: 8080-Series Parallel Interface Timing Characteristics**

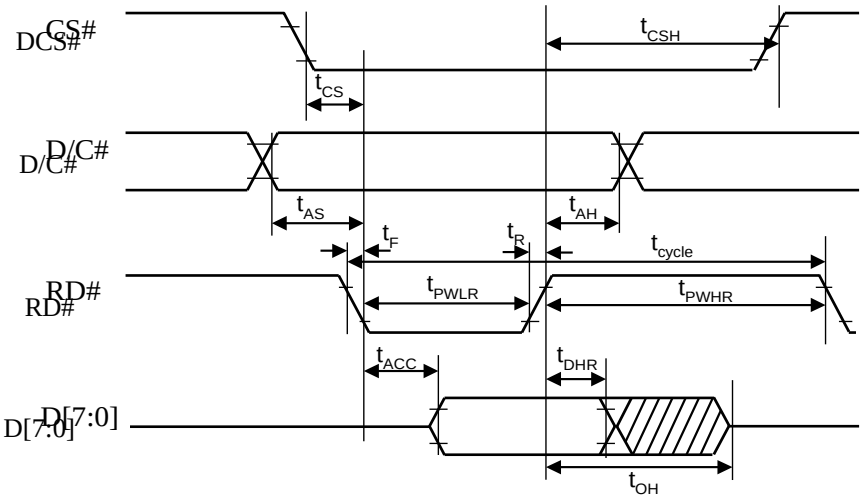
($V_{DD}$ - $V_{SS}$ = 1.65V ~3.5V, $T_A$ = 25℃)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{cycle}$ | Clock Cycle Time | 300 | - | - | ns |
| $t_{AS}$ | Address Setup Time | TBD | - | - | ns |
| $t_{AH}$ | Address Hold Time | TBD | - | - | ns |
| $t_{DSW}$ | Write Data Setup Time | TBD | - | - | ns |
| $t_{DHW}$ | Write Data Hold Time | TBD | - | - | ns |
| $t_{DHR}$ | Read Data Hold Time | TBD | - | - | ns |
| $t_{OH}$ | Output Disable Time | - | - | TBD | ns |
| $t_{ACC}$ | Access Time | - | - | TBD | ns |
| $t_{PWLR}$ | Read Low Time | TBD | - | - | ns |
| $t_{PWLW}$ | Write Low Time | TBD | - | - | ns |
| $t_{PWHR}$ | Read High Time | TBD | - | - | ns |
| $t_{PWHW}$ | Write High Time | TBD | - | - | ns |
| $t_R$ | Rise Time | - | - | 15 | ns |
| $t_F$ | Fall Time | - | - | 15 | ns |
| $t_{CS}$ | Chip select setup time | TBD | - | - | ns |
| $t_{CSH}$ | Chip select hold time to read signal | TBD | - | - | ns |
| $t_{CSF}$ | Chip select hold time | TBD | - | - | ns |

**Figure 10-2: 8080-series parallel interface characteristics**




**Write Cycle**




**Read Cycle**

**Table 10-4: Serial Interface Timing Characteristics (4-wire SPI)**

($V_{DD}$ - $V_{SS}$ = 1.65V~3.5V, $T_A$ = 25℃)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{cycle}$ | Clock Cycle Time | 100 | - | - | ns |
| $t_{AS}$ | Address Setup Time | TBD | - | - | ns |
| $t_{AH}$ | Address Hold Time | TBD | - | - | ns |
| $t_{CSS}$ | Chip Select Setup Time | TBD | - | - | ns |
| $t_{CSH}$ | Chip Select Hold Time | TBD | - | - | ns |
| $t_{DSW}$ | Write Data Setup Time | TBD | - | - | ns |
| $t_{DHW}$ | Write Data Hold Time | TBD | - | - | ns |
| $t_{CLKL}$ | Clock Low Time | TBD | - | - | ns |
| $t_{CLKH}$ | Clock High Time | TBD | - | - | ns |
| $t_R$ | Rise Time | - | - | 15 | ns |
| $t_F$ | Fall Time | - | - | 15 | ns |

**Figure 10-3: Serial interface characteristics (4-wire SPI)**

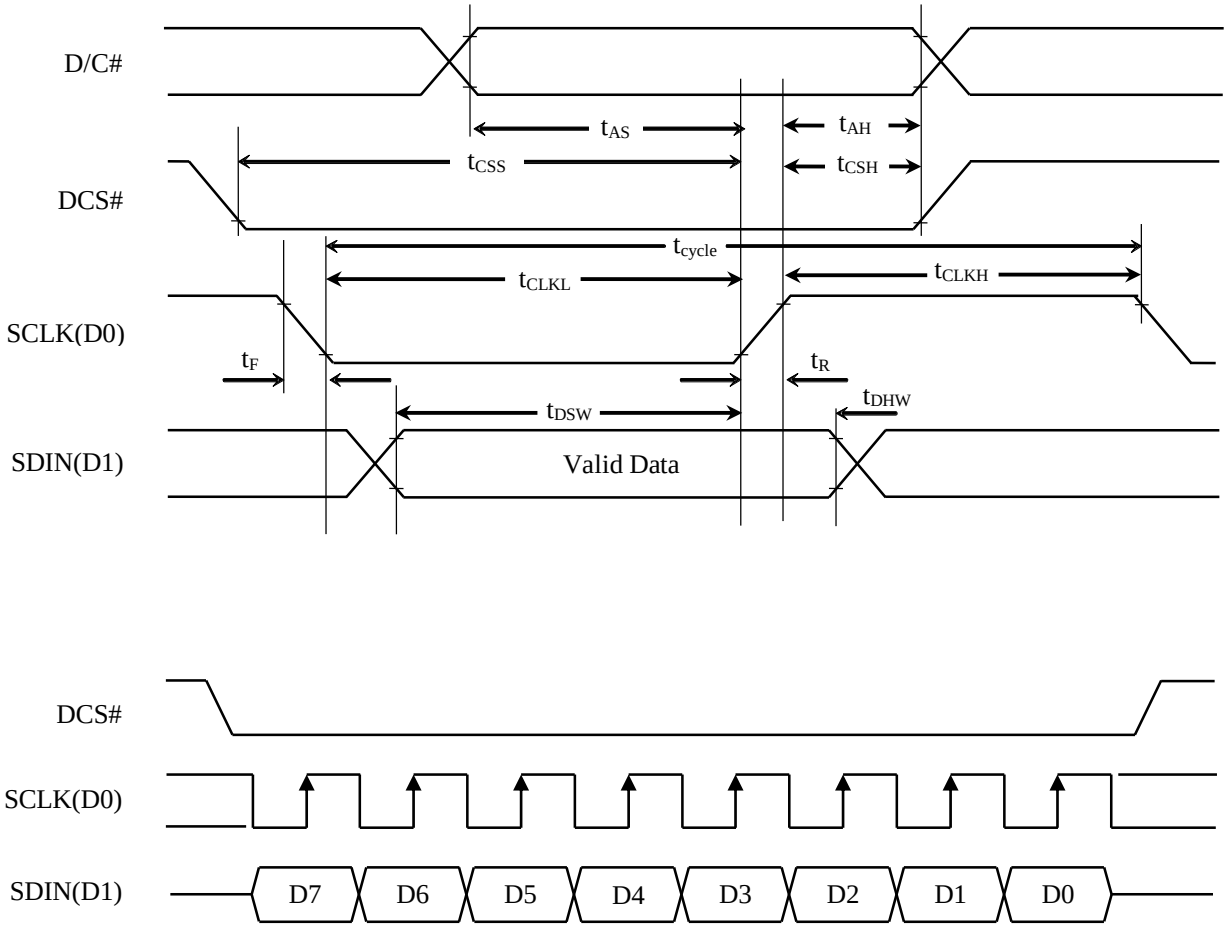


**Table 10-5: Serial Interface Timing Characteristics (3-wire SPI)**

($V_{DD}$ - $V_{SS}$ = 1.65V~3.5V, $T_A$ = 25℃)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{cycle}$ | Clock Cycle Time | 100 | - | - | ns |
| $t_{CSS}$ | Chip Select Setup Time | TBD | - | - | ns |
| $t_{CSH}$ | Chip Select Hold Time | TBD | - | - | ns |
| $t_{DSW}$ | Write Data Setup Time | TBD | - | - | ns |
| $t_{DHW}$ | Write Data Hold Time | TBD | - | - | ns |
| $t_{CLKL}$ | Clock Low Time | TBD | - | - | ns |
| $t_{CLKH}$ | Clock High Time | TBD | - | - | ns |
| $t_R$ | Rise Time | - | - | 15 | ns |
| $t_F$ | Fall Time | - | - | 15 | ns |

**Figure 10-4: Serial interface characteristics (3-wire SPI)**

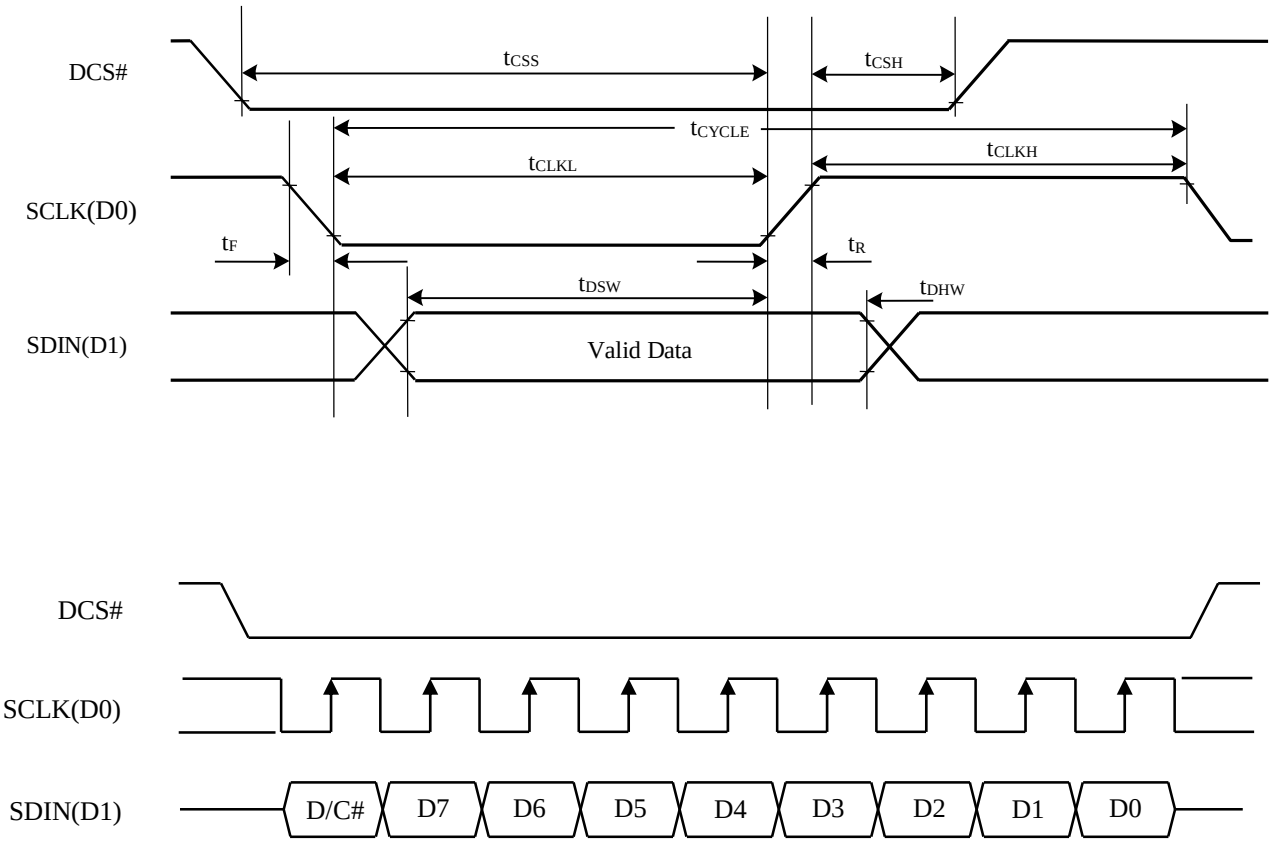
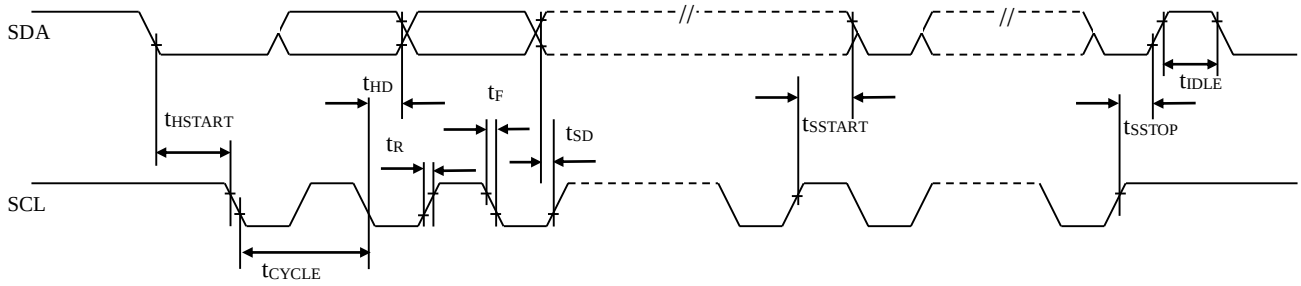


**Table 10-6: I²C Interface Timing Characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{cycle}$ | Clock Cycle Time | 2.5 | - | - | us |
| $t_{HSTART}$ | Start condition Hold Time | 0.6 | - | - | us |
| $t_{HD}$ | Data Hold Time (for "$SDA_{OUT}$" pin) | 0 | - | - | ns |
| | Data Hold Time (for "$SDA_{IN}$" pin) | 300 | - | - | ns |
| $t_{SD}$ | Data Setup Time | 100 | - | - | ns |
| $t_{SSTART}$ | Start condition Setup Time (Only relevant for a repeated Start condition) | 0.6 | - | - | us |
| $t_{SSTOP}$ | Stop condition Setup Time | 0.6 | - | - | us |
| $t_R$ | Rise Time for data and clock pin | - | - | 300 | ns |
| $t_F$ | Fall Time for data and clock pin | - | - | 300 | ns |
| $t_{IDLE}$ | Idle Time before a new transmission can start | 1.3 | - | - | us |

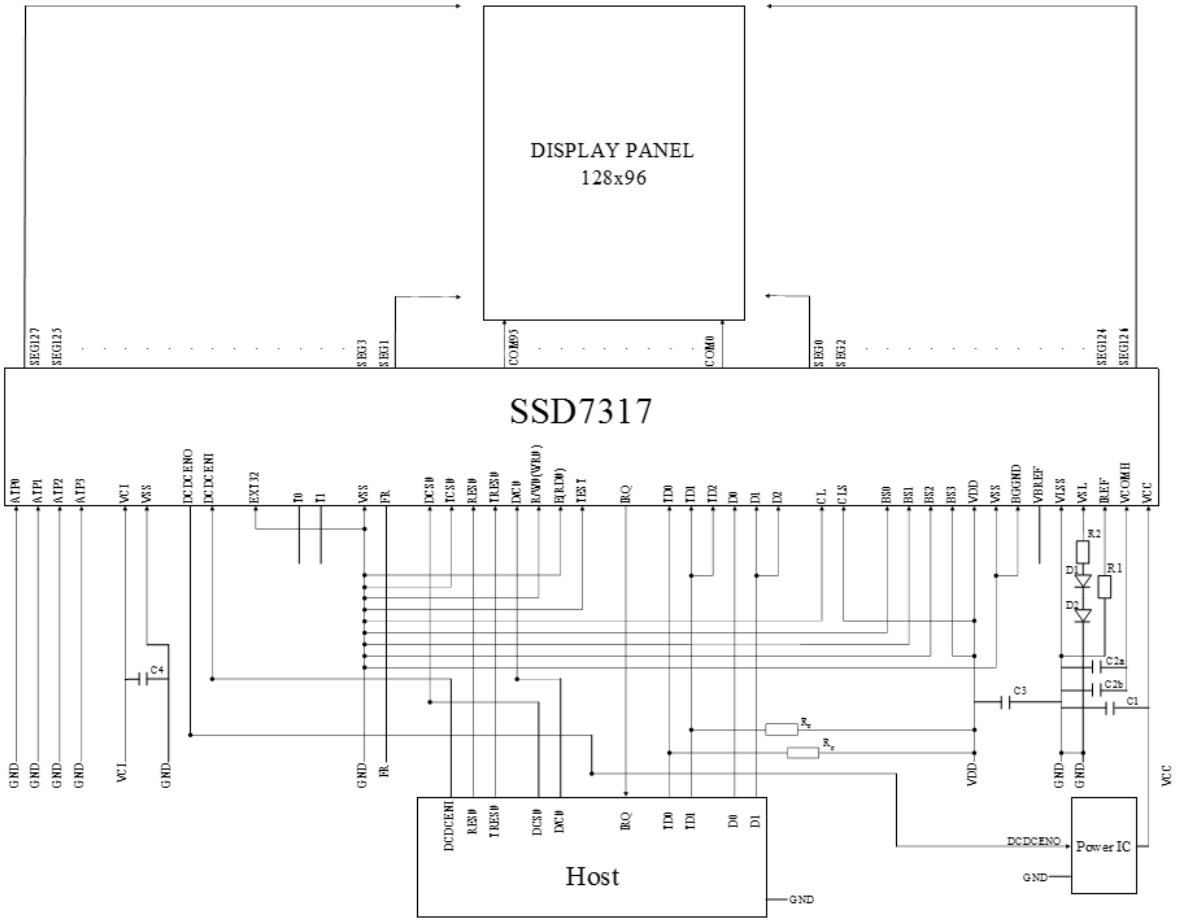
**Figure 10-5: I²C interface Timing characteristics**



# 11 APPLICATION EXAMPLE

**Figure 11-1: Application Example of SSD7317 with Touch Function**

The configuration for SPI4 mode to display interface, $I^2C$ mode to touch interface with 128x96 panel module application is shown in the following diagram: ($V_{DD}$ = 1.8V, $V_{CI}$ = 3.3V, $V_{CC}$ = 12V, $I_{REF}$ = 18.75uA)




Pin connected to AP interface: D[2:0], DCS#, D/C#, IRQ, TD[2:0], RES#, TRES#, DCDCENI
Pin connected to Power IC Enable pin: DCDCENO
Pin internally connected to $V_{SS}$: CL, D[7:3], E, R/W#, BGGND, TCS#, EXT32, TEST
Pin internally connected to $V_{DD}$: CLS
VBREF, FR, T0, T1, TR[19:0], RX[3:0], SHx should be left open.
ATP[3:0] should connect to external GND separately

C1, C2: 2.2uF (1)
C3, C4: 1.0uF (1)
R2, R3: Pull up resistor

Voltage at $I_{REF}$ = $V_{CC}$ – 2V. For $V_{CC}$ = 12V, $I_{REF}$ = 18.75uA:
R1 = (Voltage at $I_{REF}$ - $V_{SS}$) / $I_{REF}$
= (12-2) / 18.75uA
= 530KΩ

**Note**
(1) The capacitor value is recommended value. Select appropriate value against module application.
(2) Die gold bump face up.
(3) All $V_{LSS}$ pads of IC are recommended to be connected together to form a larger area of GND
(4) $V_{LSS}$ and $V_{SS}$ are not recommended to be connected on the ITO routing, but connected together in the PCB level at one common ground point for better grounding and noise insulation.

The product(s) listed in this datasheet comply with Directive 2011/65/EU of the European Parliament and of the council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People’s Republic of China Electronic Industry Standard GB/T 26572-2011 “Requirements for concentration limits for certain hazardous substances in electronic information products (电子电器产品中限用物質的限用要求)”. Hazardous Substances test report is available upon request.

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