SSD1307

Advance Information

128 x 39 Dot Matrix
OLED/PLED Segment/Common Driver with Controller

Appendix: IC Revision history of SSD1307 Specification

Version	Change Items	Effective Date
1.0	1. Changed to Advance Information 2. Update the TBD values in Table 11-1 : DC Characteristics 3. Update the TBD values in Table 12-1 : AC Characteristics	28-Dec-07
1.1	1. Revised section 7.9 Power ON and OFF sequence (power OFF sequence 3 and note 4) 2. Typo: Revise command table 26/27h : E[6:0] to E[7:0], F[6:0] to F[7:0] 3. Add SSD1307Z die tray information	22-Feb-08
1.2	1. Revised the frame freq formula (K) – P.20 2. Revise typo on CL pin connection -- P.20 3. Remove t_{AS} & t_{AH} timing in Table 12.5 4. Revise typo in Figure 12.4 5. Add D0 pin in Table 7.4 & Table 7.5	16-Oct-08
1.3	1. Revise Fig 13-1 Application diagram 2. Add +/- 0.05mm tolerance for Die Size (after sawing) 3. Update die thickness tolerance from ±25um to ±15um	07-Aug-09
1.4	1. P.7 , P.9, P.30, P,31, P.53 & P.54 Replace SSD1307Z by SSD1307Z2 and add SSD1307Z2 into ordering information 2. P.55 Revise declaimer	20-Oct-10

CONTENT

FIGURES

TABLE

1 GENERAL DESCRIPTION

SSD1307 is a single-chip CMOS OLED/PLED driver with controller for organic / polymer light emitting diode dot-matrix graphic display system. It consists of 128 segments and 39 commons. This IC is designed for Common Cathode type OLED panel.

The SSD1307 embeds with contrast control, display RAM and oscillator, which reduces the number of external components and power consumption. It has 256-step brightness control. Data/Commands are sent from general MCU through the hardware selectable 6800/8080 series compatible Parallel Interface, I^2C interface or Serial Peripheral Interface. It is suitable for many compact portable applications, such as mobile phone sub-display, MP3 player and calculator, etc.

2 FEATURES

- Resolution: 128 x 39 dot matrix panel
- Power supply
  - V_{DD} = 1.65V ~ 3.3V (IC logic)
  - V_{CC} = 7V ~ 15V (Panel driving power supply)
- For matrix display
  - OLED driving output voltage, 15V maximum
  - Segment maximum source current: 320uA
  - Common maximum sink current: 40mA
  - 256 step contrast brightness current control
- Embedded 128 x 39 bit SRAM display buffer
- Pin selectable MCU Interfaces:
  - 8-bit 6800/8080-series parallel interface
  - 3 /4 wire Serial Peripheral Interface
  - I^2C Interface
- Screen saving continuous scrolling function in both horizontal and vertical direction
- Programmable Frame Rate
- Programmable Multiplexing Ratio
- Row Re-mapping and Column Re-mapping
- On-Chip Oscillator
- Chip layout for COG , COF
- Wide range of operating temperature: -40°C to 85°C

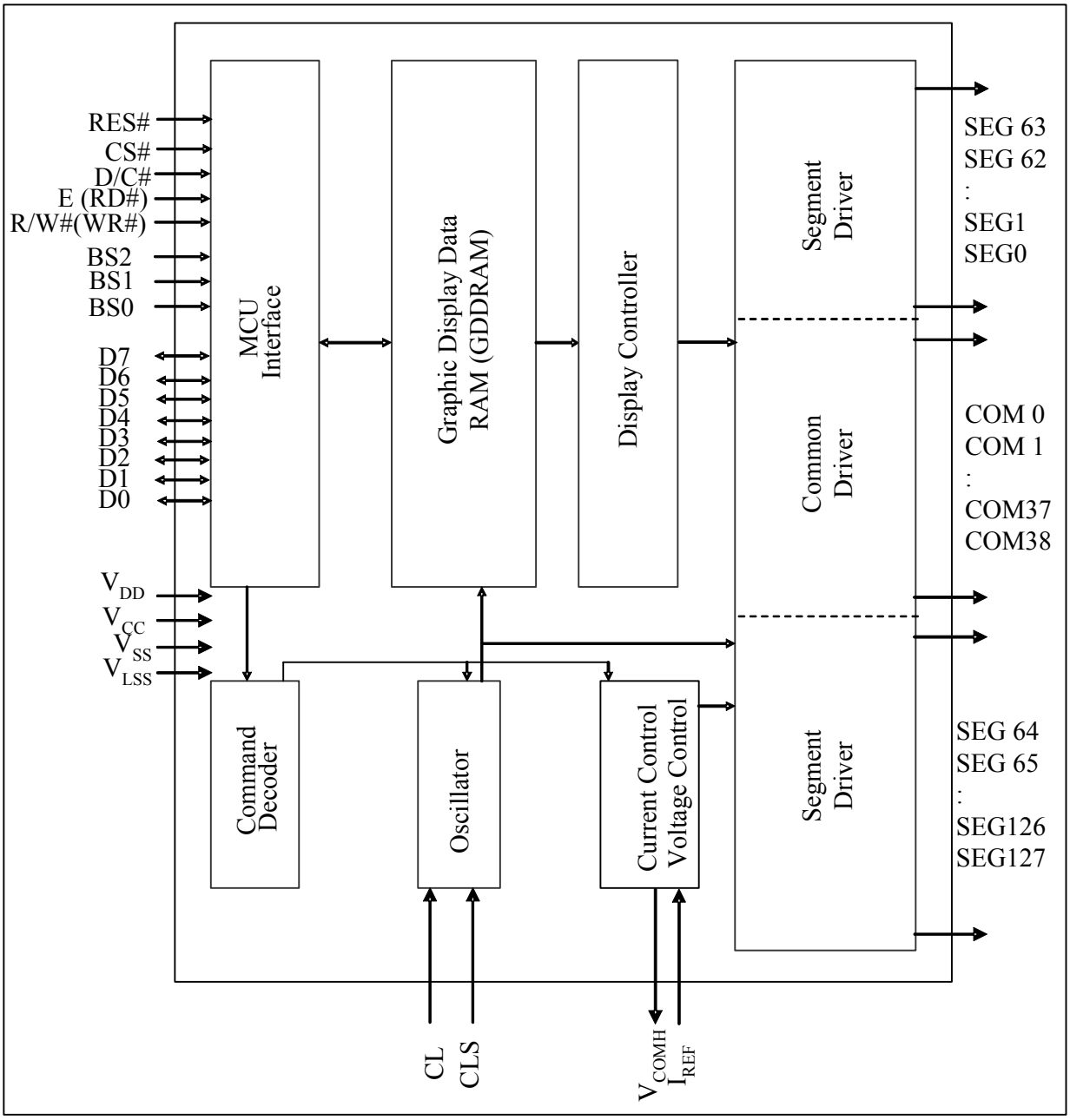
3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD1307Z2	128	39	COG	Page 9	o Min SEG pad pitch : 32.4um o Min COM pad pitch : 40um o Die thickness : 300 +/- 15 um

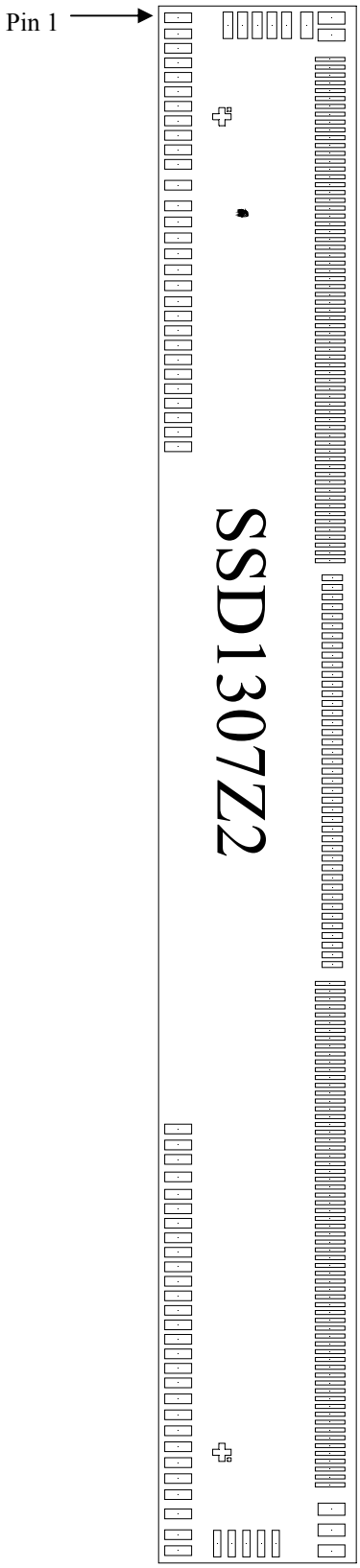
4 BLOCK DIAGRAM

Figure 4-1 : SSD1307 Block Diagram



5 DIE PAD FLOOR PLAN

Figure 5-1 : SSD1307Z2 Die Drawing

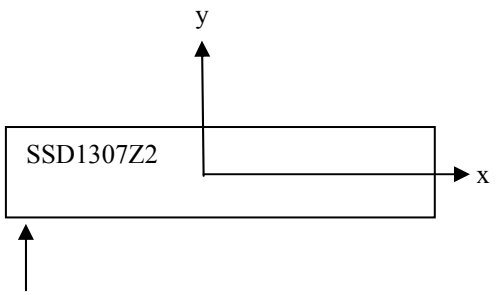


Die Size (after sawing)	6.44mm +/- 0.05mm x 0.81mm +/- 0.05mm
Die Thickness	300 um ± 15 um
Min I/O pad pitch	60 um
Min SEG pad pitch	32.4 um
Min COM pad pitch	40 um
Bump Height	Nominal 12 um

Bump Size		
Pad #	**X [um]**	**Y [um]**
1~57	40	110
240~244	110	40
58~62	110	30
63~65, 237~238	50	110
66~130 , 172~236	16.4	122
131~171	24	84
239	110	50

Note

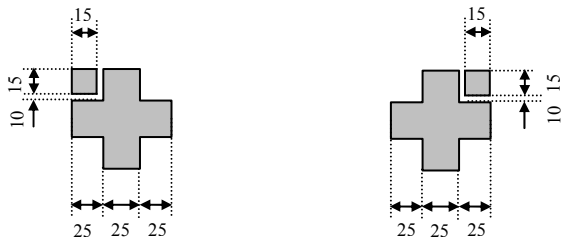
(1) Diagram showing the Gold bumps face up.
(2) Coordinates are referenced to center of the chip.
(3) Coordinate units and size of all alignment marks are in um.
(4) All alignment keys do not contain gold



Pad 1, 2, 3 .... -> 57

Gold Bumps face up

Figure 5-2 : SSD1307Z2 Alignment mark dimensions



Center: (-2762, -146)
Size: 75 x 75 μm²

Center: (2762, -146)
Size: 75 x 75 μm²

Table 5-1 : SSD1307Z2 Bump Die Pad Coordinates

Pin number	Pin name	X	Y
1	NC	-3171.0	-325.0
2	VCC	-3105.0	-325.0
3	VCC	-3045.0	-325.0
4	VCC	-2985.0	-325.0
5	VCC	-2925.0	-325.0
6	NC	-2865.0	-325.0
7	VLSS	-2805.0	-325.0
8	VLSS	-2745.0	-325.0
9	VSS	-2685.0	-325.0
10	NC	-2625.0	-325.0
11	VDD	-2565.0	-325.0
12	VDD	-2479.0	-325.0
13	FR	-2393.0	-325.0
14	VSS	-2327.0	-325.0
15	CS#	-2261.0	-325.0
16	RES#	-2195.0	-325.0
17	D/C#	-2129.0	-325.0
18	VSS	-2063.0	-325.0
19	R/W#(WR#)	-1997.0	-325.0
20	E(RD#)	-1937.0	-325.0
21	D0	-1877.0	-325.0
22	D1	-1817.0	-325.0
23	D2	-1757.0	-325.0
24	D3	-1697.0	-325.0
25	VSS	-1637.0	-325.0
26	D4	-1577.0	-325.0
27	D5	-1517.0	-325.0
28	D6	-1457.0	-325.0
29	D7	-1397.0	-325.0
30	IREF	1425.0	-325.0
31	VLSS	1491.0	-325.0
32	VLSS	1551.0	-325.0
33	NC	1623.0	-325.0
34	VCOMH	1695.0	-325.0
35	VCOMH	1755.0	-325.0
36	VCOMH	1815.0	-325.0
37	VCOMH	1875.0	-325.0
38	VCC	1935.0	-325.0
39	VCC	1995.0	-325.0
40	VCC	2055.0	-325.0
41	VCC	2115.0	-325.0
42	CL	2175.0	-325.0
43	VSS	2235.0	-325.0
44	VSS	2295.0	-325.0
45	CLS	2355.0	-325.0
46	VDD	2415.0	-325.0
47	BS0	2475.0	-325.0
48	VSS	2541.0	-325.0
49	BS1	2607.0	-325.0
50	VDD	2673.0	-325.0
51	VDD	2739.0	-325.0
52	BS2	2805.0	-325.0
53	VSS	2871.0	-325.0
54	TRB0	2937.0	-325.0
55	VDD	3017.0	-325.0
56	TRB1	3103.0	-325.0
57	VSS	3169.0	-325.0
58	TRA3	3140.0	-165.2
59	TRA2	3140.0	-105.2
60	VSS	3140.0	-45.2
61	TRA1	3140.0	14.8
62	TRA0	3140.0	74.8
63	VCC	3170.0	303.3
64	VLSS	3083.7	303.3
65	VLSS	2997.4	303.3
66	SEG63	2896.6	297.3
67	SEG62	2864.2	297.3
68	SEG61	2831.8	297.3
69	SEG60	2799.4	297.3
70	SEG59	2767.0	297.3
71	SEG58	2734.6	297.3
72	SEG57	2702.2	297.3
73	SEG56	2669.8	297.3
74	SEG55	2637.4	297.3
75	SEG54	2605.0	297.3
76	SEG53	2572.6	297.3
77	SEG52	2540.2	297.3
78	SEG51	2507.8	297.3
79	SEG50	2475.4	297.3
80	SEG49	2443.0	297.3
81	SEG48	2410.6	297.3
82	SEG47	2378.2	297.3
83	SEG46	2345.8	297.3
84	SEG45	2313.4	297.3
85	SEG44	2281.0	297.3
86	SEG43	2248.6	297.3
87	SEG42	2216.2	297.3
88	SEG41	2183.8	297.3
89	SEG40	2151.4	297.3
90	SEG39	2119.0	297.3
91	SEG38	2086.6	297.3
92	SEG37	2054.2	297.3
93	SEG36	2021.8	297.3
94	SEG35	1989.4	297.3
95	SEG34	1957.0	297.3
96	SEG33	1924.6	297.3
97	SEG32	1892.2	297.3
98	SEG31	1859.8	297.3
99	SEG30	1827.4	297.3
100	SEG29	1795.0	297.3
101	SEG28	1762.6	297.3
102	SEG27	1730.2	297.3
103	SEG26	1697.8	297.3
104	SEG25	1665.4	297.3
105	SEG24	1633.0	297.3
106	SEG23	1600.6	297.3
107	SEG22	1568.2	297.3
108	SEG21	1535.8	297.3
109	SEG20	1503.4	297.3
110	SEG19	1471.0	297.3
111	SEG18	1438.6	297.3
112	SEG17	1406.2	297.3
113	SEG16	1373.8	297.3
114	SEG15	1341.4	297.3
115	SEG14	1309.0	297.3
116	SEG13	1276.6	297.3
117	SEG12	1244.2	297.3
118	SEG11	1211.8	297.3
119	SEG10	1179.4	297.3
120	SEG9	1147.0	297.3
121	SEG8	1114.6	297.3
122	SEG7	1082.2	297.3
123	SEG6	1049.8	297.3
124	SEG5	1017.4	297.3
125	SEG4	985.0	297.3
126	SEG3	952.6	297.3
127	SEG2	920.2	297.3
128	SEG1	887.8	297.3
129	SEG0	855.4	297.3
130	VCOMH	823.0	297.3
131	NC	744.8	306.0
132	COM0	704.8	306.0
133	COM1	664.8	306.0
134	COM2	624.8	306.0
135	COM3	584.8	306.0
136	COM4	544.8	306.0
137	COM5	504.8	306.0
138	COM6	464.8	306.0
139	COM7	424.8	306.0
140	COM8	384.8	306.0
141	COM9	344.8	306.0
142	COM10	304.8	306.0
143	COM11	264.8	306.0
144	COM12	224.8	306.0
145	COM13	184.8	306.0
146	COM14	144.8	306.0
147	COM15	104.8	306.0
148	COM16	64.8	306.0
149	COM17	24.8	306.0
150	COM18	-15.2	306.0
151	COM19	-55.2	306.0
152	COM20	-95.2	306.0
153	COM21	-135.2	306.0
154	COM22	-175.2	306.0
155	COM23	-215.2	306.0
156	COM24	-255.2	306.0
157	COM25	-295.2	306.0
158	COM26	-335.2	306.0
159	COM27	-375.2	306.0
160	COM28	-415.2	306.0
161	COM29	-455.2	306.0
162	COM30	-495.2	306.0
163	COM31	-535.2	306.0
164	COM32	-575.2	306.0
165	COM33	-615.2	306.0
166	COM34	-655.2	306.0
167	COM35	-695.2	306.0
168	COM36	-735.2	306.0
169	COM37	-775.2	306.0
170	COM38	-815.2	306.0
171	NC	-855.2	306.0
172	VCOMH	-925.7	297.3
173	SEG64	-958.1	297.3
174	SEG65	-990.5	297.3
175	SEG66	-1022.9	297.3
176	SEG67	-1055.3	297.3
177	SEG68	-1087.7	297.3
178	SEG69	-1120.1	297.3
179	SEG70	-1152.5	297.3
180	SEG71	-1184.9	297.3
181	SEG72	-1217.3	297.3
182	SEG73	-1249.7	297.3
183	SEG74	-1282.1	297.3
184	SEG75	-1314.5	297.3
185	SEG76	-1346.9	297.3
186	SEG77	-1379.3	297.3
187	SEG78	-1411.7	297.3
188	SEG79	-1444.1	297.3
189	SEG80	-1476.5	297.3
190	SEG81	-1508.9	297.3
191	SEG82	-1541.3	297.3
192	SEG83	-1573.7	297.3
193	SEG84	-1606.1	297.3
194	SEG85	-1638.5	297.3
195	SEG86	-1670.9	297.3
196	SEG87	-1703.3	297.3
197	SEG88	-1735.7	297.3
198	SEG89	-1768.1	297.3
199	SEG90	-1800.5	297.3
200	SEG91	-1832.9	297.3
201	SEG92	-1865.3	297.3
202	SEG93	-1897.7	297.3
203	SEG94	-1930.1	297.3
204	SEG95	-1962.5	297.3
205	SEG96	-1994.9	297.3
206	SEG97	-2027.3	297.3
207	SEG98	-2059.7	297.3
208	SEG99	-2092.1	297.3
209	SEG100	-2124.5	297.3
210	SEG101	-2156.9	297.3
211	SEG102	-2189.3	297.3
212	SEG103	-2221.7	297.3
213	SEG104	-2254.1	297.3
214	SEG105	-2286.5	297.3
215	SEG106	-2318.9	297.3
216	SEG107	-2351.3	297.3
217	SEG108	-2383.7	297.3
218	SEG109	-2416.1	297.3
219	SEG110	-2448.5	297.3
220	SEG111	-2480.9	297.3
221	SEG112	-2513.3	297.3
222	SEG113	-2545.7	297.3
223	SEG114	-2578.1	297.3
224	SEG115	-2610.5	297.3
225	SEG116	-2642.9	297.3
226	SEG117	-2675.3	297.3
227	SEG118	-2707.7	297.3
228	SEG119	-2740.1	297.3
229	SEG120	-2772.5	297.3
230	SEG121	-2804.9	297.3
231	SEG122	-2837.3	297.3
232	SEG123	-2869.7	297.3
233	SEG124	-2902.1	297.3
234	SEG125	-2934.5	297.3
235	SEG126	-2966.9	297.3
236	SEG127	-2999.3	297.3
237	VCC	-3100.0	303.3
238	VCC	-3170.0	303.3
239	NC	-3140.0	201.8
240	VCC	-3140.0	119.0
241	VCC	-3140.0	59.0
242	VCOMH	-3140.0	-1.0
243	VCOMH	-3140.0	-61.0
244	VLSS	-3140.0	-121.0

6 PIN DESCRIPTION

Key:

I = Input	NC = Not Connected
O =Output	Pull LOW= connect to Ground
I/O = Bi-directional (input/output)	Pull HIGH= connect to V_{DD}
P = Power pin	

Table 6-1 : Pin Description

Pin Name	Type	Description
V_{DD}	P	Power supply pin for core logic operation.
V_{CC}	P	Power supply for panel driving voltage. This is also the most positive power voltage supply pin.
V_{SS}	P	This is a ground pin.
V_{LSS}	P	This is an analog ground pin. It should be connected to V_{SS} externally.
V_{COMH}	O	The pin is for COM signal deselected voltage level. A capacitor should be connected between this pin and V_{SS}.
BS[2:0]	I	MCU bus interface selection pins. Please refer to Table 6-2 for the details of setting.
I_{REF}	I	This is segment output current reference pin. A resistor should be connected between this pin and V_{SS} to maintain the I_{REF} current at 10 uA. Please refer to **Figure 7-14** for the details of resistor value.
FR	O	This pin outputs RAM write synchronization signal. Proper timing between MCU data writing and frame display timing can be achieved to prevent tearing effect. It should be kept NC if it is not used. Please refer to Section **7.4** for details usage.
CL	I	This is external clock input pin. When internal clock is enabled (i.e. HIGH in CLS pin), this pin is not used and should be connected to V_{SS}. When internal clock is disabled (i.e. LOW in CLS pin), this pin is the external clock source input pin.
CLS	I	This is internal clock enable pin. When it is pulled HIGH (i.e. connect to VDD), internal clock is enabled. When it is pulled LOW, the internal clock is disabled; an external clock source must be connected to the CL pin for normal operation.
RES#	I	This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin HIGH (i.e. connect to V_{DD}) during normal operation.
CS#	I	This pin is the chip select input. (active LOW)
D/C#	I	This is Data/Command control pin. When it is pulled HIGH (i.e. connect to V_{DD}), the data at D[7:0] is treated as data. When it is pulled LOW, the data at D[7:0] will be transferred to the command register. In I^2C mode, this pin acts as SA0 for slave address selection. When 3-wire serial interface is selected, this pin must be connected to V_{SS}. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams: Figure 12-1 to Figure 12-5.

Pin Name	Type	Description
E (RD#)	I	When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH (i.e. connect to V_{DD}) and the chip is selected. When connecting to an 8080-series microprocessor, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface is selected, this pin must be connected to V_{SS}.
R/W#(WR#)	I	This is read / write control input pin connecting to the MCU interface. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH (i.e. connect to VDD) and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I2C interface is selected, this pin must be connected to V_{SS}.
D[7:0]	IO	These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be kept NC. When I^2C mode is selected, D2, D1 should be tied together and serve as SDA_{out}, SDA_{in} in application and D0 is the serial clock input, SCL.
TRA[3:0]	-	Reserved pin and is recommended to keep it float.
TRB[1:0]	-	Reserved pin and is recommended to be connected to V_{SS}.
SEG0 ~ SEG127	O	These pins provide Segment switch signals to OLED panel. These pins are V_{SS} state when display is OFF.
COM0 ~ COM39	O	These pins provide Common switch signals to OLED panel. They are in high impedance state when display is OFF.
NC	-	This is dummy pin. Do not group or short NC pins together.

Table 6-2 : MCU Bus Interface Pin Selection

SSD1307 Pin Name	I^2C Interface	6800-parallel interface (8 bit)	8080-parallel interface (8 bit)	4-wire Serial interface	3-wire Serial interface
BS0	0	0	0	0	1
BS1	1	0	1	0	0
BS2	0	1	1	0	0

Note
(1) 0 is connected to V_{SS}
(2) 1 is connected to V_{DD}

7 FUNCTIONAL BLOCK DESCRIPTIONS

7.1 MCU Interface selection

SSD1307 MCU interface consist of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 7-1. Different MCU mode can be set by hardware selection on BS[2:0] pins (please refer to Table 6-2 for BS[2:0] setting).

Table 7-1 : MCU interface assignment under different bus interface mode

Pin Name / Bus Interface	Data/Command Interface								Control Signal				
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**E**	**R/W#**	**CS#**	**D/C#**	**RES#**
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
3-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	Tie LOW	RES#
4-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	D/C#	RES#
I^2C	Tie LOW					SDA_{OUT}	SDA_{IN}	SCL	Tie LOW			SA0	RES#

7.1.1 MCU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.
A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

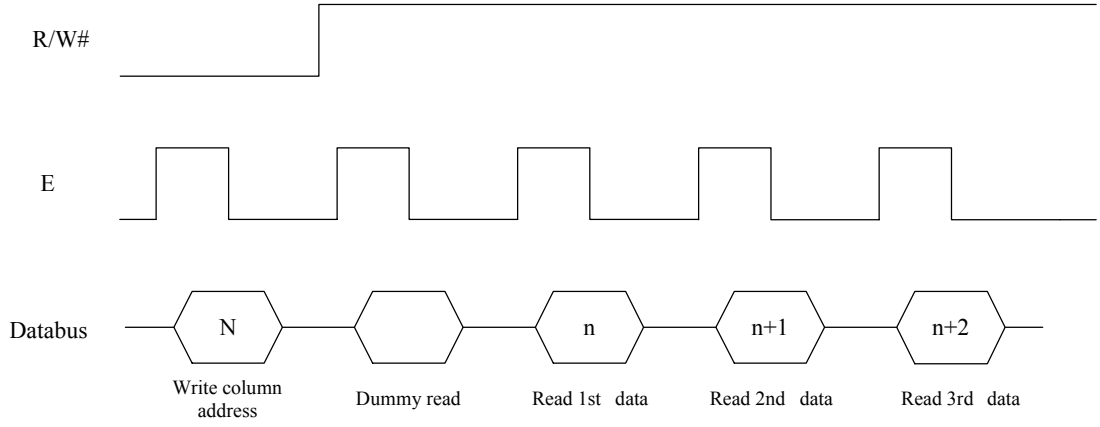
Table 7-2 : Control pins of 6800 interface

Function	E	R/W#	CS#	D/C#
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note
(1) ↓ stands for falling edge of signal
H stands for HIGH in signal
L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 7-1.

Figure 7-1 : Data read back procedure - insertion of dummy read



7.1.2 MCU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.
A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 7-2 : Example of Write procedure in 8080 parallel interface mode

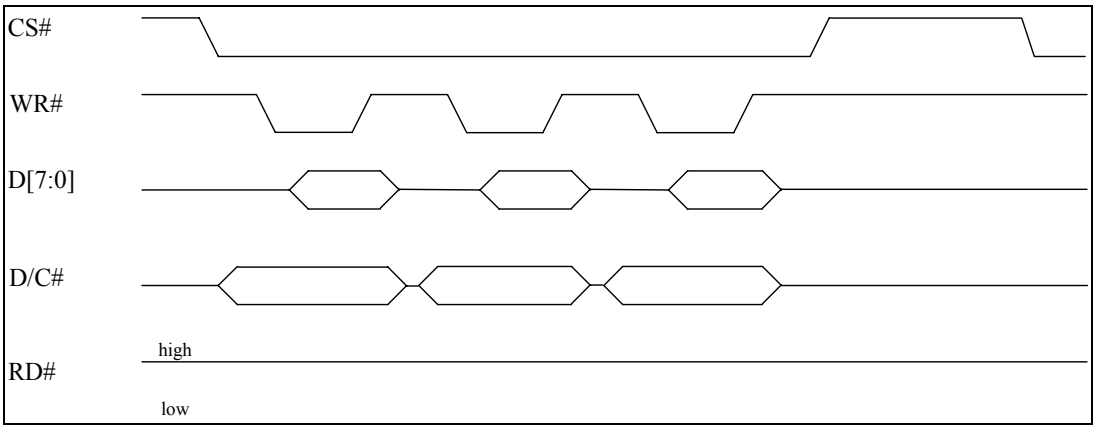


Figure 7-3 : Example of Read procedure in 8080 parallel interface mode

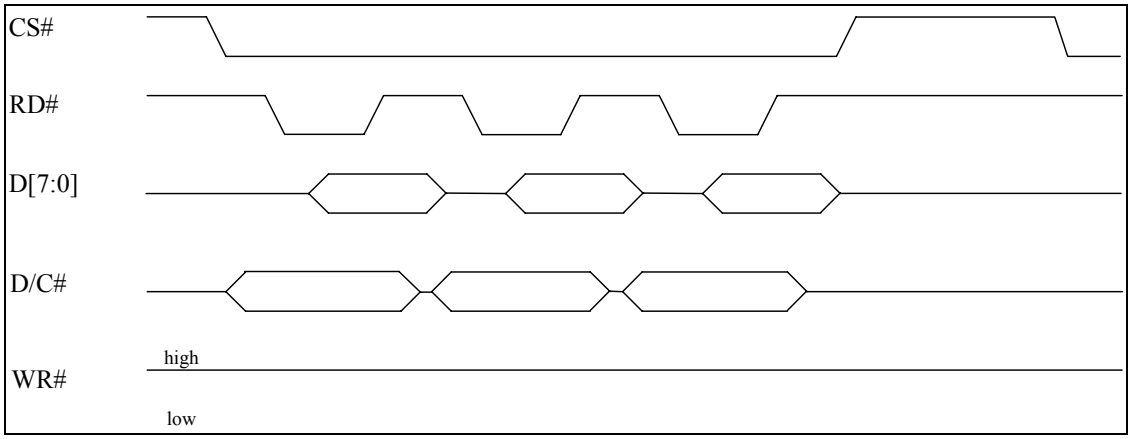


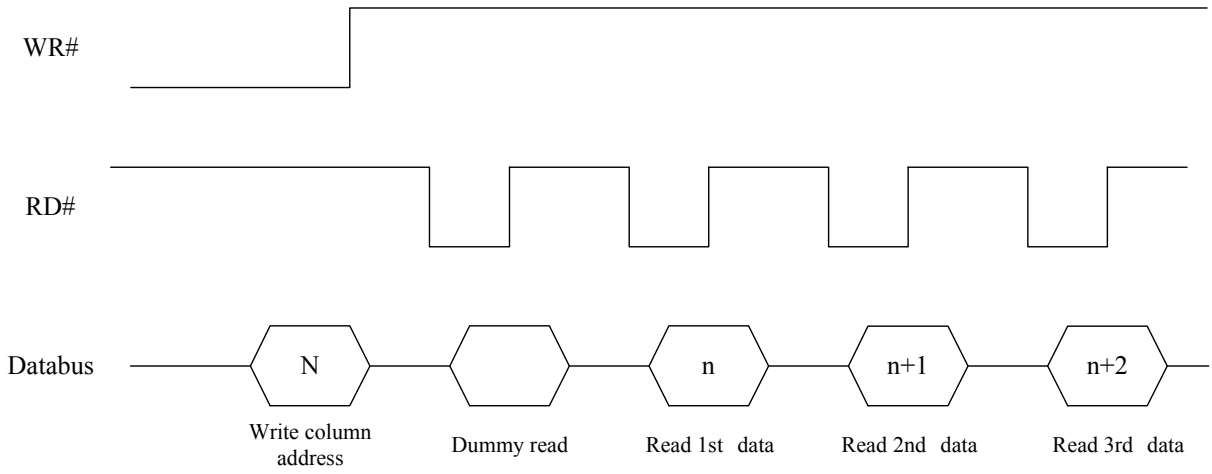
Table 7-3 : Control pins of 8080 interface

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note
(1) ↑ stands for rising edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 7-4.

Figure 7-4 : Display data read back procedure - insertion of dummy read



7.1.3 MCU Serial Interface (4-wire SPI)

The 4-wire serial interface consists of serial clock: SCLK, serial data: SDIN, D/C#, CS#. In 4-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, E and R/W# (WR#)# can be connected to an external ground.

Table 7-4 : Control pins of 4-wire Serial interface

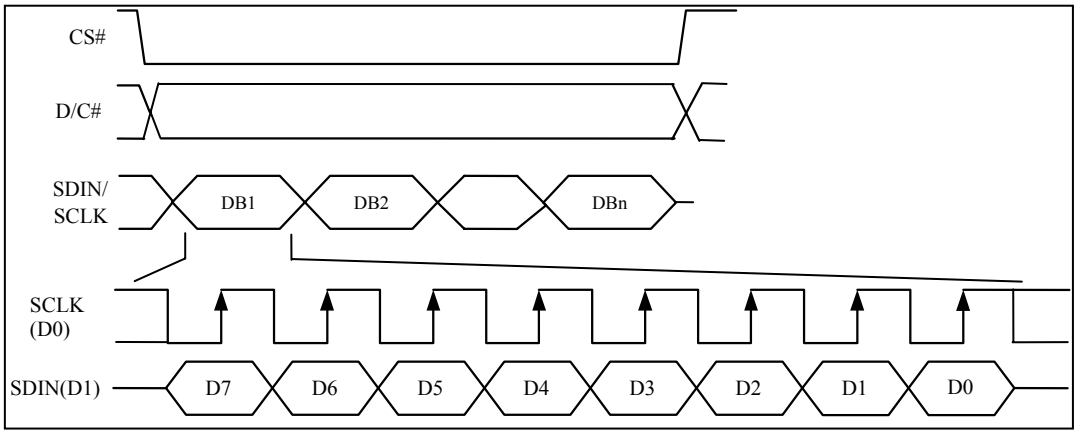
Function	E	R/W#	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	L	↑
Write data	Tie LOW	Tie LOW	L	H	↑

Note
(1) H stands for HIGH in signal
(2) L stands for LOW in signal
(3) ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

Figure 7-5 : Write procedure in 4-wire Serial interface mode



7.1.4 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#.
In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, R/W# (WR#)#, E and D/C# can be connected to an external ground.

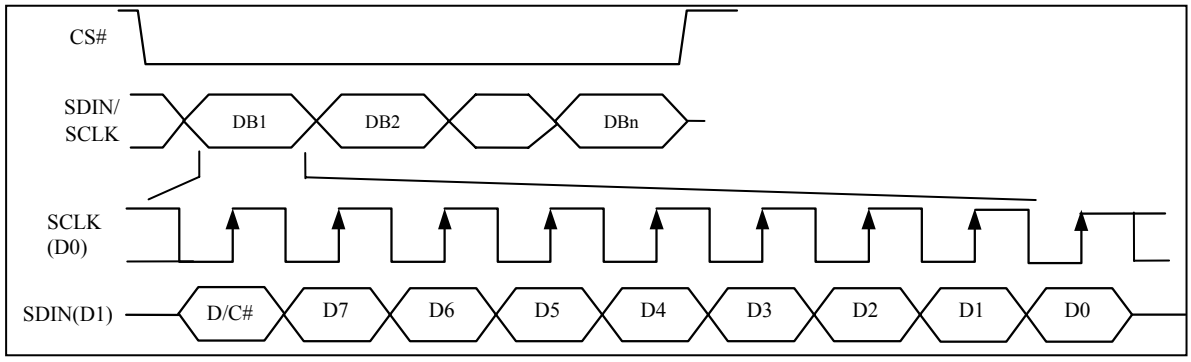
The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0). Under serial mode, only write operations are allowed.

Table 7-5 : Control pins of 3-wire Serial interface

Function	E(RD#)	R/W#(WR#)	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	Tie LOW	↑
Write data	Tie LOW	Tie LOW	L	Tie LOW	↑

Note
(1) L stands for LOW in signal
(2) ↑ stands for rising edge of signal

Figure 7-6 : Write procedure in 3-wire Serial interface mode



7.1.5 MCU I^2C Interface

The I^2C communication interface consists of slave address bit SA0, I^2C-bus data signal SDA (SDA_{OUT}/D_2 for output and SDA_{IN}/D_1 for input) and I^2C-bus clock signal SCL (D_0). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bit (SA0)
SSD1307 has to recognize the slave address before transmitting or receiving any information by the I^2C-bus. The device will respond to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format,

b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0
0 1 1 1 1 0 SA0 R/W#

"SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101", can be selected as the slave address of SSD1307. D/C# pin acts as SA0 for slave address selection.
"R/W#" bit is used to determine the operation mode of the I^2C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.

b) I^2C-bus data signal (SDA)
SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.

It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".

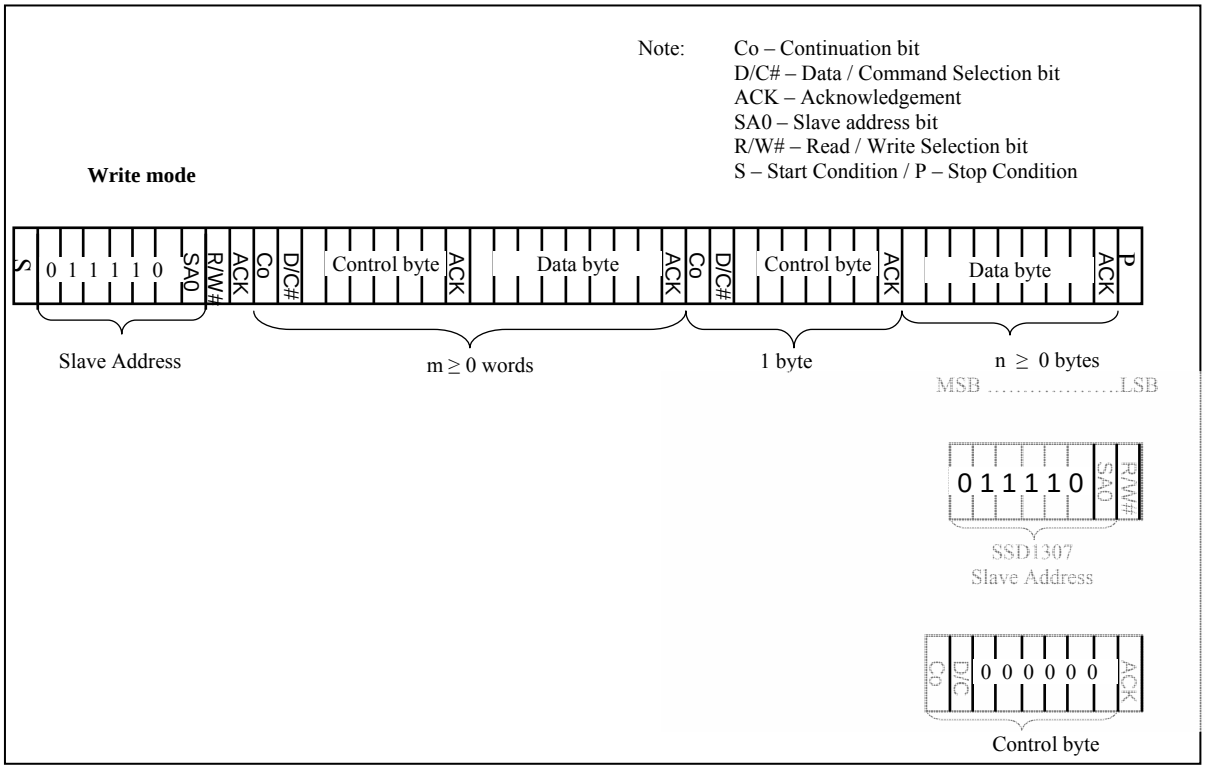
"SDA_{IN}" and "SDA_{OUT}" are tied together and serve as SDA. The "SDA_{IN}" pin must be connected to act as SDA. The "SDA_{OUT}" pin may be disconnected. When "SDA_{OUT}" pin is disconnected, the acknowledgement signal will be ignored in the I^2C-bus.

c) I^2C-bus clock signal (SCL)
The transmission of information in the I^2C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

7.1.5.1 I²C-bus Write data

The I²C-bus interface gives access to write data and command into the device. Please refer to Figure 7-7 for the write mode of I²C-bus in chronological order.

Figure 7-7 : I²C-bus data format



7.1.5.2 Write mode for I2C

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 7-8. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
2) The slave address is following the start condition for recognition use. For the SSD1307, the slave address is either "b0111100" or "b0111101" by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).
3) The write mode is established by setting the R/W# bit to logic "0".
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 7-9 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six "0" 's.
    a. If the Co bit is set as logic "0", the transmission of the following information will contain data bytes only.
    b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic "0", it defines the following data byte as a command. If the D/C# bit is set to logic "1", it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
6) Acknowledge bit will be generated after receiving each control byte or data byte.
7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 7-8. The stop condition is established by pulling the "SDA in" from LOW to HIGH while the "SCL" stays HIGH.

Figure 7-8 : Definition of the Start and Stop Condition

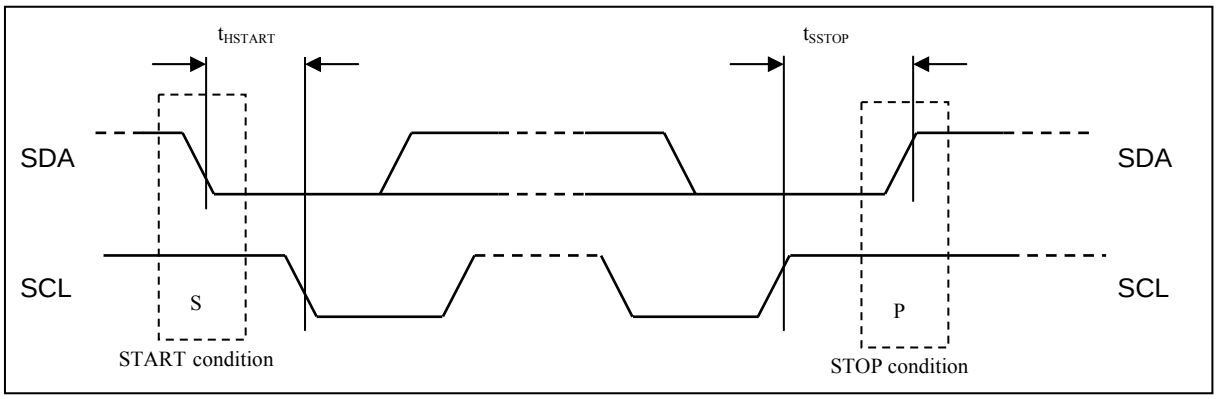
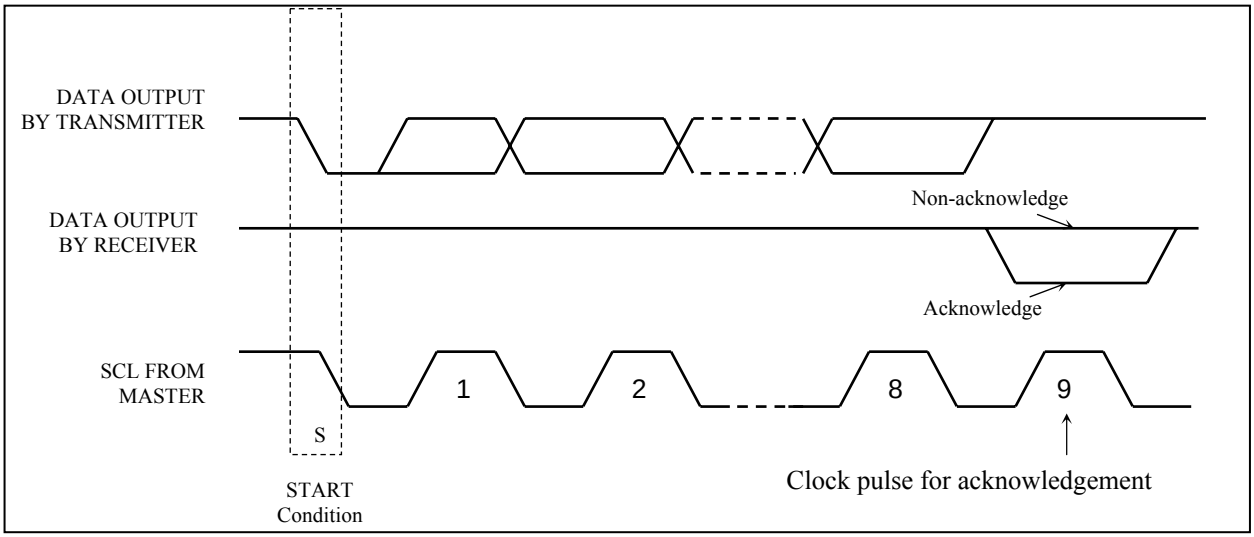


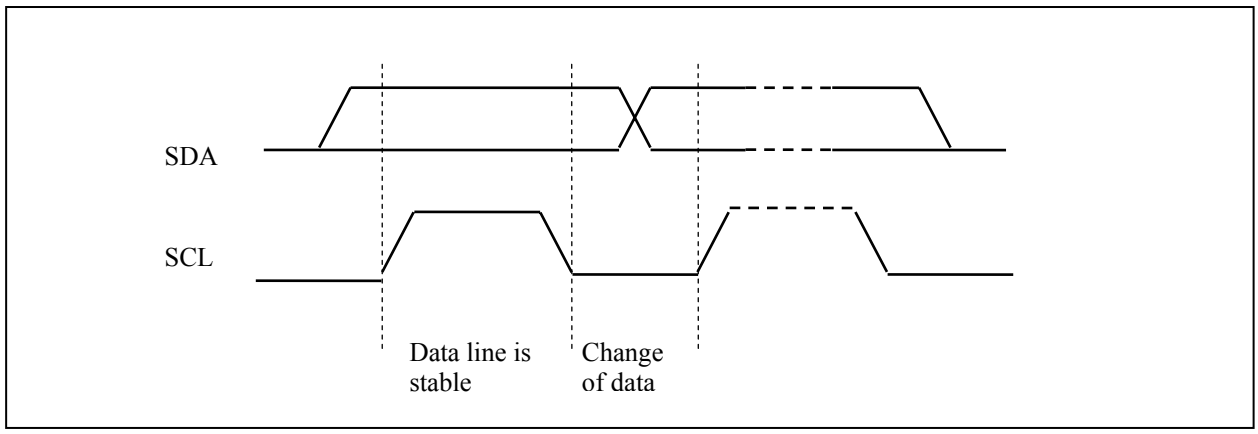
Figure 7-9 : Definition of the acknowledgement condition



Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Please refer to the Figure 7-10 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

Figure 7-10 : Definition of the data transfer condition



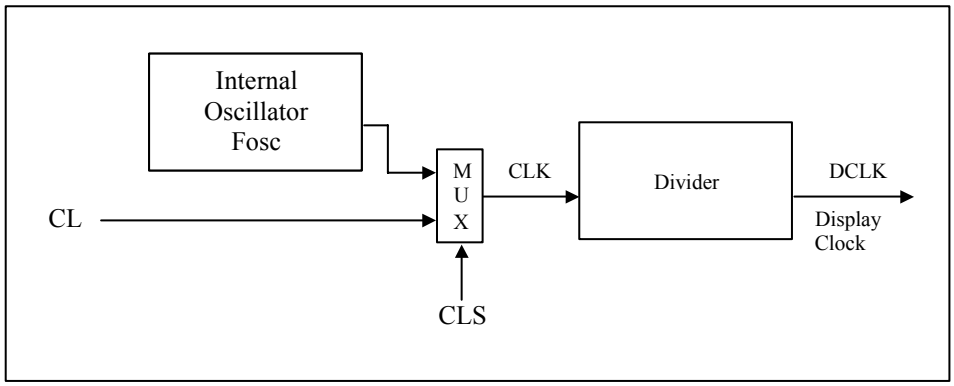
7.2 Command Decoder

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is HIGH, D[7:0] is interpreted as display data written to Graphic Display Data RAM (GDDRAM). If it is LOW, the input at D[7:0] is interpreted as a command. Then data input will be decoded and written to the corresponding command register.

7.3 Oscillator Circuit and Display Time Generator

Figure 7-11 : Oscillator Circuit and Display Time Generator



This module is an on-chip LOW power RC oscillator circuitry. The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is pulled HIGH, internal oscillator is chosen and CL should be connected to V_{SS}. Pulling CLS pin LOW disables internal oscillator and external clock must be connected to CL pins for proper operation. When the internal oscillator is selected, its output frequency Fosc can be changed by command D5h A[7:4].

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor "D" can be programmed from 1 to 16 by command D5h

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula.

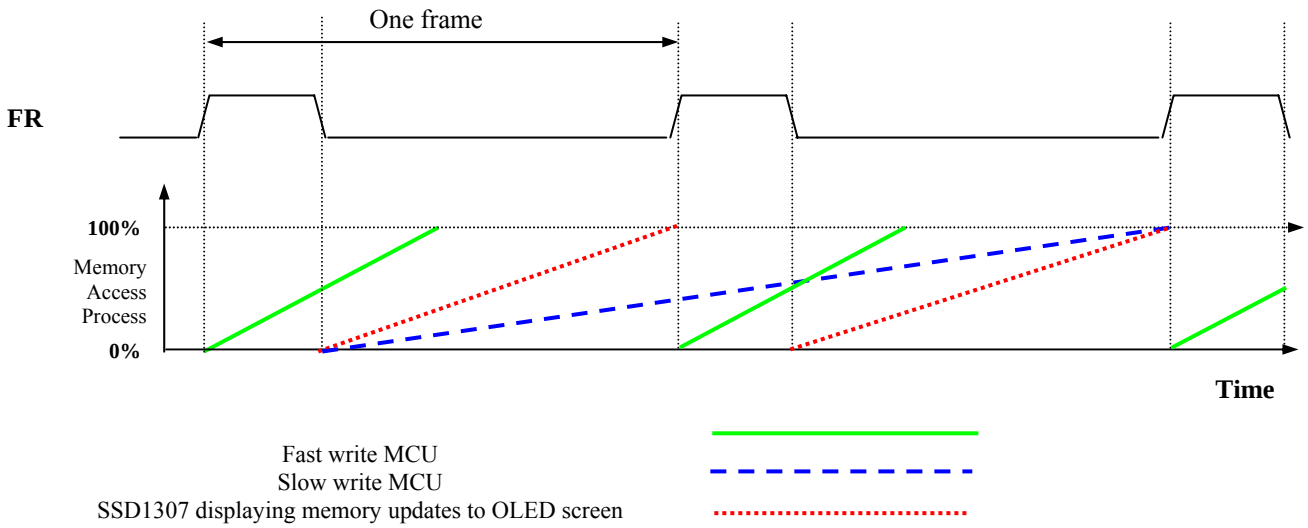
$$F_{FRM} = \frac{F_{osc}}{D \times K \times \text{No. of Mux}}$$

where

- D stands for clock divide ratio. It is set by command D5h A[3:0]. The divide ratio has the range from 1 to 16.
- K is the number of display clocks per row. The value is derived by
  K = Phase 1 period + Phase 2 period + K_o
  = 2 + 2 + 50 = 54 at power on reset (that is K_o is a constant that equals to 50)
  (Please refer to Section 7.6 "Segment Drivers / Common Drivers" for the details of the "Phase")
- Number of multiplex ratio is set by command A8h. The power on reset value is 38 (i.e. 39MUX).
- F_{OSC} is the oscillator frequency. It can be changed by command D5h A[7:4]. The higher the register setting results in higher frequency.

7.4 FR synchronization

FR synchronization signal can be used to prevent tearing effect.



The starting time to write a new image to OLED driver is depended on the MCU writing speed. If MCU can finish writing a frame image within one frame period, it is classified as fast write MCU. For MCU needs longer writing time to complete (more than one frame but within two frames), it is a slow write one.

For fast write MCU: MCU should start to write new frame of ram data just after rising edge of FR pulse and should be finished well before the rising edge of the next FR pulse.

For slow write MCU: MCU should start to write new frame ram data after the falling edge of the 1st FR pulse and must be finished before the rising edge of the 3rd FR pulse.

7.5 Reset Circuit

When RES# input is LOW, the chip is initialized with the following status:

1. Display is OFF
2. 128 x 39 Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

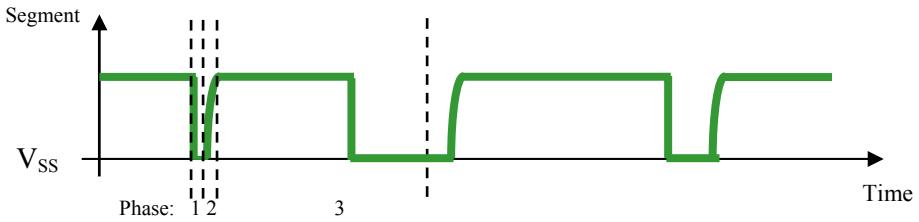
7.6 Segment Drivers / Common Drivers

Segment drivers deliver 128 current sources to drive the OLED panel. The driving current can be adjusted from 0 to 320uA with 256 steps. Common drivers generate voltage-scanning pulses.

The segment driving waveform is divided into three phases:

1. In phase 1, the OLED pixel charges of previous image are discharged in order to prepare for next image content display.
2. In phase 2, the OLED pixel is driven to the targeted voltage. The pixel is driven to attain the corresponding voltage level from V_{SS}. The period of phase 2 can be programmed in length from 1 to 15 DCLKs. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.
3. In phase 3, the OLED driver switches to use current source to drive the OLED pixels and this is the current drive stage.

Figure 7-12 : Segment Output Waveform in three phases



After finishing phase 3, the driver IC will go back to phase 1 to display the next row image data. This three-step cycle is run continuously to refresh image display on OLED panel.

In phase 3, if the length of current drive pulse width is set to 50, after finishing 50 DCLKs in current drive phase, the driver IC will go back to phase 1 for next row display.

7.7 Graphic Display Data RAM (GDDRAM)

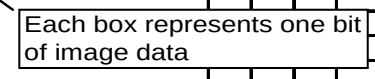
The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 x 39 bits and the RAM is divided into five pages, from PAGE0 to PAGE4, which are used for monochrome 128x39 dot matrix display, as shown in Figure 7-13.

When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row. For PAGE4, bit D7 is treated as don't care bit.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. For vertical shifting of the display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display (command D3h).

Figure 7-13 : GDDRAM pages structure of SSD1307

Segment re-mapping (command A1h)		SEG127	SEG126	SEG125	SEG124	.....	SEG4	SEG3	SEG2	SEG1	SEG0		
Segment re-mapping (command A0h [RESET])		SEG0	SEG1	SEG2	SEG3	.....	SEG123	SEG124	SEG125	SEG126	SEG127		
Page	Data	COL0	COL1	COL2	COL3	.....	COL123	COL124	COL125	COL126	COL127	COM Output Scan Direction (command C0h [RESET])	COM Output Scan Direction (command C8h)
0	D0					.....						COM0	COM38
	D1											COM1	COM37
	D2											COM2	COM36
	D3											COM3	COM35
	D4											COM4	COM34
	D5											COM5	COM33
	D6											COM6	COM32
	D7											COM7	COM31
1	D0					.....						COM8	COM30
	D1											COM9	COM29
	D2											COM10	COM28
	D3											COM11	COM27
	D4											COM12	COM26
	D5											COM13	COM25
	D6											COM14	COM24
	D7											COM15	COM23
2	D0					.....						COM16	COM22
	D1											COM17	COM21
	D2											COM18	COM20
	D3											COM19	COM19
	D4											COM20	COM18
	D5											COM21	COM17
	D6											COM22	COM16
	D7											COM23	COM15
3	D0					.....						COM24	COM14
	D1											COM25	COM13
	D2											COM26	COM12
	D3											COM27	COM11
	D4											COM28	COM10
	D5											COM29	COM9
	D6											COM30	COM8
	D7											COM31	COM7
4	D0					.....						COM32	COM6
	D1											COM33	COM5
	D2											COM34	COM4
	D3											COM35	COM3
	D4											COM36	COM2
	D5											COM37	COM1
	D6											COM38	COM0
	D7	Don't care bit											



7.8 SEG/COM Driving block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

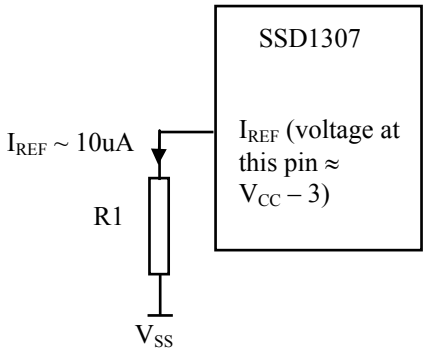
- V_{CC} is the most positive voltage supply.
- V_{COMH} is the Common deselected level. It is internally regulated.
- V_{LSS} is the ground path of the analog and panel current.
- I_{REF} is a reference current source for segment current drivers I_{SEG}. The relationship between reference current and segment current of a color is:

  I_{SEG} = (Contrast+1) /8 x I_{REF}

  in which the contrast (0~255) is set by Set Contrast command

The magnitude of I_{REF} is controlled by the value of resistor, which is connected between I_{REF} pin and Vss as shown in Figure 7-14. It is recommended to set I_{REF} to 10 ± 2uA so as to achieve I_{SEG} = 320uA at maximum contrast 255.

Figure 7-14 : I_{REF} Current Setting by Resistor Value



Since the voltage at I_{REF} pin is V_{CC} – 3V, the value of resistor R1 can be found as below:

For I_{REF} = 10uA, V_{CC} =12V:

R1 = (Voltage at I_{REF} – V_{SS}) / I_{REF}
≈ (12 – 3) / 10uA
= 900kΩ

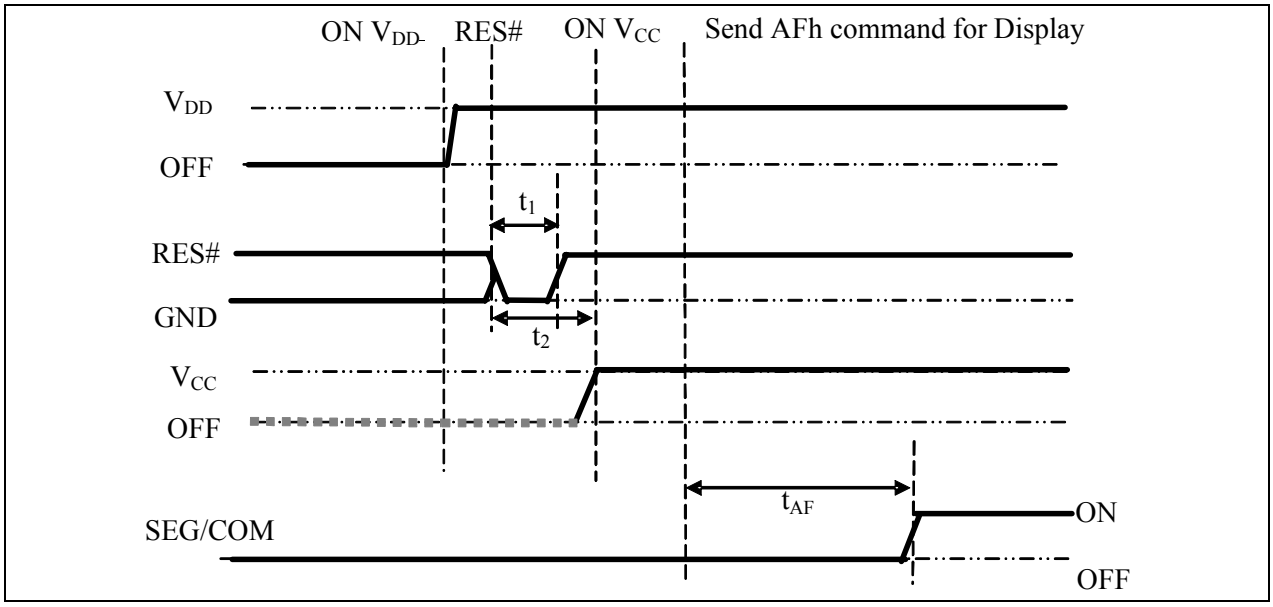
7.9 Power ON and OFF sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1307

Power ON sequence:

1. Power ON V_{DD}
2. After V_{DD} become stable, set RES# pin LOW (logic low) for at least 3us (t_1) [3] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC}.[1]
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}).

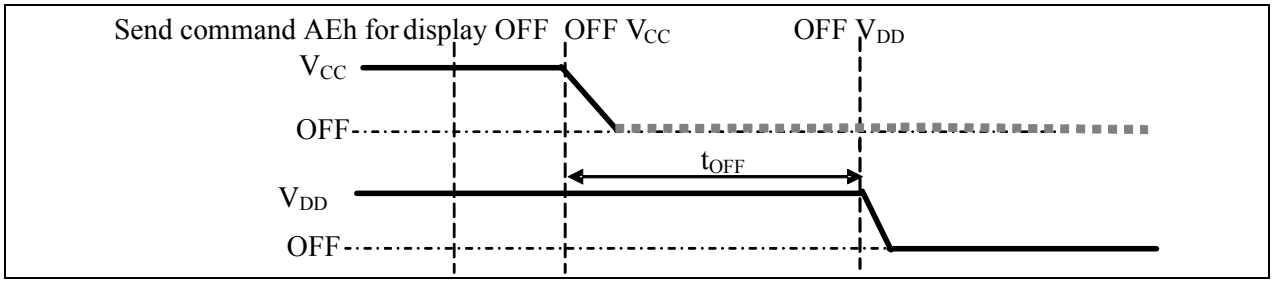
Figure 7-15 : The Power ON sequence



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}.[1], [2]
3. Power OFF V_{DD} after t_{OFF}. [4] (typical t_{OFF}=100ms)

Figure 7-16 : The Power OFF sequence



Note:

(1) V_{CC} should be kept float (i.e. disable) when it is OFF.
(2) Power Pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.
(3) The register values are reset after t_1.
(4) V_{DD} should not be Power OFF before V_{CC} Power OFF.

8 Command Table

Table 8-1: Proposed SSD1307 Command Table

(R/W#(WR#) = 0, E(RD#) = 1 unless specific setting is stated)

1. Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast Control	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 7Fh)
0	A4/A5	1	0	1	0	0	1	0	X_0	Entire Display ON	A4h, X_0=0b: Resume to RAM content display (RESET) Output follows RAM content A5h, X_0=1b: Entire display ON Output ignores RAM content
0	A6/A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display	A6h, X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel A7h, X[0]=1b: Inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel
0	AE AF	1	0	1	0	1	1	1	X_0	Set Display ON/OFF	AEh, X[0]=0b:Display OFF (sleep mode) (RESET) AFh X[0]=1b:Display ON in normal mode

2. **Scrolling Command Table**											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	26/27	0	0	1	0	0	1	1	X_0	Continuous Horizontal Scroll Setup	26h, X[0]=0, Right Horizontal Scroll 27h, X[0]=1, Left Horizontal Scroll (Horizontal scroll by 1 column) A[7:0] : Dummy byte (Set as 00h) B[2:0] : Define start page address 000b – PAGE0 | 011b – PAGE3 | 110b – invalid 001b – PAGE1 | 100b – PAGE4 | 111b – invalid 010b – PAGE2 | 101b – invalid | C[2:0] : Set time interval between each scroll step in terms of frame frequency 000b – 5 frames | 100b – 3 frames 001b – 64 frames | 101b – 4 frames 010b – 128 frames | 110b – 25 frame 011b – 256 frames | 111b – 2 frame D[2:0] : Define end page address 000b – PAGE0 | 011b – PAGE3 | 110b – invalid 001b – PAGE1 | 100b – PAGE4 | 111b – invalid 010b – PAGE2 | 101b – invalid | The value of D[2:0] must be larger or equal to B[2:0] E[7:0] : Dummy byte (Set as 00h) F[7:0] : Dummy byte (Set as FFh)
0	A[7:0]	0	0	0	0	0	0	0	0		
0	B[2:0]	*	*	*	*	*	B_2	B_1	B_0		
0	C[2:0]	*	*	*	*	*	C_2	C_1	C_0		
0	D[2:0]	*	*	*	*	*	D_2	D_1	D_0		
0	E[7:0]	0	0	0	0	0	0	0	0		
0	F[7:0]	1	1	1	1	1	1	1	1		

2. **Scrolling Command Table**

<table>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0
0
0
0
0
0</td><td>29/2A
A[2:0]
B[2:0]
C[2:0]
D[2:0]
E[5:0]</td><td>0
0
*
*
*
*</td><td>0
0
*
*
*
*</td><td>1
0
*
*
*
E_5</td><td>0
0
*
*
*
E_4</td><td>1
0
*
*
*
E_3</td><td>0
0
B_2
C_2
D_2
E_2</td><td>X_1
0
B_1
C_1
D_1
E_1</td><td>X_0
0
B_0
C_0
D_0
E_0</td><td>Continuous Vertical and Horizontal Scroll Setup</td><td>29h, X_1X_0=01b : Vertical and Right Horizontal Scroll

2Ah, X_1X_0=10b : Vertical and Left Horizontal Scroll
(Horizontal scroll by 1 column)

A[7:0] : Dummy byte (Set as 00h)

B[2:0] : Define start page address
<table><tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – invalid</td></tr><tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b –invalid</td></tr><tr><td>010b – PAGE2</td><td>101b – invalid</td><td></td></tr></table>
C[2:0] : Set time interval between each scroll step in terms of frame frequency
<table><tr><td>000b – 5 frames</td><td>100b – 3 frames</td></tr><tr><td>001b – 64 frames</td><td>101b – 4 frames</td></tr><tr><td>010b – 128 frames</td><td>110b – 25 frame</td></tr><tr><td>011b – 256 frames</td><td>111b – 2 frame</td></tr></table>
D[2:0] : Define end page address
<table><tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – invalid</td></tr><tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – invalid</td></tr><tr><td>010b – PAGE2</td><td>101b – invalid</td><td></td></tr></table>The value of D[2:0] must be larger or equal to B[2:0]

E[5:0] : Vertical scrolling offset
e.g. E[5:0]= 01h refer to offset =1 row
E[5:0] =26h refer to offset =38 rows

Note
(1) No continuous vertical scrolling is available.</td></tr>
<tr><td>0</td><td>2E</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>Deactivate scroll</td><td>Stop scrolling that is configured by command 26h/27h/29h/2Ah.

Note
(1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.</td></tr>
<tr><td>0</td><td>2F</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>Activate scroll</td><td>Start scrolling that is configured by the scrolling setup commands :26h/27h/29h/2Ah with the following valid sequences:

Valid command sequence 1: 26h ;2Fh.
Valid command sequence 2: 27h ;2Fh.
Valid command sequence 3: 29h ;2Fh.
Valid command sequence 4: 2Ah ;2Fh.

For example, if “26h; 2Ah; 2Fh.” commands are issued, the setting in the last scrolling setup command, i.e. 2Ah in this case, will be executed. In other words, setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.</td></tr>
</table>

2. **Scrolling Command Table**											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	A3	1	0	1	0	0	0	1	1	Set Vertical Scroll Area	A[5:0] : Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0).[RESET = 0d] B[5:0] : Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 39d] **Note** (1) A[5:0]+B[5:0] <= MUX ratio (2) B[5:0] <= MUX ratio (3a) Vertical scrolling offset (E[5:0] in 29h/2Ah) < B[5:0] (3b) Set Display Start Line (X5X4X3X2X1X0 of 40h~66h) < B[5:0] (4) The last row of the scroll area shifts to the first row of the scroll area. (5) For 39d MUX display A[5:0] = 0, B[5:0]=39 : whole area scrolls A[5:0]= 0, B[5:0] < 39 : top area scrolls A[5:0] + B[5:0] < 39 : central area scrolls A[5:0] + B[5:0] = 39 : bottom area scrolls
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		
0	B[5:0]	*	*	B_5	B_4	B_3	B_2	B_1	B_0		

3. **Addressing Setting Command Table**											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	00~0F	0	0	0	0	X_3	X_2	X_1	X_0	Set Lower Column Start Address for Page Addressing Mode	Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. **Note** (1) This command is only for page addressing mode.
0	10~17	0	0	0	1	0	X_2	X_1	X_0	Set Higher Column Start Address for Page Addressing Mode	Set the higher nibble of the column start address register for Page Addressing Mode using X[2:0] as data bits. The initial display line register is reset to 0000b after RESET. **Note** (1) This command is only for page addressing mode.
0 0	20 A[1:0]	0 *	0 *	1 *	0 *	0 *	0 *	0 A_1	0 A_0	Set Memory Addressing Mode	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode (RESET) A[1:0] = 11b, Invalid

3. **Addressing Setting Command Table**											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0 0	21 A[6:0] B[6:0]	0 * *	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Setup column start and end address A[6:0] : Column start address, range : 0-127d, (RESET=0d) B[6:0]: Column end address, range : 0-127d, (RESET =127d) **Note** (1) This command is only for horizontal or vertical addressing mode.
0 0 0	22 A[2:0] B[2:0]	0 * *	0 * *	1 * *	0 * *	0 * *	0 A_2 B_2	1 A_1 B_1	0 A_0 B_0	Set Page Address	Setup page start and end address A[2:0] : Page start Address, range : 0-4d, (RESET = 0d) B[2:0] : Page end Address, range : 0-4d, (RESET = 4d) **Note** (1) This command is only for horizontal or vertical addressing mode.
0	B0~B4	1	0	1	1	0	X_2	X_1	X_0	Set Page Start Address for Page Addressing Mode	Set GDDRAM Page Start Address (PAGE0~PAGE4) for Page Addressing Mode using X[2:0]. **Note** (1) This command is only for page addressing mode.

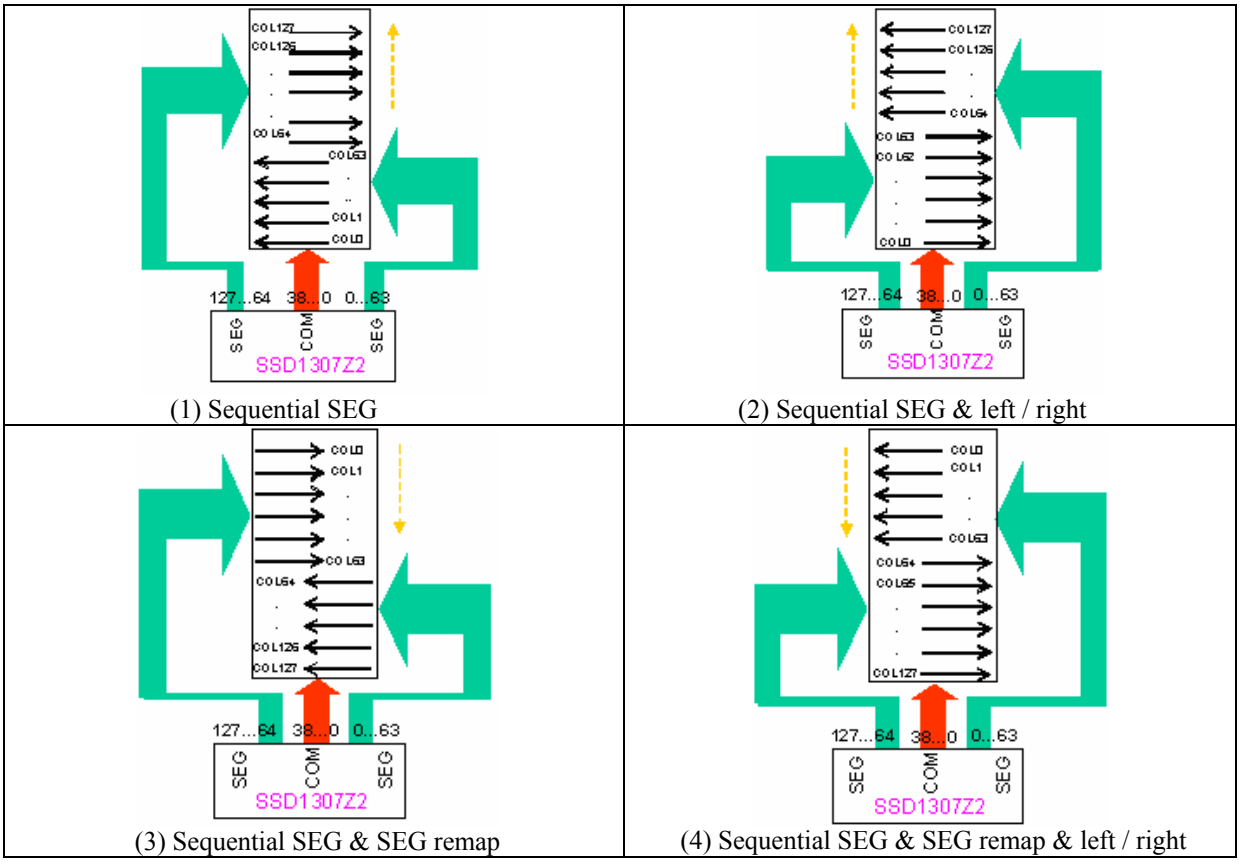
4. **Hardware Configuration (Panel resolution & layout related) Command Table**											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	40~66	0	1	X_5	X_4	X_3	X_2	X_1	X_0	Set Display Start Line	Set display RAM display offset from 0d-38d using $X_5X_4X_3X_2X_1X_0$. Display offset is reset to 000000b during RESET.
0	A0/A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map	A0h, X[0]=0b: column address 0 is mapped to SEG0 (RESET) A1h, X[0]=1b: column address 127 is mapped to SEG0
0 0	A8 A[5:0]	1 *	0 *	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[5:0] : from 16MUX to 39MUX, RESET= 100110b (i.e.38d , 39Mux) A[5:0] from 0 to 14 are invalid entry.
0	C0/C8	1	1	0	0	X_3	0	0	0	Set COM Output Scan Direction	C0h, X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N –1] C8h, X[3]=1b: remapped mode. Scan from COM[N-1] to COM0 Where N is the Multiplex ratio.
0 0	D3 A[5:0]	1 *	1 *	0 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Display Offset	Set vertical shift by COM from 0d~38d. The value is reset to 00h after RESET.

4. **Hardware Configuration (Panel resolution & layout related) Command Table**											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	DA	1	1	0	1	1	0	1	0	Set SEG Pins Hardware Configuration	A[4]=0b, Sequential SEG pin configuration A[4]=1b(RESET), Alternative (odd/even) SEG pin configuration A[5]=0b(RESET), Disable SEG Left/Right remap A[5]=1b, Enable SEG Left/Right remap
0	A[5:4]	0	0	A_5	A_4	0	0	1	0		

Table 8-2 : SEG Pins Hardware Configuration

SEG Odd / Even (Left / Right) and Top / Bottom connections are software selectable, thus there are total of 8 cases and they are shown on the followings,

Case no.	Oddeven (1) / Sequential (0) Command : DAh -> A[4]	SEG Remap Command : A0h / A1h	Left / Right Swap Command : DAh -> A[5]	Remark
1	0	0	0	
2	0	0	1	
3	0	1	0	
4	0	1	1	
5	1	0	0	Default
6	1	0	1	
7	1	1	0	
8	1	1	1	

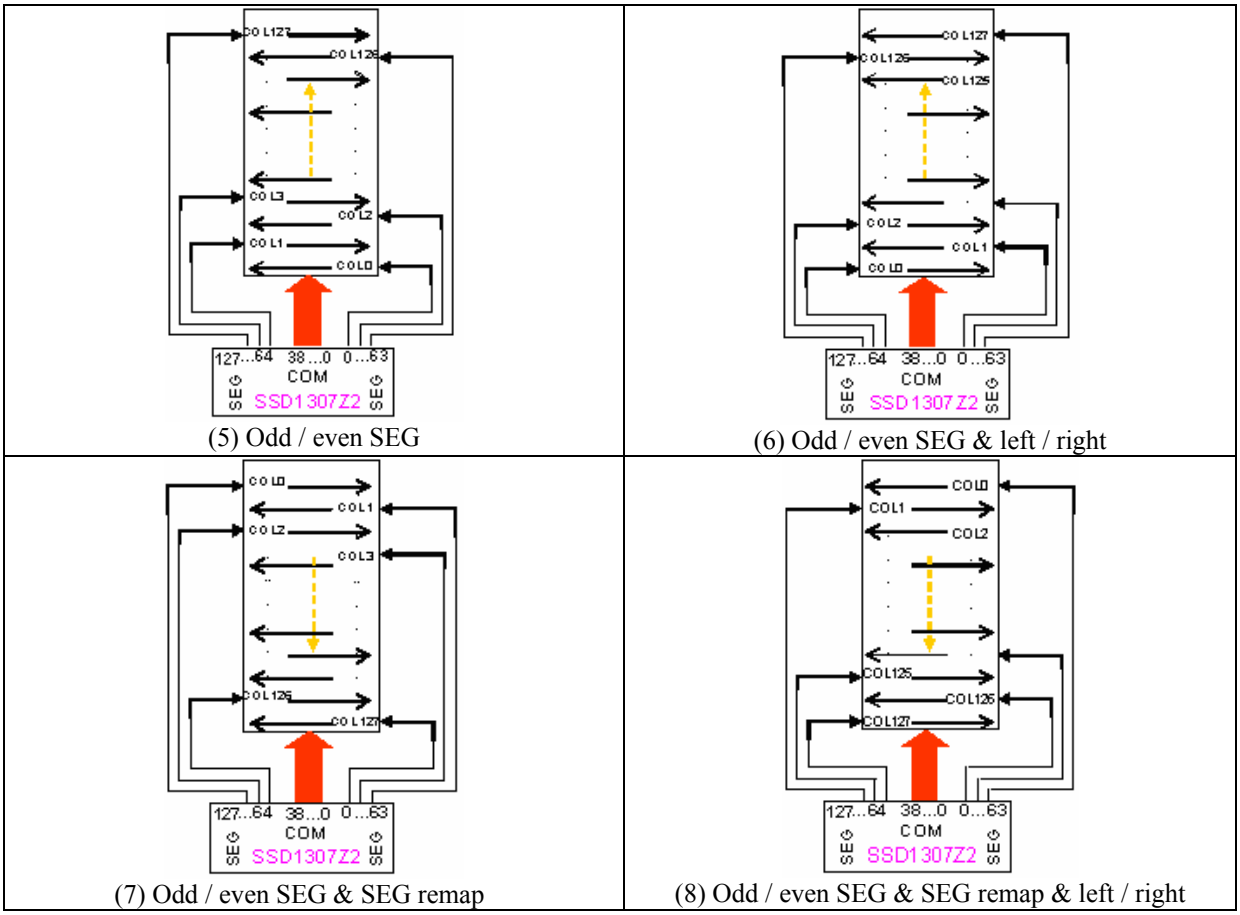


(1) Sequential SEG

(2) Sequential SEG & left / right

(3) Sequential SEG & SEG remap

(4) Sequential SEG & SEG remap & left / right



(5) Odd / even SEG

(6) Odd / even SEG & left / right

(7) Odd / even SEG & SEG remap

(8) Odd / even SEG & SEG remap & left / right

Note:

(1) The above eight figures are all with bump pads being faced up.

5. Timing & Driving scheme Setting Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	D5 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	0 A_3	1 A_2	0 A_1	1 A_0	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0] : Define the divide ratio (D) of the display clocks (DCLK): Divide ratio= A[3:0] + 1, RESET is 0001b (divide ratio = 2) A[7:4] : Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 1100b Range:0000b~1111b Frequency increases as setting value increases.
0 0	D9 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	1 A_3	0 A_2	0 A_1	1 A_0	Set Pre-charge Period	A[3:0] : Phase 1 period of up to 15 DCLK clocks. 0 is invalid entry (RESET=2h) A[7:4] : Phase 2 period of up to 15 DCLK clocks .0 is invalid entry (RESET=2h)
0 0	DB A[6:4]	1 0	1 A_6	0 A_5	1 A_4	1 0	0 0	1 0	1 0	Set V_{COMH} Deselect Level	A[6:4] / Hex code / V_{COMH} deselect level 000b / 00h / ~ 0.65 x V_{CC} 010b / 20h / ~ 0.77 x V_{CC} (RESET) 011b / 30h / ~ 0.83 x V_{CC}

6. Others											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation

Note

(1) "*" stands for "Don't care".

Table 8-3 : Read Command Table

Bit Pattern	Command	Description
$D_7D_6D_5D_4D_3D_2D_1D_0$	Status Register Read	D[7] : Reserved D[6] : "1" for display OFF / "0" for display ON D[5] : Reserved D[4] : Reserved D[3] : Reserved D[2] : Reserved D[1] : Reserved D[0] : Reserved

Note
(1) Patterns other than those given in the Command Table are prohibited to enter the chip as a command; as unexpected results can occur.

8.1 Data Read / Write

To read data from the GDDRAM, select HIGH for both the R/W# (WR#) pin and the D/C# pin for 6800-series parallel mode and select LOW for the E (RD#) pin and HIGH for the D/C# pin for 8080-series parallel mode. No data read is provided in serial mode operation.
In normal data read mode the GDDRAM column address pointer will be increased automatically by one after each data read.
Also, a dummy read is required before the first data read.
To write data to the GDDRAM, select LOW for the R/W# (WR#) pin and HIGH for the D/C# pin for both 6800-series parallel mode and 8080-series parallel mode. The serial interface mode is always in write mode. The GDDRAM column address pointer will be increased automatically by one after each data write.

Table 8-4 : Address increment table (Automatic)

D/C#	R/W# (WR#)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

9 COMMAND DESCRIPTIONS

9.1 Fundamental Command

9.1.1 Set Lower Column Start Address for Page Addressing Mode (00h~0Fh)

This command specifies the lower nibble of the 8-bit column start address for the display data RAM under Page Addressing Mode. The column address will be incremented by each data access. Please refer to Table 8-1 and Section 9.1.3 for details.

9.1.2 Set Higher Column Start Address for Page Addressing Mode (10h~17h)

This command specifies the higher nibble of the 8-bit column start address for the display data RAM under Page Addressing Mode. The column address will be incremented by each data access. Please refer to Table 8-1 and Section 9.1.3 for details.

9.1.3 Set Memory Addressing Mode (20h)

There are 3 different memory addressing mode in SSD1307: page addressing mode, horizontal addressing mode and vertical addressing mode. This command sets the way of memory addressing into one of the above three modes. In there, "COL" means the graphic display data RAM column.

Page addressing mode (A[1:0]=10xb)

In page addressing mode, after the display RAM is read / written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and page address pointer is not changed. Users have to set the new page and column addresses in order to access the next page RAM content. The sequence of movement of the PAGE and column address point for page addressing mode is shown in Figure 9-1.

Figure 9-1 : Address Pointer Movement of Page addressing mode

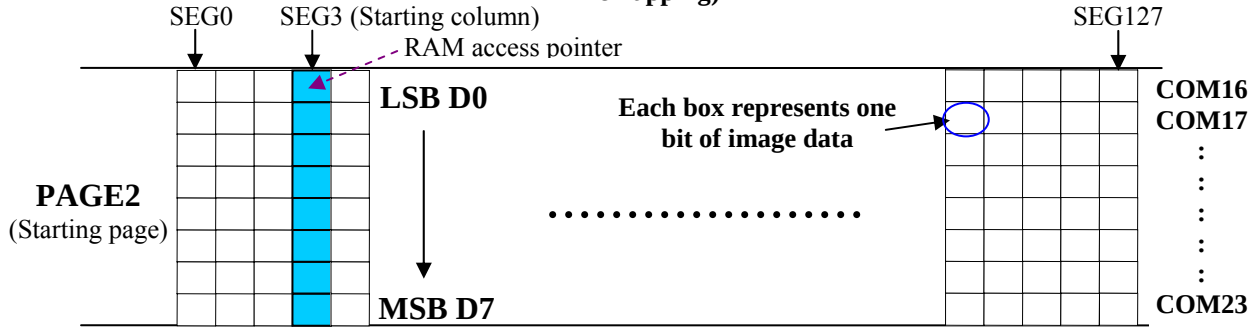
	COL0	COL 1	…..	COL 126	COL 127
PAGE0	→	→	→	→	→
PAGE1	→	→	→	→	→
PAGE2	→	→	→	→	→
PAGE3	→	→	→	→	→
PAGE4	→	→	→	→	→

In normal display data RAM read or write and page addressing mode, the following steps are required to define the starting RAM access pointer location:

- Set the page start address of the target display location by command B0h to B4h.
- Set the lower start column address of pointer by command 00h~0Fh.
- Set the upper start column address of pointer by command 10h~17h.

For example, if the page address is set to B2h, lower column address is 03h and upper column address is 10h, then that means the starting column is SEG3 of PAGE2. The RAM access pointer is located as shown in Figure 9-2. The input data byte will be written into RAM position of column 3.

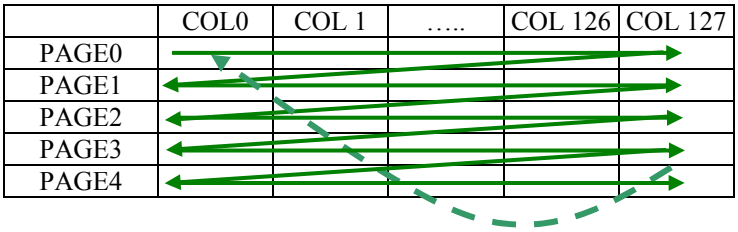
Figure 9-2 : Example of GDDRAM access pointer setting in Page Addressing Mode (No row and column-remapping)



Horizontal addressing mode (A[1:0]=00b)

In horizontal addressing mode, after the display RAM is read / written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and page address pointer is increased by 1. The sequence of movement of the page and column address point for horizontal addressing mode is shown in Figure 9-3. When both column and page address pointers reach the end address, the pointers are reset to column start address and page start address (Dotted line in Figure 9-3.)

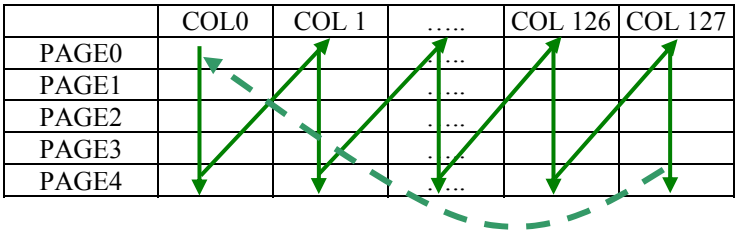
Figure 9-3 : Address Pointer Movement of Horizontal addressing mode



Vertical addressing mode: (A[1:0]=01b)

In vertical addressing mode, after the display RAM is read / written, the page address pointer is increased automatically by 1. If the page address pointer reaches the page end address, the page address pointer is reset to page start address and column address pointer is increased by 1. The sequence of movement of the page and column address point for vertical addressing mode is shown in Figure 9-4. When both column and page address pointers reach the end address, the pointers are reset to column start address and page start address (Dotted line in Figure 9-4.)

Figure 9-4 : Address Pointer Movement of Vertical addressing mode



In normal display data RAM read or write and horizontal / vertical addressing mode, the following steps are required to define the RAM access pointer location:

- Set the column start and end address of the target display location by command 21h.
- Set the page start and end address of the target display location by command 22h.

Example is shown in Figure 9-5.

9.1.4 Set Column Address (21h)

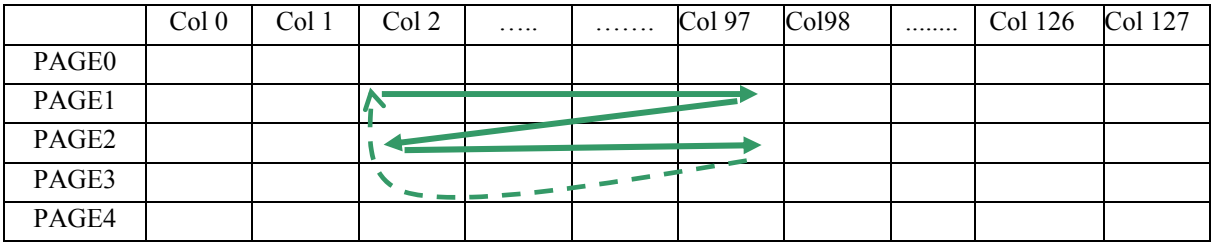
This triple byte command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command 20h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

9.1.5 Set Page Address (22h)

This triple byte command specifies page start address and end address of the display data RAM. This command also sets the page address pointer to page start address. This pointer is used to define the current read/write page address in graphic display data RAM. If vertical address increment mode is enabled by command 20h, after finishing read/write one page data, it is incremented automatically to the next page address. Whenever the page address pointer finishes accessing the end page address, it is reset back to start page address.

The figure below shows the way of column and page address pointer movement through the example: column start address is set to 2 and column end address is set to 97, page start address is set to 1 and page end address is set to 2; Horizontal address increment mode is enabled by command 20h. In this case, the graphic display data RAM column accessible range is from column 2 to column 97 and from page 1 to page 2 only. In addition, the column address pointer is set to 2 and page address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation (*solid line in Figure 9-5*). Whenever the column address pointer finishes accessing the end column 97, it is reset back to column 2 and page address is automatically increased by 1 (*solid line in Figure 9-5*). While the end page 2 and end column 97 RAM location is accessed, the page address is reset back to 1 and the column address is reset back to 2 (*dotted line in Figure 9-5*). .

Figure 9-5 : Example of Column and Row Address Pointer Movement



9.1.6 Set Display Start Line (40h~66h)

This command sets the Display Start Line register to determine starting address of display RAM, by selecting a value from 0 to 38. With value equal to 0, RAM row 0 is mapped to COM0. With value equal to 1, RAM row 1 is mapped to COM0 and so on.

Refer to Table 9-1 for more illustrations.

9.1.7 Set Contrast Control for BANK0 (81h)

This command sets the Contrast Setting of the display. The chip has 256 contrast steps from 00h to FFh. The segment output current increases as the contrast step value increases.

9.1.8 Set Segment Re-map (A0h/A1h)

This command changes the mapping between the display data column address and the segment driver. It allows flexibility in OLED module design. Please refer to Table 8-2.

This command only affects subsequent data input. Data already stored in GDDRAM will have no changes.

9.1.9 Entire Display ON (A4h/A5h)

A4h command enable display outputs according to the GDDRAM contents.
If A5h command is issued, then by using A4h command, the display will resume to the GDDRAM contents.
In other words, A4h command resumes the display from entire display "ON" stage.
A5h command forces the entire display to be "ON", regardless of the contents of the display data RAM.

9.1.10 Set Normal/Inverse Display (A6h/A7h)

This command sets the display to be either normal or inverse. In normal display a RAM data of 1 indicates an "ON" pixel while in inverse display a RAM data of 0 indicates an "ON" pixel.

9.1.11 Set Multiplex Ratio (A8h)

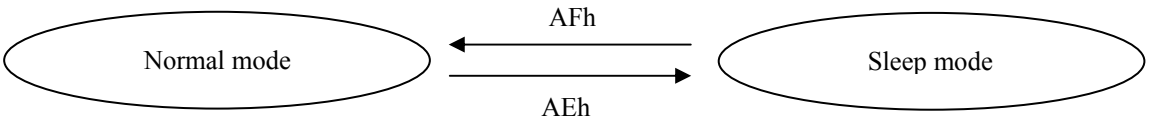
This command switches the default 39 multiplex mode to any multiplex ratio, ranging from 16 to 39. The output pads COM0~COM38 will be switched to the corresponding COM signal.

9.1.12 Set Display ON/OFF (AEh/AFh)

These single byte commands are used to turn the OLED panel display ON or OFF.
When the display is ON, the selected circuits by Set Master Configuration command will be turned ON.
When the display is OFF, those circuits will be turned OFF and the segment and common output are in V_{SS} state and high impedance state, respectively. These commands set the display to one of the two states:

- AEh : Display OFF
- AFh : Display ON

Figure 9-6 : Transition between different modes



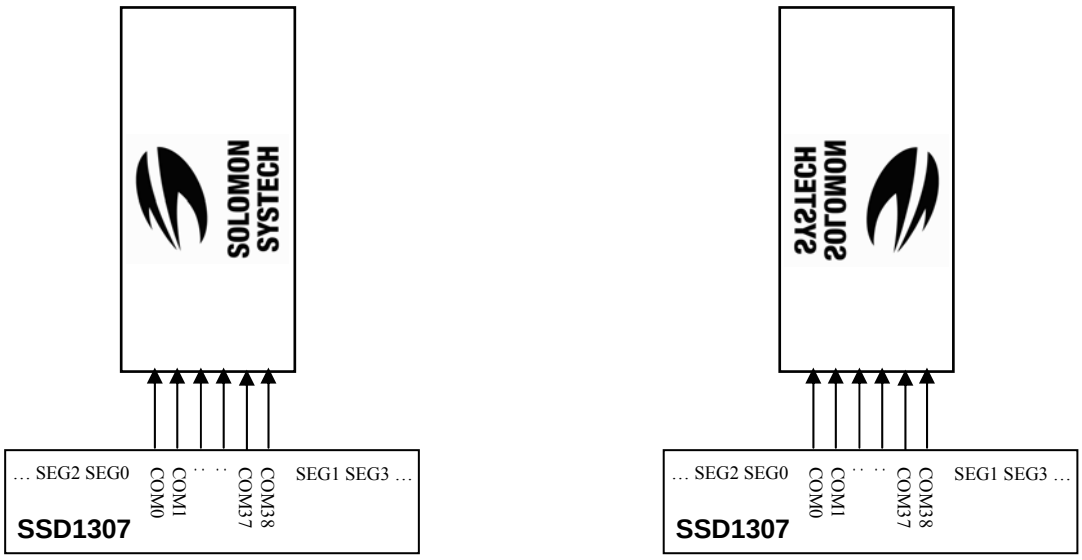
9.1.13 Set Page Start Address for Page Addressing Mode (B0h~B4h)

This command positions the page start address from 0 to 4 in GDDRAM under Page Addressing Mode.
Please refer to Table 8-1 and Section 9.1.3 for details.

9.1.14 Set COM Output Scan Direction (C0h/C8h)

This command sets the scan direction of the COM output, allowing layout flexibility in the OLED module design. Additionally, the display will show once this command is issued. For example, if this command is sent during normal display, then the graphic display will be vertically flipped immediately. Please refer to Figure 9-7 and Table 9-2 for details.

Figure 9-7 : Example of row address mapping



Row 0 maps to COM0 pin

Row 38 maps to COM0 pin

9.1.15 Set Display Offset (D3h)

This is a double byte command. The second command specifies the mapping of the display start line to one of COM0~COM38 (assuming that COM0 is the display start line then the display start line register is equal to 0).

For example, to move the COM4 towards the COM0 direction by 4 lines the 6-bit data in the second byte should be given as 000100b. To move in the opposite direction by 4 lines the 6-bit data should be given by 39 – 4, so the second byte would be 100011b. The following two tables (Table 9-1, Table 9-2) show the examples of setting the command C0h/C8h and D3h.

Table 9-1 : Example of Set Display Offset and Display Start Line without Remap

	Output												
	39		39		39		32		32		32		Set MUX ration (A8h)
	Normal		Normal		Normal		Normal		Normal		Normal		COM normal / remap (C0h / C8h)
Hardware	0		4		0		0		4		0		Display offset (D3h)
pin name	0		0		4		0		0		4		Display start line (40h - 66h)
COM0	ROW0	RAM0	ROW4	RAM4	ROW0	RAM4	ROW0	RAM0	ROW4	RAM4	ROW0	RAM4	
COM1	ROW1	RAM1	ROW5	RAM5	ROW1	RAM5	ROW1	RAM1	ROW5	RAM5	ROW1	RAM5	
COM2	ROW2	RAM2	ROW6	RAM6	ROW2	RAM6	ROW2	RAM2	ROW6	RAM6	ROW2	RAM6	
COM3	ROW3	RAM3	ROW7	RAM7	ROW3	RAM7	ROW3	RAM3	ROW7	RAM7	ROW3	RAM7	
COM4	ROW4	RAM4	ROW8	RAM8	ROW4	RAM8	ROW4	RAM4	ROW8	RAM8	ROW4	RAM8	
COM5	ROW5	RAM5	ROW9	RAM9	ROW5	RAM9	ROW5	RAM5	ROW9	RAM9	ROW5	RAM9	
COM6	ROW6	RAM6	ROW10	RAM10	ROW6	RAM10	ROW6	RAM6	ROW10	RAM10	ROW6	RAM10	
COM7	ROW7	RAM7	ROW11	RAM11	ROW7	RAM11	ROW7	RAM7	ROW11	RAM11	ROW7	RAM11	
COM8	ROW8	RAM8	ROW12	RAM12	ROW8	RAM12	ROW8	RAM8	ROW12	RAM12	ROW8	RAM12	
COM9	ROW9	RAM9	ROW13	RAM13	ROW9	RAM13	ROW9	RAM9	ROW13	RAM13	ROW9	RAM13	
COM10	ROW10	RAM10	ROW14	RAM14	ROW10	RAM14	ROW10	RAM10	ROW14	RAM14	ROW10	RAM14	
COM11	ROW11	RAM11	ROW15	RAM15	ROW11	RAM15	ROW11	RAM11	ROW15	RAM15	ROW11	RAM15	
COM12	ROW12	RAM12	ROW16	RAM16	ROW12	RAM16	ROW12	RAM12	ROW16	RAM16	ROW12	RAM16	
COM13	ROW13	RAM13	ROW17	RAM17	ROW13	RAM17	ROW13	RAM13	ROW17	RAM17	ROW13	RAM17	
COM14	ROW14	RAM14	ROW18	RAM18	ROW14	RAM18	ROW14	RAM14	ROW18	RAM18	ROW14	RAM18	
COM15	ROW15	RAM15	ROW19	RAM19	ROW15	RAM19	ROW15	RAM15	ROW19	RAM19	ROW15	RAM19	
COM16	ROW16	RAM16	ROW20	RAM20	ROW16	RAM20	ROW16	RAM16	ROW20	RAM20	ROW16	RAM20	
COM17	ROW17	RAM17	ROW21	RAM21	ROW17	RAM21	ROW17	RAM17	ROW21	RAM21	ROW17	RAM21	
COM18	ROW18	RAM18	ROW22	RAM22	ROW18	RAM22	ROW18	RAM18	ROW22	RAM22	ROW18	RAM22	
COM19	ROW19	RAM19	ROW23	RAM23	ROW19	RAM23	ROW19	RAM19	ROW23	RAM23	ROW19	RAM23	
COM20	ROW20	RAM20	ROW24	RAM24	ROW20	RAM24	ROW20	RAM20	ROW24	RAM24	ROW20	RAM24	
COM21	ROW21	RAM21	ROW25	RAM25	ROW21	RAM25	ROW21	RAM21	ROW25	RAM25	ROW21	RAM25	
COM22	ROW22	RAM22	ROW26	RAM26	ROW22	RAM26	ROW22	RAM22	ROW26	RAM26	ROW22	RAM26	
COM23	ROW23	RAM23	ROW27	RAM27	ROW23	RAM27	ROW23	RAM23	ROW27	RAM27	ROW23	RAM27	
COM24	ROW24	RAM24	ROW28	RAM28	ROW24	RAM28	ROW24	RAM24	ROW28	RAM28	ROW24	RAM28	
COM25	ROW25	RAM25	ROW29	RAM29	ROW25	RAM29	ROW25	RAM25	ROW29	RAM29	ROW25	RAM29	
COM26	ROW26	RAM26	ROW30	RAM30	ROW26	RAM30	ROW26	RAM26	ROW30	RAM30	ROW26	RAM30	
COM27	ROW27	RAM27	ROW31	RAM31	ROW27	RAM31	ROW27	RAM27	ROW31	RAM31	ROW27	RAM31	
COM28	ROW28	RAM28	ROW32	RAM32	ROW28	RAM32	ROW28	RAM28	-	-	ROW28	RAM32	
COM29	ROW29	RAM29	ROW33	RAM33	ROW29	RAM33	ROW29	RAM29	-	-	ROW29	RAM33	
COM30	ROW30	RAM30	ROW34	RAM34	ROW30	RAM34	ROW30	RAM30	-	-	ROW30	RAM34	
COM31	ROW31	RAM31	ROW35	RAM35	ROW31	RAM35	ROW31	RAM31	-	-	ROW31	RAM35	
COM32	ROW32	RAM32	ROW36	RAM36	ROW32	RAM36	-	-	-	-	-	-	
COM33	ROW33	RAM33	ROW37	RAM37	ROW33	RAM37	-	-	-	-	-	-	
COM34	ROW34	RAM34	ROW38	RAM38	ROW34	RAM38	-	-	-	-	-	-	
COM35	ROW35	RAM35	ROW0	RAM0	ROW35	RAM0	-	-	ROW0	RAM0	-	-	
COM36	ROW36	RAM36	ROW1	RAM1	ROW36	RAM1	-	-	ROW1	RAM1	-	-	
COM37	ROW37	RAM37	ROW2	RAM2	ROW37	RAM2	-	-	ROW2	RAM2	-	-	
COM38	ROW38	RAM38	ROW3	RAM3	ROW38	RAM3	-	-	ROW3	RAM3	-	-	
Display examples	(a)		(b)		(c)		(d)		(e)		(f)		

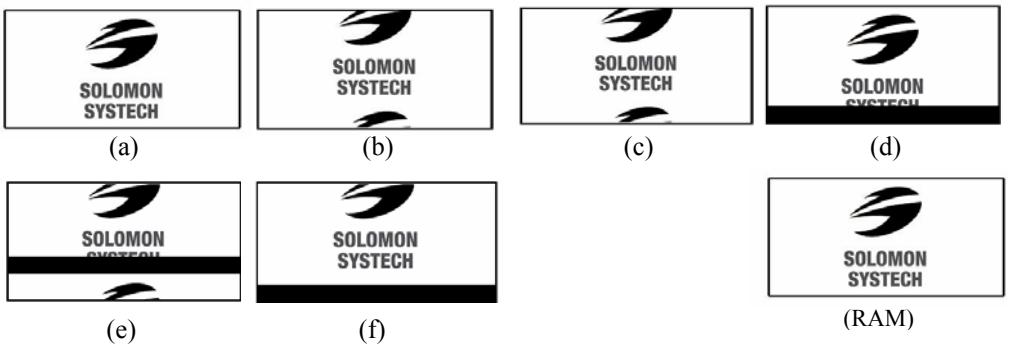
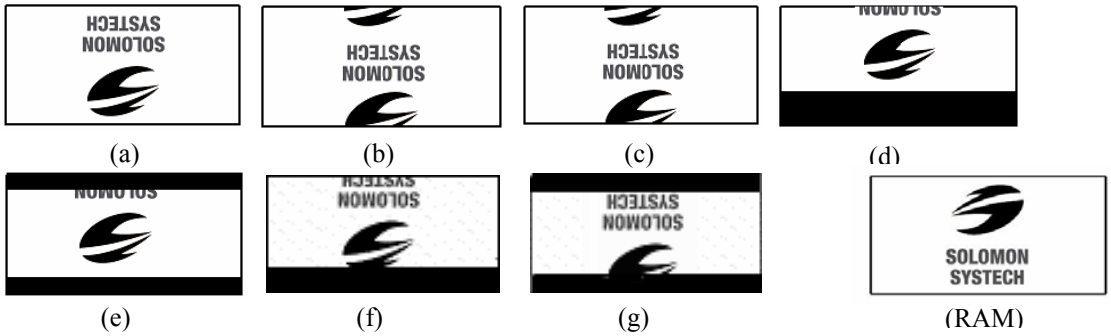


Table 9-2 : Example of Set Display Offset and Display Start Line with Remap

	Output														
	39		39		39		32		32		32		32		Set MUX ration (A8h)
	Remap		Remap		Remap		Remap		Remap		Remap		Remap		COM normal / remap (C0h / C8h)
Hardware	0		4		0		0		4		0		4		Display offset (D3h)
pin name	0		0		4		0		0		4		8		Display start line (40h - 66h)
COM0	ROW38	RAM 38	ROW3	RAM3	ROW38	RAM3	ROW31	RAM31	-	-	ROW31	RAM35	-	-	
COM1	ROW37	RAM37	ROW2	RAM2	ROW37	RAM2	ROW30	RAM30	-	-	ROW30	RAM34	-	-	
COM2	ROW36	RAM36	ROW1	RAM1	ROW36	RAM1	ROW29	RAM29	-	-	ROW29	RAM33	-	-	
COM3	ROW35	RAM35	ROW0	RAM0	ROW35	RAM0	ROW28	RAM28	-	-	ROW28	RAM32	-	-	
COM4	ROW34	RAM34	ROW38	RAM38	ROW34	RAM38	ROW27	RAM27	ROW31	RAM31	ROW27	RAM31	ROW31	RAM0	
COM5	ROW33	RAM33	RAM37	RAM37	ROW33	RAM37	ROW26	RAM26	ROW30	RAM30	ROW26	RAM30	ROW30	RAM38	
COM6	ROW32	RAM32	RAM36	RAM36	ROW32	RAM36	ROW25	RAM25	ROW29	RAM29	ROW25	RAM29	ROW29	RAM37	
COM7	ROW31	RAM31	RAM35	RAM35	ROW31	RAM35	ROW24	RAM24	ROW28	RAM28	ROW24	RAM28	ROW28	RAM36	
COM8	ROW30	RAM30	RAM34	RAM34	ROW30	RAM34	ROW23	RAM23	ROW27	RAM27	ROW23	RAM27	ROW27	RAM35	
COM9	ROW29	RAM29	RAM33	RAM33	ROW29	RAM33	ROW22	RAM22	ROW26	RAM26	ROW22	RAM26	ROW26	RAM34	
COM10	ROW28	RAM28	RAM32	RAM32	ROW28	RAM32	ROW21	RAM21	ROW25	RAM25	ROW21	RAM25	ROW25	RAM33	
COM11	ROW27	RAM27	RAM31	RAM31	ROW27	RAM31	ROW20	RAM20	ROW24	RAM24	ROW20	RAM24	ROW24	RAM32	
COM12	ROW26	RAM26	RAM30	RAM30	ROW26	RAM30	ROW19	RAM19	ROW23	RAM23	ROW19	RAM23	ROW23	RAM31	
COM13	ROW25	RAM25	RAM29	RAM29	ROW25	RAM29	ROW18	RAM18	ROW22	RAM22	ROW18	RAM22	ROW22	RAM30	
COM14	ROW24	RAM24	RAM28	RAM28	ROW24	RAM28	ROW17	RAM17	ROW21	RAM21	ROW17	RAM21	ROW21	RAM29	
COM15	ROW23	RAM23	RAM27	RAM27	ROW23	RAM27	ROW16	RAM16	ROW20	RAM20	ROW16	RAM20	ROW20	RAM28	
COM16	ROW22	RAM22	RAM26	RAM26	ROW22	RAM26	ROW15	RAM15	ROW19	RAM19	ROW15	RAM19	ROW19	RAM27	
COM17	ROW21	RAM21	RAM25	RAM25	ROW21	RAM25	ROW14	RAM14	ROW18	RAM18	ROW14	RAM18	ROW18	RAM26	
COM18	ROW20	RAM20	RAM24	RAM24	ROW20	RAM24	ROW13	RAM13	ROW17	RAM17	ROW13	RAM17	ROW17	RAM25	
COM19	ROW19	RAM19	RAM23	RAM23	ROW19	RAM23	ROW12	RAM12	ROW16	RAM16	ROW12	RAM16	ROW16	RAM24	
COM20	ROW18	RAM18	RAM22	RAM22	ROW18	RAM22	ROW11	RAM11	ROW15	RAM15	ROW11	RAM15	ROW15	RAM23	
COM21	ROW17	RAM17	RAM21	RAM21	ROW17	RAM21	ROW10	RAM10	ROW14	RAM14	ROW10	RAM14	ROW14	RAM22	
COM22	ROW16	RAM16	RAM20	RAM20	ROW16	RAM20	ROW9	RAM9	ROW13	RAM13	ROW9	RAM13	ROW13	RAM21	
COM23	ROW15	RAM15	RAM19	RAM19	ROW15	RAM19	ROW8	RAM8	ROW12	RAM12	ROW8	RAM12	ROW12	RAM20	
COM24	ROW14	RAM14	RAM18	RAM18	ROW14	RAM18	ROW7	RAM7	ROW11	RAM11	ROW7	RAM11	ROW11	RAM19	
COM25	ROW13	RAM13	RAM17	RAM17	ROW13	RAM17	ROW6	RAM6	ROW10	RAM10	ROW6	RAM10	ROW10	RAM18	
COM26	ROW12	RAM12	RAM16	RAM16	ROW12	RAM16	ROW5	RAM5	ROW9	RAM9	ROW5	RAM9	ROW9	RAM17	
COM27	ROW11	RAM11	RAM15	RAM15	ROW11	RAM15	ROW4	RAM4	ROW8	RAM8	ROW4	RAM8	ROW8	RAM16	
COM28	ROW10	RAM10	RAM14	RAM14	ROW10	RAM14	ROW3	RAM3	ROW7	RAM7	ROW3	RAM7	ROW7	RAM15	
COM29	ROW9	RAM9	RAM13	RAM13	ROW9	RAM13	ROW2	RAM2	ROW6	RAM6	ROW2	RAM6	ROW6	RAM14	
COM30	ROW8	RAM8	RAM12	RAM12	ROW8	RAM12	ROW1	RAM1	ROW5	RAM5	ROW1	RAM5	ROW5	RAM13	
COM31	ROW7	RAM7	RAM11	RAM11	ROW7	RAM11	ROW0	RAM0	ROW4	RAM4	ROW0	RAM4	ROW4	RAM12	
COM32	ROW6	RAM6	RAM10	RAM10	ROW6	RAM10	-	-	ROW3	RAM3	-	-	ROW3	RAM11	
COM33	ROW5	RAM5	RAM9	RAM9	ROW5	RAM9	-	-	ROW2	RAM2	-	-	ROW2	RAM10	
COM34	ROW4	RAM4	RAM8	RAM8	ROW4	RAM8	-	-	ROW1	RAM1	-	-	ROW1	RAM9	
COM35	ROW3	RAM3	RAM7	RAM7	ROW3	RAM7	-	-	ROW0	RAM0	-	-	ROW0	RAM8	
COM36	ROW2	RAM2	RAM6	RAM6	ROW2	RAM6	-	-	-	-	-	-	-	-	
COM37	ROW1	RAM1	RAM5	RAM5	ROW1	RAM5	-	-	-	-	-	-	-	-	
COM38	ROW0	RAM0	ROW4	RAM4	ROW0	RAM4	-	-	-	-	-	-	-	-	
Display examples	(a)		(b)		(c)		(d)		(e)		(f)		(g)		



9.1.16 Set Display Clock Divide Ratio/ Oscillator Frequency (D5h)

This command consists of two functions:

- Display Clock Divide Ratio (D) (A[3:0])
  Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 16, with reset value = 0001b. Please refer to section 7.3 for the details relationship of DCLK and CLK.

- Oscillator Frequency (A[7:4])
  Program the oscillator frequency Fosc that is the source of CLK if CLS pin is pulled high. The 4-bit value results in 16 different frequency settings available as shown below. The default setting is 1100b.

9.1.17 Set Pre-charge Period (D9h)

This command is used to set the duration of the pre-charge period. The interval is counted in number of DCLK, where RESET equals to 2 DCLKs.

9.1.18 Set COM Pins Hardware Configuration (DAh)

This command sets the COM signals pin configuration to match the OLED panel hardware layout. Table 8-2 shows the COM pin configuration under different conditions (for MUX ratio = 39).

9.1.19 Set V_{COMH} Deselect Level (DBh)

This command adjusts the VCOMH regulator output.

9.1.20 NOP (E3h)

No Operation Command

9.2 Graphic Acceleration Command

9.2.1 Horizontal Scroll Setup (26h/27h)

This command consists of consecutive bytes to set up the horizontal scroll parameters and determines the scrolling start page, end page and scrolling speed.

Before issuing this command the horizontal scroll must be deactivated (2Eh). Otherwise, RAM content may be corrupted.

The SSD1307 horizontal scroll is designed for 128 columns scrolling. The following two figures (Figure 9-8, Figure 9-9, and Figure 9-10) show the examples of using the horizontal scroll:

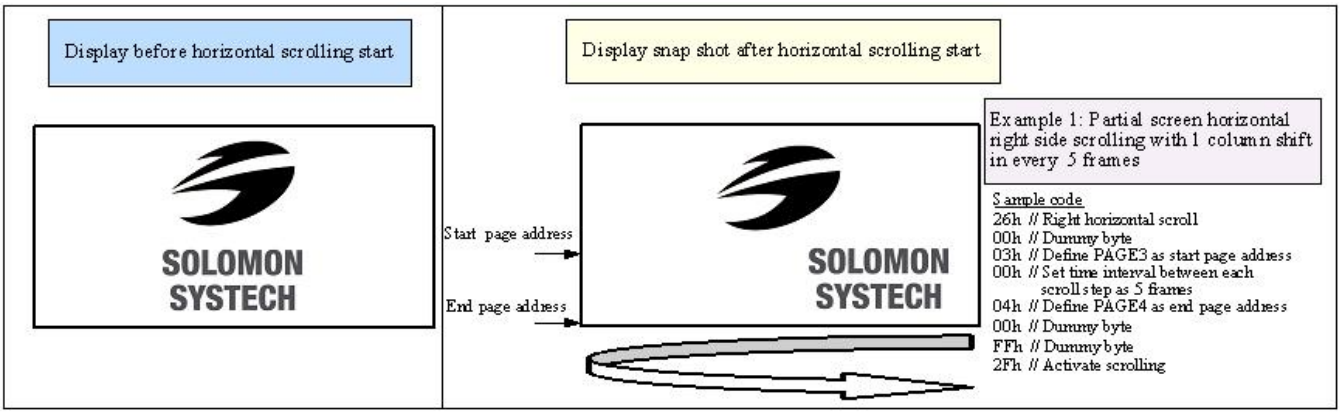
Figure 9-8 : Horizontal scroll example: Scroll RIGHT by 1 column

Original Setting	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	…	…	…	SEG122	SEG123	SEG124	SEG125	SEG126	SEG127
After one scroll step	SEG127	SEG0	SEG1	SEG2	SEG3	SEG4	…	…	…	SEG121	SEG122	SEG123	SEG124	SEG125	SEG126

Figure 9-9 : Horizontal scroll example: Scroll LEFT by 1 column

Original Setting	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	…	…	…	SEG122	SEG123	SEG124	SEG125	SEG126	SEG127
After one scroll step	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	…	…	…	SEG123	SEG124	SEG125	SEG126	SEG127	SEG0

Figure 9-10 : Horizontal scrolling setup example



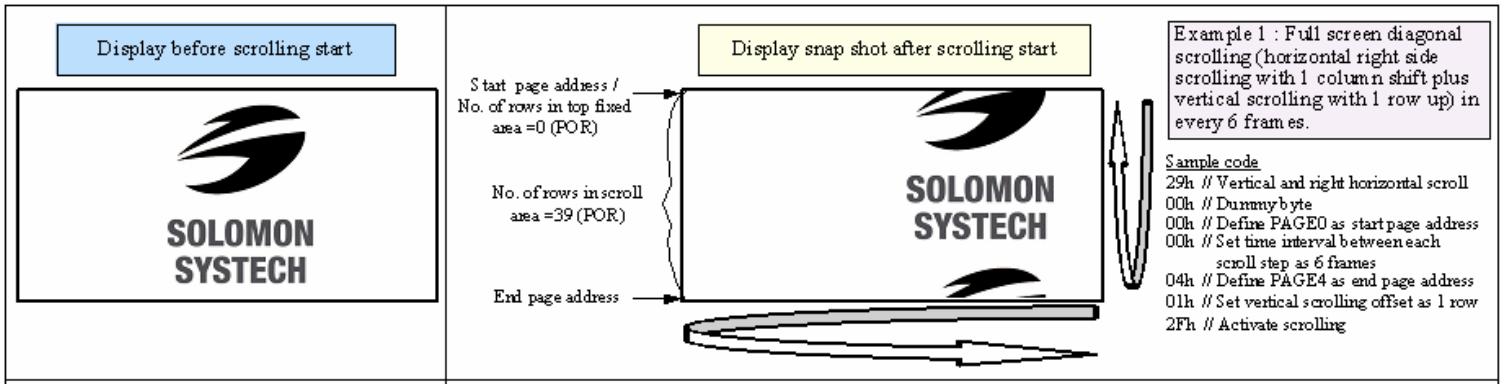
9.2.2 Continuous Vertical and Horizontal Scroll Setup (29h/2Ah)

This command consists of 6 consecutive bytes to set up the continuous vertical scroll parameters and determines the scrolling start page, end page, scrolling speed and vertical scrolling offset.

The bytes B[2:0], C[2:0] and D[2:0] of command 29h/2Ah are for the setting of the continuous horizontal scrolling. The byte E[5:0] is for the setting of the continuous vertical scrolling offset. All these bytes together are for the setting of continuous diagonal (horizontal + vertical) scrolling. If the vertical scrolling offset byte E[5:0] is set to zero, then only horizontal scrolling is performed (like command 26/27h).

Before issuing this command the scroll must be deactivated (2Eh). Otherwise, RAM content may be corrupted. The following figure (Figure 9-11) show the example of using the continuous vertical and horizontal scroll:

Figure 9-11 : Continuous Vertical and Horizontal scrolling setup example



9.2.3 Deactivate Scroll (2Eh)

This command stops the motion of scrolling. After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.

9.2.4 Activate Scroll (2Fh)

This command starts the motion of scrolling and should only be issued after the scroll setup parameters have been defined by the scrolling setup commands: 26h / 27h / 29h / 2Ah. The setting in the latest scrolling setup command overwrites the setting in the previous scrolling setup command.

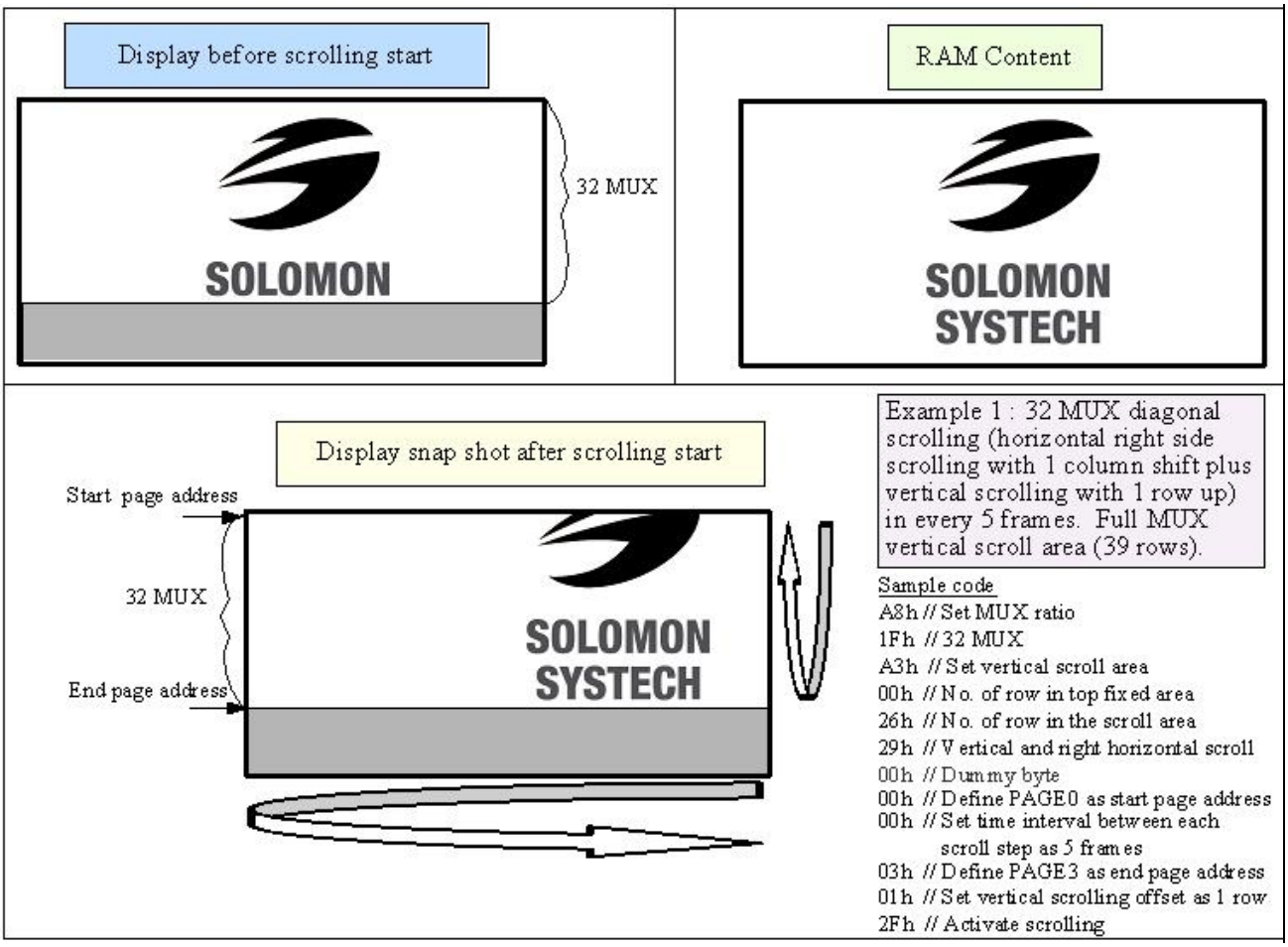
The following actions are prohibited after the scrolling is activated

1. RAM access (Data write or read)
2. Changing the horizontal scroll setup parameters

9.2.5 Set Vertical Scroll Area (A3h)

This command consists of 3 consecutive bytes to set up the vertical scroll area. For the continuous vertical scroll function (command 29h / 2Ah), the number of rows in the vertical scroll area can be set smaller than or equating to the MUX ratio. Figure 9-12 shows some vertical scrolling example with different settings in vertical scroll area.

Figure 9-12 : Vertical scroll area setup examples



10 MAXIMUM RATINGS

Table 10-1 : Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4	V
V_{CC}		0 to 16	V
V_{SEG}	SEG output voltage	0 to V_{CC}	V
V_{COM}	COM output voltage	0 to 0.9*V_{CC}	V
V_{in}	Input voltage	V_{SS}-0.3 to V_{DD}+0.3	V
T_A	Operating Temperature	-40 to +85	ºC
T_{stg}	Storage Temperature Range	-65 to +150	ºC

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

11 DC CHARACTERISTICS

Condition (Unless otherwise specified):

Voltage referenced to V_{SS}, V_{DD} =1.65 V to 3.3V, T_A = 25°C

Table 11-1 : DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CC}	Operating Voltage	-	7	-	15	V
V_{DD}	Logic Supply Voltage	-	1.65	-	3.3	V
V_{OH}	High Logic Output Level	I_{OUT} = 100uA, 3.3MHz	0.9 x V_{DD}	-	-	V
V_{OL}	Low Logic Output Level	I_{OUT} = 100uA, 3.3MHz	-	-	0.1 x V_{DD}	V
V_{IH}	High Logic Input Level	-	0.8 x V_{DD}	-	-	V
V_{IL}	Low Logic Input Level	-	-	-	0.2 x V_{DD}	V
$I_{DD,SLEEP}$	Sleep mode Current	V_{DD} = 1.65V~3.3V, V_{CC} = 7V~15V Display OFF, No panel attached	-	-	10	uA
$I_{CC,SLEEP}$	Sleep mode Current	V_{DD} = 1.65V~3.3V, V_{CC} = 7V~15V Display OFF, No panel attached	-	-	10	uA
I_{CC}	V_{CC} Supply Current V_{DD} = 2.8V, V_{CC} =12, I_{REF} =10uA, No loading, Display ON, All ON	Contrast = FFh	-	455	590	uA
I_{DD}	V_{DD} Supply Current V_{DD} =2.8V, V_{CC} = 12, I_{REF} = 10uA , No loading, Display ON, All ON,		-	23	30	uA
I_{SEG}	Segment Output Current, V_{DD} = 2.8V, V_{CC}=12V, I_{REF}=10uA, Display ON.	Contrast=FFh	285	316	345	uA
		Contrast=AFh	-	217	-	
		Contrast=7Fh	-	158	-	
		Contrast=3Fh	-	78	-	
		Contrast=0Fh	-	19	-	
Dev	Segment output current uniformity	Dev = (I_{SEG} – I_{MID})/I_{MID} I_{MID} = (I_{MAX} + I_{MIN})/2 I_{SEG}[0:127] = Segment current at contrast setting range = 3Fh to FFh	-3	-	3	%
Adj. Dev	Adjacent pin output current uniformity (contrast setting range = 3Fh to FFh)	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])	-2	-	2	%

12 AC CHARACTERISTICS

Conditions:

Voltage referenced to V_{SS}
V_{DD}=1.65 to3.3V
T_A = 25°C

Table 12-1 : AC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC} (1)	Oscillation Frequency of Display Timing Generator	V_{DD} = 2.8V	378	420	462	kHz
F_{FRM}	Frame Frequency for 39 MUX Mode	128x39 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F_{OSC} x 1/(DxKx39) (2)	-	Hz
RES#	Reset low pulse width		3	-	-	us

Note

(1) F_{OSC} stands for the frequency value of the internal oscillator and the value is measured when command D5h A[7:4] is in default value.

(2) D: divide ratio (default value = 2)
K: number of display clocks per row period (default value = 54)
Please refer to Table 8-1 (Set Display Clock Divide Ratio/Oscillator Frequency, D5h) for detailed description

Table 12-2 : 6800-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V to 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Figure 12-1 : 6800-series MCU parallel interface characteristics

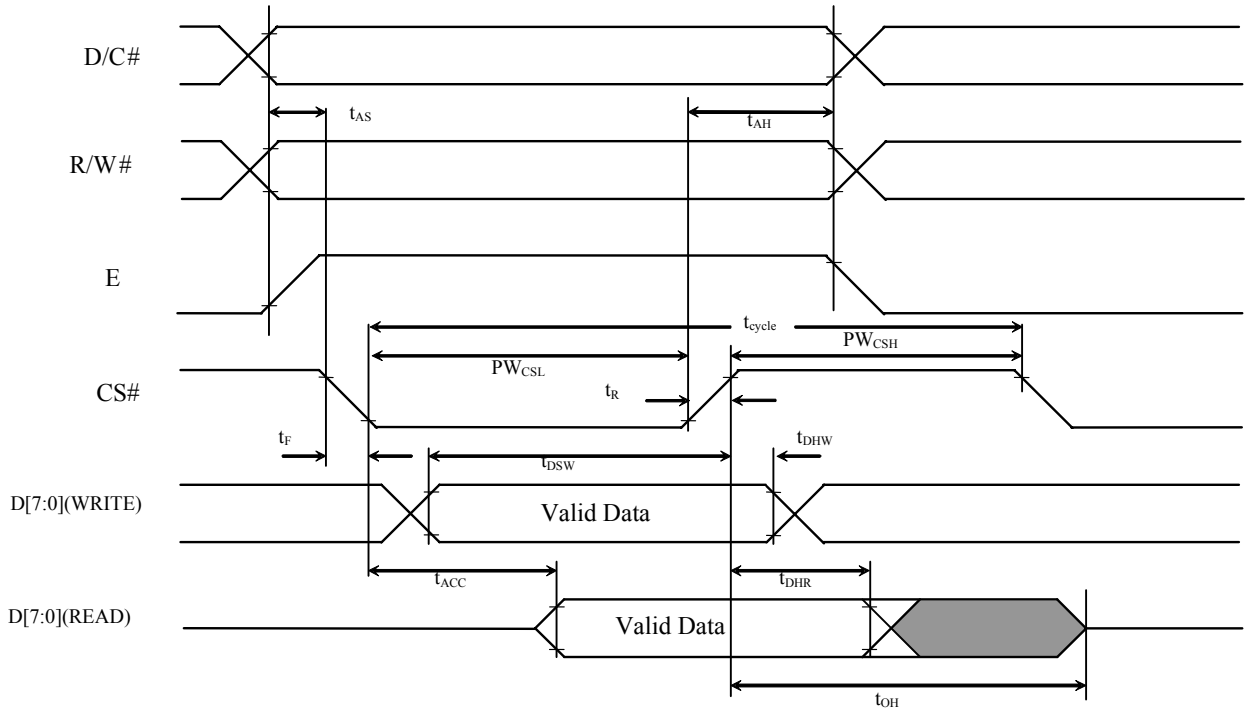


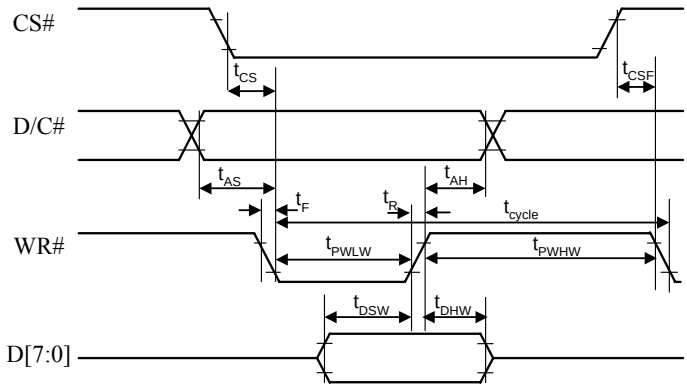
Table 12-3 : 8080-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V ~3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure 12-2 : 8080-series parallel interface characteristics

Write cycle



Read Cycle

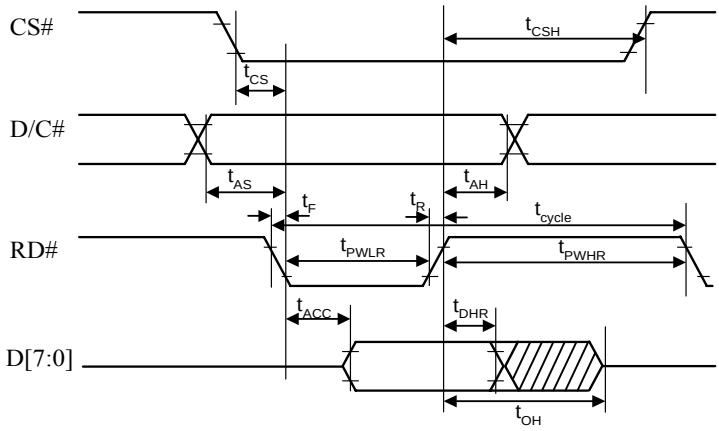


Table 12-4 : Serial Interface Timing Characteristics (4-wire SPI)

(V_{DD} - V_{SS} = 1.65V~3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Figure 12-3 : Serial interface characteristics (4-wire SPI)

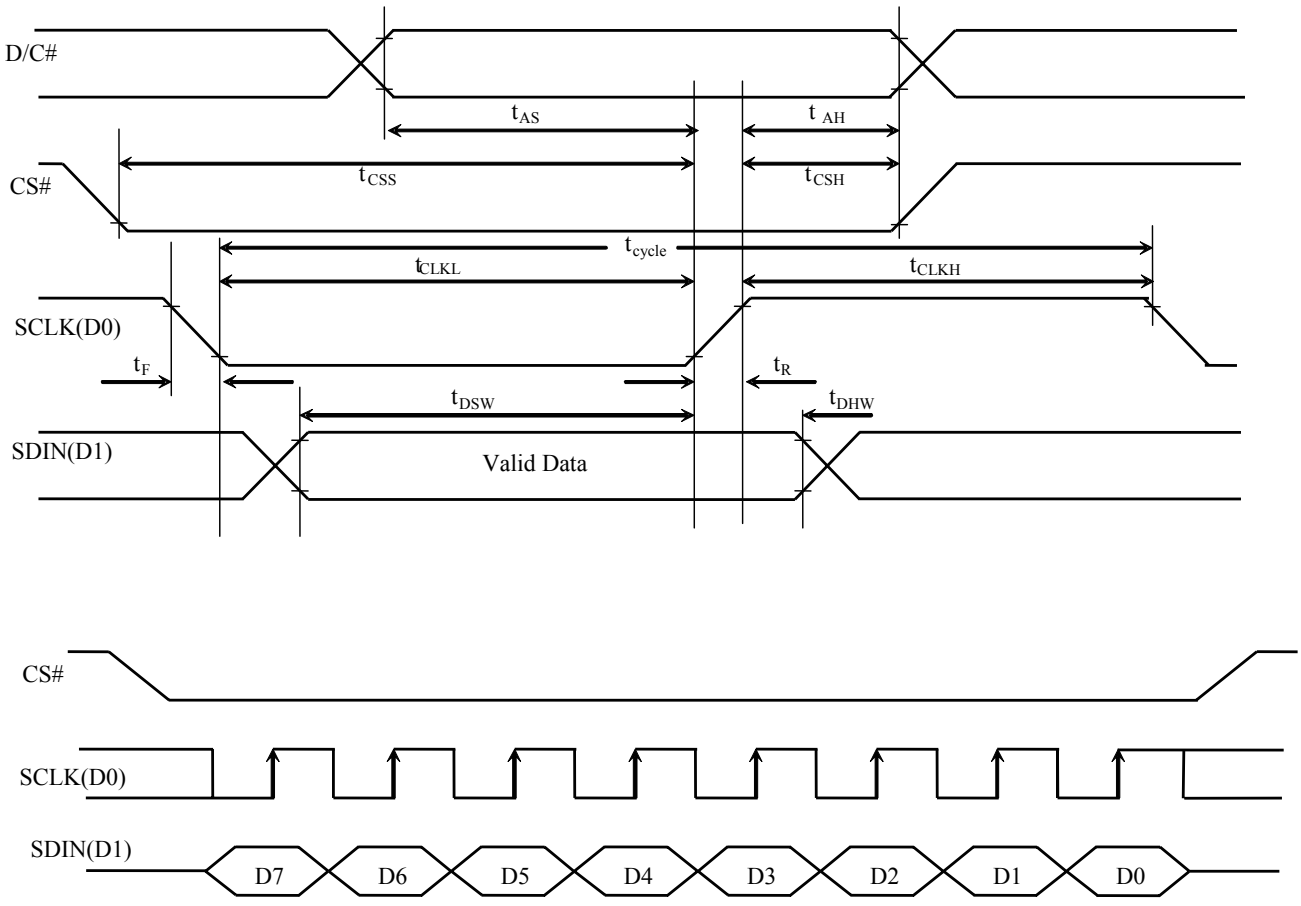
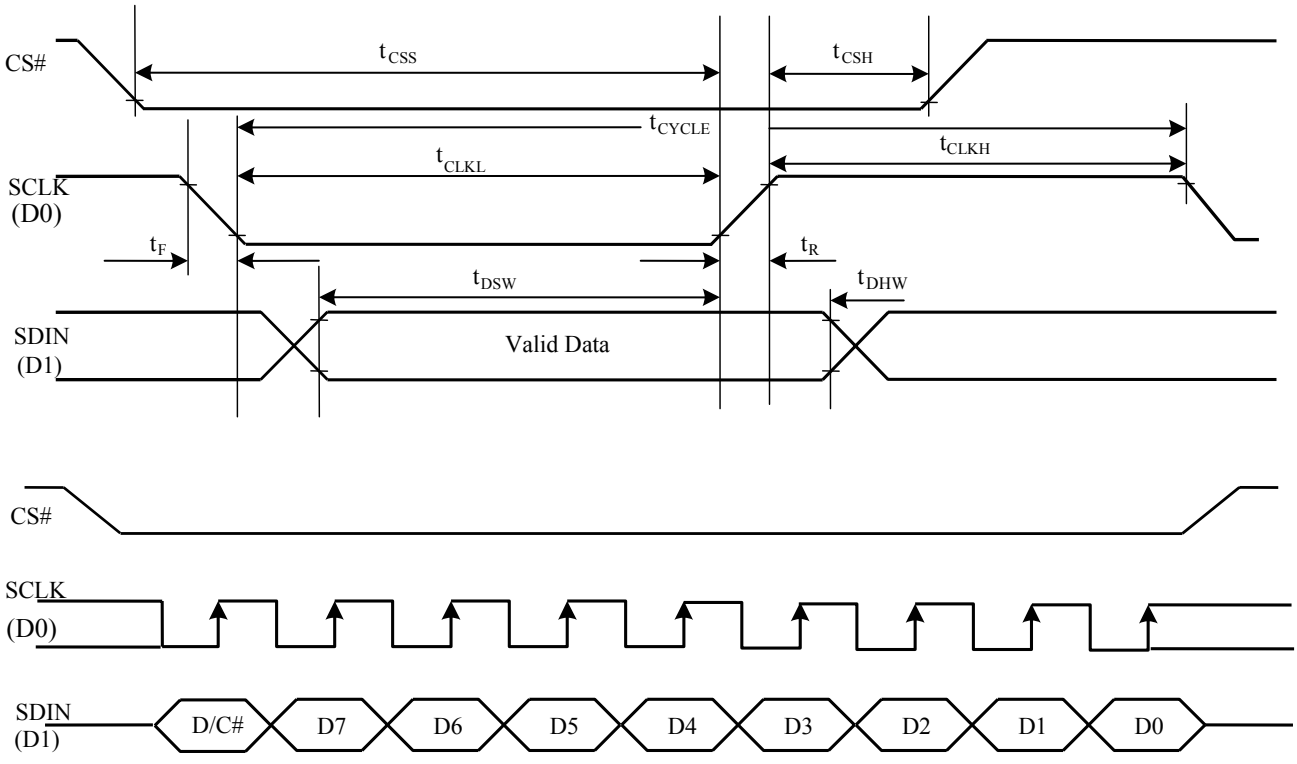


Table 12-5 : Serial Interface Timing Characteristics (3-wire SPI)

(V_{DD} - V_{SS} = 1.65V~3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Figure 12-4 : Serial interface characteristics (3-wire SPI)



Conditions:

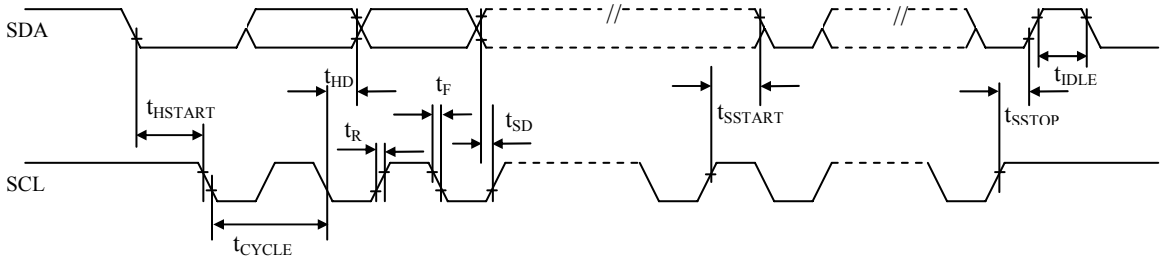
V_{DD} - V_{SS} = 1.65V ~ 3.3V

T_A = 25°C

Table 12-6 : I²C Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

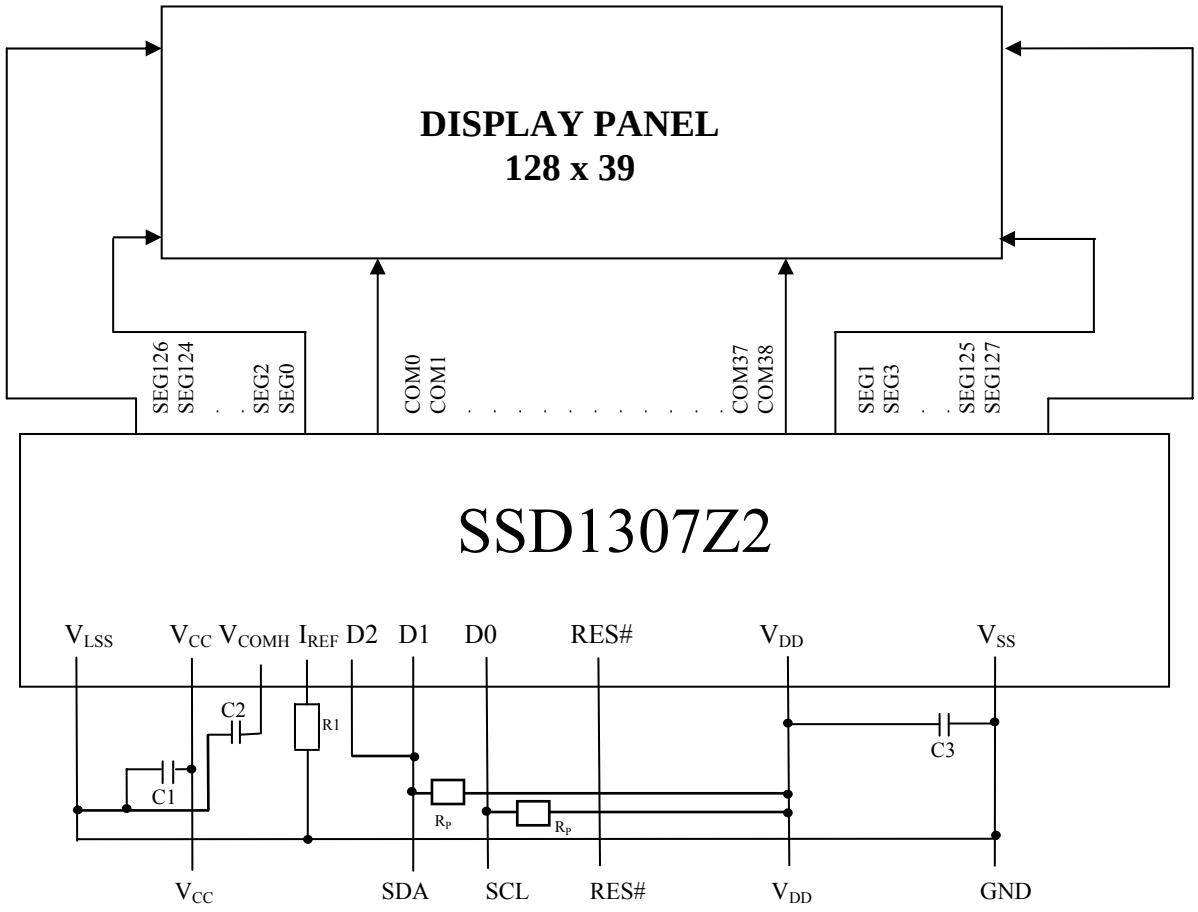
Figure 12-5 : I²C interface Timing characteristics



13 Application Example

Figure 13-1 : Application Example of SSD1307Z2

The configuration for I^2C interface mode is shown in the following diagram:
(V_{DD}=2.8V, V_{CC} =12V, I_{REF}=10uA)



Pin connected to MCU interface: D[2:0], RES#
Pin internally connected to V_{SS}: D[7:3], BS0, BS2, E, R/W#, CS#, CL, TRB[1:0]
Pin internally connected to V_{DD}: BS1, CLS
TRA[3:0], FR should be left open.
D/C# acts as SA0 for slave address selection [3]

C1, C2: 2.2uF [1]
C3: 1.0uF [1] place close to IC VDD and VSS pins on PCB
R_P : Pull up resistor

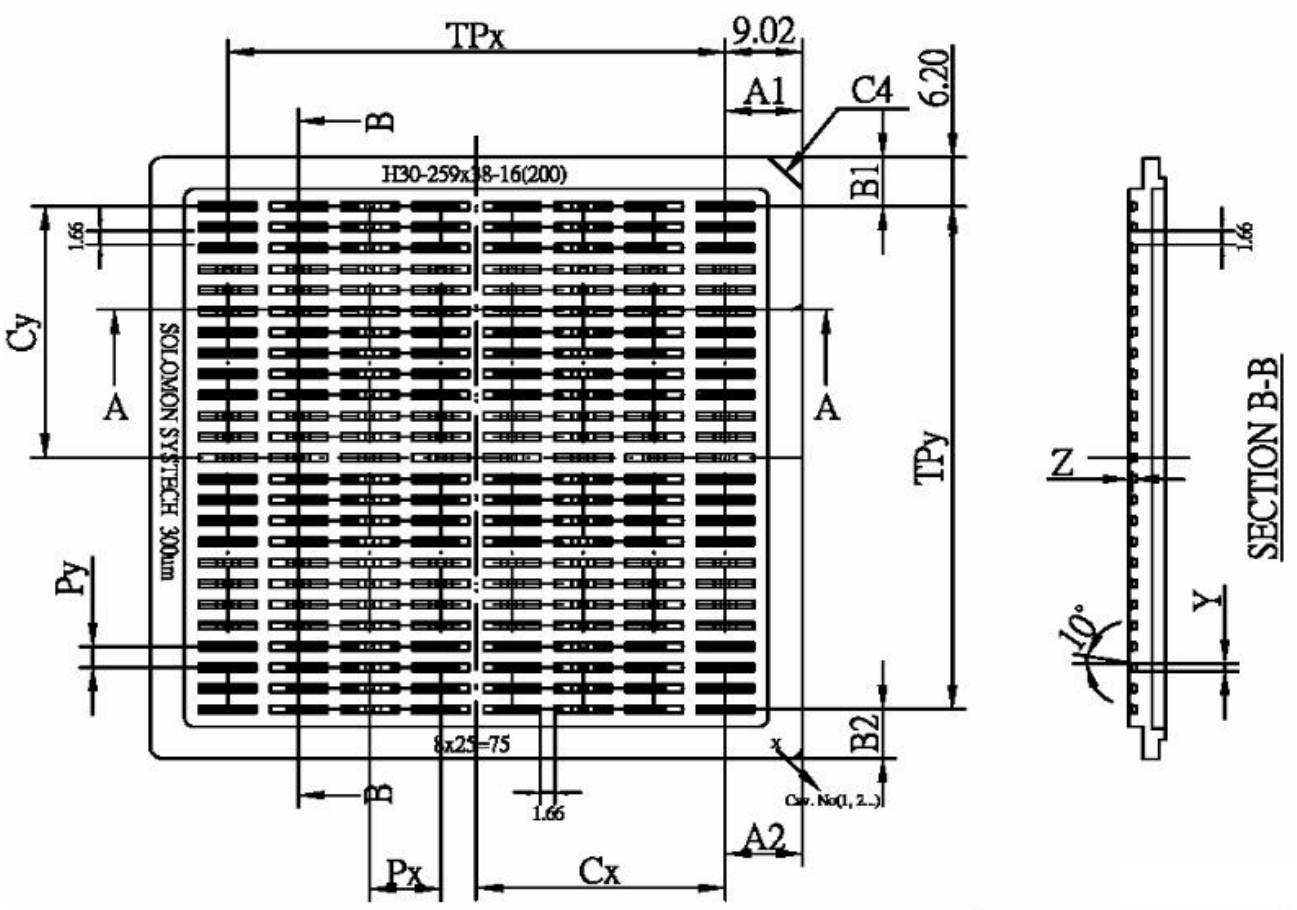
Voltage at I_{REF} = V_{CC} – 3V. For V_{CC} = 12V, I_{REF} = 10uA:
R1 = (Voltage at I_{REF} - V_{SS}) / I_{REF}
≈ (12-3)V / 10uA
= 900KΩ

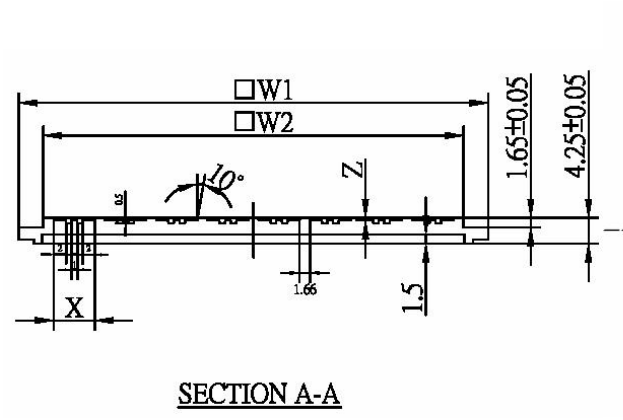
Note
[1] The capacitor value is recommended value. Select appropriate value against module application.
[2] Die gold bump face down.
[3] Refer to Section 7.1.5 for details.
[4] It is recommended to tie V_{LSS} and V_{SS} at one common ground point to minimize circulating ground noise.

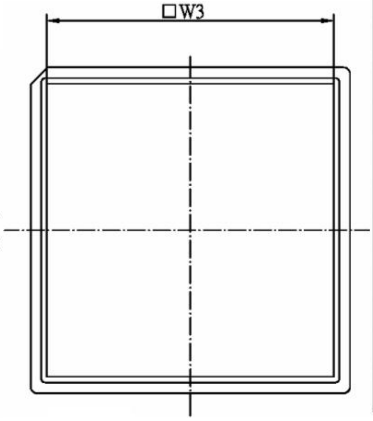
14 PACKAGE INFORMATION

14.1 SSD1307Z2 Die Tray Information

Figure 14-1 SSD1307Z2 die tray information







Symbol	Spec (mm)	(mil)
W1	76.00±0.1	(2992)
W2	68.00±0.1	(2677)
W3	68.30±0.1	(2689)
TPx	57.96±0.08	(2282)
TPy	63.60±0.08	(2504)
Px	8.28±0.04	(326)
Py	2.65±0.04	(104)
Cx	28.98±0.08	(1141)
Cy	31.80±0.08	(1252)
X	6.59±0.05	(259)
Y	0.96±0.05	(38)
Z	0.40±0.05	(16)
N	200(pocket number)	
Chip-x	6.49 mm	
Chip-y	0.86 mm	
Chip-z	0.30 mm	

The product(s) listed in this datasheet comply with Directive 2002/95/EC of the European Parliament and of the council of 27 January 2004 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People's Republic of China Electronic Industry Standard SJ/T 11363-2006 "Requirements for concentration limits for certain hazardous substances in electronic information products (电子信息产品中有毒有害物质的限量要求)". Hazardous Substances test report is available upon request.

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