



## Amendment history of SSD1325 Specification

Revision	Description of any change	Issued	Effective
0.10 A5MA1 16-JUL-03	PRELIMINARY EDITION  Approver list: Product Marketing-Raymond Ho Design Engineering-Ricky Ng Product Engineering-Bryan Ma Quality & Manufacturing-Frank Leung	Jeffrey Young	23-Jul-03
0.20 A5MA3 20-Oct-03	Remove programmable feature for VSL in page 1 Revised display offset description Remove VSL command and command description Remove confidential watermark Revise ordering information page Add SSD1325UR1 and SSD1325T3R1 package information  Approver list: Product Marketing-Raymond Ho Design Engineering-Ricky Ng Product Engineering-Bryan Ma Quality & Manufacturing-Frank Leung	Jeffrey Young	30-Oct-03
1.0 A7MB1 12-Jul-04	Release Advance info Copy from SSD0323_v1.1 spec Remove VSL commend in commend table Add T3R1 and UR1 info Revise T3 & U cut line tolerance  Approver list: Product Marketing-Raymond Ho Design Engineering-Ricky Ng Product Engineering-Jeffrey Young Quality & Manufacturing-Frank Leung	Jack Tsang	11-Aug-04
1.1 A7MB1 15-Dec-04	Add U2 info  Approver list: Product Marketing-Raymond Ho Design Engineering-Ricky Ng Product Engineering-Jeffrey Young Quality & Manufacturing-Frank Leung	Jack Tsang	03-Jan-05
1.2 A7MB1 30-Aug-05	Add T1 and T6 info  Approver list: Product Marketing-Raymond Ho Design Engineering-Ricky Ng Product Engineering-Jeffrey Young Quality & Manufacturing-Frank Leung	Jack Tsang	03-Oct-05
1.3 A7MB2 01-Feb-06	1. Added application example for SSD1325T1R1 2. Revised command B1h, B3h, BCh, BEh 3. Removed command CFh 4. Revised command descriptions: "Set Row Period" and "Set Display Clock Divide Ratio" 5. Revised Table 25 SSD1325U2 pin assignment 6. Revised V <sub>COMH</sub> part in Table 16 Maximum ratings 7. Added V <sub>COMH</sub> part in Table 17 DC Characteristics	Ada Ng	06-Feb-06

Revision	Description of any change	Issued	Effective
	<p>8. Corrected the SCLK(D<sub>0</sub>) waveform in Figure 11 Serial Interface Characteristic:</p> <p>Original:</p>  <p>Now:</p>  <p>Approver list:  Product Marketing-Raymond Ho  Design Engineering-Ricky Ng  Product Engineering-Jeffrey Young  Quality &amp; Manufacturing-Frank Leung</p>		
1.4 A7MB2 22-Aug-06	<ol style="list-style-type: none"> <li>Add Graphic Acceleration Commands : <ul style="list-style-type: none"> <li>23h Graphic Command Options</li> <li>24h Graphic Command : Draw Rectangle</li> <li>25h Graphic Command : Copy Rectangle</li> <li>26h Graphic Command : Horizontal Scroll</li> <li>2Eh Graphic Command : stop moving</li> <li>2Fh Graphic Command : start moving</li> </ul> </li> <li>Revise AEh, AFh, B8h in command table</li> <li>Correct pin 31 of SSD1325T1R1 from VSL to NC</li> <li>Remove VSL pin in SSD1325T1R1 application diag</li> <li>Revise SSD1325 die drawing and pad coordinate</li> <li>Replace POR by Reset</li> <li>Revise Maximum rating</li> <li>Add a note on capacitor value on application example</li> <li>Add a note about Fosc under Table 18</li> <li>Add a note in B1 command ( 0 DCLK is invalid in Phase 1&amp;2)</li> <li>Revise D/C#, CL pin description</li> <li>Revise MCU interface</li> <li>Revise Dev value (Overall pin to pin) in Table 23 - DC Characteristics (Changes for removing external V<sub>COMH</sub>)</li> <li>Revise Block Diagram (V<sub>COMH</sub> is pointing out)</li> <li>Revise V<sub>COMH</sub> pin description</li> <li>Update command ADh ( No external V<sub>COMH</sub> option)</li> <li>Update command BEh Set V<sub>COMH</sub> voltage (removed set V<sub>COMH</sub> to 1*V<sub>ref</sub>)</li> <li>No V<sub>COMH</sub> info in table 16 Maximum ratings</li> <li>No V<sub>COMH</sub> info in Table 17 DC Characteristics</li> <li>Remove the “pointing-inside arrow” of V<sub>COMH</sub> pin in Application Example.</li> <li>Remove VIH and VIL test condition in Table 17- DC Characteristic</li> </ol> <p>Approver list:  Product Marketing-Raymond Ho  Design Engineering-Ricky Ng  Product Engineering-Jeffrey Young  Quality &amp; Manufacturing-Daniel Ho</p>	Ada Ng	04-Sep-06
1.5 A7MB2 27-Sep-06	<ol style="list-style-type: none"> <li>Add power on OFF sequence ( reference:SSD1303 rev2.4)</li> <li>Add RESET timing in Table 24 AC Characteristics (reference: SSD1303 rev2.4)</li> </ol> <p>Approver list:  Product Marketing-Jack Tsang  Design Engineering-Ricky Ng  Product Engineering-Jeffrey Young  Quality &amp; Manufacturing-Daniel Ho</p>	Ada Ng	05-Oct-06
1.6 A7MB2 18-Oct-06	<ol style="list-style-type: none"> <li>Revise hex code of AEh in command table</li> <li>Revise Figure 1 – Segment current vs Contrast setting</li> <li>Revise command description of Set Contrast Control Register</li> </ol> <p>Approver list:  Product Marketing-Jack Tsang</p>	Ada Ng	24-Oct-06

Revision	Description of any change	Issued	Effective
	Design Engineering-Ricky Ng Product Engineering-Jeffrey Young Quality & Manufacturing-Daniel Ho		
1.7 A7MB2 26-Jul-07	1) Add commands B0h and B4h ( source: SSD0323 rev1.6) 2) The title of "Set DC-DC Converter" description is changed to "Set Master Configuration" on page 32 3) Add note in ADh Set Master Configuration command table  Approver list: Product Marketing-Bryan Ma Design Engineering-Ricky Ng Product Engineering-Johnkid Lo Quality & Manufacturing-Daniel Ho Test/TPE Engineering – Stephen Leung	Ada Ng	03-Jul-07
1.8 A7MB2 06-Aug-07	1. Revise pin description of VSL and VSLCAP pin 2. Move SSD1325UR1, SSD1325T3R1, SSD1325U2 and SSD1325T1R1 dwg to appendix 3. Revise application example from SSD1325T1R1 to SSD1325T6R1 4. Add light sensitivity command under Table 22- Maximum Ratings 5. Add commands BFh in command table, VSL pin description & application example  Approver list: Product Marketing-Bryan Ma Design Engineering-Ricky Ng Product Engineering-Johnkid Lo Quality & Manufacturing-Daniel Ho Test/TPE Engineering – Stephen Leung	Ada Ng	08-Aug-07
1.9 A7MB2 16-Oct-07	1. Add a Remark column in the Ordering Information table 2. Remove the internal DC-DC block from the SSD1325 Block Diagram 3. Amend the die size 4. Update the Pin Description table, add pin descriptions for FR and DOF# 5. Remove the internal DC-DC voltage converter and its corresponding information from Advance Info to Appendix 6. Add details on section 8.2 (Segment drivers / Common drivers) 7. Add details on section 8.6 (Current Control and Voltage Control) 8. Revise the Command Table (ADh, ...) 9. Revise sections 10.1.6 (Set Display Start Line (A1h)) & 10.1.7 (Set Display Offset (A2h)) by adding examples 10. Revise section 10.1.10 (Set Master Configuration (ADh)) 11. Add Remark on section 15.1 SSD1325Z Die Tray Information 12. Add SSD1325T2R1 dwg and corresponding information to appendix 13. Add application example of SSD1325Z SPI serial interface 14. Revise the adjacent pin uniformity limit to +/-1.5% 15. Revise the typo errors 16. Update the datasheet format for standardization  Approver list: Product Marketing-Bryan Ma Design Engineering-Ricky Ng Product Engineering-Johnkid Lo Quality & Manufacturing-Daniel Ho Test/TPE Engineering – Stephen Leung	Ada Ng	16-Oct-07

Revision	Description of any change	Issued	Effective
2.0 A7MB2 12-Dec-07	1. Amend the die size 2. Revise the die tray information  Approver list: Product Marketing-Bryan Ma Design Engineering-Ricky Ng Product Engineering-Johnkid Lo Quality & Manufacturing-Daniel Ho Test/TPE Engineering – Stephen Leung	Ada Ng	19-Dec-07
2.1 A7MB2 13-May-08	1. Revise default value in BCh & BEh command table 2. Remove below figures: Figure 30 : $V_{COMH}$ Vs Bit Value Figure 31 : $V_p$ Vs Bit Value 2. Add and Revise Power ON OFF sequence notes (2~5)  Approver list: Product Marketing-Raymond Ho Design Engineering-Ricky Ng Product Engineering-Johnkid Lo Quality & Manufacturing-Daniel Ho Test/TPE Engineering – Stephen Leung	Ada Ng	15-May-08
2.2 A7MB2 11-Aug-08	1. Deleted the statement “OLED driving output voltage, 14V maximum” in the Features list (section 2)  Approvers: Marketing – Raymond Ho Design – Kenneth Lee PE – Johnkid Lo PQA – Daniel Ho TE/TPE – Stephen Leung	Ada Ng	11-Aug-08
2.3 A7MB2 A7MB2+ 09-Jul-10	1. Add Moo# A7MB2+ 2. Replace SSD1325Z by SSD1325Z2 and add SSD1325Z2 into section 3 ordering information (P.8) 3. Revise die thickness tolerance from $\pm 25\mu m$ to $\pm 15\mu m$ in section 5 (P.10) 4. Added +/- 50um tolerance for Die Size (after sawing) Section 5 (P.10 ) 5. Revise typo in AEh / AFh command (P.33) 6. Revise typo in B3h command (p.34) from “RESET= 0100b represents 655KHz” to “RESET= 0100b represents 630KHz” 7. Revise disclaimer (P.63)  Approvers: Marketing – Raymond Ho Design – Kenneth Lee PE – Johnkid Lo PQA – Daniel Ho TE/TPE – PL Che / Warren Wong	Ada Ng	16-Jul-10

# SSD1325

## *Advance Information*

**128 x 80, 16 Gray Scale Dot Matrix  
OLED/PLED Segment/Common Driver with Controller**

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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SSD1325

Rev 2.3

P 1/63

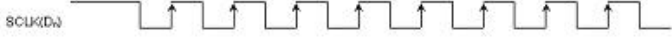

Jul 2010

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### Appendix: IC Revision history of SSD1325 Specification

Version	Change Items	Effective Date
1.0	<ol style="list-style-type: none"> <li>1. Changed to Advance Info</li> <li>2. Added information of SSD1325T3R1 and SSD1325UR1</li> <li>3. Revised the cutline tolerance of SSD1325T3R1 and SSD1325UR1</li> </ol>	11-Aug-04
1.1	<ol style="list-style-type: none"> <li>1. Added information of SSD1325U2</li> </ol>	03-Jan-05
1.2	<ol style="list-style-type: none"> <li>1. Added information of SSD1325T1R1 and SSD1325T6R1</li> </ol>	03-Oct-05
1.3	<ol style="list-style-type: none"> <li>1. Added application example of SSD1325T1R1</li> <li>2. Revised commands B1h, B3h, BCh, BEh</li> <li>3. Revised command descriptions: “Set Row Period” and “Set Display Clock Divide Ratio”</li> <li>4. Revised SSD1325U2 pin assignment</li> <li>5. Corrected the SCLK(D0) waveform in the figure of Serial Interface Characteristic: Original:    Now:  </li> </ol>	06-Feb-06
1.4	<ol style="list-style-type: none"> <li>1. Added Graphic Acceleration Commands (23h, 24h, 25h, 26h, 2Eh, 2Fh)</li> <li>2. Revised commands AEh, AFh, B8h in command table</li> <li>3. Revise SSD1325 die drawing and pad coordinate</li> <li>4. Added a note on capacitor value on application example</li> <li>5. Added a note in B1 command ( 0 DCLK is invalid in Phase 1&amp;2)</li> <li>6. Revised D/C#, CL pin description</li> <li>7. Revised MCU interface section</li> </ol>	04-Sep-06
1.5	<ol style="list-style-type: none"> <li>1. Added power on / off sequence</li> <li>2. Add RESET timing in the AC Characteristics Table</li> </ol>	05-Oct-06
1.6	<ol style="list-style-type: none"> <li>1. Revised hex code of AEh in command table</li> <li>2. Revised the figure of Segment Current vs Contrast Setting</li> <li>3. Revised command description of Set Contrast Control Register</li> </ol>	24-Oct-06
1.7	<ol style="list-style-type: none"> <li>1. Added commands B0h and B4h on the command table</li> <li>2. Added note in command ADh (Set Master Configuration) in command table</li> </ol>	03-Jul-07
1.8	<ol style="list-style-type: none"> <li>1. Revised pin description of VSL and VSLCAP pin</li> <li>2. Removed SSD1325UR1, SSD1325T3R1, SSD1325U2 and SSD1325T1R1 dwgs</li> <li>3. Revised application example from SSD1325T1R1 to SSD1325T6R1</li> <li>4. Added light sensitivity note under Table 22 - Maximum Ratings</li> <li>5. Added commands BFh in command table, VSL pin description &amp; application example</li> </ol>	08-Aug-07
1.9	<ol style="list-style-type: none"> <li>1. Added a Remark column in the Ordering Information table</li> <li>2. Removed the internal DC-DC block from the SSD1325 Block Diagram</li> <li>3. Amended the die size</li> <li>4. Updated the Pin Description table and added pin descriptions for FR and DOF#</li> </ol>	16-Oct-07

Version	Change Items	Effective Date
	<ol style="list-style-type: none"> <li>5. Removed the internal DC-DC voltage converter and its corresponding information</li> <li>6. Added details on section 8.2 (Segment drivers / Common drivers)</li> <li>7. Added details on section 8.6 (Current Control and Voltage Control)</li> <li>8. Revised sections 10.1.6 (Set Display Start Line (A1h)) &amp; 10.1.7 (Set Display Offset (A2h)) by adding examples</li> <li>9. Revised section 10.1.10 (Set Master Configuration (ADh))</li> <li>10. Added Remark on section 15.1 SSD1325Z Die Tray Information</li> <li>11. Added application example of SSD1325Z SPI serial interface</li> <li>12. Revise the adjacent pin uniformity limit to +/-1.5%</li> </ol>	
2.0	<ol style="list-style-type: none"> <li>1. Amended the die size</li> <li>2. Revised the die tray information</li> </ol>	19-Dec-07
2.1	<ol style="list-style-type: none"> <li>1. Revised the default values of commands BCh and BEh in command table</li> <li>2. Removed the below figures: Figure 30 : VCOMH vs Bit Value Figure 31 : VP vs Bit Value</li> <li>3. Added and revised Power on / off Sequence notes (2~5)</li> </ol>	15-May-08
2.2	<ol style="list-style-type: none"> <li>1. Deleted the statement “OLED driving output voltage, 14V maximum” in the Features list (section 2)</li> </ol>	11-Aug-08
2.3	<ol style="list-style-type: none"> <li>1. Replace SSD1325Z by SSD1325Z2 and add SSD1325Z2 into section 3 ordering information (P.8)</li> <li>2. Revise die thickness tolerance from ±25um to ±15um in section 5 (P.10)</li> <li>3. Added +/- 50um tolerance for Die Size section 5 (P.10 )</li> <li>8. Revise typo in AEh / AFh command (P.33)</li> <li>4. Revise typo in B3h command (p.34)</li> <li>5. Revise disclaimer (P.63)</li> </ol>	16-Jul-10

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## 1 GENERAL DESCRIPTION

SSD1325 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. It consists of 208 high voltage/current driving output pins for driving 128 segments and 80 commons. This IC is designed for Common Cathode type OLED/PLED panel.

SSD1325 displays data directly from its internal 128x80x4 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from general MCU through the hardware selectable 6800-/8080-series compatible Parallel Interface or Serial Peripheral Interface.

It has a 128-step contrast control and a 16 gray level control. The embedded on-chip oscillator and DC-DC voltage converter reduce the number of external components.

## 2 FEATURES

- Support max. 128 x 80 matrix panel
- Power supply:  $V_{DD}=2.4V - 3.5V$   
 $V_{CC}=8.0V - 16.0V$
- For matrix display:
  - Can output maximum segment source current: 300uA
  - Common maximum sink current: 40mA
- Embedded 128 x 80 x 4 bit SRAM display memory
- 128 step contrast current control on monochrome passive OLED panel
- 16 gray scale
- Internal Oscillator
- Programmable Frame Rate
- 8-bit 6800-series Parallel Interface, 8080-series Parallel Interface, Serial Peripheral Interface.
- Row re-mapping and Column re-mapping
- Low power consumption (<5.0uA @sleep mode)
- Wide range of operating temperature: -40 to 85 °C

## 3 ORDERING INFORMATION

Table 1 : Ordering Information

Ordering Part Number	SEG	COM	Package Form	Reference	Remarks
SSD1325Z2	128	80	COG	Page 10, 59	<ul style="list-style-type: none"><li>• Min SEG pad pitch: 52.2um</li><li>• Min COM pad pitch: 51.8um</li></ul>
SSD1325T6R1	128	80	TAB	Page 60	<ul style="list-style-type: none"><li>• 8-bit 80 / 68 / SPI interface</li><li>• Output lead pitch: 0.12mm x 0.998 = 0.11976mm</li><li>• 4 SPH, 35m film</li><li>• Full resolution 128 x 80</li></ul>

## 4 BLOCK DIAGRAM

Figure 1 : SSD1325 Block Diagram

