DATASHEET

凌陽科技 SUNPLUS

SPLC063A1

80 Channel Segment LCD Driver

FEB. 20, 2003

Version 1.5

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80 CHANNEL SEGMENT LCD DRIVER

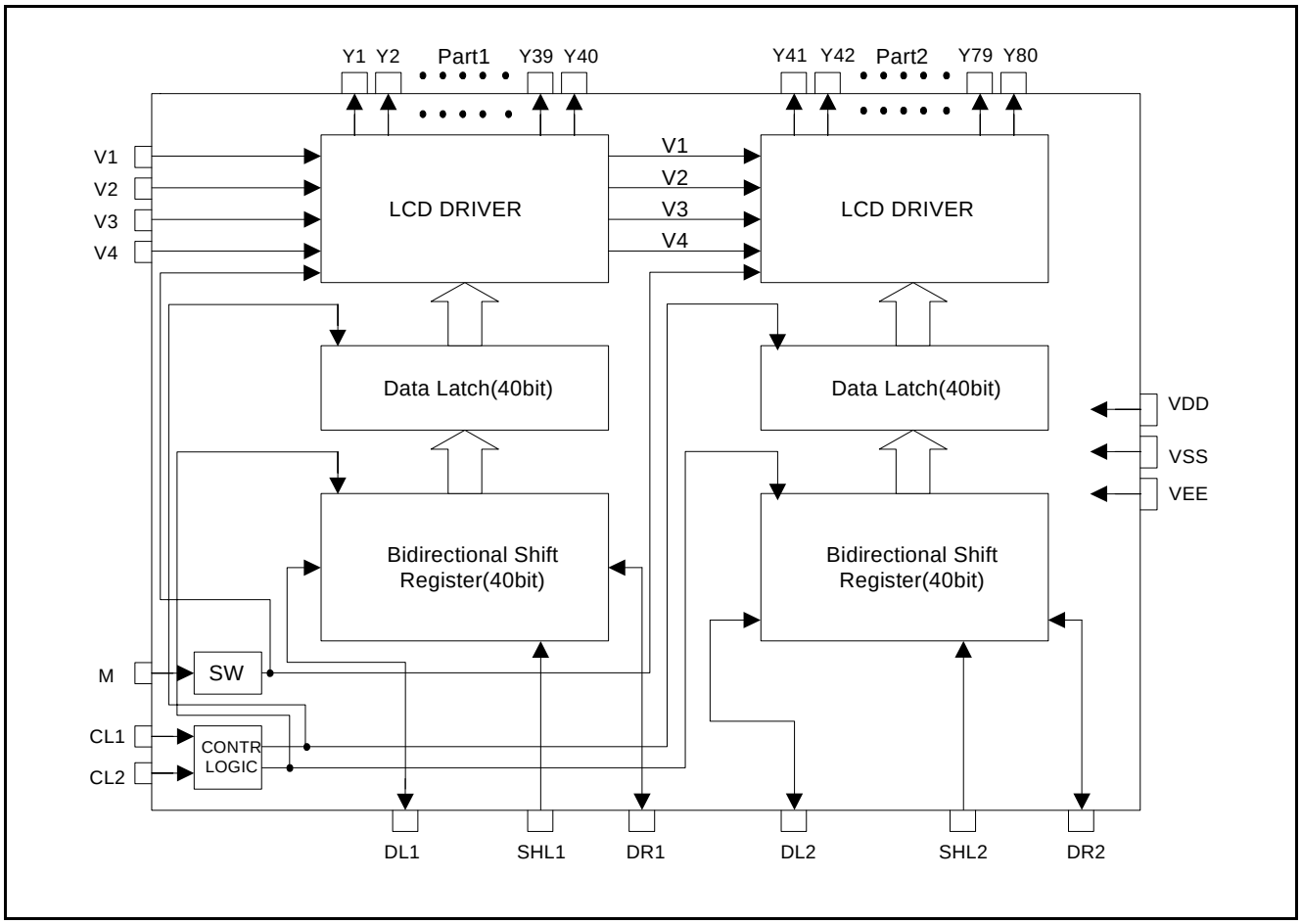
1. GENERAL DESCRIPTION

The SPLC063A1 is a LCD driver LSI which is fabricated by low power CMOS technology. Basically it consists of two set of 40-bit bi-directional shift registers, 40 data latch flip-flops and 40 liquid crystal display driver circuits. It has 80-channel outputs and can be applied as segment driver. The SPLC063A1 receives serial display data from a display control LSI, converts it into parallel data and supplies liquid crystal display waveforms to the liquid crystal. Its interface is compatible with the SPLC100. It reduces the number of LSI's and lowers the cost of a LCD module.

2. FEATURES

- Liquid crystal display driver with serial/parallel conversion function.
- Interface compatible with the SPLC100; connectable with SPLC780.
- Internal output circuits for LCD driver: 80
- Internal serial/parallel conversion circuits:
  - 40-bit bi-directional shift register X 2
  - 40-bit latch X 2
- Power supply:
  - Internal logic: 2.7V - 5.5V
  - Liquid crystal display driver circuit: 3.0V - 11V
- CMOS process.

3. BLOCK DIAGRAM



3.1. Block Functions

3.1.1. LCD driver

Select one of four levels of voltage V1, V2, V3, and V4 for driving a LCD and transfer it to the output terminals according to the combination of M and the data in the latch circuit.

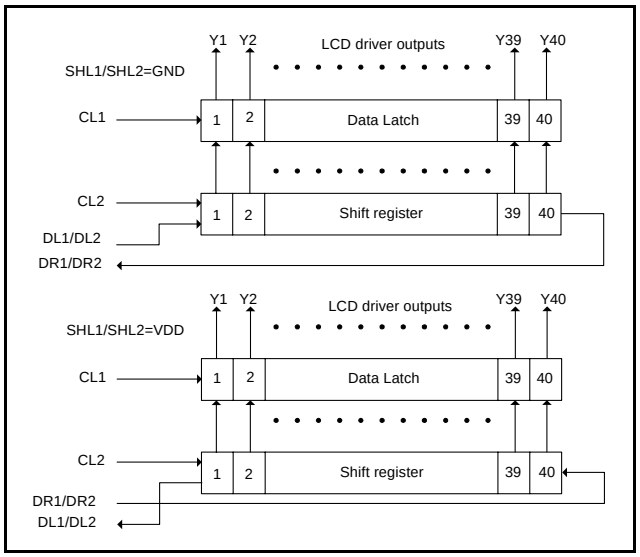
3.1.2. Data latch

Latches the data input from the bi-directional shift register at the fall of CL1 and transfer its outputs to the LCD driver circuits.

3.1.3. Bi-directional shift register

Shifts the serial data at the fall of CL2 and transfuse the output of each bit of the register to the latch circuit. When SHL1/SHL2 = GND, the data input from DL1/DL2 shifts from bit 1 to bit 40 in order of entry.

On the other hand, when SHL1/SHL2 = VDD, the data shifts from bit 40 to bit-1. The data of the last bit of the register is latched to be output from DR1/DR2 at the rise of CL2, when SHL1/SHL2 = GND. The data of the last bit of the register is latched to be output from DL1/DL2 at the rise of CL2 when SHL1/SHL2 = VDD.



Relation between SHL1/SHL2 and the Shift Direction

4. SIGNAL DESCRIPTIONS

<table>
<tr><th>Mnemonic (No.)</th><th>Input
Output</th><th colspan="2">Name</th><th>Description</th><th>Interface</th></tr>
<tr><td>VDD (59)</td><td rowspan="3">Power</td><td colspan="2">Operating Voltage</td><td>For logical circuit (2.7V - 5.5V)</td><td rowspan="3">Power Supply</td></tr>
<tr><td>VSS (GND) (55)</td><td colspan="2" rowspan="2">Negative Supply Voltage</td><td>0V (GND)</td></tr>
<tr><td>VEE (50)</td><td>For LCD driver circuit</td></tr>
<tr><td>V1, V2 (51, 52)</td><td>Input</td><td colspan="2" rowspan="2">LCD driver output voltage level</td><td>Bias voltage level for LCD driver (Select level)</td><td rowspan="2">Power</td></tr>
<tr><td>V3, V4 (53, 54)</td><td>Input</td><td>Bias voltage level for LCD driver
(Nonselect level)</td></tr>
<tr><td>Y1 - Y40</td><td>Output</td><td rowspan="3">Part1</td><td>LCD driver</td><td>LCD driver output</td><td>LCD</td></tr>
<tr><td>SHL1 (57)</td><td>Input</td><td rowspan="2">Data Interface</td><td>Selection of the shift direction of shift register
<table><tr><td>SHL1</td><td>DL1</td><td>DR1</td></tr><tr><td>VDD</td><td>OUT</td><td>IN</td></tr><tr><td>VSS</td><td>IN</td><td>OUT</td></tr></table></td><td>VDD or VSS</td></tr>
<tr><td>DL1, DR1 (61, 62)</td><td>Input
Output</td><td>Data input/output of shift register (part1)</td><td>Controller or SPLC063A1</td></tr>
<tr><td>Y41 - Y80</td><td>Output</td><td rowspan="3">Part2</td><td>LCD driver</td><td>LCD driver output</td><td>LCD</td></tr>
<tr><td>SHL2 (58)</td><td>Input</td><td rowspan="2">Data Interface</td><td>Selection of the shift direction of shift register
<table><tr><td>SHL2</td><td>DL2</td><td>DR2</td></tr><tr><td>VDD</td><td>OUT</td><td>IN</td></tr><tr><td>VSS</td><td>IN</td><td>OUT</td></tr></table></td><td>VDD or VSS</td></tr>
<tr><td>DL2, DR2 (63, 64)</td><td>Input Output</td><td>Data input/output of shift register (part 2)</td><td>Controller or SPLC063A1</td></tr>
<tr><td>M (65)</td><td>Input</td><td colspan="2">Alternated signal for LCD driver output</td><td>The alternating signal to convert LCD driver waveform to AC</td><td>Controller</td></tr>
<tr><td>CL1, CL2 (56, 60)</td><td>Input</td><td colspan="2">Data shift/latch clock</td><td>CL1: Data latch clock
CL2: Data shift clock</td><td>Controller</td></tr>
</table>

5. FUNCTIONAL DESCRIPTIONS

5.1. Dot Matrix LCD Driver with 80 Channel Outputs.

5.2. Input / Output Signal

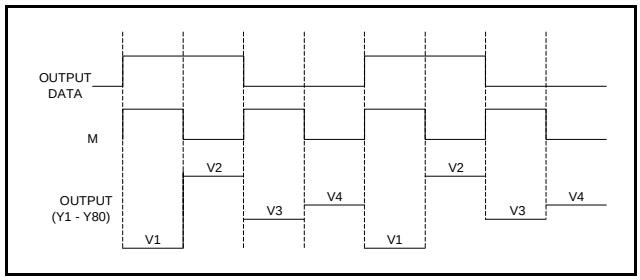
— Output: 40 X 2 channel waveform for LCD driving

— Input:

1). Serial display data and control pulse from the controller LSI.

2). Bias voltage (V1 - V4).

5.3. LCD Output Waveform



V1, V2: selected level

V3, V4: Non-selected level

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit
Operation Voltage	VDD	-0.3 to +7.0	V
LCD Driver Supply Voltage	VEE	VDD-12V to VDD+0.3V	V
Operating Temperature	T_A	-20 to +75	°C
Storage Temperature	T_{STO}	-55 to +125	°C
Input voltage (1)	V_{IN1}	-0.3 to VDD+0.3	V
Input voltage (2)	V_{IN2}	VDD+0.3 to VEE-0.3	V

Note1: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

Note2: Input Voltage (2) applies to V1 - V4; Input Voltage (1) applies to other pins.

6.2. DC Characteristics

(VDD = 2.7V - 5.5V, VDD - VEE = 3.0V - 11V, T_A = +25℃)

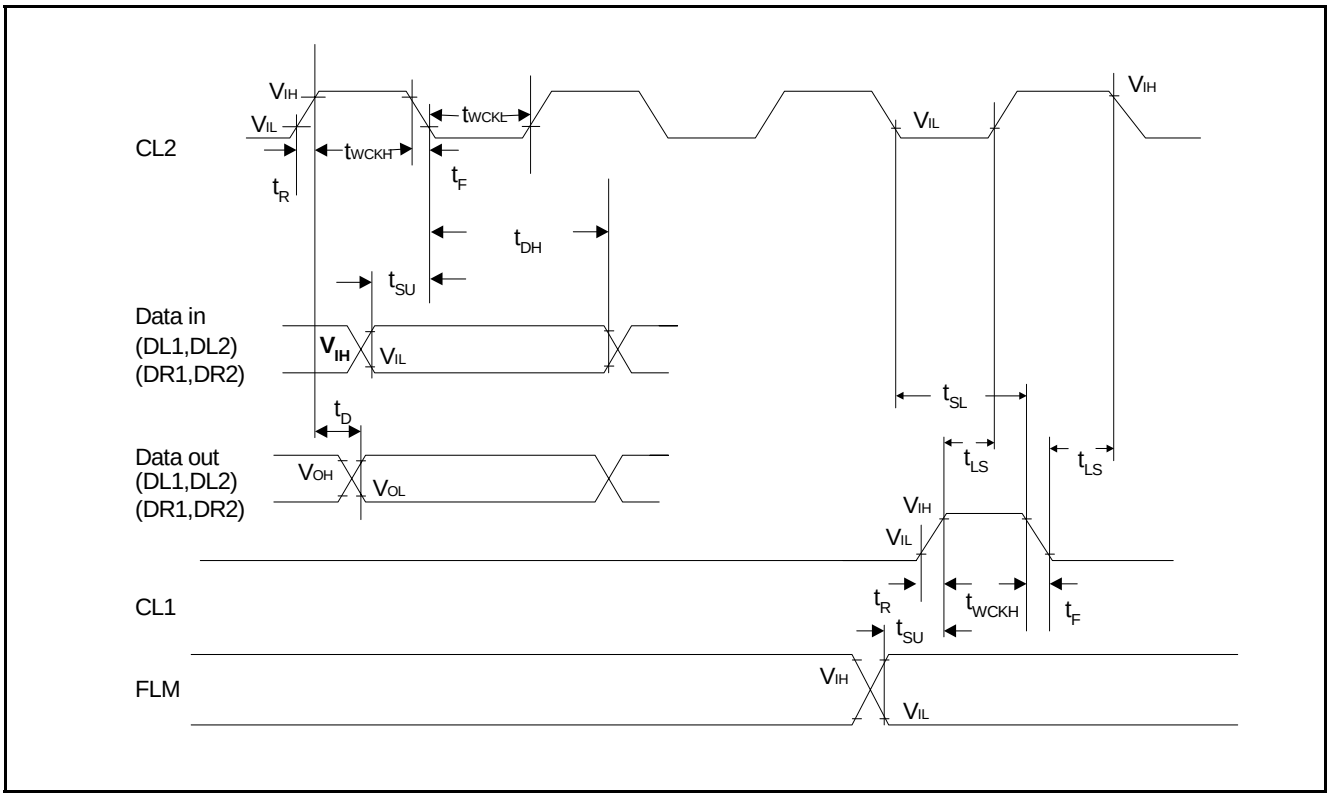
Characteristic	Symbol	Test Condition	Min.	Max.	Unit	Applicable Pin
Operating Current	I_{DD}	f_{CL2} = 400KHz	-	1.0	mA	VDD, VEE
Supply Current	I_{EE}	f_{CL1} = 1.0KHz	-	10	µA	
Input High Voltage	V_{IH}		0.7VDD	VDD	V	CL1, CL2, DL1, DL2, DR1, DR2, SHL1, SHL2, M
Input Low Voltage	V_{IL}		0	0.3VDD		
Input Leakage Current	I_{LKG}	V_{IN} = 0 to VDD	-5.0	5.0	µA	
Output High Voltage	V_{OH}	I_{OH} = -0.4mA	VDD-0.4	-	V	DL1, DL2, DR1, DR2
Output Low Voltage	V_{OL}	I_{OL} = +0.4mA	-	0.4		
Voltage Descending	V_{D1}	I_{ON} = 0.1mA for one of Y1 - Y80	-	1.1	V	V(V1 - V4)-Y(Y1 - Y80)
	V_{D2}	I_{ON} = 0.05mA for each Y1 - Y80	-	1.5		
Leakage Current	I_V	V_{IN} = VDD to VEE (Output Y1 - Y80; floating)	-10	10	µA	V1 - V4

6.3. AC Characteristics

(VDD = 2.7V - 5.5V, VDD - VEE = 3.0V - 11V, T_A = +25℃)

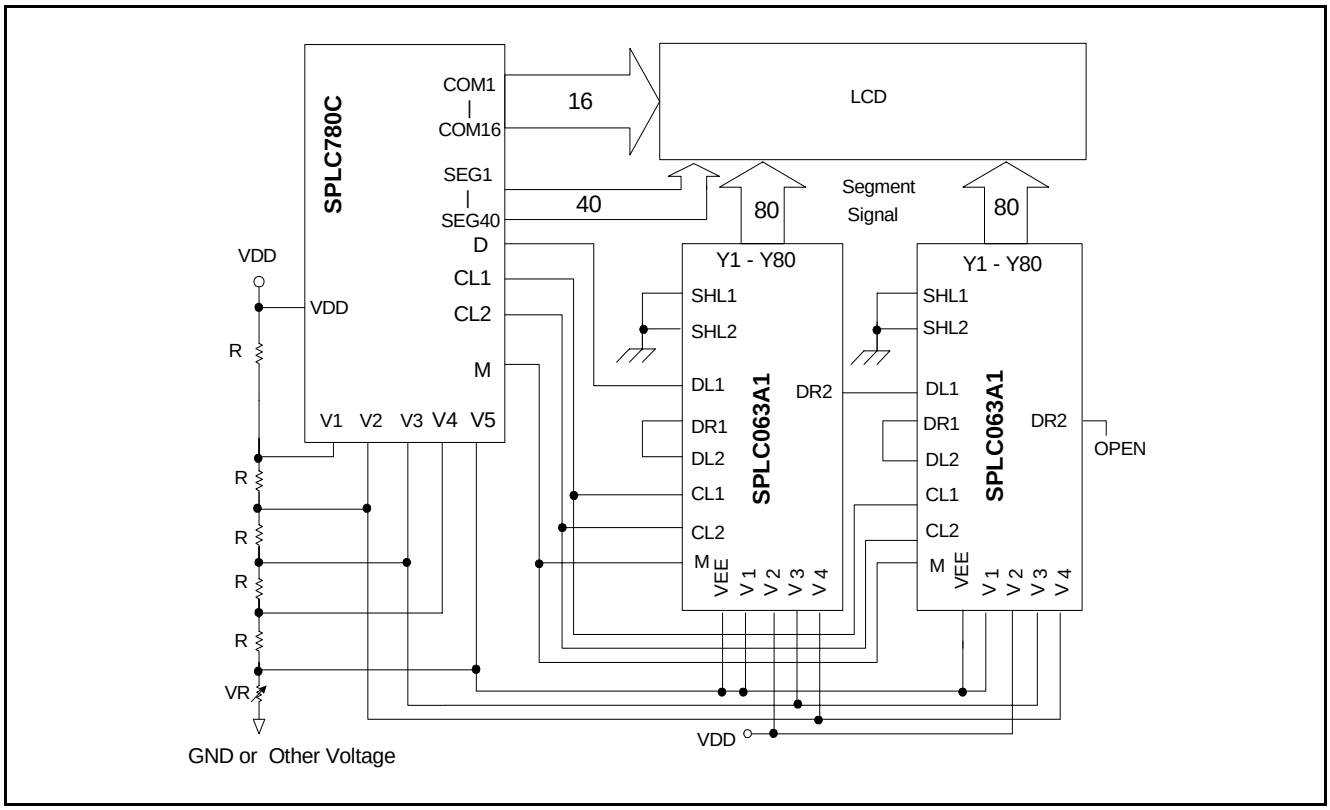
Characteristic	Symbol	Application Pin	Min.	Max.	Unit	Test Condition
Data shift frequency	f_{CL}	CL2	-	400	KHz	
Clock High level Width	t_{WCKH}	CL1, CL2	800	-	ns	
Clock Low level Width	t_{WCKL}	CL2	800	-		
Data set-up time	t_{SU}	DL1, DL2, DR1, DR2	300	-		
Clock set-up time	t_{SL}	CL1, CL2	500	-		(CL2→CL1)
Clock set-up time	t_{LS}		500	-		(CL1→CL2)
Clock rise/fall time	t_R/t_F		-	200		
Date delay time	t_D	DL1, DL2, DR1, DR2	-	500		C_L = 15pF
Date hold time	t_{DH}	DL1, DL2, DR1, DR2	300	-		

6.4. Timing Characteristic

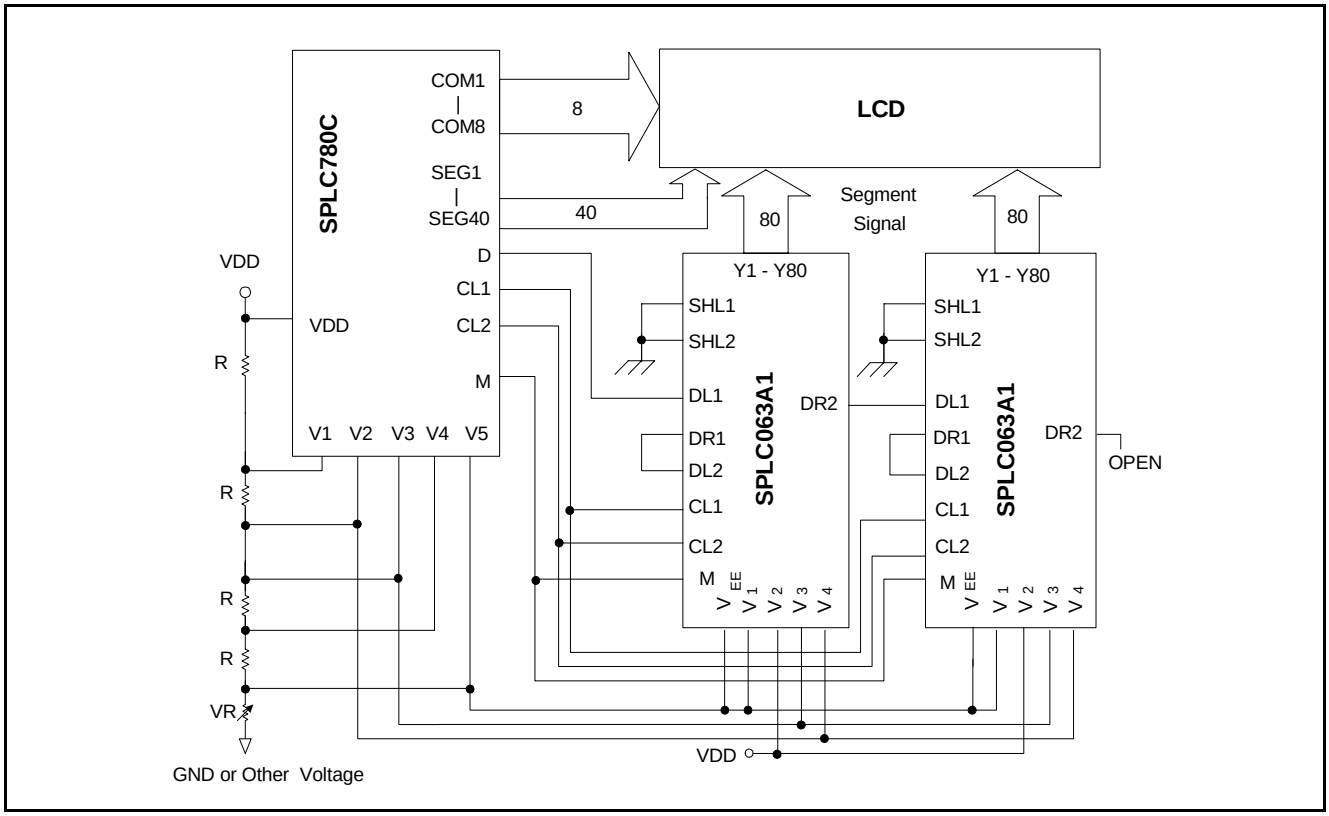


7. APPLICATION CIRCUITS

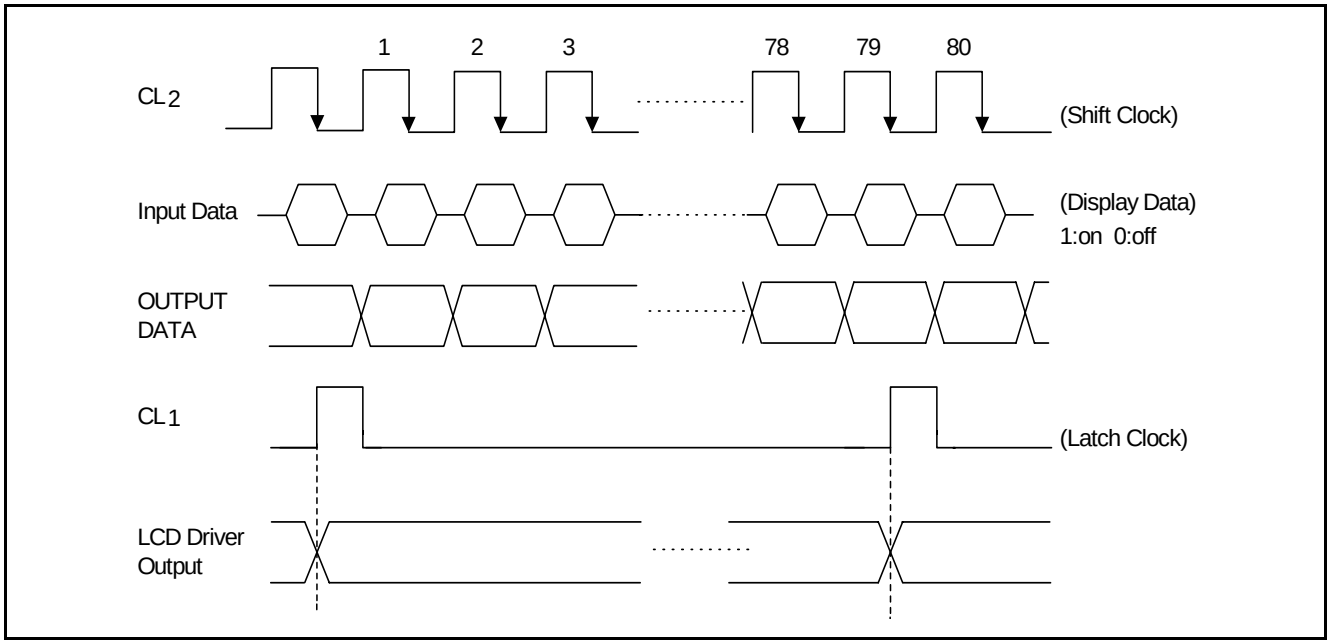
7.1. Application Circuit for 1/16 Duty, 1/5 Bias



7.2. Application Circuit for 1/8 Duty, 1/4 Bias

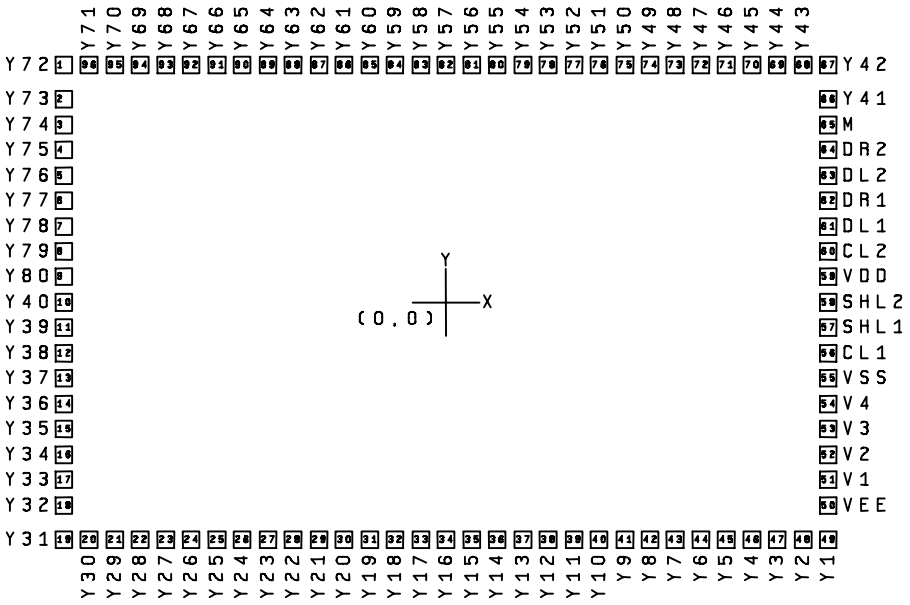


7.3. Timing Chart of Input and Output Data



8. PACKAGE/PAD LOCATIONS

8.1. PAD Assignment



Chip Size: 4480μm×2940μm

Pad Size : 90μm×90μm

This IC's substrate should be connected to VDD

Note1: Chip size included scribe line.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

8.2. Ordering Information

Product Number	Package Type
SPLC063A1-nnnnV-C	Chip form
SPLC063A1-nnnnV-PQ06	Package form - QFP 100L

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (V = A - Z).

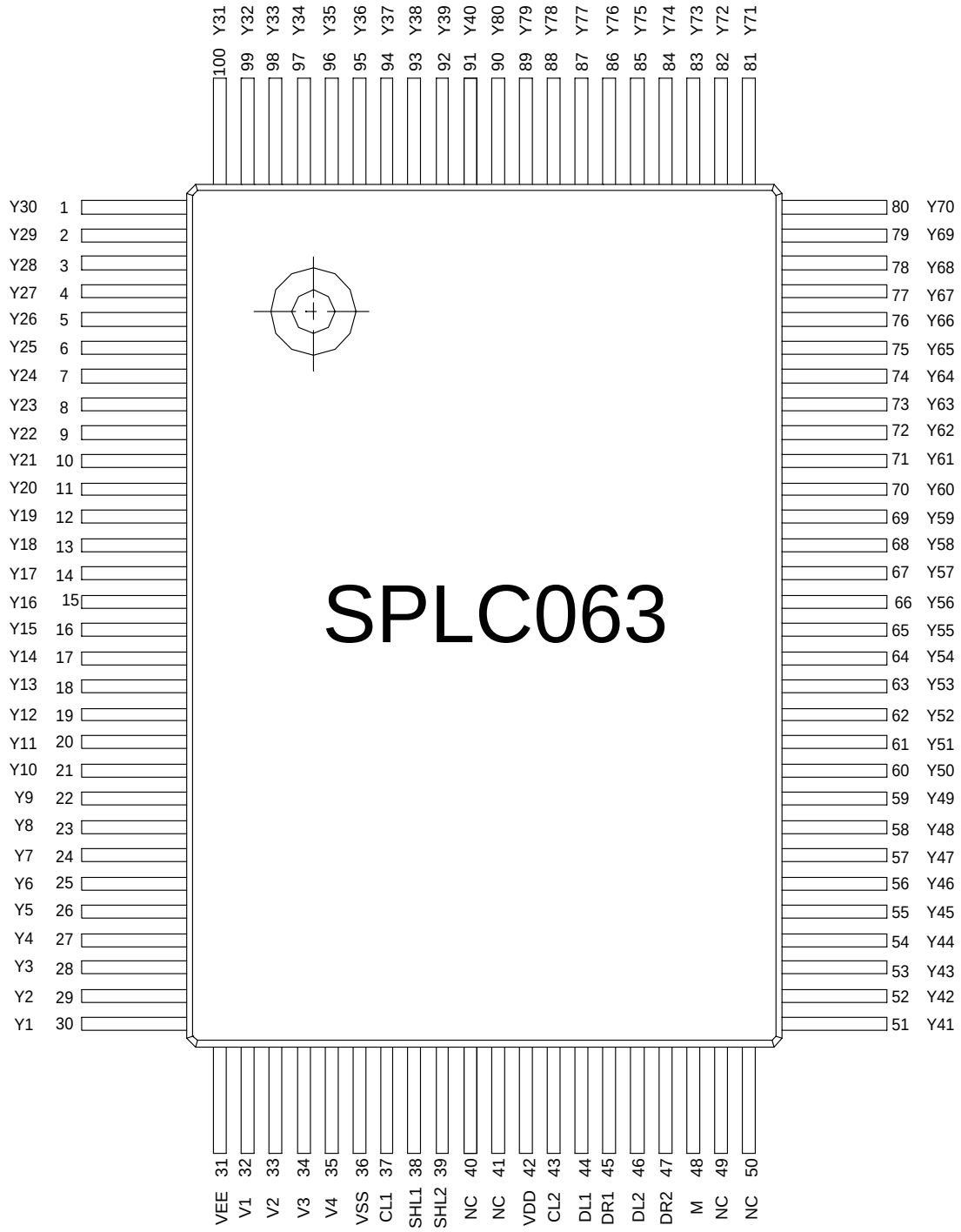
8.3. PAD Locations

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	Y72	-2057	1273	49	Y1	2056	-1273
2	Y73	-2040	1097	50	VEE	2043	-1097
3	Y74	-2040	959	51	V1	2043	-960
4	Y75	-2040	822	52	V2	2043	-823
5	Y76	-2040	685	53	V3	2043	-685
6	Y77	-2040	548	54	V4	2043	-548
7	Y78	-2040	411	55	VSS	2043	-412
8	Y79	-2040	273	56	CL1	2043	-274
9	Y80	-2040	136	57	SHL1	2043	-137
10	Y40	-2040	0	58	SHL2	2043	0
11	Y39	-2040	-137	59	VDD	2043	136
12	Y38	-2040	-274	60	CL2	2043	273
13	Y37	-2040	-412	61	DL1	2043	411
14	Y36	-2040	-548	62	DR1	2043	548
15	Y35	-2040	-685	63	DL2	2043	685
16	Y34	-2040	-823	64	DR2	2043	822
17	Y33	-2040	-960	65	M	2043	959
18	Y32	-2040	-1097	66	Y41	2043	1097
19	Y31	-2057	-1273	67	Y42	2056	1273
20	Y30	-1920	-1273	68	Y43	1920	1273
21	Y29	-1783	-1273	69	Y44	1782	1273
22	Y28	-1646	-1273	70	Y45	1645	1273
23	Y27	-1508	-1273	71	Y46	1508	1273
24	Y26	-1372	-1273	72	Y47	1371	1273
25	Y25	-1234	-1273	73	Y48	1234	1273
26	Y24	-1097	-1273	74	Y49	1096	1273
27	Y23	-960	-1273	75	Y50	959	1273
28	Y22	-823	-1273	76	Y51	823	1273
29	Y21	-686	-1273	77	Y52	685	1273
30	Y20	-548	-1273	78	Y53	548	1273
31	Y19	-411	-1273	79	Y54	410	1273
32	Y18	-274	-1273	80	Y55	274	1273
33	Y17	-137	-1273	81	Y56	137	1273
34	Y16	0	-1273	82	Y57	0	1273
35	Y15	137	-1273	83	Y58	-137	1273
36	Y14	274	-1273	84	Y59	-274	1273
37	Y13	410	-1273	85	Y60	-411	1273
38	Y12	548	-1273	86	Y61	-548	1273
39	Y11	685	-1273	87	Y62	-686	1273
40	Y10	823	-1273	88	Y63	-823	1273
41	Y9	959	-1273	89	Y64	-960	1273
42	Y8	1096	-1273	90	Y65	-1097	1273
43	Y7	1234	-1273	91	Y66	-1234	1273
44	Y6	1371	-1273	92	Y67	-1372	1273

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
45	Y5	1508	-1273	93	Y68	-1508	1273
46	Y4	1645	-1273	94	Y69	-1646	1273
47	Y3	1782	-1273	95	Y70	-1783	1273
48	Y2	1920	-1273	96	Y71	-1920	1273

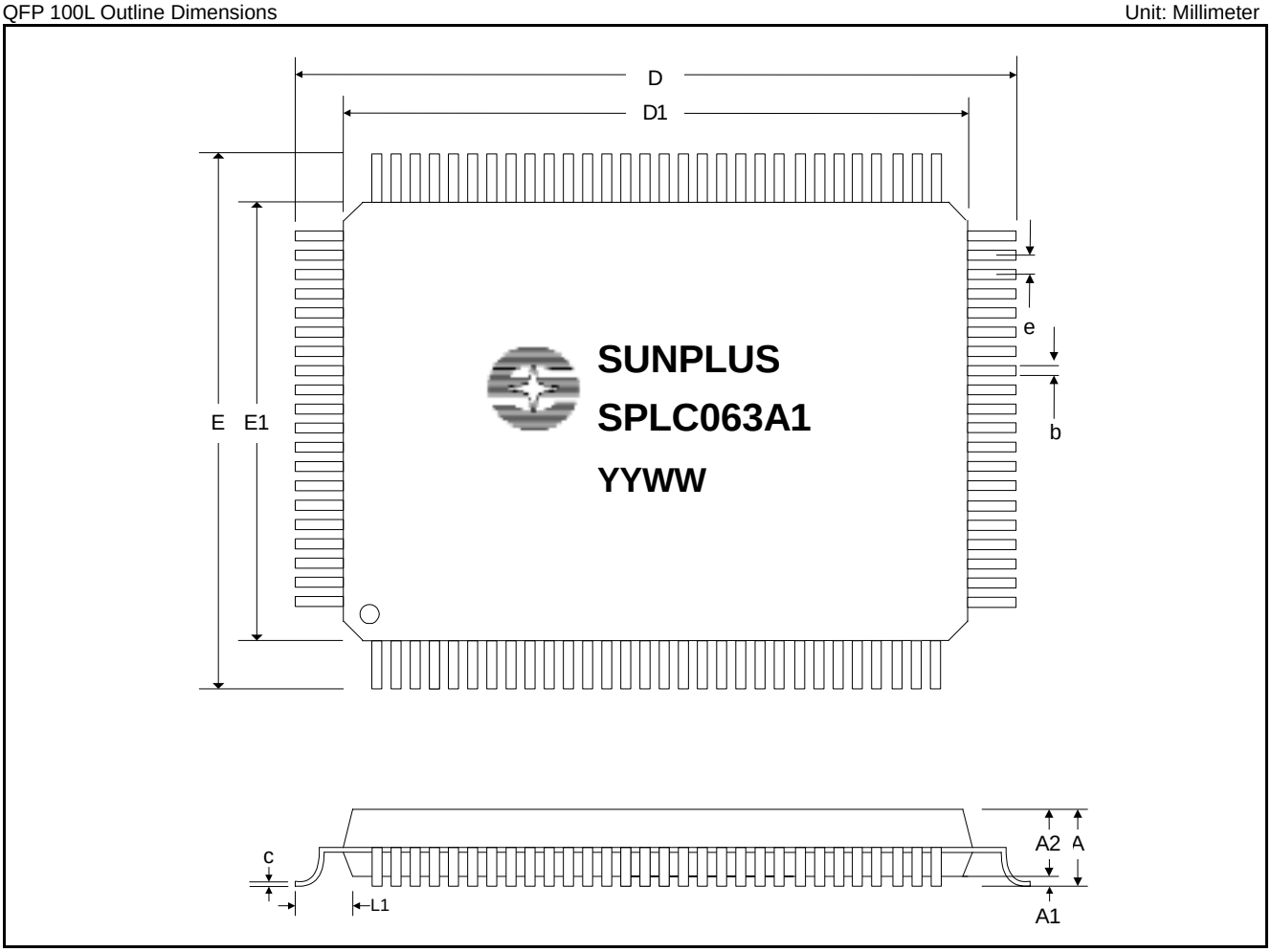
8.4. Package Configuration

QFP 100L Top View



8.5. Package Information

QFP 100L Outline Dimensions Unit: Millimeter



Symbol	Min.	Nom.	Max.	Unit
D		23.20 REF		Millimeter
D1		20.00 REF		Millimeter
E		17.20 REF		Millimeter
E1		14.00 REF		Millimeter
e		0.65 REF		Millimeter
b	0.22	0.30	0.38	Millimeter
A	-	-	3.40	Millimeter
A1	0.25	-	-	Millimeter
A2	2.50	2.72	2.90	Millimeter
c	0.11	0.15	0.23	Millimeter
L1		1.60 REF		Millimeter

9. DISCLAIMER

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10. REVISION HISTORY

Date	Revision #	Description	Page
NOV. 02, 1999	1.0	Original	
JUN. 15, 2000	1.1	1. DC characteristics range: VDD: 2.7V - 5.5V, VDD - VEE: 3.0V - 11V 2. Correct DC characteristics 3. Correct AC characteristics 4. Add PAD size description	
MAY. 04, 2001	1.2	1. Correct PAD Size and Chip Size 2. Renew to a new document format	
OCT. 16, 2001	1.3	1. Modify application circuits: SPLC780A2 to SPLC780C 2. Add Note1 and Note2 in the "*8.1 PAD Assignment*" 3. Add package information in the "*8.2 Ordering Information*" 4. Renew to a new document format	9 11 11
JUL. 09, 2002	1.4	1. Update "*8.2 Ordering Information*" 2. Update "*8.5 Package Information*"	11 14
FEB. 20, 2003	1.5	Correct pad size : 96μm×96μm -> 90μm×90μm	11