DATA SHEET

SUNPLUS

SPLC701B

11x12 and 6x12 Text and Graphics Liquid Crystal Display Controller/Driver

MAY. 17, 2005

Version 1.5

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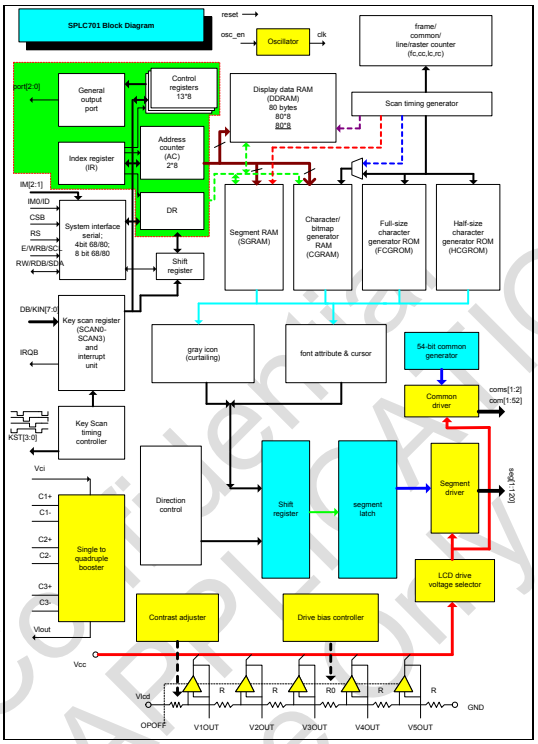
11x12 and 6x12 Text and GRAPHICS LIQUID CRYSTAL DISPLAY CONTROLLER/DRIVER

1. GENERAL DESCRIPTION

The SPLC701B, a fresh designed LCD controller with advanced CMOS technology from SUNPLUS, is able to display one to four lines of 10 kanji-font characters with 11 x 12 dots full-size format. A 5 x 12 dot half-size alphanumeric characters can also be displayed. It also has the capability to show 120 x 52 dots graphical LCD, 160 mono-blinking icons, and 40 gray-scale icons. With modern technology, the SPLC701B contain nine primary functions in a single compact chip.

1). Five types of MPU interface, 80/68 8-bit/4-bit and clock synchronous serial interface.
2). Key-scan support.
3). Varieties of dot-matrix LCD.
4). Three RAMs: one for character code, one for icon, and the other for graphics or user font.
5). Two ROMs: one for kanji-font, the other for alphanumeric characters.
6). 120-segment / 54-common driver.
7). 1X-4X booster.
8). Voltage follower & bias circuits.
9). Built-in RC-oscillator.

2. BLOCK DIAGRAM



3. FEATURES

- Driver Output Circuits
  - Common outputs: 52 common + 2 common for icon
  - Segment outputs: 120 segment
- Internal Memory
  - Full-size Character Generator ROM (FCGROM):1,072,896 bits (8,128 characters x 11 x 12 dots)
  - Half-size Character Generator ROM (HCGROM): 15,360 bits (256 characters x 5 x 12 dots)
  - Character Generator RAM (CGRAM): 6,240 bits (40 characters x 12 x 13 dots)
  - Display Data RAM (DDRAM): 640 bits (80 half-size characters or 40 full-size characters)
  - Segment/Icon RAM (SGRAM/ICONRAM): 480 bits (160 mono-blinking icon + 40 gray- scale icon)
- MPU Interface
  - 8-bit parallel interface mode: 68-series and 80-series
  - 4-bit parallel interface mode: 68-series and 80-series
  - Serial interface mode: 3-pin clock synchronous serial interface
- Function Set
  - Font attribute
  - Character/line cursor
  - Full screen reversal
  - Combined display (super-imposed display) of kanji characters and bitmap graphics
  - Partial display
  - Vertical scroll (dot unit)
  - COM / SEG bi-directions (4-type LCD application available)
  - H/W reset (RESETB)
- I/O Peripheral Support
  - Up to 4*8(32key) key matrix (only serial interface)
  - Three general output ports
  - One interrupt source
- Build-In Analog Circuit
  - Internal RC OSC circuit or external clock
  - Electronic-volume for contrast control (32 steps)
  - Voltage converter (1 to 4 times)
  - Voltage follower & bias circuit
- Operating Voltage Range
  - Power voltage (VCC): 2.0V - 3.6V
  - LCD driving voltage (VLCD = V1 - VSS): 4.5V - 12V (max.)
- Low-Power Operating
  - Single, double, triple, or quadruple booster for LCD voltage
  - Amplifier for low-power LCD driving supply and bleeder-resistors incorporated
  - Power saving functions: standby and sleep modes
  - Wake-up function: key scan interrupt
  - Multiple duty selection
  - Programmable LCD duty ratios and bias values
- Display Capability
  - Text mode (4-line 10-character or 20 half-size characters) + 200 icons
  - Graphical mode (120x52 graphics display) + 200 icons
  - Super-imposed mode (Text mode + Graphical mode)
  - Icon is consisted of 160 mono-blinking icons + 40 gray-scale icons
- Applicable Duty Ratios

Display Size(NL)	Duty	Contents of Outputs
0 line(000)	2	Icon
1 line(001)	15	Icon + 1*10 full-size characters (120*13 dot-matrix)
2 line(010)	28	Icon + 2*10 full-size characters (120*26 dot-matrix)
3 line(011)	41	Icon + 3*10 full-size characters (120*39 dot-matrix)
4 line(100)	54	Icon + 4*10 full-size characters (120*52 dot-matrix)

- Applicable Character/Pixel Per Line

Character/Pixel	NC
6 full-size character/72 pixel	00
8 full-size character/96 pixel	01
10 full-size character/120 pixel	10

4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
IM2 - 0	2 - 4	I	Interface mode, 80/68/serial; 8/4, please refer below table on next section
OPOFF	5	I	Voltage follower(V1-V5 OP) off VDD: disable internal OP VSS: enable internal OP
TEST	6	I	Test pin, please leave it open
DB7/KIN7 DB6/KIN6 DB5/KIN5 DB4/KIN4 DB3/KIN3 DB2/KIN2 DB1/KIN1 DB0/KIN0	15 16 17 18 19 20 21 22	I/O	**Parallel interface:** Data bus **Serial interface:** Key scan bus
RESETB	23	I	System reset signal, low active
CSB	24	I	Chip select, low active
RS	25	I	**Parallel interface:** Register select **Serial interface:** 32-key wakeup enable
E/WRB/SCL	26	I	68enable/80wrb/serial CLK
RW/RDB/SDA	27	I/O	68rw/80rdb/serial data
OSC1	33	I	Test pin, please leave it open
OSC2	32	I	Test pin, please leave it open
VTEST1	61	I	Tied to VSS
VTEST2	62	-	Test pin, please leave it open
VTEST3*	63	I	Tied to VSS
PORT2 - 0	7 - 9	O	Port2 - 0 are general digital output
IRQB	10	O	Interrupt request when key was pressed, low active
KST3 - 0	11 - 14	O	Key strobe signal (key scan cycle: internal CLK divided by 64,128,256,512)
COMS2/S1 COMS1/S2	92 245	O	Common output signals for icon(such as battery, antenna, status icon)
COM7/46 - COM26/27 COM47/6 - COM52/1 COM46/7 - COM42/11 COM41/12 - COM35/18 COM34/19 - COM31/22 COM30/23 - COM28/25 COM27/26 COM6/COM47 COM5/COM48 COM4/49 - COM1/52	65 - 85 86 - 91 213 - 217 219 - 226 228 - 231 233 - 235 237 238 239 241 - 244	O	Common output signals for character/graphics
SEG120/1 - SEG1/120	212 - 93	O	Segment output signals for segment-icon display and character/graphics display.
VCI	37, 38	-	Power supply to the booster, if VCI short with VDD, **do not use ITO to short <VDD,VCI>** , please short it on FPC metal line or PCB trace, <VSS,VDD> need 0.1μ capacitor placed to IC as close as possible.

Mnemonic	PIN No.	Type	Description
VDD (VCC)	34, 35	-	Power supply for logic, if VCI short with VDD, **do not use ITO to short <VDD,VCI>** , please short it on FPC metal line or PCB trace, **<VSS,VDD>** need **0.1μ capacitor** placed to IC as close as possible.
VSS VSSP	28, 29 30, 31	I	Ground pin, **do not use ITO to short <VSS,VSSP>**, please short it on FPC metal line or PCB trace, **<VSS,VDD>** need **0.1μ capacitor** placed to IC as close as possible.
VLCD	54, 55	-	Power supply for LCD driver. **<VLCD,VSS>** need **0.1μ capacitor** placed to IC as close as possible.
V5 - 1	60 - 56	I/O	Using capacitor to stabilize the output or supply voltage externally.
VLOUT	52, 53	-	Booster output. **<VLOUT,VSS>** need **0.1μ capacitor** placed to IC as close as possible.
C1+	48, 49	Booster capacitance	External capacitance should be connected when booster works at 2X/3X/4X.
C1-	50, 51	Booster capacitance	External capacitance should be connected when booster works at 2X/3X/4X.
C2+	44, 45	Booster capacitance	External capacitance should be connected when booster works at 3X/4X.
C2-	46, 47	Booster capacitance	External capacitance should be connected when booster works at 3X/4X.
C3+	40, 41	Booster capacitance	External capacitance should be connected when booster works at 4X.
C3-	42, 43	Booster capacitance	External capacitance should be connected when booster works at 4X.
VDDDUM1 – 2	240, 74	Dummy	Dummy for default mode setting
VSSDUM1 – 2	1, 64	Dummy	Dummy for default mode setting
TI3 TI2 TI1 TI0 SE	236 232 227 223 218	Test pin	Test pin, please leave it open
XFUSE1, XFUSE0	36, 39	Test pin	Test pin, please leave it open

4.1. Code information

Sunplus provide multi-lingual character, below is some example.

Code #	Description	Status
002	Simplified Chinese	ES
003	Japanese Kanji	Production
004	Traditional Chinese	ES
005	Korean	ES
xxx	Unicode database of 30,000 characters	ES

5. FUNCTIONAL DESCRIPTIONS

5.1. System Interface

The SPLC701B provides five types of MPU interface:

1). Three-pin clock-synchronized serial interface

2). Motorola 68-system 4-bit

3). Motorola 68-system 8-bit

4). Intel 80-system 4-bit

5). Intel 80-system 8-bit

The interface mode is selected by the IM[2-0] pins.

IM2	IM1	MPU Interface Mode
0	0	Clock-synchronized serial interface
0	1	68-system bus interface
1	0	Inhibited
1	1	80-system bus interface

Serial:

When two SPLC701B share the same csb, scl, sda bus, the two panel is identified by whether IM0 equal start byte ID bit.

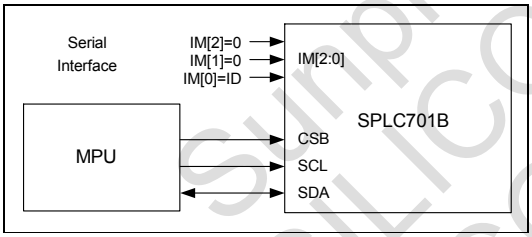
IM0	Start Byte
0	01110-**0**
1	01110-**1**

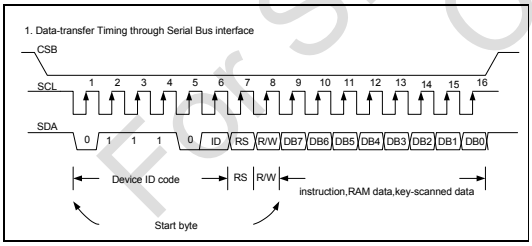
Parallel:

Bus width selection:

IM0	Bus Width Selection
0	8-bit
1	4-bit

5.2. Serial Interface





Setting the IM1 and IM2 pins (interface mode pins) to the GND level allows standard clock-synchronized serial data transfer, using the chip select line (CSB), serial data line (SDA), and serial transfer clock line (SCL). For a serial interface, the IM0/ID pin function uses an ID pin.

The SPLC701B initiates serial data transfer by transferring the start byte at the falling edge of CSB input. It ends serial data transfer at the rising edge of CSB input. The SPLC701B is selected when the 6-bit chip address in the start byte transferred from the transmitting device matches the 6-bit device identification code assigned to the SPLC701B. The SPLC701B, when selected, receives the subsequent data string. The least significant bit of the identification code can be determined by the ID pin. The five upper bits must be 01110. The seventh bit of the start byte is used as a register select bit (RS): that is, when RS = 0, an instruction can be issued or key scan data can be read, and when RS = 1, data can be written to or read from RAM. Read or write is selected according to the eighth bit of the start byte (R/W bit) as shown in below table. After receiving the start byte, the SPLC701B receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first. Two bytes of RAM read data after the start byte are invalid. The SPLC701B starts to read correct RAM data from the third byte.

Register Selection by RS and R/W Bits.

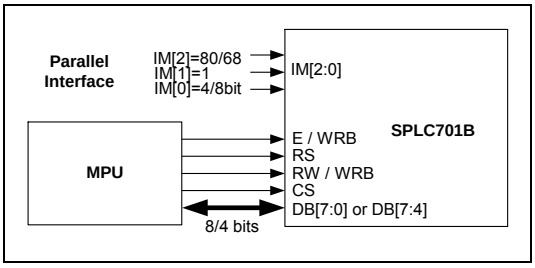
RS	RW	Description
0	0	Write to the Index Register (IR)
0	1	Parallel: Read the Status Register; Serial: Key Scan Data Register(SR)
1	0	Write to the control registers: RAM Address Register, and RAM-Write-Data-Register(WD)
1	1	Read the RAM-Read-Data-Register(RD)

Note1: Key scan interface is available for serial interface only.

Note2: In bus mode, RS and RW are pin input; in serial mode, RS and RW are embedded in the start byte.

Note3: Every time you want to access R15 - 0, make sure IR is correctly point to it.

5.3. Parallel Interface



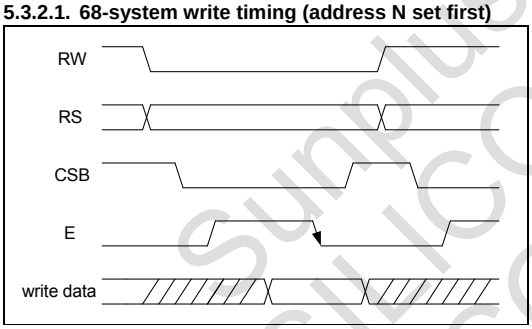
5.3.1. 8-bit interface

Setting the IM2/1/0 (interface mode) to the GND/VCC/GND level allows E-clock-synchronized 8-bit parallel data transfer. Setting the IM2/1/0 (interface mode) to the VCC/VCC/GND level allows 80-system 8-bit parallel data transfer. When the number of buses or the mounting area is limited, use a 4-bit bus interface or serial data transfer. Using a parallel bus interface disables the key scan function. To prevent this, use a clock-synchronized serial interface.

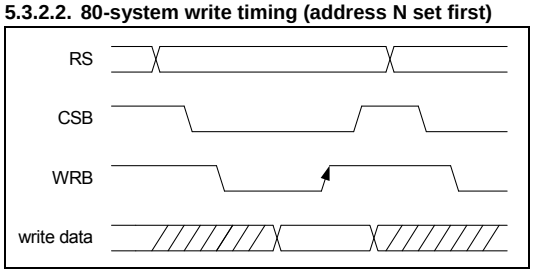
5.3.2. 4-bit interface

Setting the IM2/1/0 (interface mode) to the GND/VCC/VCC level allows E-clock-synchronized 4-bit parallel data transfer using pins DB7/KIN7-DB4/KIN4. Setting the IM2/1/0 (interface mode) to the VCC/VCC/VCC level allows 80-system 4-bit parallel data transfer. 8-bit instructions and RAM data are divided into upper/lower nibbles and the transfer starts from the upper nibble.

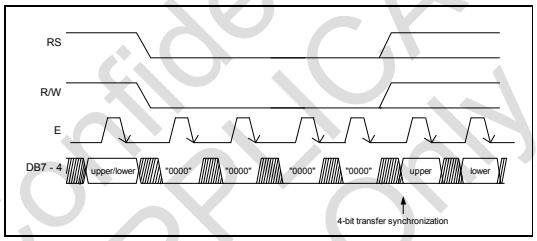
5.3.2.1. 68-system write timing (address N set first)



5.3.2.2. 80-system write timing (address N set first)



The SPLC701B supports the transfer synchronization function which resets the upper/lower counter to count upper/lower 4-bit data transfer in the 4-bit bus interface. Noise causing transfer mismatch between the upper and lower nibbles can be corrected by a reset triggered by consecutively writing a 0000 instruction four times. The next transfer starts from the upper nibble. Executing synchronization function periodically can recover any runaway in the display system.



4-bit Transfer Synchronization

5.4. Control Register

The SPLC701B contains five types of registers:

Name	Description
IR(Index Register)	Specify the index address of the register to be accessed.
SR(Status/ Scan Register)	Parallel: busy flag, LCD scan status Serial: key scan data
CR(Control Register)	Clear display Start oscillation Driver output control LCD drive waveform LCD drive control Power control Key scan cycle / IRQ enable / General Output Entry mode Cursor control Display control Scroll control Half-size font bank selection Half-size font attribute selection

Name	Description
AR(Address Register)	Address for internal SRAM Auto up/down count when access
DR(Data Register)	Data register for internal SRAM WD: data written to WD is automatically written into internal SRAM RD: Data is read and temporarily latch in RD

Execution time for instructions (excluding display cleared) is zero clock cycle and instructions can be written consecutively. Data written into the WD from MPU is also automatically written into the DDRAM, CGRAM, or SGRAM. Data is read and temporarily latched in the RD while reading from the RAM. Also, the first read data is invalid and the second data is normal. After reading, data in the DDRAM, CGRAM, or SGRAM at the next address is sent to the RD for the next reading from the MPU.

5.5. Key Scan Registers (Scan0 to Scan3)

The key matrix scanner senses and holds the key states at each rising edge of the key strobe signals that are output by the SPLC701B. The key strobe signals are output as time-multiplexed signals from KST0 to KST3. After passing through the key matrix, these strobe signals are used to sample the key status on eight inputs from KIN0 to KIN7, enabling up to 32 keys to be scanned. The states of inputs, KIN0 to KIN7, are sampled by key strobe signal KST0 and latched into register, SCAN0.

Similarly, the data sampled by strobe signals, KST1 to KST3, is latched into registers, SCAN1 to SCAN3, respectively. **Software should read twice to forth time to determine a valid key, and the read cycle must be greater than key-scan cycle.**

5.6. General Output Ports (Port2 - 0)

The SPLC701B contains three general output ports. These ports are unable to drive currents, such as, for LED or back-light. An external transistor is a must for current boosting.

5.7. Address Counter (AC)

The Address Counter (AC) assigns addresses to the DDRAM, CGRAM, or SGRAM. When an address is written into RAM Address Register, the address information is sent to the AC. Selection of the DDRAM, CGRAM, and SGRAM is also determined concurrently by the RAM selected bit (RM1/0). After writing data into DDRAM, CGRAM, or SGRAM, the AC is automatically incremented by 1 (or decremented by 1). After reading the data, the AC is automatically updated or not updated by the RDM bit.

The cursor display position is determined by the address counter value.

1	2	3	4	5	6	7	8	9	10	11	12	Display position
00	01	02	03	04	05	06	07	08	09	0A	0B	DDRAM address

(AC = 02)

Note: The cursor/blink or black-white reversed control is also active when the address counter indicates the CGRAM or SGRAM.

5.8. Display Data RAM (DDRAM)

Display data RAM (DDRAM) stores display data represented in 8-bit character codes in the character display mode. Its capacity is 80 x 8 bits, or 80 characters, which is equivalent to an area of 10 characters x 4 lines. Any number of display lines (LCD drive duty ratio) from 1 to 4 can be selected by software. Here, assignment of DDRAM addresses is identical to all display modes. The displayed line at the top of the display (display-start-line) can also be selected through register's setting. The graphical display mode does not use data in the DDRAM.

5.9. Full-Size Character Generator ROM (FCGROM)

Full-size character generator ROM (FCGROM) generates 11 x 12-dot character patterns from 13-bit character codes. It is equipped with 8,128 full-size font patterns such as the JIS Level-1 and Level-2 Kanji Set or non-Kanji Set. The 11*12 font is displayed within 12*13 area.

5.10. Half-Size Character Generator ROM (HCGROM)

Half-size character generator ROM (HCGROM) generates 5 x 12-dot character patterns from 7-bit character codes. It is formed with two banks of 128 half-size font patterns and 256 half-size fonts in total. The 5*12 font is displayed within 6*13 area.

5.11. Booster (DC-DC Converter)

The booster doubles, triples, or quadruples a voltage input to the Vci pin. With this, both the internal logic units and LCD drivers can be controlled with a single power supply. Boost output level from single to quadruple boost can be programmed by software.

5.12. Cursor/Blink Controller

The cursor / blink (or black-white reversed) control is used to create a cursor or a flashing area on the display in a position corresponding to the location stored in the Address Counter (AC).

5.13. Character Generator RAM (CGRAM)

In text mode, character generator RAM (CGRAM) allows users to redefine the character patterns in the character display mode.