SPLC780D
16COM/40SEG Controller/Driver

Preliminary
AUG. 06, 2003
Version 0.1
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1. GENERAL DESCRIPTION

The SPLC780D, a dot-matrix LCD controller and driver from SUNPLUS, is a unique design for displaying alpha-numeric, Japanese-Kana characters and symbols. The SPLC780D provides two types of interfaces to MPU: 4-bit and 8-bit interfaces. The transferring speed of 8-bit is twice faster than 4-bit. A single SPLC780D is able to display up to two 8-character lines. By cascading with SPLC100 or SPLC063, the display capability can be extended. The CMOS technology ensures the power saves in the most efficient way and the performance keeps in the highest rank.

2. FEATURES

- Character generator ROM: 10880 bits
  - Character font 5 x 8 dots: 192 characters
  - Character font 5 x 10 dots: 64 characters
- Character generator RAM: 512 bits
  - Character font 5 x 8 dots: 8 characters
  - Character font 5 x 10 dots: 4 characters
- 4-bit or 8-bit MPU interfaces
- Direct driver for LCD: 16 COMs x 40 SEGs
- Duty factor (selected by program):
  - 1/8 duty: 1 line of 5 x 8 dots
  - 1/11 duty: 1 line of 5 x 10 dots
  - 1/16 duty: 2 lines of 5 x 8 dots / line
- Built-in power on automatic reset circuit
- Built-in oscillator circuit (with external resistor)
- Support external clock operation
- Low Power Consumption
- Package form: 80 QFP or bare chip available

3. BLOCK DIAGRAM

[Diagram of the SPLC780D's block diagram showing the various components and their connections.]
4. SIGNAL DESCRIPTIONS

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>PIN No.</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>33</td>
<td>I</td>
<td>Power input</td>
</tr>
<tr>
<td>VSS</td>
<td>23</td>
<td>I</td>
<td>Ground</td>
</tr>
<tr>
<td>OSC1</td>
<td>24</td>
<td>-</td>
<td>Both OSC1 and OSC2 are connected to resistor for internal oscillator circuit. For external clock operation, the clock is input to OSC1.</td>
</tr>
<tr>
<td>OSC2</td>
<td>25</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V1 - V5</td>
<td>26 - 30</td>
<td>I</td>
<td>Supply voltage for LCD driving.</td>
</tr>
<tr>
<td>E</td>
<td>38</td>
<td>I</td>
<td>A start signal for reading or writing data.</td>
</tr>
<tr>
<td>RW</td>
<td>37</td>
<td>I</td>
<td>A signal for selecting read or write actions. 1: Read, 0: Write.</td>
</tr>
<tr>
<td>RS</td>
<td>36</td>
<td>I</td>
<td>A signal for selecting registers. 1: Data Register (for read and write) 0: Instruction Register (for write), Busy flag - Address Counter (for read).</td>
</tr>
<tr>
<td>DB0 - DB3</td>
<td>39 - 42</td>
<td>I/O</td>
<td>Low 4-bit data</td>
</tr>
<tr>
<td>DB4 - DB7</td>
<td>43 - 46</td>
<td>I/O</td>
<td>High 4-bit data</td>
</tr>
<tr>
<td>CL1</td>
<td>31</td>
<td>O</td>
<td>Clock to latch serial data D.</td>
</tr>
<tr>
<td>CL2</td>
<td>32</td>
<td>O</td>
<td>Clock to shift serial data D.</td>
</tr>
<tr>
<td>M</td>
<td>34</td>
<td>O</td>
<td>Switch signal to convert LCD waveform to AC.</td>
</tr>
<tr>
<td>D</td>
<td>35</td>
<td>O</td>
<td>Sends character pattern data corresponding to each common signal serially. 1: Selection, 0: Non-selection.</td>
</tr>
<tr>
<td>SEG1 - SEG22</td>
<td>22 - 1</td>
<td>O</td>
<td>Segment signals for LCD.</td>
</tr>
<tr>
<td>SEG23 - SEG40</td>
<td>80 - 63</td>
<td></td>
<td></td>
</tr>
<tr>
<td>COM1 - COM16</td>
<td>47 - 62</td>
<td>O</td>
<td>Common signals for LCD.</td>
</tr>
</tbody>
</table>

4.1. Ordering Information

<table>
<thead>
<tr>
<th>Product Number</th>
<th>Package Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPLC780D-NnnV-C</td>
<td>Chip form</td>
</tr>
<tr>
<td>SPLC780D-NnnV-PQ05</td>
<td>Package form - QFP 80L</td>
</tr>
</tbody>
</table>

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).
5. FUNCTIONAL DESCRIPTIONS

5.1. Oscillator

SPLC780D oscillator supports not only the internal oscillator operation, but also the external clock operation.

5.2. Control and Display Instructions

Control and display instructions are described in details as follows:

5.2.1. Clear display

It clears the entire display and sets Display Data RAM Address 0 in Address Counter.

5.2.2. Return home

X: Do not care (0 or 1)

It sets Display Data RAM Address 0 in Address Counter and the display returns to its original position. The cursor or blink goes to the most-left side of the display (to the 1st line if 2 lines are displayed). The contents of the Display Data RAM do not change.

5.2.3. Entry mode set

During writing and reading data, it defines cursor moving direction and shifts the display.

<table>
<thead>
<tr>
<th>Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>000000001</td>
<td>I / D = 1: Increment, I / D = 0: Decrement.</td>
</tr>
<tr>
<td>S = 1: The display shift, S = 0: The display does not shift.</td>
<td></td>
</tr>
</tbody>
</table>

5.2.4. Display ON/OFF control

<table>
<thead>
<tr>
<th>Code</th>
<th>RS</th>
<th>R/W</th>
<th>DB7</th>
<th>DB6</th>
<th>DB5</th>
<th>DB4</th>
<th>DB3</th>
<th>DB2</th>
<th>DB1</th>
<th>DB0</th>
</tr>
</thead>
<tbody>
<tr>
<td>000000001</td>
<td>D = 1: Display on, D = 0: Display off</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C = 1: Cursor on, C = 0: Cursor off</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B = 1: Blinks on, B = 0: Blinks off</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

5.2.5. Cursor or display shift

Without changing DD RAM data, it moves cursor and shifts display.

<table>
<thead>
<tr>
<th>Code</th>
<th>RS</th>
<th>R/W</th>
<th>DB7</th>
<th>DB6</th>
<th>DB5</th>
<th>DB4</th>
<th>DB3</th>
<th>DB2</th>
<th>DB1</th>
<th>DB0</th>
</tr>
</thead>
<tbody>
<tr>
<td>000000001</td>
<td>S/C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R/L</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Blink display alternately

<table>
<thead>
<tr>
<th>S/C</th>
<th>R/L</th>
<th>Description</th>
<th>Address Counter</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Shift cursor to the left</td>
<td>AC = AC - 1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Shift cursor to the right</td>
<td>AC = AC + 1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Shift display to the left. Cursor follows the display shift</td>
<td>AC = AC</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Shift display to the right. Cursor follows the display shift</td>
<td>AC = AC</td>
</tr>
</tbody>
</table>
5.2.6. Function set

<table>
<thead>
<tr>
<th>Code</th>
<th>RS</th>
<th>R/W</th>
<th>DB7</th>
<th>DB6</th>
<th>DB5</th>
<th>DB4</th>
<th>DB3</th>
<th>DB2</th>
<th>DB1</th>
<th>DB0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>DL</td>
<td>N</td>
<td>F</td>
<td>X</td>
<td></td>
</tr>
</tbody>
</table>

X: Do not care (0 or 1)

DL: It sets interface data length.
   DL = 1: Data transferred with 8-bit length (DB7 - 0).
   DL = 0: Data transferred with 4-bit length (DB7 - 4).

It requires two times to accomplish data transferring.

N: It sets the number of the display line.
   N = 0: One-line display.
   N = 1: Two-line display.

F: It sets the character font.
   F = 0: 5 x 8 dots character font.
   F = 1: 5 x 10 dots character font.

<table>
<thead>
<tr>
<th>N</th>
<th>F</th>
<th>No. of Display Lines</th>
<th>Character Font</th>
<th>Duty Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>5 x 8 dots</td>
<td>1 / 8</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>5 x 10 dots</td>
<td>1 / 11</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>2</td>
<td>5 x 8 dots</td>
<td>1 / 16</td>
</tr>
</tbody>
</table>

It cannot display two lines with 5 x 10 dots character font.

5.2.7. Set character generator RAM address

<table>
<thead>
<tr>
<th>Code</th>
<th>RS</th>
<th>R/W</th>
<th>DB7</th>
<th>DB6</th>
<th>DB5</th>
<th>DB4</th>
<th>DB3</th>
<th>DB2</th>
<th>DB1</th>
<th>DB0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>a</td>
<td>a</td>
<td>a</td>
<td>a</td>
<td>a</td>
<td>a</td>
</tr>
</tbody>
</table>

It sets Character Generator RAM Address (aaaaaa)\textsubscript{16} to the Address Counter.

Character Generator RAM data can be read or written after this setting.

5.2.8. Set display data RAM address

<table>
<thead>
<tr>
<th>Code</th>
<th>RS</th>
<th>R/W</th>
<th>DB7</th>
<th>DB6</th>
<th>DB5</th>
<th>DB4</th>
<th>DB3</th>
<th>DB2</th>
<th>DB1</th>
<th>DB0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>a</td>
<td>a</td>
<td>a</td>
<td>a</td>
<td>a</td>
<td>a</td>
<td>a</td>
<td>a</td>
</tr>
</tbody>
</table>

It sets Display Data RAM Address (aaaaaa)\textsubscript{16} to the Address Counter.

Display data RAM can be read or written after this setting.

In one-line display (N = 0),

\[(aaaaaa)_{16}: (00)_{16} \cdot (4F)_{16} .\]

In two-line display (N = 1),

\[(aaaaaa)_{16}: (00)_{16} \cdot (27)_{16} \text{ for the first line},
(aaaaaa)_{16}: (40)_{16} \cdot (67)_{16} \text{ for the second line} .\]

5.2.9. Read busy flag and address

<table>
<thead>
<tr>
<th>Code</th>
<th>RS</th>
<th>R/W</th>
<th>DB7</th>
<th>DB6</th>
<th>DB5</th>
<th>DB4</th>
<th>DB3</th>
<th>DB2</th>
<th>DB1</th>
<th>DB0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>BF</td>
<td>a</td>
<td>a</td>
<td>a</td>
<td>a</td>
<td>a</td>
<td>a</td>
<td>a</td>
</tr>
</tbody>
</table>

When BF = 1, it indicates the system is busy now and it will not accept any instruction until not busy (BF = 0). At the same time, the content of Address Counter (aaaaaa)\textsubscript{16} is read.

5.2.10. Write data to character generator RAM or display data RAM

<table>
<thead>
<tr>
<th>Code</th>
<th>RS</th>
<th>R/W</th>
<th>DB7</th>
<th>DB6</th>
<th>DB5</th>
<th>DB4</th>
<th>DB3</th>
<th>DB2</th>
<th>DB1</th>
<th>DB0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>d</td>
<td>d</td>
<td>d</td>
<td>d</td>
<td>d</td>
<td>d</td>
<td>d</td>
<td>d</td>
</tr>
</tbody>
</table>

It writes data (dddddddd)\textsubscript{16} to character generator RAM or display data RAM.

5.2.11. Read data from character generator RAM or display data RAM

<table>
<thead>
<tr>
<th>Code</th>
<th>RS</th>
<th>R/W</th>
<th>DB7</th>
<th>DB6</th>
<th>DB5</th>
<th>DB4</th>
<th>DB3</th>
<th>DB2</th>
<th>DB1</th>
<th>DB0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>d</td>
<td>d</td>
<td>d</td>
<td>d</td>
<td>d</td>
<td>d</td>
<td>d</td>
<td>d</td>
</tr>
</tbody>
</table>

It reads data (dddddddd)\textsubscript{16} from character generator RAM or display data RAM.

To read data correctly, do the following:
1. The address of the Character Generator RAM or Display Data RAM or shift the cursor instruction.
2. The “Read” instruction.
### 5.3. Instruction Table

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Instruction Code</th>
<th>Description</th>
<th>Execution time (fosc=270KHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clear Display</td>
<td>0 0 0 0 0 0 0 0 1</td>
<td>Write “20H” to DDRAM and set DDRAM address to “00H” from AC</td>
<td>1.52ms</td>
</tr>
<tr>
<td>Return Home</td>
<td>0 0 0 0 0 0 0 0 1</td>
<td>Set DDRAM address to “00H” from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.</td>
<td>1.52ms</td>
</tr>
<tr>
<td>Entry Mode Set</td>
<td>0 0 0 0 0 0 0 0 1</td>
<td>Assign cursor moving direction and enable the shift of entire display</td>
<td>38µs</td>
</tr>
<tr>
<td>Display ON/OFF Control</td>
<td>0 0 0 0 0 0 1</td>
<td>Set display(D), cursor(C), and blinking of cursor(B) on/off control bit.</td>
<td>38µs</td>
</tr>
<tr>
<td>Cursor or Display Shift</td>
<td>0 0 0 0 0 1</td>
<td>Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.</td>
<td>38µs</td>
</tr>
<tr>
<td>Function Set</td>
<td>0 0 0 0 1</td>
<td>Set interface data length (DL: 8-bit/4-bit), numbers of display line (N: 2-line/1-line) and, display font type (F:5x10 dots/5x8 dots)</td>
<td>38µs</td>
</tr>
<tr>
<td>Set CGRAM Address</td>
<td>0 0 0 1 AC5 AC4 AC3 AC2 AC1 AC0</td>
<td>Set CGRAM address in address counter.</td>
<td>38µs</td>
</tr>
<tr>
<td>Set DDRAM Address</td>
<td>0 0 1 AC6 AC5 AC4 AC3 AC2 AC1 AC0</td>
<td>Set DDRAM address in counter</td>
<td>38µs</td>
</tr>
<tr>
<td>Read Busy Flag and Address Counter</td>
<td>0 1 BF AC5 AC4 AC3 AC2 AC1 AC0</td>
<td>Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.</td>
<td>38µs</td>
</tr>
<tr>
<td>Write Data to RAM</td>
<td>1 0 D7 D6 D5 D4 D3 D2 D1 D0</td>
<td>Write data into internal RAM (DDRAM/CGRAM).</td>
<td>38µs</td>
</tr>
<tr>
<td>Read Data from RAM</td>
<td>1 1 D7 D6 D5 D4 D3 D2 D1 D0</td>
<td>Read data from internal RAM (DDRAM/CGRAM).</td>
<td>38µs</td>
</tr>
</tbody>
</table>

**Note:** “-” don’t care
### 5.4. 8-Bit Operation and 8-Digit 1-Line Display (Using Internal Reset)

<table>
<thead>
<tr>
<th>No.</th>
<th>Instruction</th>
<th>Display</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Power on. (SPLC780D starts initializing)</td>
<td></td>
<td>Power on reset. No display.</td>
</tr>
<tr>
<td>2</td>
<td>Function set</td>
<td>RS RW DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0</td>
<td>Set to 8-bit operation and select 1-line display line and character font.</td>
</tr>
<tr>
<td>3</td>
<td>Display on / off control</td>
<td>0 0 0 0 0 0 1 1 1 0</td>
<td>Display on. Cursor appear.</td>
</tr>
<tr>
<td>4</td>
<td>Entry mode set</td>
<td>0 0 0 0 0 0 1 0 1 0</td>
<td>Increase address by one. It will shift the cursor to the right when writing to the DD RAM/CG RAM. Now the display has no shift.</td>
</tr>
<tr>
<td>5</td>
<td>Write data to CG RAM / DD RAM</td>
<td>1 0 0 1 0 1 0 1 1 1</td>
<td>Write &quot; W &quot;. The cursor is incremented by one and shifted to the right.</td>
</tr>
<tr>
<td>6</td>
<td>Write data to CG RAM / DD RAM</td>
<td>1 0 0 1 0 0 0 1 0 1</td>
<td>Write &quot; E &quot;. The cursor is incremented by one and shifted to the right.</td>
</tr>
<tr>
<td>7</td>
<td>:</td>
<td>:</td>
<td>:</td>
</tr>
<tr>
<td>8</td>
<td>Write data to CG RAM / DD RAM</td>
<td>1 0 0 1 0 0 0 1 0 1</td>
<td>Write &quot; E &quot;. The cursor is incremented by one and shifted to the right.</td>
</tr>
<tr>
<td>9</td>
<td>Entry mode set</td>
<td>0 0 0 0 0 0 0 1 1 1</td>
<td>Set mode for display shift when writing</td>
</tr>
<tr>
<td>10</td>
<td>Write data to CG RAM / DD RAM</td>
<td>1 0 0 0 1 0 0 0 0 0</td>
<td>Write &quot; (space). The cursor is incremented by one and shifted to the right.</td>
</tr>
<tr>
<td>11</td>
<td>Write data to CG RAM / DD RAM</td>
<td>1 0 0 1 0 0 0 0 1 1</td>
<td>Write &quot; C &quot;. The cursor is incremented by one and shifted to the right.</td>
</tr>
<tr>
<td>12</td>
<td>:</td>
<td>:</td>
<td>:</td>
</tr>
<tr>
<td>13</td>
<td>Write data to CG RAM / DD RAM</td>
<td>1 0 0 1 0 1 1 0 0 1</td>
<td>Write &quot; Y &quot;. The cursor is incremented by one and shifted to the right.</td>
</tr>
<tr>
<td>14</td>
<td>Cursor or display shift</td>
<td>0 0 0 0 0 0 1 0 0 X X</td>
<td>Only shift the cursor's position to the left (Y).</td>
</tr>
<tr>
<td>15</td>
<td>Cursor or display shift</td>
<td>0 0 0 0 0 0 1 0 0 X X</td>
<td>Only shift the cursor's position to the left (M).</td>
</tr>
<tr>
<td>16</td>
<td>Write data to CG RAM / DD RAM</td>
<td>1 0 0 1 0 0 1 1 1 0</td>
<td>Write &quot; N &quot;. The display moves to the left.</td>
</tr>
<tr>
<td>17</td>
<td>Cursor or display shift</td>
<td>0 0 0 0 0 0 1 1 1 X X</td>
<td>Shift the display and the cursor's position to the right.</td>
</tr>
<tr>
<td>18</td>
<td>Cursor or display shift</td>
<td>0 0 0 0 0 0 1 0 1 X X</td>
<td>Shift the display and the cursor's position to the right.</td>
</tr>
<tr>
<td>19</td>
<td>Write data to CG RAM / DD RAM</td>
<td>1 0 0 1 0 0 0 0 0 0</td>
<td>Write &quot; (space). The cursor is incremented by one and shifted to the right.</td>
</tr>
<tr>
<td>20</td>
<td>:</td>
<td>:</td>
<td>:</td>
</tr>
<tr>
<td>21</td>
<td>Return home</td>
<td>0 0 0 0 0 0 0 0 0 1 0</td>
<td>Both the display and the cursor return to the original position (address 0).</td>
</tr>
</tbody>
</table>
### 5.5. 4-Bit Operation and 8-Digit 1-Line Display (Using Internal Reset)

<table>
<thead>
<tr>
<th>No.</th>
<th>Instruction</th>
<th>Display</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Power on.</td>
<td></td>
<td>Power on reset. No display.</td>
</tr>
<tr>
<td></td>
<td>(SPLC780D starts initializing)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Function set</td>
<td></td>
<td>Set to 4-bit operation.</td>
</tr>
<tr>
<td></td>
<td>RS R/W DB7 DB6 DB5 DB4</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 0 0 0 1 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Function set</td>
<td></td>
<td>Set to 4-bit operation and select 1-line display line and character font.</td>
</tr>
<tr>
<td></td>
<td>RS R/W DB7 DB6 DB5 DB4</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 0 0 0 X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Display on.</td>
<td></td>
<td>Display on.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Cursor appears.</td>
</tr>
<tr>
<td>5</td>
<td>Increase address by one.</td>
<td></td>
<td>Increase address by one.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>It will shift the cursor to the right when writing to the DD RAM / CG RAM.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Now the display has no shift.</td>
</tr>
<tr>
<td>6</td>
<td>Write &quot;W&quot;.</td>
<td>W</td>
<td>The cursor is incremented by one and shifted to the right.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 0 0 1 1 1</td>
<td></td>
</tr>
</tbody>
</table>

### 5.6. 8-Bit Operation and 8-Digit 2-Line Display (Using Internal Reset)

<table>
<thead>
<tr>
<th>No.</th>
<th>Instruction</th>
<th>Display</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Power on.</td>
<td></td>
<td>Power on reset. No display.</td>
</tr>
<tr>
<td></td>
<td>(SPLC780D starts initializing)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Function set</td>
<td></td>
<td>Set to 8-bit operation and select 2-line display line and 5 x 8 dot character font.</td>
</tr>
<tr>
<td></td>
<td>RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 0 0 0 1 1 1 0 X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Display on / off control</td>
<td></td>
<td>Display on.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Cursor appear.</td>
</tr>
<tr>
<td>4</td>
<td>Entry mode set</td>
<td></td>
<td>Increase address by one.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>It will shift the cursor to the right when writing to the DD RAM / CG RAM.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Now the display has no shift.</td>
</tr>
<tr>
<td>5</td>
<td>Write data to CG RAM / DD RAM</td>
<td>W</td>
<td>Write &quot;W&quot;.</td>
</tr>
<tr>
<td></td>
<td>1 0 0 1 0 1 0 1 1 1</td>
<td></td>
<td>The cursor is incremented by one and shifted to the right.</td>
</tr>
<tr>
<td>6</td>
<td>:</td>
<td>:</td>
<td>:</td>
</tr>
<tr>
<td>7</td>
<td>Write data to CG RAM / DD RAM</td>
<td>WELCOME</td>
<td>Write &quot;E&quot;.</td>
</tr>
<tr>
<td></td>
<td>1 0 0 1 0 0 0 1 0 1</td>
<td></td>
<td>The cursor is incremented by one and shifted to the right.</td>
</tr>
<tr>
<td>8</td>
<td>Set DD RAM address</td>
<td>WELCOME</td>
<td>It sets DD RAM's address.</td>
</tr>
<tr>
<td></td>
<td>0 0 1 1 0 0 0 0 0 0</td>
<td></td>
<td>The cursor is moved to the beginning position of the 2nd line.</td>
</tr>
<tr>
<td>9</td>
<td>Write data to CG RAM / DD RAM</td>
<td>WELCOME</td>
<td>Write &quot;T&quot;.</td>
</tr>
<tr>
<td></td>
<td>1 0 0 1 0 1 0 1 0 0</td>
<td></td>
<td>The cursor is incremented by one and shifted to the right.</td>
</tr>
<tr>
<td>10</td>
<td>:</td>
<td>:</td>
<td>:</td>
</tr>
<tr>
<td>11</td>
<td>Write data to CG RAM / DD RAM</td>
<td>WELCOME</td>
<td>Write &quot;T&quot;.</td>
</tr>
<tr>
<td></td>
<td>1 0 0 1 0 1 0 1 0 0</td>
<td></td>
<td>The cursor is incremented by one and shifted to the right.</td>
</tr>
<tr>
<td>No.</td>
<td>Instruction</td>
<td>Display</td>
<td>Operation</td>
</tr>
<tr>
<td>-----</td>
<td>-----------------------------</td>
<td>---------</td>
<td>---------------------------------------------------------------------------</td>
</tr>
<tr>
<td>12</td>
<td>Entry mode set</td>
<td></td>
<td>When writing, it sets mode for the display shift.</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>0 0 0 0 0 0 0 1 1 1</strong></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>Write data to CG RAM / DD RAM</td>
<td></td>
<td>Write &quot;Y&quot;. The cursor is incremented by one and shifted to the right.</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>1 0 0 1 0 1 0 1 0 0 1</strong></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td></td>
<td></td>
<td>Both the display and the cursor return to the original position (address 0).</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>0 0 0 0 0 0 0 0 1 0 0</strong></td>
<td></td>
</tr>
</tbody>
</table>

5.7. Reset Function

At power on, SPLC780D starts the internal auto-reset circuit and executes the initial instructions. The initial procedures are shown as follows:

```
<table>
<thead>
<tr>
<th>Power On</th>
<th>Wait time &gt; 15 ms after VDD &gt; 4.5V</th>
</tr>
</thead>
<tbody>
<tr>
<td>RS R/W</td>
<td>DB7 DB6 DB5 DB4 DB3 DB1 DB0</td>
</tr>
<tr>
<td>0 0 0 0 0 1 1 X X X X</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Wait time &gt; 4.1 ms</th>
</tr>
</thead>
<tbody>
<tr>
<td>RS R/W</td>
</tr>
<tr>
<td>0 0 0 0 1 1 X X X X</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Wait time &gt; 100 us</th>
</tr>
</thead>
<tbody>
<tr>
<td>RS R/W</td>
</tr>
<tr>
<td>0 0 0 0 1 1 X X X X</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Initialization Ends</th>
</tr>
</thead>
<tbody>
<tr>
<td>RS R/W</td>
</tr>
<tr>
<td>0 0 0 0 0 0 1 0 0 0</td>
</tr>
<tr>
<td>0 0 0 0 0 0 0 0 0 0 1</td>
</tr>
</tbody>
</table>
```

[ 8-Bit Interface ]

- Wait time > 40ms After VDD > 2.7V
- BF cannot be checked before this instruction.
  - Function set ( Interface is 8 bits length. )
- BF cannot be checked before this instruction.
  - Function set ( Interface is 8 bits length. )
- BF cannot be checked before this instruction.
  - Function set ( Interface is 8 bits length. )
- BF can be checked after the following instructions.
  - Function set ( Interface is 8 bits length. Specify the number of display lines and character font. )
  - The number of display lines and character font cannot be changed afterwards.
    - Display off
    - Display clear
    - Entry mode set
Power On

Wait time > 15 ms after VDD > 4.5V

RS  R/W  DB7  DB6  DB5  DB4
0   0 0    0       1       1

Wait time > 4.1 ms

RS  R/W  DB7  DB6  DB5  DB4
0   0 0    0       1       1

Wait time > 100 us

RS  R/W  DB7  DB6  DB5  DB4
0   0 0    0       1       1

[ 4-Bit Interface ]

Wait time > 40ms After VDD > 2.7V

BF cannot be checked before this instruction.
Function set ( Interface is 8 bits length .)

BF cannot be checked before this instruction.
Function set ( Interface is 8 bits length .)

BF cannot be checked before this instruction.
Function set ( Interface is 8 bits length .)

BF can be checked after the following instructions .
Function set ( Set interface to be 4 bits length) Interface is 8 bits length .
Function set ( Interface is 4 bits length .
Specify the number of the display lines and character font .)

The number of display lines and character font cannot be changed afterwards .

Display off
Display clear
Entry mode set
5.8. Display Data RAM (DD RAM)
The 80-bit DD RAM is normally used for storing display data. Those DD RAM not used for display data can be used as general data RAM. Its address is configured in the Address Counter. The relationships between Display Data RAM Address and LCD's position are depicted as follows.

![Diagram of Display Data RAM Address and LCD Position]

When the display shift operation is performed, the display data RAM's address moves as:

(i) Left shift

| 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 |

(ii) Right shift

| 4F | 00 | 01 | 02 | 03 | 04 | 05 | 06 |

5.9. Timing Generation Circuit
The timing generating circuit is able to generate timing signals to the internal circuits. In order to prevent the internal timing interface, the MPU access timing and the RAM access timing are generated independently.

5.10. LCD Driver Circuit
Total of 16 commons and 40 segments signal drivers are valid in the LCD driver circuit. When a program specifies the character fonts and line numbers, the corresponding common signals output drive-waveforms and the others still output unselected waveforms.

5.11. Character Generator ROM (CG ROM)
Using 8-bit character code, the character generator ROM generates 5 x 8 dots or 5 x 10 dots character patterns. It also can generate 192's 5 x 8 dots character patterns and 64's 5 x 10 dots character patterns.

5.12. Character Generator RAM (CG RAM)
Users can easily change the character patterns in the character generator RAM through program. It can be written to 5 x 8 dots, 8-character patterns or 5 x 10 dots for 4-character patterns.
The following diagram shows the SPLC780D character patterns:
Correspondence between Character Codes and Character Patterns.

<table>
<thead>
<tr>
<th>Character Code</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>CG RAM (1)</td>
<td>CG RAM (1)</td>
<td>CG RAM (1)</td>
<td>CG RAM (1)</td>
<td>CG RAM (1)</td>
<td>CG RAM (1)</td>
<td>CG RAM (1)</td>
<td>CG RAM (1)</td>
<td>CG RAM (1)</td>
<td>CG RAM (1)</td>
<td>CG RAM (1)</td>
<td>CG RAM (1)</td>
<td>CG RAM (1)</td>
<td>CG RAM (1)</td>
<td>CG RAM (1)</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>CG RAM (2)</td>
<td>CG RAM (2)</td>
<td>CG RAM (2)</td>
<td>CG RAM (2)</td>
<td>CG RAM (2)</td>
<td>CG RAM (2)</td>
<td>CG RAM (2)</td>
<td>CG RAM (2)</td>
<td>CG RAM (2)</td>
<td>CG RAM (2)</td>
<td>CG RAM (2)</td>
<td>CG RAM (2)</td>
<td>CG RAM (2)</td>
<td>CG RAM (2)</td>
<td>CG RAM (2)</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>CG RAM (3)</td>
<td>CG RAM (3)</td>
<td>CG RAM (3)</td>
<td>CG RAM (3)</td>
<td>CG RAM (3)</td>
<td>CG RAM (3)</td>
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<td>CG RAM (3)</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>CG RAM (4)</td>
<td>CG RAM (4)</td>
<td>CG RAM (4)</td>
<td>CG RAM (4)</td>
<td>CG RAM (4)</td>
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<td>CG RAM (4)</td>
<td>CG RAM (4)</td>
<td>CG RAM (4)</td>
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</tr>
<tr>
<td>4</td>
<td>CG RAM (5)</td>
<td>CG RAM (5)</td>
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<td>CG RAM (5)</td>
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<td>5</td>
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</tr>
<tr>
<td>6</td>
<td>CG RAM (7)</td>
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<td>CG RAM (7)</td>
<td>CG RAM (7)</td>
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</tr>
<tr>
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</tr>
<tr>
<td>8</td>
<td>CG RAM (9)</td>
<td>CG RAM (9)</td>
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</tr>
<tr>
<td>9</td>
<td>CG RAM (10)</td>
<td>CG RAM (10)</td>
<td>CG RAM (10)</td>
<td>CG RAM (10)</td>
<td>CG RAM (10)</td>
<td>CG RAM (10)</td>
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<td>CG RAM (10)</td>
<td>CG RAM (10)</td>
<td>CG RAM (10)</td>
<td>CG RAM (10)</td>
<td></td>
</tr>
<tr>
<td>C</td>
<td>CG RAM (13)</td>
<td>CG RAM (13)</td>
<td>CG RAM (13)</td>
<td>CG RAM (13)</td>
<td>CG RAM (13)</td>
<td>CG RAM (13)</td>
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<td>CG RAM (13)</td>
<td>CG RAM (13)</td>
<td>CG RAM (13)</td>
<td>CG RAM (13)</td>
<td>CG RAM (13)</td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>CG RAM (14)</td>
<td>CG RAM (14)</td>
<td>CG RAM (14)</td>
<td>CG RAM (14)</td>
<td>CG RAM (14)</td>
<td>CG RAM (14)</td>
<td>CG RAM (14)</td>
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<td>CG RAM (14)</td>
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<td>CG RAM (14)</td>
<td>CG RAM (14)</td>
<td>CG RAM (14)</td>
<td>CG RAM (14)</td>
<td>CG RAM (14)</td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>CG RAM (15)</td>
<td>CG RAM (15)</td>
<td>CG RAM (15)</td>
<td>CG RAM (15)</td>
<td>CG RAM (15)</td>
<td>CG RAM (15)</td>
<td>CG RAM (15)</td>
<td>CG RAM (15)</td>
<td>CG RAM (15)</td>
<td>CG RAM (15)</td>
<td>CG RAM (15)</td>
<td>CG RAM (15)</td>
<td>CG RAM (15)</td>
<td>CG RAM (15)</td>
<td>CG RAM (15)</td>
<td></td>
</tr>
</tbody>
</table>

Higher 4-bit (D4 to D7) of Character Code (Hexadecimal)

Lower 4-bit (D0 to D3) of Character Code (Hexadecimal)
The relationships between Character Generator RAM Addresses, Character Generator RAM Data (character patterns), and Character Codes are depicted as follows:

5.12.1. 5 x 8 dot character patterns

Note1: It means that the bit0-2 of the character code correspond to the bit3-5 of the CG RAM address.

Note2: These areas are not used for display, but can be used for the general data RAM.

Note3: When all of the bit4 -7 of the character code are 0, CG RAM character patterns are selected.

Note4: " 1 ": Selected, " 0 ": No selected , " X " : Do not care (0 or 1).

Note5: For example (1), set character code (b2 = b1 = b0 = 0, b3 = 0 or 1, b7-b4 = 0) to display " T ". That means character code (00) 16,and (08) 16 can display " T " character.

Note6: The bits 02 of the character code RAM is the character pattern line position. The 8th line is the cursor position and display is formed by logical OR with the cursor.
5.12.2. 5 X 10 dot character patterns

<table>
<thead>
<tr>
<th>Character Code (DD RAM Data)</th>
<th>CG RAM Address</th>
<th>Character Patterns (CG RAM Data)</th>
</tr>
</thead>
<tbody>
<tr>
<td>b7 b6 b5 b4 b3 b2 b1 b0</td>
<td>b5 b4 b3 b2 b1 b0</td>
<td>b7 b6 b5 b4 b3 b2 b1 b0</td>
</tr>
<tr>
<td>0 0 0 0 X 0 0 X</td>
<td>0 0 0 0</td>
<td>1 0 0 0 0 1</td>
</tr>
<tr>
<td>0 0 0 1</td>
<td>1 0 0 0 1</td>
<td></td>
</tr>
<tr>
<td>0 0 1 0</td>
<td>1 0 0 0 1</td>
<td></td>
</tr>
<tr>
<td>0 0 1 1</td>
<td>1 0 0 0 1</td>
<td></td>
</tr>
<tr>
<td>0 1 0 0</td>
<td>1 0 0 0 1</td>
<td></td>
</tr>
<tr>
<td>0 1 0 1</td>
<td>1 0 0 0 1</td>
<td></td>
</tr>
<tr>
<td>1 0 0 0</td>
<td>1 0 0 0 1</td>
<td></td>
</tr>
<tr>
<td>1 0 0 1</td>
<td>1 1 1 1</td>
<td></td>
</tr>
<tr>
<td>1 0 1 0</td>
<td>0 0 0 0 0 0</td>
<td></td>
</tr>
<tr>
<td>1 0 1 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 1 0 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 1 0 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 1 1 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 1 1 1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note1:** It means that the bit1~2 of the character code correspond to the bit4~5 of the CG RAM address.

**Note2:** These areas are not used for display, but can be used for the general data RAM.

**Note3:** When all of the bit4-7 of the character code are 0, CG RAM character patterns are selected.

**Note4:** "1": Selected, "0": No selected, "X": Do not care (0 or 1).

**Note5:** For example (1), set character code (b2 = b1 = 0, b3 = b0 = 0 or 1, b7-b4 = 0) to display "U". That means all of the character codes (00) 16, (01) 16, (08) 16, and (09) 16 can display "U" character.

**Note6:** The bits 03 of the character code RAM is the character pattern line position. The 11th line is the cursor position and display is formed by logical OR with the cursor.
5.13. Cursor/Blink Control Circuit

This circuit generates the cursor or blink in the cursor / blink control circuit. The cursor or the blink appears in the digit at the Display Data RAM Address defined in the Address Counter. When the Address Counter is (07) 16, the cursor position is shown as belows:

<table>
<thead>
<tr>
<th>b6 b5 b4 b3 b2 b1 b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0 1 1 1</td>
</tr>
</tbody>
</table>

In a 1-line display

<table>
<thead>
<tr>
<th>digit</th>
<th>1 2 3 4 5 6 7 8 9 10</th>
</tr>
</thead>
<tbody>
<tr>
<td>00 01 02 03 04 05 06 07 08 09</td>
<td></td>
</tr>
</tbody>
</table>

The cursor position

Display position

Display data RAM address (Hexadecimal)

In a 2-line display

<table>
<thead>
<tr>
<th>digit</th>
<th>1 2 3 4 5 6 7 8 9 10</th>
</tr>
</thead>
<tbody>
<tr>
<td>00 01 02 03 04 05 06 07 08 09</td>
<td></td>
</tr>
<tr>
<td>40 41 42 43 44 45 46 47 48 49</td>
<td></td>
</tr>
</tbody>
</table>

Display position

Display data RAM address (Hexadecimal)

The cursor position

5.14. Interfacing to MPU

There are two types of data operations: 4-bit and 8-bit operations. Using 4-bit MPU, the interfacing 4bit data is transferred by 4-busline (DB4 to DB7). Thus, DB0 to DB3 bus lines are not used. Using 4-bit MPU to interface 8-bit data requires two times transferring. First, the higher 4-bit data is transferred by 4-busline (for 8-bit operation, DB7 to DB4). Secondly, the lower 4-bit data is transferred by 4busline (for 8 bit operation, DB3 to DB0). For 8-bit MPU, the 8-bit data is transferred by 8 buslines (DB0 to DB7).

5.15. Supply Voltage for LCD Drive

Different voltages can be supplied to SPLC780D’s pins (V5 - 1) for obtaining LCD drive-waveform. The relationships between bias, duty factor and supply voltages are shown as follows:

<table>
<thead>
<tr>
<th>Supply Voltage</th>
<th>Duty Factor</th>
<th>1/8, 1/11</th>
<th>1/16</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/4</td>
<td>V1</td>
<td>VDD – 1/4 V&lt;sub&gt;LC&lt;/sub&gt;, VDD – 1/5 V&lt;sub&gt;LC&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td>1/5</td>
<td>V2</td>
<td>VDD – 1/2 V&lt;sub&gt;LC&lt;/sub&gt;, VDD – 2/5 V&lt;sub&gt;LC&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td></td>
<td>V3</td>
<td>VDD – 1/2 V&lt;sub&gt;LC&lt;/sub&gt;, VDD – 3/5 V&lt;sub&gt;LC&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td></td>
<td>V4</td>
<td>VDD – 3/4 V&lt;sub&gt;LC&lt;/sub&gt;, VDD – 4/5 V&lt;sub&gt;LC&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td></td>
<td>V5</td>
<td>VDD – V&lt;sub&gt;LC&lt;/sub&gt;, VDD – V&lt;sub&gt;LC&lt;/sub&gt;</td>
<td></td>
</tr>
</tbody>
</table>
5.15.1. The power connections for LCD (1/4 Bias, 1/5 Bias) are shown belows:

The bypass-capacitor improves the LCD display quality.

The bias voltage must have the following relations:

VDD > V1 > V2 > V3 > V4 > V5.
5.15.2. The relationship between LCD frame’s frequency and oscillator’s frequency.

(Assume the oscillation frequency is 250KHz, 1 clock cycle time = 4.0µs)

5.15.2.1. 1/8 Duty, TYPE-B waveform

5.15.2.2. 1/11 Duty, TYPE-B waveform

5.15.2.3. 1/16 Duty, TYPE-B waveform
5.16. REGISTER --- IR (Instruction Register) and DR
(Data Register)
SPLC780D contains two 8-bit registers: Instruction Register (IR) and Data Register (DR). Using combinations of the RS pin and the R/W pin selects the IR and DR, see below:

<table>
<thead>
<tr>
<th>RS</th>
<th>R/W</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>IR write (Display clear, etc.)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Read busy flag (DB7) and Address Counter (DB0 - DB6)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>DR write (DR to Display data RAM or Character generator RAM)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>DR read (Display data RAM or Character generator RAM to DR)</td>
</tr>
</tbody>
</table>

The IR can be written by MPU, but it cannot be read by MPU.

5.17. Busy Flag (BF)
When RS = 0 and R/W = 1, the busy flag is output to DB7. As the busy flag =1, SPLC780D is in busy state and does not accept any instruction until the busy flag = 0.

5.18. Address Counter (AC)
The Address Counter assigns addresses to Display Data RAM and Character Generator RAM. When an instruction for address is written in IR, the address information is sent from IR to AC. After writing to/reading from Display Data RAM or Character Generator RAM, AC is automatically incremented by one (or decremented by one). The contents of AC are output to DB0 - DB6 when RS = 0 and R/W = 1.

5.19. I/O Port Configuration
5.19.1. Input port: E

5.19.2. Input port: R/W, RS

5.19.3. Output port: CL1, CL2, M, D

5.19.4. Input / Output port: DB7 - DB0
### 6. ELECTRICAL SPECIFICATIONS

#### 6.1. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Ratings</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Voltage</td>
<td>VDD</td>
<td>-0.3V to +7.0V</td>
</tr>
<tr>
<td>Driver Supply Voltage</td>
<td>V&lt;sub&gt;LCD&lt;/sub&gt;</td>
<td>VDD - 12V to VDD + 0.3V</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>-0.3V to VDD + 0.3V</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>T&lt;sub&gt;A&lt;/sub&gt;</td>
<td>-30 ℃ to +80 ℃</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>T&lt;sub&gt;STO&lt;/sub&gt;</td>
<td>-55 ℃ to +125 ℃</td>
</tr>
</tbody>
</table>

*Note:* Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

#### 6.2. DC Characteristics (VDD = 2.7V to 4.5V, T<sub>A</sub> = 25 ℃)

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Limit</th>
<th>Unit</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Current</td>
<td>I&lt;sub&gt;D&lt;/sub&gt;</td>
<td>0.2 mA</td>
<td>mA</td>
<td>External clock (Note)</td>
</tr>
<tr>
<td>Input High Voltage</td>
<td>V&lt;sub&gt;H1&lt;/sub&gt;</td>
<td>0.7VDD</td>
<td>V</td>
<td>Pins: (E, RS, R/W, DB0 - DB7)</td>
</tr>
<tr>
<td>Input Low Voltage</td>
<td>V&lt;sub&gt;L1&lt;/sub&gt;</td>
<td>-0.3V</td>
<td>V</td>
<td>Pin OSC1</td>
</tr>
<tr>
<td>Input High Voltage</td>
<td>V&lt;sub&gt;H2&lt;/sub&gt;</td>
<td>0.7VDD</td>
<td>V</td>
<td>Pins: (RS, R/W, DB0 - DB7)</td>
</tr>
<tr>
<td>Input Low Voltage</td>
<td>V&lt;sub&gt;L2&lt;/sub&gt;</td>
<td>-0.2V</td>
<td>V</td>
<td>VDD = 3.0V</td>
</tr>
<tr>
<td>Input High Current</td>
<td>I&lt;sub&gt;H&lt;/sub&gt;</td>
<td>-1.0 µA</td>
<td>µA</td>
<td>Pins: CL1, CL2, M, D</td>
</tr>
<tr>
<td>Input Low Current</td>
<td>I&lt;sub&gt;L&lt;/sub&gt;</td>
<td>-5.0 µA</td>
<td>µA</td>
<td>Pins: CL1, CL2, M, D</td>
</tr>
<tr>
<td>Output High Voltage (TTL)</td>
<td>V&lt;sub&gt;OH1&lt;/sub&gt;</td>
<td>0.75VDD</td>
<td>V</td>
<td>I&lt;sub&gt;OH&lt;/sub&gt; = -0.1mA</td>
</tr>
<tr>
<td>Output Low Voltage (TTL)</td>
<td>V&lt;sub&gt;OL1&lt;/sub&gt;</td>
<td>-</td>
<td>V</td>
<td>Pins: DB0 - DB7</td>
</tr>
<tr>
<td>Output High Voltage (CMOS)</td>
<td>V&lt;sub&gt;OH2&lt;/sub&gt;</td>
<td>0.8VDD</td>
<td>V</td>
<td>I&lt;sub&gt;OH&lt;/sub&gt; = 40µA,</td>
</tr>
<tr>
<td>Output Low Voltage (CMOS)</td>
<td>V&lt;sub&gt;OL2&lt;/sub&gt;</td>
<td>-</td>
<td>V</td>
<td>Pins: COM1 - COM16</td>
</tr>
<tr>
<td>Driver ON Resistance (COM)</td>
<td>R&lt;sub&gt;COM&lt;/sub&gt;</td>
<td>20 KΩ</td>
<td>KΩ</td>
<td>Pins: SEG1 - SEG40</td>
</tr>
<tr>
<td>Driver ON Resistance (SEG)</td>
<td>R&lt;sub&gt;SEG&lt;/sub&gt;</td>
<td>-</td>
<td>KΩ</td>
<td>Pins: SEG1 - SEG40</td>
</tr>
</tbody>
</table>

*Note:* F<sub>osc</sub> = 250KHz, VDD = 3.0V, pin E = “L”, RS, R/W, DB0 - DB7 are open, all outputs are no loads.
6.3. AC Characteristics (VDD = 2.7V to 4.5V, T_A = 25℃)

6.3.1. Internal clock operation

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Limit</th>
<th>Unit</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>OSC Frequency</td>
<td>FOSC1</td>
<td>190  270  350</td>
<td>kHz</td>
<td>VDD = 3.0V, Rf = 75KΩ±2%</td>
</tr>
</tbody>
</table>

6.3.2. External clock operation

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Limit</th>
<th>Unit</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>External Frequency</td>
<td>FOSC2</td>
<td>125  250  350</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>Duty Cycle</td>
<td></td>
<td>45  50  55</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Rise/Fall Time</td>
<td>t_r, t_f</td>
<td></td>
<td>0.2 μs</td>
<td></td>
</tr>
</tbody>
</table>

6.3.3. Write mode (Writing data from MPU to SPLC780D)

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Limit</th>
<th>Unit</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>E Cycle Time</td>
<td>t_c</td>
<td>1000 - -</td>
<td>ns</td>
<td>Pin E</td>
</tr>
<tr>
<td>E Pulse Width</td>
<td>t_PW</td>
<td>450 - -</td>
<td>ns</td>
<td>Pin E</td>
</tr>
<tr>
<td>E Rise/Fall Time</td>
<td>t_r, t_f</td>
<td>- - 25</td>
<td>ns</td>
<td>Pin E</td>
</tr>
<tr>
<td>Address Setup Time</td>
<td>t_SPI1</td>
<td>60 - -</td>
<td>ns</td>
<td>Pins: RS, R/W, E</td>
</tr>
<tr>
<td>Address Hold Time</td>
<td>t_HD1</td>
<td>20 - -</td>
<td>ns</td>
<td>Pins: RS, R/W, E</td>
</tr>
<tr>
<td>Data Setup Time</td>
<td>t_SPI2</td>
<td>195 - -</td>
<td>ns</td>
<td>Pins: DB0 - DB7</td>
</tr>
<tr>
<td>Data Hold Time</td>
<td>t_HD2</td>
<td>10 - -</td>
<td>ns</td>
<td>Pins: DB0 - DB7</td>
</tr>
</tbody>
</table>

6.3.4. Read mode (Reading data from SPLC780D to MPU)

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Limit</th>
<th>Unit</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>E Cycle Time</td>
<td>t_c</td>
<td>1000 - -</td>
<td>ns</td>
<td>Pin E</td>
</tr>
<tr>
<td>E Pulse Width</td>
<td>t_PW</td>
<td>450 - -</td>
<td>ns</td>
<td>Pin E</td>
</tr>
<tr>
<td>E Rise/Fall Time</td>
<td>t_r, t_f</td>
<td>- - 25</td>
<td>ns</td>
<td>Pin E</td>
</tr>
<tr>
<td>Address Setup Time</td>
<td>t_SPI1</td>
<td>60 - -</td>
<td>ns</td>
<td>Pins: RS, R/W, E</td>
</tr>
<tr>
<td>Address Hold Time</td>
<td>t_HD1</td>
<td>20 - -</td>
<td>ns</td>
<td>Pins: RS, R/W, E</td>
</tr>
<tr>
<td>Data Output Delay Time</td>
<td>t_D0</td>
<td>- - 360</td>
<td>ns</td>
<td>Pins: DB0 - DB7</td>
</tr>
<tr>
<td>Data hold time</td>
<td>t_D02</td>
<td>5.0 - -</td>
<td>ns</td>
<td>Pins DB0 - DB7</td>
</tr>
</tbody>
</table>
6.4. DC Characteristics (VDD = 4.5V to 5.5V, TA = 25 ℃)

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Limit</th>
<th>Unit</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Typ.</td>
<td>Max.</td>
</tr>
<tr>
<td>Operating Current</td>
<td>I_{DD}</td>
<td>-</td>
<td>0.55</td>
<td>0.8 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input High Voltage</td>
<td>V_{HI}</td>
<td></td>
<td>2.2</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Pins: (E, RS, RW, DB0 - DB7)</td>
</tr>
<tr>
<td>Input Low Voltage</td>
<td>V_{IL}</td>
<td></td>
<td>-0.3</td>
<td>- VDD</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input High Voltage</td>
<td>V_{HE}</td>
<td></td>
<td>VDD-1</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Pin OSC1</td>
</tr>
<tr>
<td>Input Low Voltage</td>
<td>V_{LE}</td>
<td></td>
<td>-0.2</td>
<td>- 1.0 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input High Current</td>
<td>I_{H}</td>
<td></td>
<td>-2.0</td>
<td>- 2.0 µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Pins: (RS, RW, DB0 - DB7)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>VDD = 5.0V</td>
</tr>
<tr>
<td>Input Low Current</td>
<td>I_{L}</td>
<td>-20</td>
<td>-50</td>
<td>-100 µA</td>
</tr>
<tr>
<td>Output High Voltage (TTL)</td>
<td>V_{OH1}</td>
<td></td>
<td>2.4</td>
<td>- VDD</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output Low Voltage (TTL)</td>
<td>V_{OL1}</td>
<td></td>
<td>-</td>
<td>0.4 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output High Voltage (CMOS)</td>
<td>V_{OH2}</td>
<td></td>
<td>0.9VDD</td>
<td>- VDD</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output Low Voltage (CMOS)</td>
<td>V_{OL2}</td>
<td></td>
<td>-</td>
<td>0.1VDD</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Driver ON Resistance (COM)</td>
<td>R_{COM}</td>
<td></td>
<td>-</td>
<td>20 KΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Driver ON Resistance (SEG)</td>
<td>R_{SEG}</td>
<td></td>
<td>-</td>
<td>30 KΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LCD Voltage</td>
<td>V_{LCD}</td>
<td></td>
<td>3.0</td>
<td>- 11 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: \( F_{OSC} = 250\text{kHz}, \) VDD = 5.0V, pin E = “L”, RS, RW, DB0 - DB7 are open, all outputs are no loads.

6.5. AC Characteristics (VDD = 4.5V to 5.5V, TA = 25 ℃)

6.5.1. Internal clock operation

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Limit</th>
<th>Unit</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Typ.</td>
<td>Max.</td>
</tr>
<tr>
<td>OSC Frequency</td>
<td>F_{OSC1}</td>
<td>190</td>
<td>270</td>
<td>350 KHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>VDD = 5.0V, RF = 91KΩ, 2%</td>
</tr>
</tbody>
</table>

6.5.2. External clock operation

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Limit</th>
<th>Unit</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Typ.</td>
<td>Max.</td>
</tr>
<tr>
<td>External Frequency</td>
<td>F_{OSC2}</td>
<td>125</td>
<td>250</td>
<td>350 KHz</td>
</tr>
<tr>
<td>Duty Cycle</td>
<td></td>
<td>45</td>
<td>50</td>
<td>55%</td>
</tr>
<tr>
<td>Rise/Fall Time</td>
<td>t_{rr}, t_{ff}</td>
<td>-</td>
<td>-</td>
<td>0.2 µs</td>
</tr>
</tbody>
</table>
### 6.5.3. Write mode (Writing Data from MPU to SPLC780D)

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Limit</th>
<th>Unit</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>E Cycle Time</td>
<td>t_E</td>
<td>500</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>E Pulse Width</td>
<td>t_W</td>
<td>230</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>E Rise/Fall Time</td>
<td>t_{R, F}</td>
<td>-</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>Address Setup Time</td>
<td>t_SP1</td>
<td>40</td>
<td>-</td>
<td>Pins: RS, R/W, E</td>
</tr>
<tr>
<td>Address Hold Time</td>
<td>t_{HD1}</td>
<td>10</td>
<td>-</td>
<td>Pins: RS, R/W, E</td>
</tr>
<tr>
<td>Data Setup Time</td>
<td>t_{SP2}</td>
<td>80</td>
<td>-</td>
<td>Pins: DB0 - DB7</td>
</tr>
<tr>
<td>Data Hold Time</td>
<td>t_{HD2}</td>
<td>10</td>
<td>-</td>
<td>Pins: DB0 - DB7</td>
</tr>
</tbody>
</table>

### 6.5.4. Read mode (Reading Data from SPLC780D to MPU)

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Limit</th>
<th>Unit</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>E Cycle Time</td>
<td>t_C</td>
<td>500</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>E Pulse Width</td>
<td>t_W</td>
<td>230</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>E Rise/Fall Time</td>
<td>t_{R, F}</td>
<td>-</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>Address Setup Time</td>
<td>t_SP1</td>
<td>40</td>
<td>-</td>
<td>Pins: RS, R/W, E</td>
</tr>
<tr>
<td>Address Hold Time</td>
<td>t_{HD1}</td>
<td>10</td>
<td>-</td>
<td>Pins: RS, R/W, E</td>
</tr>
<tr>
<td>Data Output Delay Time</td>
<td>t_O</td>
<td>-</td>
<td>120</td>
<td>ns</td>
</tr>
<tr>
<td>Data Hold time</td>
<td>t_{HD2}</td>
<td>5.0</td>
<td>-</td>
<td>Pins: DB0 - DB7</td>
</tr>
</tbody>
</table>

### 6.5.5. Interface mode with LCD Driver (SPLC100A1)

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Limit</th>
<th>Unit</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock pulse width high</td>
<td>t_{PWH}</td>
<td>800</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Clock pulse width low</td>
<td>t_{PWL}</td>
<td>800</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Clock setup time</td>
<td>t_{CS}</td>
<td>500</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Data setup time</td>
<td>t_DSP</td>
<td>300</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Data hold time</td>
<td>t_D</td>
<td>300</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>M delay time</td>
<td>t_{D}</td>
<td>-1000</td>
<td>1000</td>
<td>ns</td>
</tr>
</tbody>
</table>

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AUG. 06, 2003
Preliminary Version: 0.1
6.5.6. Write mode timing diagram (Writing Data from MPU to SPLC780D)

RS

R / W

E

DB7 - 0

6.5.7. Read mode timing diagram (Reading Data from SPLC780D to MPU)

RS

R / W

E

DB0 - DB7

6.5.8. Interface mode with SPLC100A1 timing diagram
7. APPLICATION CIRCUITS

7.1. R-Oscillator

The oscillation resistor \( R_f \) is used only for the internal oscillator operation mode.

\[ R_f : 75.0 \Omega \pm 2\% \text{ (when VDD = 3.0V)} \]
\[ R_f : 91K \Omega \pm 2\% \text{ (when VDD = 5.0V)} \]

Since the oscillation frequency varies depending on the \( \text{OSC}_1 \) and \( \text{OSC}_2 \) pin capacitance, the wiring length to these pins should be minimized.

![Graphs showing frequency vs. resistance for VDD = 3.0V and VDD = 5.0V](image)

7.2. Interface to MPU

7.2.1. Interface to 8-bit MPU (6805)

![Circuit diagram](image)

7.2.2. Interface to 8-bit MPU (Z80)

![Circuit diagram](image)
7.3. SPLC780D Application Circuit
7.4. Applications for LCD

(Example 1): 5 x 8 dots, 8 characters x 1 line [1/4 Bias, 1/8 Duty]

(Example 2): 5 x 10 dots, 8 characters x 1 line [1/4 Bias, 1/11 Duty]

(Example 3): 5 x 8 dots, 8 characters x 2 lines [1/5 Bias, 1/16 Duty]
(Example 4): 5 x 8 dots, 16 characters x 1 line [1/5 Bias, 1/16 Duty]

(Example 5): 5 x 8 dots, 4 characters x 2 lines [1/4 Bias, 1/8 Duty]
8. CHARACTER GENERATOR ROM

8.1. SPLC780D - 001
9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment and Locations

Please contact Sunplus sales representatives for more information.
9.2. Package Configuration

QFP 80L Top View
### 9.3. Package Information

#### QFP 80L Outline Dimensions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Min.</th>
<th>Nom.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>23.20</td>
<td>REF</td>
<td></td>
<td>Millimeter</td>
</tr>
<tr>
<td>D1</td>
<td>20.00</td>
<td>REF</td>
<td></td>
<td>Millimeter</td>
</tr>
<tr>
<td>E</td>
<td>17.20</td>
<td>REF</td>
<td></td>
<td>Millimeter</td>
</tr>
<tr>
<td>E1</td>
<td>14.00</td>
<td>REF</td>
<td></td>
<td>Millimeter</td>
</tr>
<tr>
<td>e</td>
<td>0.80</td>
<td>REF</td>
<td></td>
<td>Millimeter</td>
</tr>
<tr>
<td>b</td>
<td>0.30</td>
<td>0.35</td>
<td>0.45</td>
<td>Millimeter</td>
</tr>
<tr>
<td>A</td>
<td>-</td>
<td>0.35</td>
<td>3.40</td>
<td>Millimeter</td>
</tr>
<tr>
<td>A1</td>
<td>0.25</td>
<td>-</td>
<td>-</td>
<td>Millimeter</td>
</tr>
<tr>
<td>A2</td>
<td>2.50</td>
<td>2.72</td>
<td>2.90</td>
<td>Millimeter</td>
</tr>
<tr>
<td>c</td>
<td>0.11</td>
<td>0.15</td>
<td>0.23</td>
<td>Millimeter</td>
</tr>
<tr>
<td>L1</td>
<td>1.60</td>
<td>REF</td>
<td></td>
<td>Millimeter</td>
</tr>
</tbody>
</table>
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# REVISION HISTORY

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision #</th>
<th>Description</th>
<th>Page</th>
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<td>0.1</td>
<td>Original</td>
<td>34</td>
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