



*HIGH-VOLTAGE MIXED-SIGNAL IC*

# UC1610

128 x 160 4S STN LCD Controller-Driver



**MP Specifications**  
**Revision 1.11**

**April 13, 2005**

# ULTRACHIP

*The Coolest LCD Driver, Ever!!*



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# UC1610

*Single-Chip, Ultra-Low Power  
128COM x 160SEG Matrix  
Passive Color LCD Controller-Driver*

## INTRODUCTION

UC1610 is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of ultra-low power hand-held devices.

This chip employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture to achieve near crosstalk free images, with well balanced gray shades.

In addition to low power COM and SEG drivers, UC1610 contains all necessary circuits for high-V LCD power supply, bias voltage generation, timing generation and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

## MAIN APPLICATIONS

- Cellular Phones and other battery operated palm top devices or portable Instruments

## FEATURE HIGHLIGHTS

- Single chip controller-driver for 128x160 matrix STN LCD with 4 gray shades.
- One software readable ID pin to support configurable vender identification.
- Partial scroll function and programmable data update window to support flexible manipulation of screen data.
- Support both row ordered and column ordered display buffer RAM access
- Support industry standard 2-wire, 3-wire, 4-wire serial bus (I<sup>2</sup>C, S9, S8, S8uc) and 8-bit/4-bit parallel bus (8080 or 6800).
- Special driver structure and gray shade modulation scheme. Consistent low power consumption under all display patterns.
- Fully programmable Mux Rate, partial display window, Bias Ratio and Line Rate allow many flexible power management options.
- Four software programmable frame rates up to 130Hz. Support the use of fast Liquid Crystal material for speedy LCD response.
- Software programmable 4 temperature compensation coefficients.
- On-chip Power-ON Reset and Software RESET command, make RST pin optional.
- Self-configuring 8x charge pump with on-chip pumping capacitors. Only 3 external capacitors are required to operate.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- Very low pin count (9~10 pins with S9 or I<sup>2</sup>C) allows exceptional image quality in COG format on conventional ITO glass.
- Many on-chip and I/O pad layout features to support optimized COG applications.
- V<sub>DD</sub> (digital) range: 1.8V ~ 3.3V  
V<sub>DD</sub> (analog) range: 2.6V ~ 3.3V  
LCD V<sub>OP</sub> range: 5.0V ~ 15V
- Available in gold bump dies  
Bump pitch: 50μM  
Bump gap: 17μM.  
Bump surface: >3,000μM<sup>2</sup>

**ORDERING INFORMATION**

Part Number	Versions	Description
UC1610IGAB	Gold Bumped Die	Bare die with gold bumps with I <sup>2</sup> C interface

**General Notes****APPLICATION INFORMATION**

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

**BARE DIE DISCLAIMER**

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing for a period of ninety (90) days from the date of UltraChip's delivery. There is no post wafer saw/pack testing performed on individual die. Although the latest processes are utilized for wafer sawing and die pick-&-place into wafer pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their applications in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

**USE OF I<sup>2</sup>C**

The implementation of I<sup>2</sup>C is already included and tested in all silicon. However, unless I<sup>2</sup>C licensing obligation is executed satisfactorily, it is not legal to use UltraChip product for I<sup>2</sup>C applications. Unless I<sup>2</sup>C version is ordered from UltraChip, the customer will take the responsibility for all such licensing liabilities.

**LIFE SUPPORT APPLICATIONS**

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

**CONTENT DISCLAIMER**

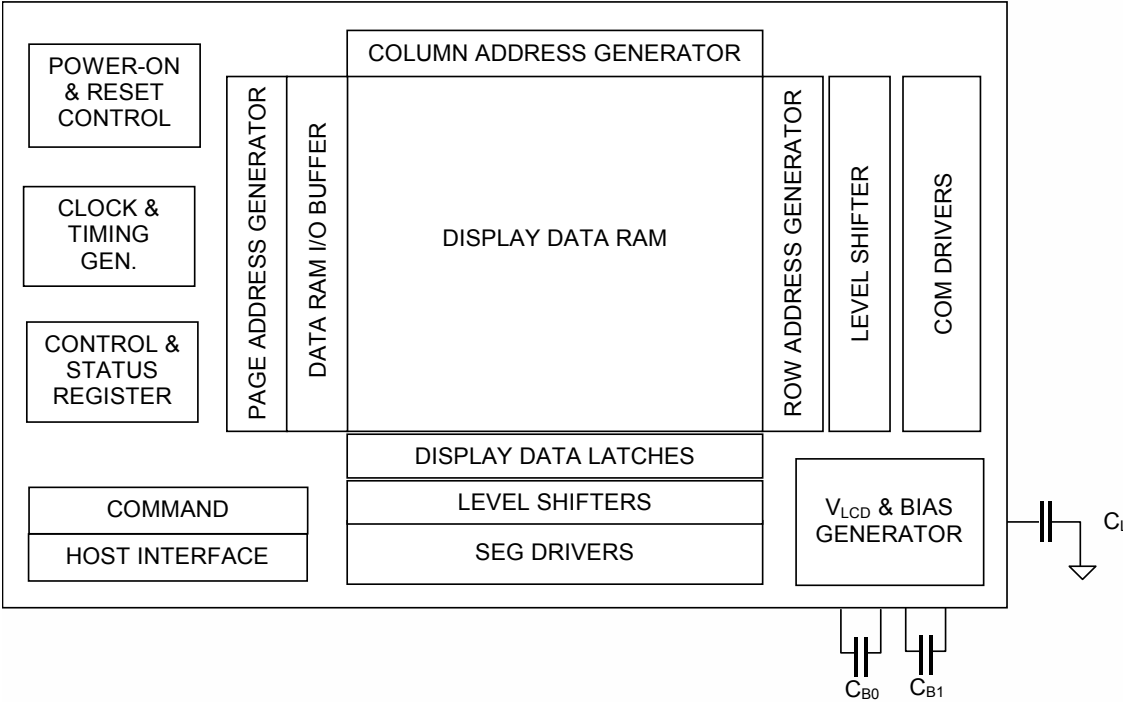
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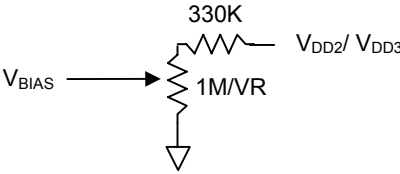
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**BLOCK DIAGRAM**



**PIN DESCRIPTION**

Name	Type	Pins	Description
<b>MAIN POWER SUPPLY</b>			
V <sub>DD</sub> V <sub>DD2</sub> V <sub>DD3</sub>	PWR	5 3 3	V <sub>DD2</sub> /V <sub>DD3</sub> is the analog power supply and it should be connected to the same power source. V <sub>DD</sub> is the digital power supply and it should be connected to a voltage source that is no higher than V <sub>DD2</sub> /V <sub>DD3</sub> . Please maintain the following relationship: $V_{DD} + 1.3V \geq V_{DD2/3} \geq V_{DD}$ Minimize the trace resistance for V <sub>DD</sub> and V <sub>DD2</sub> /V <sub>DD3</sub> .
V <sub>SS</sub> V <sub>SS2</sub>	GND	6 5	Ground. Connect V <sub>SS</sub> and V <sub>SS2</sub> to the shared GND pin. Minimize the trace resistance for this node.
<b>LCD POWER SUPPLY &amp; VOLTAGE CONTROL</b>			
V <sub>BIAS</sub>	I	1	This is the reference voltage to generate the actual SEG driving voltage. V <sub>BIAS</sub> can be used to fine tune V <sub>LCD</sub> by external variable resistors. Internal resistor network has been provided to simplify external trimming circuit. The following network is sufficient for most applications.  An internal RC filter is provided to filter noise on the V <sub>BIAS</sub> pin. When not use, it is OK to leave V <sub>BIAS</sub> open circuit. If noise starts to cause problem, connect a small bypass capacitor between V <sub>BIAS</sub> and V <sub>SS</sub> .
V <sub>B1+</sub> V <sub>B1-</sub> V <sub>B0+</sub> V <sub>B0-</sub>	PWR	9, 9 9, 9	LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of C <sub>BX</sub> value between V <sub>BX+</sub> and V <sub>BX-</sub> . The resistance of these traces directly affects the driving strength of SEG electrodes and impacts the image of the LCD module. Minimize the trace resistance is critical in achieving high quality image.
V <sub>LCDIN</sub> V <sub>LCDOUT</sub>	PWR	2 2	High voltage LCD Power Supply. Connect these pins together. By-pass capacitor C <sub>L</sub> is optional. It can be connected between V <sub>LCD</sub> and V <sub>SS</sub> . When C <sub>L</sub> is used, keep the trace resistance under 300 Ohm.

**NOTE**

- Recommended capacitor values:  
C<sub>B</sub>: 150~250x LCD load capacitance or 2μF (2V), whichever is higher.  
C<sub>L</sub>: 0.06μF~0.3μF (25V) is appropriate for most applications.

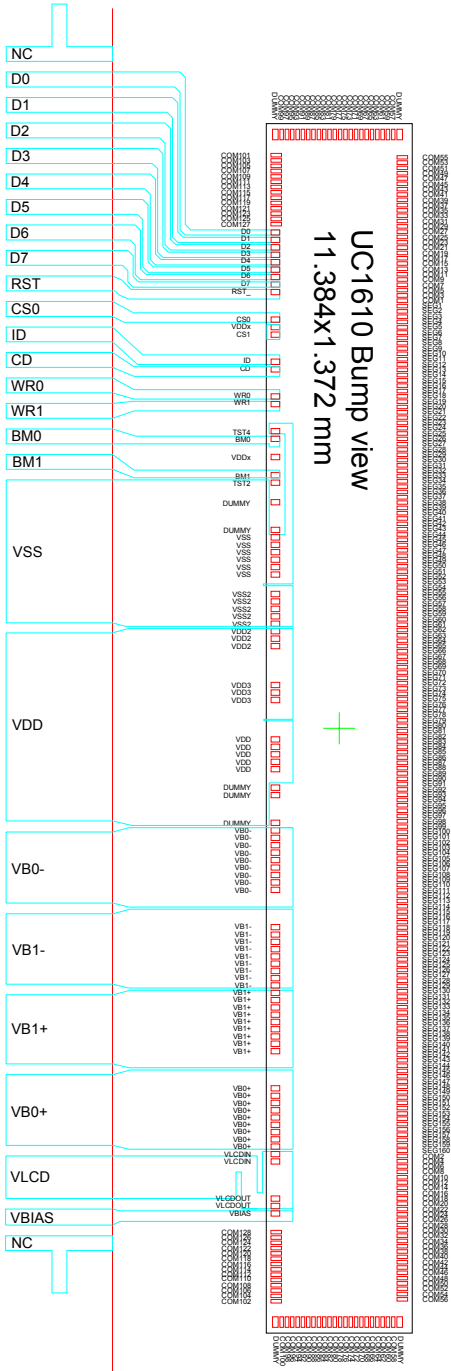


Name	Type	Pins	Description																																													
<b>HOST INTERFACE</b>																																																
BM0 BM1	I	1 1	<p>Bus mode: The interface bus mode is determined by BM[1:0] and D[7:6] by the following relationship:</p> <table border="1"> <thead> <tr> <th>BM[1:0]</th> <th>D[7:6]</th> <th>Mode</th> </tr> </thead> <tbody> <tr> <td>11</td> <td>Data</td> <td>6800/8-bit</td> </tr> <tr> <td>10</td> <td>Data</td> <td>8080/8-bit</td> </tr> <tr> <td>01</td> <td>00</td> <td>6800/4-bit</td> </tr> <tr> <td>00</td> <td>00</td> <td>8080/4-bit</td> </tr> <tr> <td>01</td> <td>10</td> <td>3-wire SPI w/ 9-bit token (S9: conventional)</td> </tr> <tr> <td>01</td> <td>11</td> <td>2-wire I<sup>2</sup>C</td> </tr> <tr> <td>00</td> <td>10</td> <td>4-wire SPI w/ 8-bit token (S8: conventional)</td> </tr> <tr> <td>00</td> <td>11</td> <td>3-wire SPI w/ 8-bit token (S8uc: Ultra-Compact)</td> </tr> </tbody> </table>	BM[1:0]	D[7:6]	Mode	11	Data	6800/8-bit	10	Data	8080/8-bit	01	00	6800/4-bit	00	00	8080/4-bit	01	10	3-wire SPI w/ 9-bit token (S9: conventional)	01	11	2-wire I <sup>2</sup> C	00	10	4-wire SPI w/ 8-bit token (S8: conventional)	00	11	3-wire SPI w/ 8-bit token (S8uc: Ultra-Compact)																		
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CS1/A2 CS0/A3	I	1 1	<p>Chip Select. Chip is selected when CS1="H" and CS0 = "L". When the chip is not selected, D[7:0] will be high impedance.</p> <p>In I<sup>2</sup>C mode, these two pins indicate the I<sup>2</sup>C bus address' bit 2 and bit 3.</p>																																													
RST	I	1	<p>When RST="L", all control registers are re-initialized by their default states. Since UC1610 has built-in Power-ON Reset and Software Reset command, RST pin is not required for proper chip operation.</p> <p>An RC Filter has been included on-chip. There is no need for external RC noise filter. When RST is not used, connect the pin to V<sub>DD</sub>.</p>																																													
CD	I	1	<p>Select Control data or Display data for read/write operation. In S9 and I<sup>2</sup>C modes, CD pin is not used. Connect CD to V<sub>SS</sub> when not used.</p> <p>"L": Control data      "H": Display data</p>																																													
ID	I	1	<p>ID pin is for production control. The connection will affect the content of D[7] when using <i>Get Status</i> command. Connect to V<sub>DD</sub> for "H" or V<sub>SS</sub> for "L".</p>																																													
WR0 WR1	I	1 1	<p>WR[1:0] controls the read/write operation of the host interface. See Host Interface section for more detail.</p> <p>In parallel mode, WR[1:0] meaning depends on whether the interface is in the 6800 mode or the 8080 mode. In serial interface modes, these two pins are not used, connect them to V<sub>SS</sub>.</p>																																													
D0~D7	I/O	8	<p>Bi-directional bus for both serial and parallel host interfaces.</p> <p>In serial modes, connect D[0] to SCK, D[3] to SDA,</p> <table border="1"> <thead> <tr> <th></th> <th>BM=1x (Parallel)</th> <th>BM=0x (Parallel)</th> <th>BM=01 (S9/I<sup>2</sup>C)</th> <th>BM=00 (S8/S8uc)</th> </tr> </thead> <tbody> <tr> <td>D0</td> <td>D0</td> <td>D0/D4</td> <td>SCK</td> <td>SCK</td> </tr> <tr> <td>D1</td> <td>D1</td> <td>D1/D5</td> <td>–</td> <td>–</td> </tr> <tr> <td>D2</td> <td>D2</td> <td>D2/D6</td> <td>–</td> <td>–</td> </tr> <tr> <td>D3</td> <td>D3</td> <td>D3/D7</td> <td>SDA</td> <td>SDA</td> </tr> <tr> <td>D4</td> <td>D4</td> <td>–</td> <td>–</td> <td>–</td> </tr> <tr> <td>D5</td> <td>D5</td> <td>–</td> <td>–</td> <td>–</td> </tr> <tr> <td>D6</td> <td>D6</td> <td>–</td> <td>S9/I<sup>2</sup>C</td> <td>S8/S8uc</td> </tr> <tr> <td>D7</td> <td>D7</td> <td>0</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <p>Connect unused pins to V<sub>SS</sub>.</p>		BM=1x (Parallel)	BM=0x (Parallel)	BM=01 (S9/I <sup>2</sup> C)	BM=00 (S8/S8uc)	D0	D0	D0/D4	SCK	SCK	D1	D1	D1/D5	–	–	D2	D2	D2/D6	–	–	D3	D3	D3/D7	SDA	SDA	D4	D4	–	–	–	D5	D5	–	–	–	D6	D6	–	S9/I <sup>2</sup> C	S8/S8uc	D7	D7	0	1	1
	BM=1x (Parallel)	BM=0x (Parallel)	BM=01 (S9/I <sup>2</sup> C)	BM=00 (S8/S8uc)																																												
D0	D0	D0/D4	SCK	SCK																																												
D1	D1	D1/D5	–	–																																												
D2	D2	D2/D6	–	–																																												
D3	D3	D3/D7	SDA	SDA																																												
D4	D4	–	–	–																																												
D5	D5	–	–	–																																												
D6	D6	–	S9/I <sup>2</sup> C	S8/S8uc																																												
D7	D7	0	1	1																																												

Name	Type	Pins	Description
<b>HIGH VOLTAGE LCD DRIVER OUTPUT</b>			
SEG1 ~ SEG160	HV	160	SEG (column) driver outputs. Support up to 160 pixels. Leave unused drivers open-circuit.
COM1 ~ COM128	HV	128	COM (row) driver outputs. Support up to 128 rows. Leave unused COM drivers open-circuit.
<b>Misc. PINS</b>			
V <sub>DDX</sub>		2	Auxiliary V <sub>DD</sub> . These pins are connected to the main V <sub>DD</sub> bus on chip. They are provided to facilitate chip configurations in COG application. These pins should not be used to provide V <sub>DD</sub> power to the chip. It is not necessary to connect V <sub>DDX</sub> to main V <sub>DD</sub> externally.
TST4	I	1	Test control. Connect TST4 to V <sub>SS</sub> during normal use.
TST2	I/O	1	Test I/O pin. Leave these pins open during normal use.

**Note:** Several control registers will specify “0 based index” for COM and SEG electrodes. In those situations, COM<sub>X</sub> or SEG<sub>X</sub> will correspond to index X-1, and the value ranges for those index registers will be 0~127 for COM and 0~159 for SEG.

RECOMMENDED COG LAYOUT



NOTES FOR V<sub>DD</sub> WITH COG:

The typical operation condition of UC1610, V<sub>DD</sub>=1.75V, should be met under all operating conditions. Unless V<sub>DD</sub> and V<sub>DD2/3</sub> ITO trances can each be controlled to be 5Ω or lower; otherwise V<sub>DD</sub>-V<sub>DD2/3</sub> separation can cause the actual on-chip V<sub>DD</sub> to drop below V<sub>DD</sub>=1.75V during high speed data write condition. Therefore, for COG, V<sub>DD</sub>-V<sub>DD2/3</sub> separation requires very careful ITO layout and very stringent testing before MP.

## CONTROL REGISTERS

UC1610 contains registers which control the chip operation. These registers can be modified by commands. The following table is a summary of the control registers, their meanings and their default values. Commands supported by UC1610 will be described in the next two sections. First, a summary table, followed by a detailed instruction-by-instruction description.

**Name:** The Symbolic reference of the register.  
Note that, some symbol name refers to bits (flags) within another register.

**Default:** Numbers shown in **Bold** font are default values after *Power-Up-Reset* and *System-Reset*.

Name	Bits	Default	Description
SL	7	0H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (for no scrolling) and (127– 2xFL). Setting SL outside of this range causes undefined effect on the displayed image.
FL	4	0H	Fixed Lines. The first FLx2 lines of each frame are fixed and are not affected by scrolling (SL). When FL is non-zero, the screen is effectively separated into two regions: one scrollable, one non-scrollable. When partial display mode is activated, the display of these 2xFL lines are also controlled by LC[0].
CR	8	0H	Return Column Address. Useful for cursor implementation.
CA	8	0H	Display Data RAM Column Address (Used in Host to Display Data RAM access)
PA	5	0H	Display Data RAM Page Address (Used in Host to Display Data RAM access)
BR	2	2H	Bias Ratio. The ratio between $V_{LCD}$ and $V_{BIAS}$ . 00b: 5                      01b: 10 <b>10b: 11</b> 11b: 12
TC	2	0H	Temperature Compensation (per °C) <b>00b: -0.05%</b> 01b: -0.10% 10b: -0.15%              11b: -0.20%
PM	8	B2H	Electronic Potentiometer to fine tune $V_{BIAS}$ and $V_{LCD}$
OM	2	–	Operating Modes (Read only) 00b: Reset                      01b: (Not used) 10b: Sleep                      11b: Normal
ID	1	PIN	Access the connected status of ID pin.
RS	1		Reset in progress. Host Interface not ready
PC	4	DH	Power Control. PC[1:0]: 00b: LCD: ≤ 16nF <b>01b: LCD: 16~21nF</b> 10b: LCD: 21~28nF              11b: LCD: 28~38nF PC[3:2]: 00b: External $V_{LCD}$ 01b: Internal $V_{LCD}$ (6X pump, low $V_{LCD}$ , only used when BR=5) 10b: Internal $V_{LCD}$ (7X pump) <b>11b: Internal <math>V_{LCD}</math> (8X pump, standard)</b>
DC	3	00H	Display Control: DC[0]: PXV: Pixels Inverse. Bit-wise data inversion. (Default <b>0: OFF</b> ) DC[1]: APO: All Pixels ON (Default <b>0: OFF</b> ) DC[2]: Display ON/OFF (Default <b>0: OFF</b> )

Name	Bits	Default	Description
AC	5	01H	Address Control: AC[0]: WA: Automatic column/page Wrap Around (Default <b>1: ON</b> ) AC[1]: Auto-Increment order <b>0: Column (CA) first</b> 1: Row (PA) first AC[2]: PID: PA (Page Address) auto increment direction ( <b>L:+1 H:-1</b> ) AC[3]: CUM: Cursor update mode, (Default <b>0: OFF</b> ) when CUM=1, CA increment on write only, wrap around suspended AC[4]: Window Program Enable <b>0: Disable</b> 1: Enable
WPC0	8	00H	Window program starting column address. Value range: 0 ~159.
WPP0	5	00H	Window program starting Page Address. Value range: 0~31.
WPC1	8	9FH	Window program ending column address. Value range: 0~159.
WPP1	5	1FH	Window program ending Page Address. Value range: 0~31.
CEN	7	7FH	COM scanning end (last COM with full line cycle, 0 based index)
DST	7	00H	Display start (first COM with active scan pulse, 0 based index)
DEN	7	7FH	Display end (last COM with active scan pulse, 0 based index)
			Please maintain the following relationship: CEN = the actual number of pixel rows on the LCD - 1 CEN ≥ DEN ≥ DST+ 9
LC	9	008H	LCD Control: LC[0]: Enable the first FLx2 lines in partial display mode (Default <b>OFF</b> ). LC[1]: MX, Mirror X. SEG/Column sequence inversion (Default: <b>OFF</b> ) LC[2]: MY, Mirror Y. COM/Row sequence inversion (Default: <b>OFF</b> ) LC[4:3]: Line Rate (Klps: Kilo-Line-per-second) <b>00b: 12.1 Klps (95fps)</b> 01b: 13.4 Klps (105fps) 10b: 14.7 Klps (115fps)            11b: 16.6 Klps (130fps) (Frame-Rate = Line-Rate / Mux-Rate, Frame rate at 128 is listed) LC[6:5]: Gray-Shade control. Control the difference of percentage between data "01" and "10" <b>00b: 24%</b> 01b: 29% 10b: 36%                              11b: 40% LC[8:7]: Partial Display Control <b>00b: Disable</b> Mux-Rate = CEN+1 (DST, DEN not used) 10b: Enable                      Mux-Rate = CEN+1 11b: Enabled                      Mux-Rate = DEN-DST+1
APC0	8	--	Advanced Product Configuration. For UltraChip only. Do <u>NOT</u> use.
APC1	8	--	

**COMMAND SUMMARY**

The following is a list of host commands supported by UC1610

- C/D: 0: Control, 1: Data  
 W/R: 0: Write Cycle, 1: Read Cycle  
 # Useful Data bits  
 - Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status	0	1	ID	MX	MY	WA	DE	PM7	PM6	1	Get Status	N/A
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	#	#	#	#	Set CA[7:4]	0
5	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	0
6	Set Panel Loading	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	1
7	Set Pump Control	0	0	0	0	1	0	1	1	#	#	Set PC[3:2]	11b
8	Set Adv. Program Control (double byte command)	0	0	0	0	1	1	0	0	0	R	Set APC[R][7:0], R = 0, or 1	N/A
		0	0	#	#	#	#	#	#	#	#		
9	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0
	Set Scroll Line MSB	0	0	0	1	0	1	-	#	#	#	Set SL[6:4]	0
10	Set Page Address	0	0	0	1	1	#	#	#	#	#	Set PA[4:0]	0
11	Set V <sub>BIAS</sub> Potentiometer (double-byte command)	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	B2H
		0	0	#	#	#	#	#	#	#	#		
12	Set Partial Display Control	0	0	1	0	0	0	0	1	#	#	Set LC[8:7]	00b: Disable
13	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
14	Set Fixed Lines	0	0	1	0	0	1	#	#	#	#	Set FL[3:0]	0
15	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	00b
16	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0
17	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0
18	Set Display Enable	0	0	1	0	1	0	1	1	1	#	Set DC[2]	0b
19	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	000b
20	Set LCD Gray Shade	0	0	1	1	0	1	0	0	#	#	Set LC[6:5]	00b
21	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
22	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
23	Set Test Control (double byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
		0	0	#	#	#	#	#	#	#	#		
24	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	10b: 11
25	Reset Cursor Update Mode	0	0	1	1	1	0	1	1	1	0	AC[3]=0, CA=CR	AC[3]=0
26	Set Cursor Update Mode	0	0	1	1	1	0	1	1	1	1	AC[3]=1, CR=CA	AC[3]=1
27	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[6:0]	127
		0	0	-	#	#	#	#	#	#	#		
28	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[6:0]	0
		0	0	-	#	#	#	#	#	#	#		
29	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[6:0]	127
		0	0	-	#	#	#	#	#	#	#		
30	Set Window Program Starting Column Address	0	0	1	1	1	1	0	1	0	0	Set WPC0[7:0]	0
		0	0	#	#	#	#	#	#	#	#		
31	Set Window Programming Starting Page Address	0	0	1	1	1	1	0	1	0	1	Set WPP0[4:0]	0
		0	0	-	-	-	#	#	#	#	#		
32	Set Window Programming Ending Column Address	0	0	1	1	1	1	0	1	1	0	Set WPC1[7:0]	159
		0	0	#	#	#	#	#	#	#	#		
33	Set Window Programming Ending Page Address	0	0	1	1	1	1	0	1	1	1	Set WPP1[4:0]	31
		0	0	-	-	-	#	#	#	#	#		
34	Enable window program	0	0	1	1	1	1	1	0	0	#	Set AC[4]	0: Disable

\* All other bit patterns other than the commands listed above may result in undefined behavior.

## COMMAND DESCRIPTION

### (1) WRITE DATA TO DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8bits data write to DDRAM							

### (2) READ DATA FROM DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1	8bits data from DDRAM							

Write/Read Data Byte (command 1, 2 ) operation use internal Page Address register (PA) and Column Address register (CA). Four rows of LCD pixel image are defined as one page in DDRAM. Each column of pixel corresponds to one column of DDRAM data. PA and CA registers can be programmed by issuing *Set Page Address* and *Set Column Address* commands. If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the CA boundary, and system programmers need to set the values of PA and CA explicitly. If WA is ON (1), when CA reaches end of column address, CA will be reset to 0 and PA will be incremented or decremented, depending on the setting of Row Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 31), PA will be wrapped around to the other end of RAM and continue.

### (3) GET STATUS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	1	ID	MX	MY	WA	DE	PM7	PM6	1

Status flag definitions:

*ID*: Provide access to ID pin connection status.

*MX*: Status of register LC[1], mirror X.

*MY*: Status of register LC[2], mirror Y.

*WA*: Status of register AC[0]. Automatic column/page wrap around.

*DE*: Display enable flag. DE=1 when display is enabled

### (4) SET COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address LSB CA[3:0]	0	0	0	0	0	0	CA3	CA2	CA1	CA0
Set Column Address MSB CA[7:4]	0	0	0	0	0	1	CA7	CA6	CA5	CA4

Set DDRAM column address for read/write access. Each CA corresponds to one individual SEG electrode.

CA value range: 0~159

### (5) SET TEMPERATURE COMPENSATION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Comp. TC[1:0]	0	0	0	0	1	0	0	1	TC1	TC0

Set  $V_{BIAS}$  temperature compensation coefficient (%-per-degree-C)

Temperature compensation curve definition:

00b= -0.05%/°C    01b= -0.10%/°C    10b= -0.15%/°C    11b= -0.20%/°C

**(6) SET PANEL LOADING**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Panel Loading PC[1:0]	0	0	0	0	1	0	1	0	PC1	PC0

Set PC[1:0] according to the capacitance loading of LCD panel.

Panel loading definition: 00b≤16nF      **01b=16~21nF**      10b=21~28nF      11b=28~38nF

**(7) SET PUMP CONTROL**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Pump Control PC[3:2]	0	0	0	0	1	0	1	1	PC3	PC2

Set PC[3:2] to program the build-in charge pump stages.

Pump control definition:

00b=External V<sub>LCD</sub>      01b= Internal V<sub>LCD</sub> (6X pump, for BR=5)  
 01b= Internal V<sub>LCD</sub> (7X pump)      **11b= Internal V<sub>LCD</sub> (8X pump, standard)**

**(8) SET ADVANCED PROGRAM CONTROL**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set APC[R] (Double byte command)	0	0	0	0	1	1	0	0	0	R
	0	0	APC register parameter							

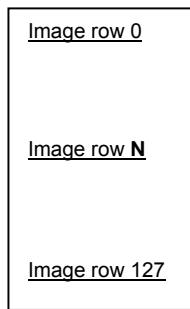
For UltraChip only. Please do NOT use.

**(9) SET SCROLL LINE**

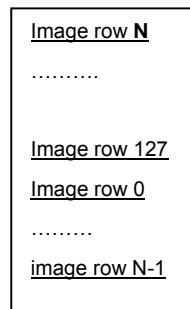
Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line LSB SL[3:0]	0	0	0	1	0	0	SL3	SL2	SL1	SL0
Set Scroll Line MSB SL[6:4]	0	0	0	1	0	1	-	SL6	SL5	SL4

Set the scroll line number.

Scroll line setting will scroll the displayed image up by SL rows. The valid value for SL is between 0 (no scrolling) and (127-2xFL). FL is the register value programmed by *Set Fixed Lines* command.



SL=0



SL=N

**(10) SET PAGE ADDRESS**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Page Address PA [4:0]	0	0	0	1	1	PA4	PA3	PA2	PA1	PA0

Set DDRAM Page Address for read/write access.

Possible value = 0~31



**(11) SET V<sub>BIAS</sub> POTENTIOMETER**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set V <sub>BIAS</sub> Potentiometer. PM [7:0] (Double byte command)	0	0	1	0	0	0	0	0	0	1
	0	0	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

Program V<sub>BIAS</sub> Potentiometer (PM[7:0]). See section LCD VOLTAGE SETTING for more detail.

Effective range: **0 ~ 255**

**(12) SET PARTIAL DISPLAY CONTROL**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Display Enable LC [8:7]	0	0	1	0	0	0	0	1	LC8	LC7

This command is used to enable partial display function.

LC[8:7] : **00b: Disable Partial Display**, Mux-Rate = CEN+1 (DST, DEN not used.)

10b: Enable Partial Display, Mux-Rate = CEN+1

11b: Enable Partial Display, Mux-Rate = DEN-DST+1

**(13) SET RAM ADDRESS CONTROL**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	1	0	0	0	1	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control.

AC[0]: WA, Automatic column/page wrap around.

0: CA or PA (depends on AC[1]= 0 or 1) will stop incrementing after reaching boundary

1: CA or PA (depends on AC[1]= 0 or 1) will restart, and PA or CA will increment by one step.

AC[1]: Auto-Increment order

0 : column (CA) increment (+1) first until CA reaches CA boundary, then PA will increment by (+/-1).

1 : row (PA) increment (+/-1) first until PA reach PA boundary, then CA will increment by (+1) .

AC[2]: PID, Page Address (PA) auto increment direction ( 0/1 = +/- 1 )

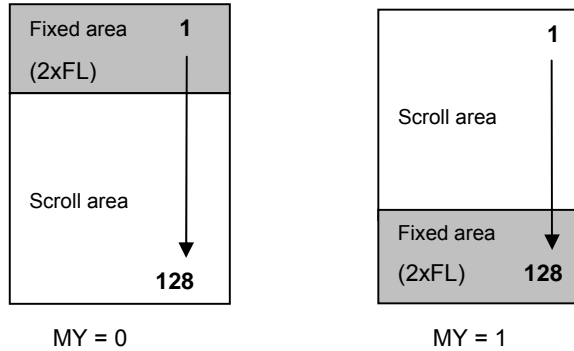
When WA=1 and CA reaches CA boundary, PID controls whether Page Address will be adjusted by +1 or -1.

AC[2:0] controls the auto-increment behavior of CA and PA. When Window Program is enabled (AC[4]=ON), see command description (32) ~ (36) for more details. When Window Program is disabled (AC[4]=OFF), the behavior of CA, PA auto-increment is the same as WPC[1:0] and WPP[1:0] values are the default values and AC[4]=ON.

**(14) SET FIXED LINES**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Fixed Lines FL [3:0]	0	0	1	0	0	1	FL3	FL2	FL1	FL0

The fixed line function is used to implement the partial scroll function by dividing the screen into scroll and fixed area. Set Fixed Lines command will define the fixed area, which will not be affected by the SL scroll function. The fixed area covers the top 2xFL rows for mirror Y (MY) is 0 and bottom 2xFL rows for MY=1. One example of the visual effect on LCD is illustrated in the figure below.



**(15) SET LINE RATE**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Line Rate LC [4:3]	0	0	1	0	1	0	0	0	LC4	LC3

Program LC [4:3] for line rate setting (Frame-Rate = Line-Rate / Mux-Rate). The line rate is automatically scaled down by 1/2 and 1/4 at Mux-Rate = 56 and 24.

The following are line rates at Mux Rate = 57~128.

LC[4:3]: **00b: 12.1 Klps**    01b: 13.4 Klps    10b: 14.7 Klps    11b: 16.6 Klps  
 (Klps: Kilo-Line-per-second)

**(16) SET ALL PIXEL ON**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON DC [1]	0	0	1	0	1	0	0	1	0	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM.

**(17) SET INVERSE DISPLAY**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	1	0	1	0	0	1	1	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM.

**(18) SET DISPLAY ENABLE**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC [2]	0	0	1	0	1	0	1	1	1	DC2

This command is for programming register DC[2].

When DC[2] is set to 0, the IC will put itself into Sleep mode. All drivers, voltage generation circuit and timing circuit will be halted to conserve power. When any of the DC[2] bits is set to 1, UC1610 will first exit from Sleep Mode, restore the power and then turn on COM drivers and SEG drivers. There is no other explicit user action or timing sequence required to enter or exit the Sleep mode.

**(19) SET LCD MAPPING CONTROL**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Mapping Control LC [2:0]	0	0	1	1	0	0	0	MY	MX	LC0

This command is used for program LC[2:0] for COM (row) mirror (MY), SEG (column) mirror (MX).

LC2 controls Mirror Y (MY): MY is implemented by reversing the mapping order between RAM and COM electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image.

LC1 controls Mirror X (MX): MX is implemented by selecting the CA or 127-CA as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data.

LC0 controls whether the soft icon section (0~ 2xFL) is display or not during partial display mode.

**(20) SET LCD GRAY SHADE**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Gray Shade [6:5]	0	0	1	1	0	1	0	0	LC6	LC5

Program gray scale register (LC[6:5]). This register controls the voltage RMS separation between the two gray shade levels (data "01" and data "10")

00b=24%      01b=29%      10b=36%      11b=40%

**(21) SYSTEM RESET**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	1	1	1	0	0	0	1	0

This command will activate the system reset. Control register values will be reset to their default values. Data stored in RAM will not be affected.

**(22) NOP**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No Operation	0	0	1	1	1	0	0	0	1	1

This command is used for "no operation".

**(23) SET TEST CONTROL**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT	0	0	1	1	1	0	0	1	TT	
(Double byte command)	0	0	Testing parameter							

This command is used for UltraChip production testing. Please do not use.

**(24) SET LCD BIAS RATIO**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [1:0]	0	0	1	1	1	0	1	0	BR1	BR0

Bias ratio definition:

00b = 5                      01b = 10                      10b = 11                      11b = 12

**(25) RESET CURSOR UPDATE MODE**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC[3]=0 CA=CR	0	0	1	1	1	0	1	1	1	AC3

This command is used to reset cursor update mode function.

**(26) SET CURSOR UPDATE MODE**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC[3]=1 CR=CA	0	0	1	1	1	0	1	1	1	AC3

This command is used for set cursor update mode function. When cursor update mode sets, UC1610 will update register CR with the value of register CA. The column address CA will increment with write RAM data operation but the address wraps around will be suspended no matter what WA setting is. However, the column address will not increment in read RAM data operation.

The set cursor update mode can be used to implement “write after read RAM” function. The column address (CA) will be restored to the value, which is before the set cursor update mode command, when reset cursor update mode.

The purpose of this pair of commands and their features is to support “write after read” function for cursor implementation.

**(27) SET COM END**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set CEN	0	0	1	1	1	1	0	0	0	1
(Double-byte command)	0	0	CEN register parameter							

This command programs the ending COM electrode. CEN defines the number of used COM electrodes, and it should correspond to the number of pixel-rows in the LCD.

**(28) SET DISPLAY START**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DST	0	0	1	1	1	1	0	0	1	0
(Double-byte command)	0	0	DST register parameter							

This command programs the starting COM electrode, which has been assigned a full scanning period, and which will output an active COM scanning pulse.

**(29) SET DISPLAY END**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DEN (Double-byte command)	0	0	1	1	1	1	0	0	1	1
	0	0	<i>DEN</i> register parameter							

This command programs the ending COM electrode, which has been assigned a full scanning period, and which will output an active COM scanning pulse.

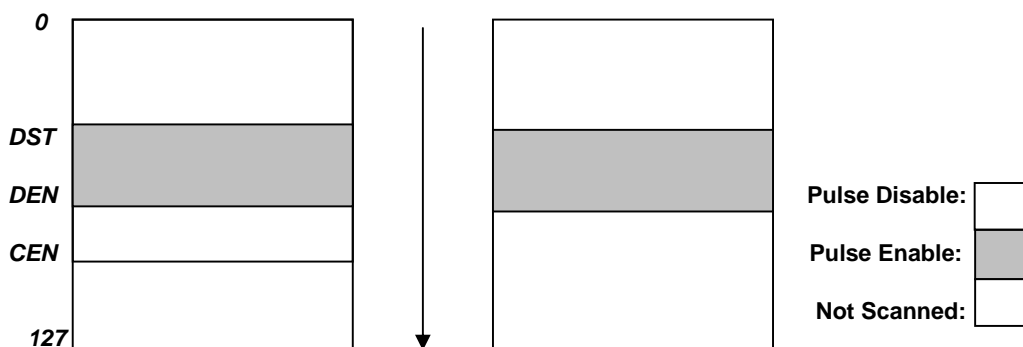
CEN, DST DEN are 0-based index of COM electrodes. They control only the COM electrode activity, and do not affect the mapping of display RAM to each COM electrodes. The image displayed by each pixel row is therefore not affected by the setting of these three registers.

When LC[8]=1, two partial display modes are possible with UC1610:

LC[7]=1: ON-OFF only, ultra-low-power mode (if Mux-Rate ≤ 32, set BR=5, PC[3:2]=01b).

LC[7]=0: Full gray shade low power mode (BR and PM stays the same)

When LC[8:7]=11b, the Mux-Rate is narrowed down to just the range between DST and DEN. When Mux-Rate is under 32, set BR=5, PC[3:2]=01b, and adjust PM to reduce  $V_{LCD}$  and achieve the lowest power consumption. When LC[8:7]=10b, the Mux-Rate is still CEN+1. This is achieved by suppressing only the scanning pulses, but not the scanning time slots, for COM electrodes that is outside of DST~DEN. Under this mode, the gray-scale quality of the display is preserved, while the power can be reduced significantly. In either case, DST/DEN defines a small subsection of the display which will remain active while shutting down all the rest of the display to conserve energy.



**(30) SET WINDOW PROGRAM STARTING COLUMN ADDRESS**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC0 (Double-byte command)	0	0	1	1	1	1	0	1	0	0
	0	0	WPC0[7:0] register parameter							

This command is to program the starting column address of RAM program window.

**(31) SET WINDOW PROGRAM STARTING PAGE ADDRESS**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP0 (Double-byte command)	0	0	1	1	1	1	0	1	0	1
	0	0	-	-	-	WPP0[4:0] register parameter				

This command is to program the starting Page Address of RAM program window.

**(32) SET WINDOW PROGRAM ENDING COLUMN ADDRESS**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC1 (Double-byte command)	0	0	1	1	1	1	0	1	1	0
	0	0	WPC1[7:0] register parameter							

This command is to program the ending column address of RAM program window.

**(33) SET WINDOW PROGRAM ENDING PAGE ADDRESS**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP1 (Double-byte command)	0	0	1	1	1	1	0	1	1	1
	0	0	-	-	-	WPP1[4:0] register parameter				

This command is to program the ending Page Address of RAM program window.

**(34) SET WINDOW PROGRAM ENABLE**

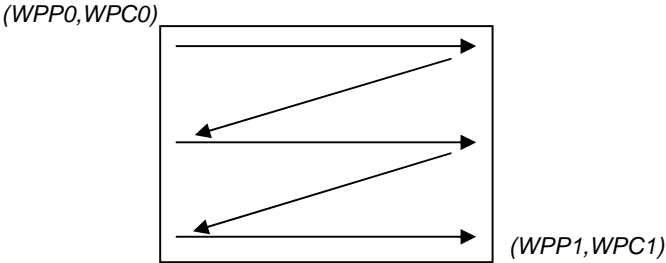
Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Window Program Enable AC[4]	0	0	1	1	1	1	1	0	0	AC4

This command is to enable the Window Program Function. Window Program Enable should always be reset when changing the window program boundary and then set right before starting the new boundary program.

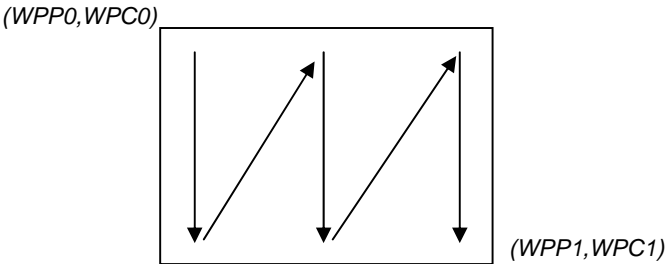
Window Program Function can be used to refresh the RAM data in a specified window of DDRAM address. When window programming is enabled, the CA and PA increment and wrap around will be automatically adjusted, and therefore allow effective data update within the window.

The direction of Window Program will depend on the WA (AC[0]), PID (AC[2]), auto-increment order (AC[1]) and MX (LC[1]) register setting. WA decides whether the program RAM address advances to next row / column after reaching the specified window column / row boundary. PID controls the RAM address incrementing from WPP0 toward WPP1 (PID=0) or reverse the direction (PID=1). Auto-increment order directs the RAM address increment vertically (AC[1]=1) or horizontally (AC[1]=0). MX results the RAM column address incrementing from 127-WPC0 to 127-WPC1 (MX=1) or WPC0 to WPC1 (MX=0).

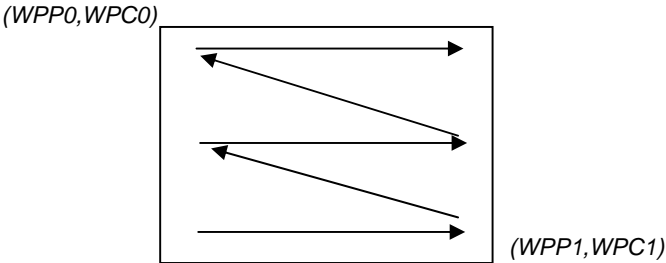
Auto-increment order = 0 MX=0 PID = 0



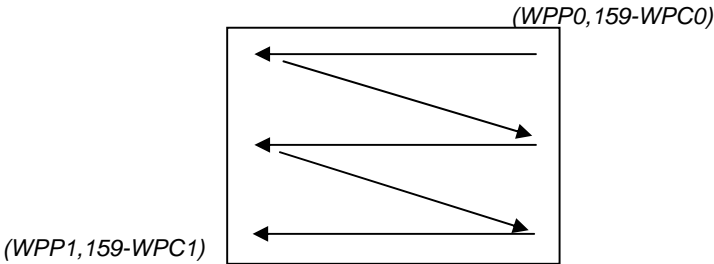
Auto-increment order = 1 MX=0 PID = 0



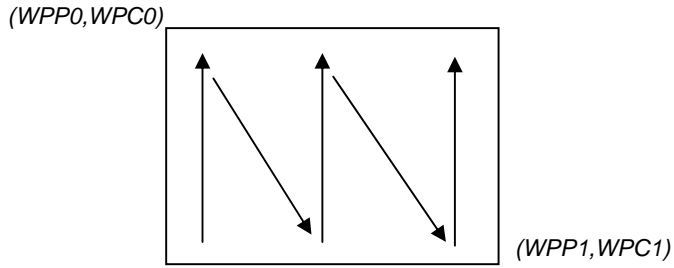
Auto-increment order = 0 MX=0 PID = 1



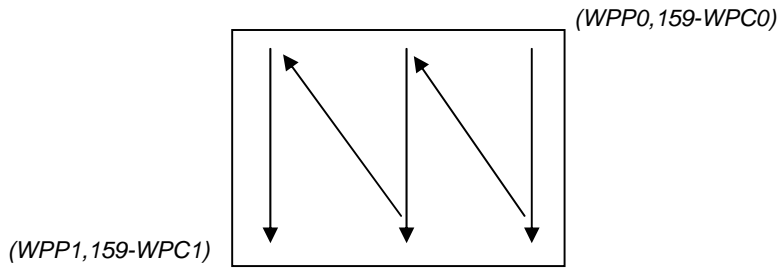
Auto-increment order = 0 MX=1 PID = 0



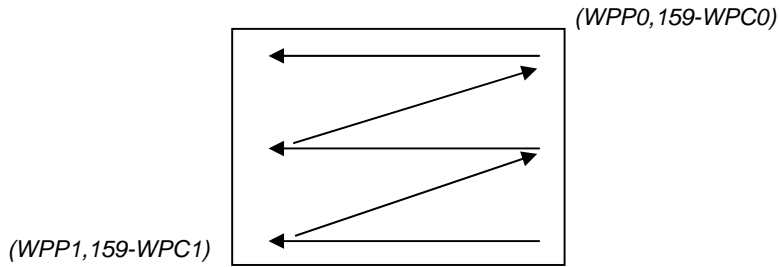
Auto-increment order = 1 MX=0 PID = 1



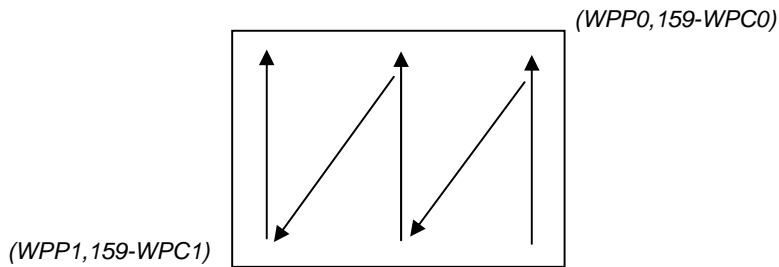
Auto-increment order = 1 MX=1 PID = 0



Auto-increment order = 0 MX=1 PID = 1



Auto-increment order = 1 MX=1 PID = 1





## LCD VOLTAGE SETTING

### MULTIPLEX RATES

Multiplex Rate is completely software programmable in UC1610 via registers CEN, DST, DEN, and partial display control LC[8:7].

Combined with low power partial display mode and a low bias ratio of 5, UC1610 can support wide variety of display control options. For example, when a system goes into stand-by mode, a large portion of LCD screen can be turned off to conserve power.

### BIAS RATIO SELECTION

Bias Ratio (*BR*) is defined as the ratio between  $V_{LCD}$  and  $V_{BIAS}$ , i.e.

$$BR = V_{LCD} / V_{BIAS},$$

where  $V_{BIAS} = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$ .

The theoretical optimum *Bias Ratio* can be estimated by  $\sqrt{Mux} + 1$ . *BR* of value 15~20% lower/higher than the optimum value calculated above will not cause significant visible change in image quality.

Due to the nature of STN operation, an LCD designed for good gray-shade performance at high Mux Rate (e.g. MR=128), can generally perform very well as a black and white display, at lower Mux Rate. However, it is also true that such technique generally cannot maintain LCD's quality of gray shade performance, since the contrast of the LCD will increase as the Mux Rate decreases, and the shades near the two ends of the spectrum will start to lose visibility.

UC1610 supports four *BR* as listed below. *BR* can be selected by software program.

BR	0	1	2	3
Bias Ratio	5	10	11	12

Table 1: Bias Ratios

### TEMPERATURE COMPENSATION

Four (4) different temperature compensation coefficients can be selected via software. The four coefficients are given below:

TC	0	1	2	3
% per °C	-0.05	-0.10	-0.15	-0.20

Table 2: Temperature Compensation

### V<sub>LCD</sub> GENERATION

$V_{LCD}$  may be supplied either by internal charge pump or by external power supply. The source of  $V_{LCD}$  is controlled by PC[3:2]. For good product reliability, it is recommended to keep  $V_{LCD}$  under 15V over the entire operating range.

When  $V_{LCD}$  is generated internally, the voltage level of  $V_{LCD}$  is determined by three control registers: *BR* (Bias Ratio), *PM* (Potentiometer), and *TC* (Temperature Compensation), with the following relationship:

$$V_{LCD} = (C_{V0} + C_{PM} \times PM) \times (1 + (T - 25) \times C_T \%)$$

where

$C_{V0}$  and  $C_{PM}$  are two constants, whose value depends on the setting of *BR* register, as illustrated in the table on the next page,

*PM* is the numerical value of *PM* register,

*T* is the ambient temperature in °C, and

$C_T$  is the temperature compensation coefficient as selected by *TC* register.

### V<sub>LCD</sub> FINE TUNING

Gray shade and color STN LCD is sensitive to even a 1% mismatch between IC driving voltage and the  $V_{OP}$  of LCD. However, it is difficult for LCD makers to guarantee such high precision matching of parts from different vendors. It is therefore necessary to adjust  $V_{LCD}$  to match the actual  $V_{OP}$  of the LCD.

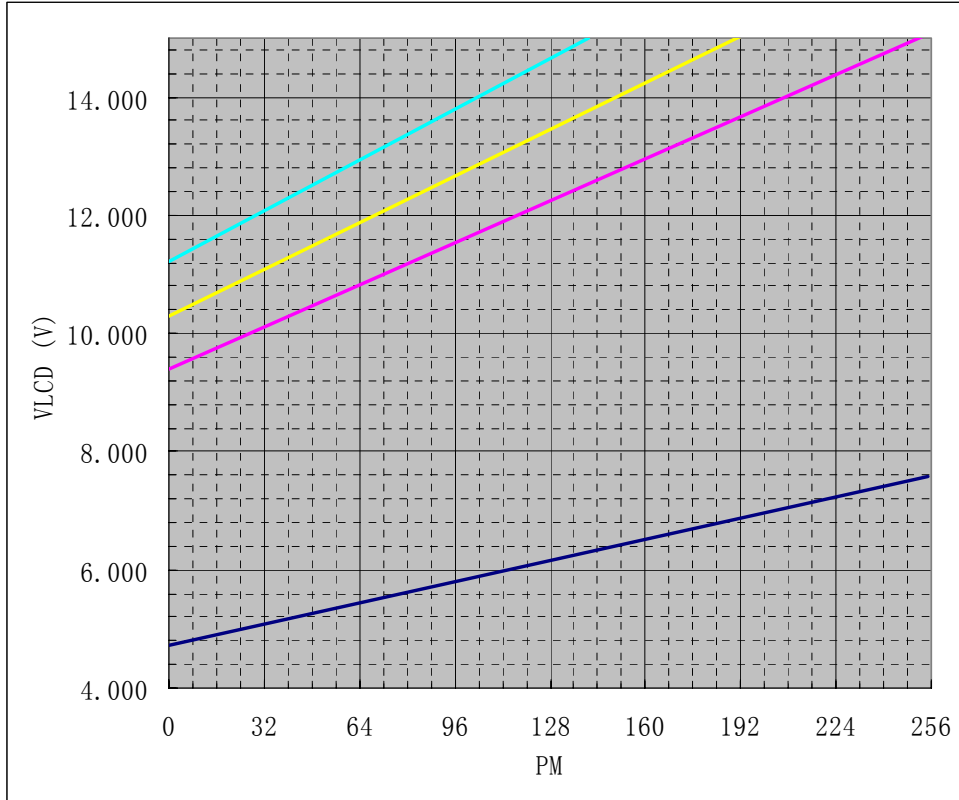
For the best result, software based approach for  $V_{LCD}$  adjustment is the recommended method for  $V_{LCD}$  fine tuning.

For applications where mechanical manual fine tuning of  $V_{LCD}$  becomes necessary, then  $V_{BIAS}$  pin may be used with an external trim pot to fine tune the  $V_{LCD}$ . Please refer to Application Notes for more detailed discussion on this subject.

### LOAD DRIVING STRENGTH

The power supply circuit of UC1610 is designed to handle LCD panels with load capacitance up to ~30nF when  $V_{DD2} = 2.7V$ . 30nF is also the recommended limit for LCD panel size for COG applications. For larger LCD panels, use higher  $V_{DD}$ .

**V<sub>LCD</sub> QUICK REFERENCE**



V<sub>LCD</sub> Relationship to BR and PM at 25 °C

BR	C <sub>vo</sub> (V)	C <sub>PM</sub> (mV)	PM	V <sub>LCD</sub> (V)
5	4.728	11.234	0	4.728
			255	7.592
10	9.390	22.235	0	9.390
			253	15.015
11	10.308	24.529	0	10.308
			192	15.018
12	11.228	26.844	0	11.228
			141	15.013

**Note:** For best reliability, keep V<sub>LCD</sub> under 15V over all temperature.

## HI-V GENERATOR AND BIAS REFERENCE CIRCUIT

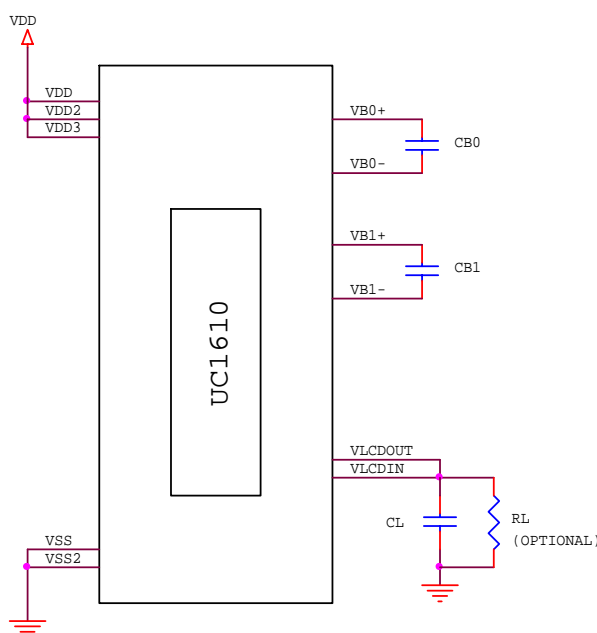


FIGURE 1: Reference circuit using internal Hi-V generator circuit

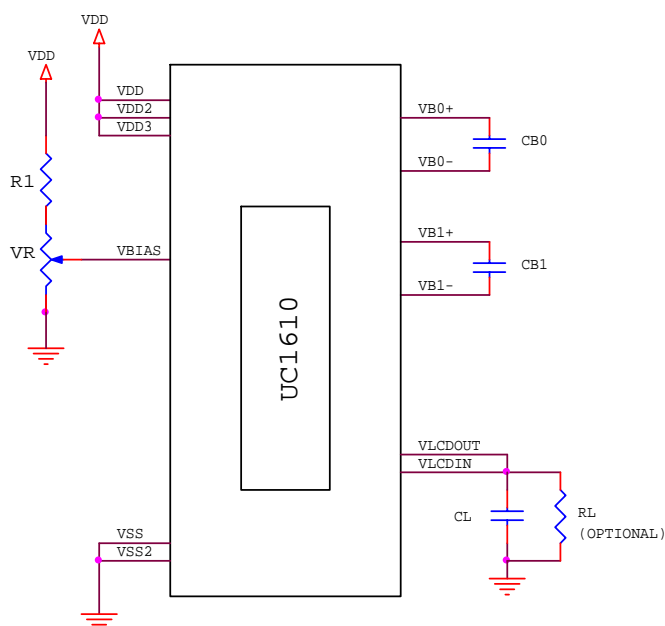


FIGURE 2: Reference circuit using external Bias source

**Note**

- Sample component values: (The illustrated circuit and component values are for reference only. Please optimize for specific requirements of each application.)
  - CB: 150 ~ 250x LCD load capacitance or 2 $\mu$ F (2V), whichever is higher.
  - CL: 0.06  $\mu$ F ~ 0.3 $\mu$ F (16V) is appropriate for most applications.
  - RL: 10M $\Omega$ . Acts as a draining circuit when the power is abnormally shut down.
  - VR: 1M $\Omega$
  - R1: 330k $\Omega$

## LCD DISPLAY CONTROLS

### CLOCK & TIMING GENERATOR

UC1610 contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

Four different line rates are provided for system design flexibility. The line rate is controlled by register LC[4:3]. When Mux-Rate is above 56, frame rate is calculated as:

$$\text{Frame Rate} = \text{Line-Rate} / \text{Mux-Rate.}$$

When Mux-Rate is lowered to 56 (and 24), line rate will be scaled down by 2 (and 4) times automatically to reduce power consumption.

Flicker-free frame rate is dependent on LC material and gray-shade modulation scheme. Choose lower frame rate for lower power, and choose higher frame rate to improve LCD contrast and minimize flicker.

When fast LC material with  $(t_r + t_f) < 160\text{ms}$  is used, faster line rate may be required under 4-shade mode to maintain good contrast ratio at operating temperature  $>50^\circ\text{C}$ .

### DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When COM drivers are in idle mode, their outputs are high-impedance (open circuit). When SEG drivers are in idle mode, their outputs are shorted to  $V_{SS}$ .

### DRIVER ARRANGEMENTS

The naming conventions are: COM(x), where  $x=1\sim 128$ , refers to the COM driver for the x-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows fixed and it is not affected by SL, CST, CEN, DST, DEN, MX or MY settings.

### DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

### DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2] via *Set Display Enable* command. When DC[2] is set to OFF (logic "0"), both COM and SEG drivers will become idle and UC1610 will put itself into Sleep Mode to conserve power.

When DC[2] is set to ON, the DE flag will become "1", and UC1610 will first exit from Sleep Mode, restore the power ( $V_{LCD}$ ,  $V_D$  etc.) and then turn on COM and SEG drivers.

### ALL PIXELS ON (APO)

When set, this flag will force all SEG drivers to output ON signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

### INVERSE (PXV)

When this flag is set to ON, SEG drivers will output the inverse of the value it received from the display buffer RAM (bit-wise inversion). This flag has no impact on data stored in RAM.

### PARTIAL SCROLL

Control register FL specifies a region of rows which are not affected by the SL register. Since SL register can be used to implement scroll function. The FL register can be used to implement fixed region when the other part of the display is scrolled by SL.

### PARTIAL DISPLAY

UC1610 provides flexible control of Mux Rate and active display area. Please refer to command description (28) ~ (30) for more detail.

### GRAY-SHADE MODULATION

UC1610 uses a proprietary frame rate modulation scheme to generate 4 levels of gray shade. The relative levels of the gray shades can be programmed by setting register bit LC[6:5]. It controls the relative position of the light gray and dark gray shades. For detailed value, please refer to the register definition table.

## ITO LAYOUT CONSIDERATIONS

Since the COM scanning pulses of UC1610 can be as short as 44 $\mu$ S, it is critical to control the RC delay of COM and SEG signal to minimize crosstalk and maintain good mass production consistency.

For COG applications, low resistance ITO glass will help reduce SEG signal RC decay, minimize  $V_{DD}$ ,  $V_{SS}$  noise, and ensure sufficient  $V_{DD2}$ ,  $V_{SS2}$  supply for on-chip DC-DC converter.

### ITO TRACES FOR COM SIGNALS

Excessive COM scanning pulse RC decay can cause fluctuation of contrast and increase of COM direction crosstalk.

Please limit the worst case of COM signals RC delay ( $RC_{MAX}$ ) as calculated below

$$(R_{ROW} / 2.7 + R_{COM}) \times C_{ROW} < 2.6\mu S$$

where

- $C_{ROW}$ : LCD loading capacitance of one row of pixels. It can be calculated by  $C_{LCD}/\text{Mux-Rate}$ , where  $C_{LCD}$  is the LCD panel capacitance.
- $R_{ROW}$ : ITO resistance over one row of pixels within the active area
- $R_{COM}$ : COM routing resistance from IC to the active area + COM driver output impedance.

(Use worst case values for all calculations)

In addition, please limit the min-max spread of RC decay to be:

$$|RC_{MAX} - RC_{MIN}| < 1\mu S$$

so that the COM distortions on the top of the screen to the bottom of the screen are uniform.

### ITO TRACES FOR SEG SIGNALS

Excessive SEG signal RC decay can cause image dependent changes of medium gray shades and sharply increase of SEG direction crosstalk.

To minimize crosstalk, please limit the worst case of SEG signal RC delay as calculated below.

$$(R_{COL} / 2.7 + R_{SEG}) \times C_{COL} < 0.35\mu S$$

where

- $C_{COL}$ : LCD loading capacitance of one pixel column. It can be calculated by  $C_{LCD}/\#\_column$ , where  $C_{LCD}$  is the LCD panel capacitance.
- $R_{COL}$ : ITO resistance over one column of pixels within the active area
- $R_{SEG}$ : SEG routing resistance from IC to the active area + SEG driver output impedance.

(Use worst case values for all calculations)

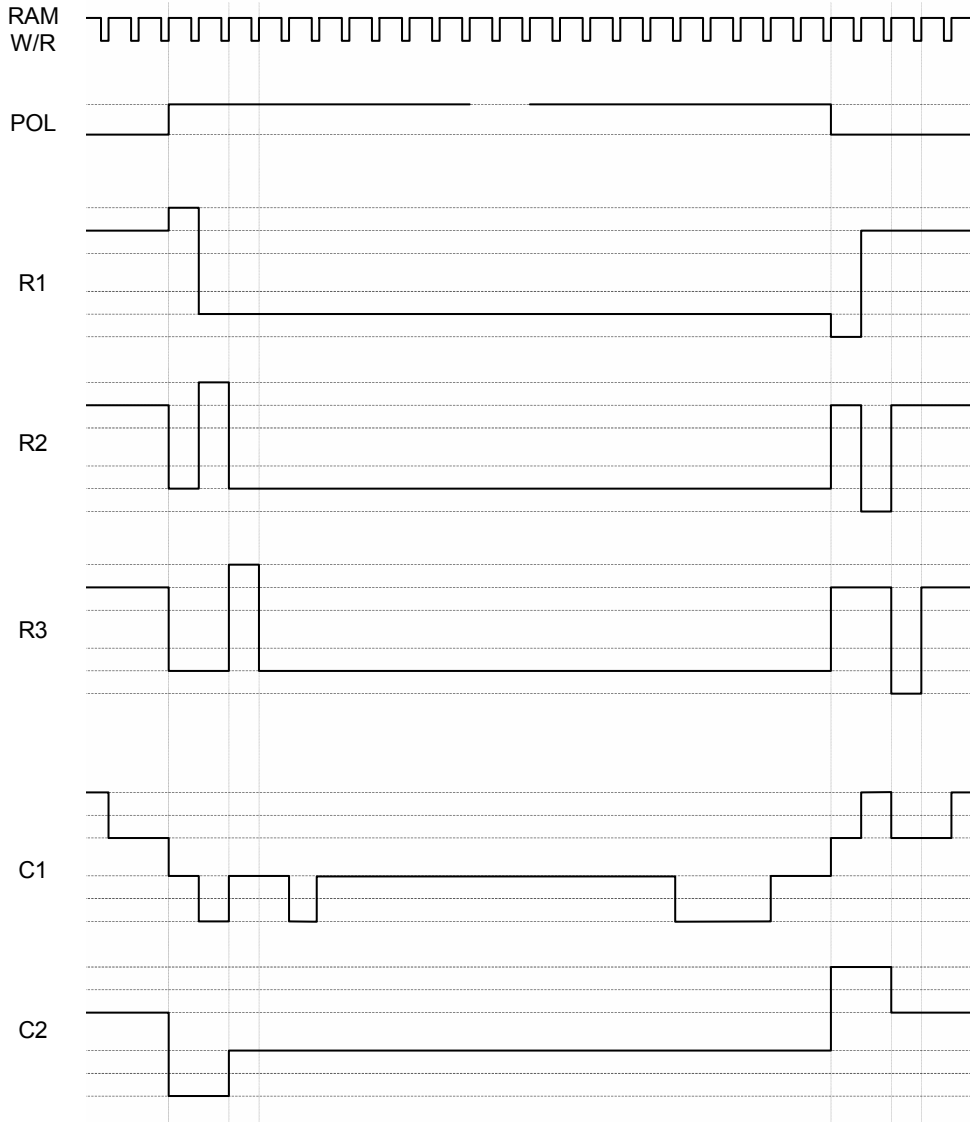


FIGURE 3: COM and SEG Driving Waveform

## HOST INTERFACE

As summarized in the table below, UC1610 supports two parallel bus protocols, in either 8-bit or 4-bit bus width, and four serial bus protocols.

Designers can either use parallel bus to achieve high data transfer rate, or use serial bus to create compact LCD modules.

Bus Type		8080		6800		S8 (4wr)	S8uc (3wr)	S9 (3wr)	I <sup>2</sup> C	
Width		8-bit	4-bit	8-bit	4-bit	Serial				
Access		Read/Write				Write Only			R/W	
Control & Data Pins	BM[1:0]	10	00	11	01	00		01		
	D[7:6]	Data	00	Data	00	10	11	10	11	
	CS[1:0]	Chip Select							A[3:2]	
	CD	Control/Data							-	
	WR0	$\overline{WR}$		$R/\overline{W}$		1	1	0	1	
	WR1	$\overline{RD}$		EN		1	1	0	1	
	D[5:4]	Data	-	Data	-	-				
	D[3:0]	Data	Data	Data	Data	D0=SCK, D3=SDA				

\* Connect unused control pins and data bus pins to V<sub>DD</sub> or V<sub>SS</sub>.

**Table 3:** Host interfaces Choices

**PARALLEL INTERFACE**

The timing relationship between UC1610 internal control signals, RD and WR, and their associated bus actions are shown in the figure below.

The Display RAM read interface is implemented as a two-stage pipe-line. This architecture requires that, every time memory address is modified, either in 8-bit mode or 4-bit mode, by either *Set CA*, or *Set PA* command, a dummy read cycle need to be performed before the actual data can propagate through the pipe-line and be read from data port D[7:0].

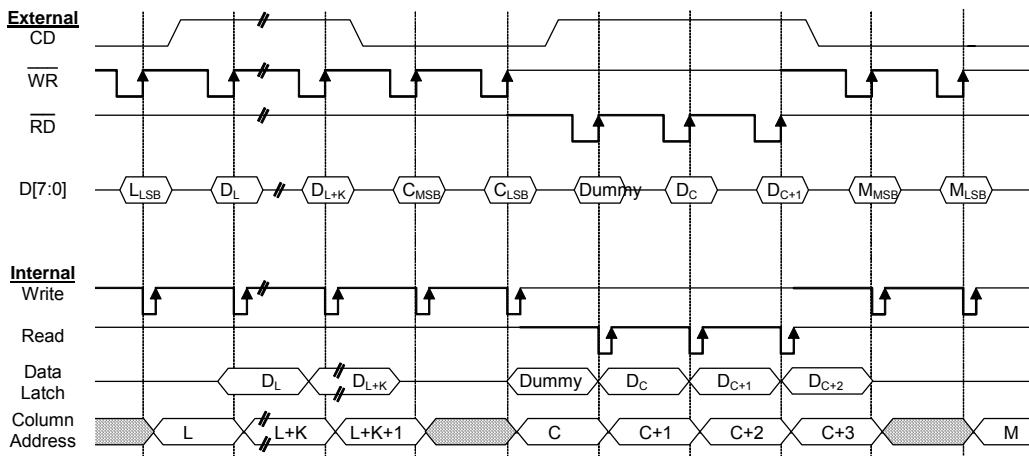
There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

**8-BIT & 4-BIT BUS OPERATION**

UC1610 supports both 8-bit and 4-bit bus width. The bus width is determined by pin BM[1].

4-bit bus operation exactly doubles the clock cycles of 8-bit bus operation, MSB followed by

LSB, including the dummy read, which also requires two clock cycles. The bus cycle of 4-bit mode is reset each time Chip-Select or CD pin changes state.



**FIGURE 4: 8 bit Parallel Interface & Related Internal Signals**



**SERIAL INTERFACE**

UC1610 supports three serial modes, one 4-wire SPI mode (S8), one compact 3/4-wire mode (S8uc) and one 3-wire SPI mode (S9). Bus interface mode is determined by the wiring of the BM[1:0] and D[7:6]. See table in last page for more detail.

**S8 (4-WIRE) INTERFACE**

Only write operations are supported in 4-wire serial mode. Pin CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse. Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

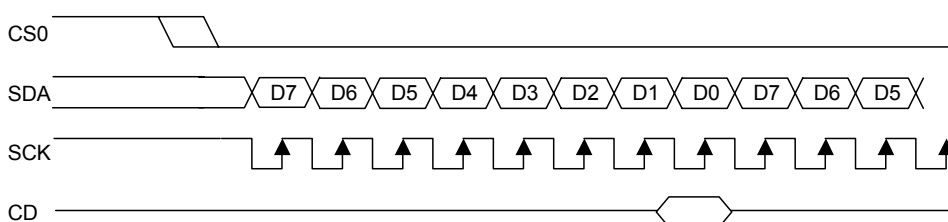


FIGURE 5.a: 4-wire Serial Interface (S8)

**S8UC (3/4-WIRE) INTERFACE**

Only write operations are supported in this 3/4-wire serial mode. The data format is identical as S8. However, in addition to CS pins, CD pin transitions

will also reset the bus cycle in this mode. So, if CS pins are hardwired to enable chip-select, the bus can work properly with only three signal pins.

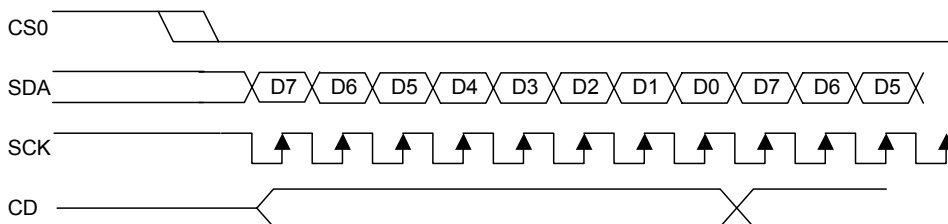


FIGURE 5.b: 3/4-wire Serial Interface (S8uc)

**S9 (3-WIRE) INTERFACE**

Only write operations are supported in this 3-wire serial mode. Pin CS[1:0] are used for chip select and bus cycle reset. On each write cycle, the first bit is CD, which determines the content of the following 8 bits of data, MSB first. These 8 command or data bits are latched on rising SCK edges into an 8-bit data holder. If CD=0, the data byte will be decoded as command. If CD=1, this

8-bit will be treated as data and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse.

By sending CD information explicitly in the bit stream, control pin CD is not used, and should be connected to either V<sub>DD</sub> or V<sub>SS</sub>. The toggle of CS0 or CS1 for each byte of data/command is recommended but optional.

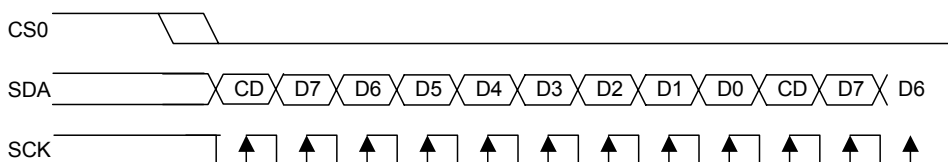


FIGURE 5.c: 3-wire Serial Interface (S9)

**2-WIRE SERIAL INTERFACE (I<sup>2</sup>C)**

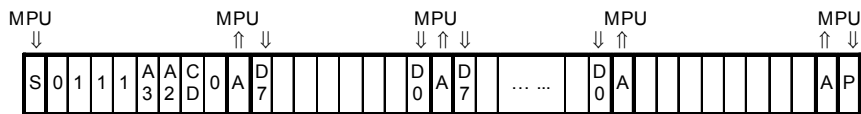
When BM[1:0] is set to “LH” and D[7:6] is set to “HH”, UC1610 is configured as an I<sup>2</sup>C bus signaling protocol compliant slave device. Please refer to I<sup>2</sup>C standard for details of the bus signaling protocol, and AC Characteristic section for timing parameters of UltraChip implementation.

In this mode, pins CS[1:0] become A[3:2] and is used to configure UC1610's device address. Proper wiring to V<sub>DD</sub> or V<sub>SS</sub> is required for the IC to operate properly for I<sup>2</sup>C mode.

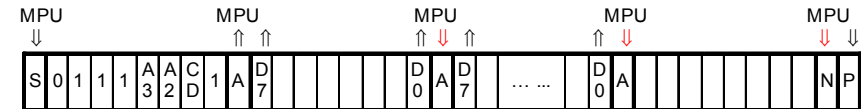
Each UC1610 I<sup>2</sup>C interface sequence starts with a START condition (S) from the bus master, followed by a sequence header, containing a device address, the mode of transfer (CD, 0:Control, 1:Data), and the direction of the transfer (RW, 0:Write, 1:Read).

Since both WR and CD are expressed explicitly in the header byte, the control pins WR[1:0] and CD are not used in I<sup>2</sup>C mode and should be connected to V<sub>SS</sub>.

**Write Mode**



**Read Mode**

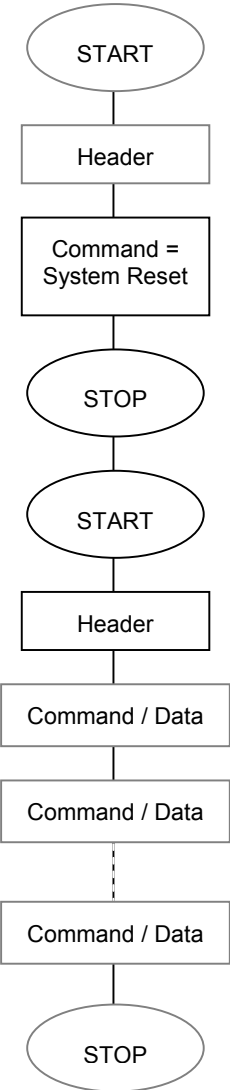


The direction (read or write) and content type (command or data) of the data bytes following each header byte are fixed for the sequence. To change the direction (R↔W) or the content type (C↔D), start a new sequence with a START (S) flag, followed by a new header.

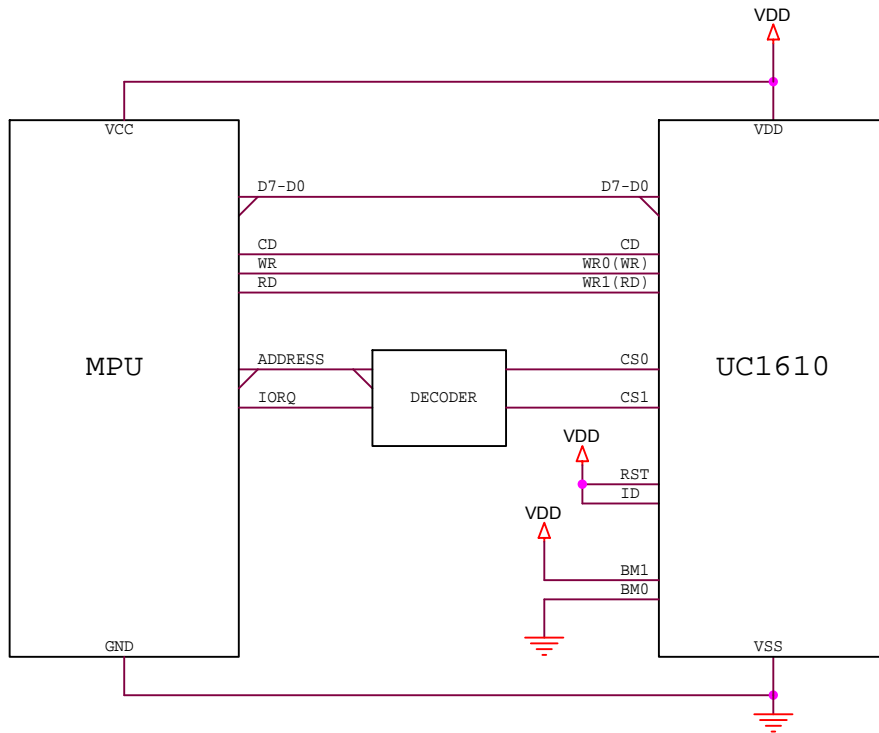
After receiving the header, the UC1610 will send out an acknowledge signal (A). Then, depends on the setting of the header, the transmitting device (either the bus master or UC1610) will start placing data bits on SDA, MSB to LSB, and the sequence will repeat until a STOP signal (P, in WRITE), or a Not Acknowledge (N, in READ mode) is sent by the bus master.

When using I<sup>2</sup>C serial mode, if the command of System Reset is to be written, the writing sequence must be finished (STOP) before succeeding data or commands start. The flow chart on the right shows a writing sequence with a "System Reset" command.

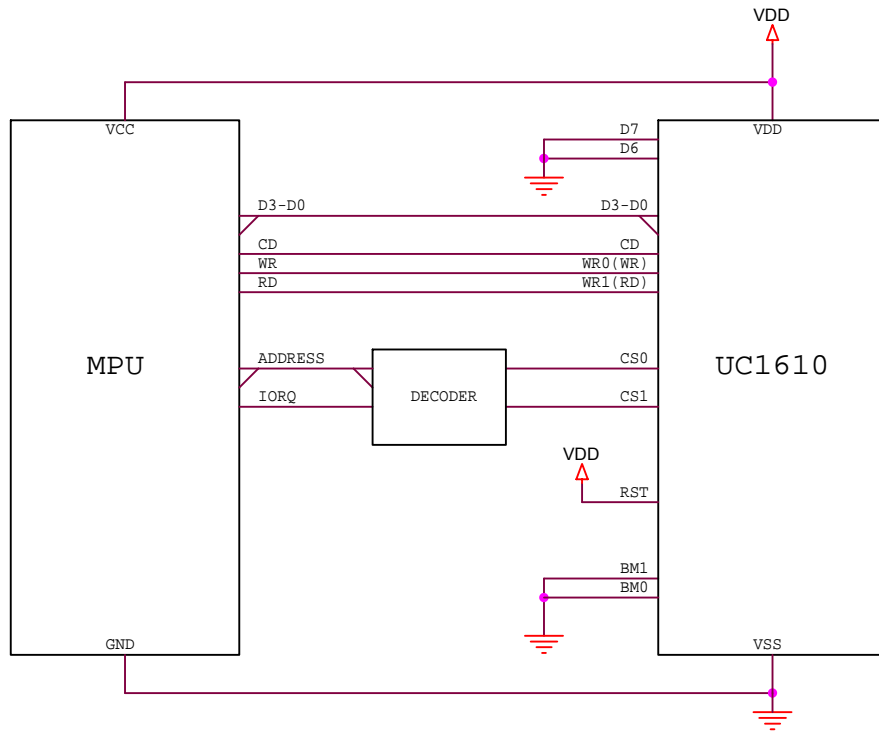
Note that, for data read (CD=1), the first byte of data transmitted will be dummy.



**HOST INTERFACE REFERENCE CIRCUIT**



**FIGURE 6: 8080/8bit parallel mode reference circuit**



**FIGURE7: 8080/4bit parallel mode reference circuit**

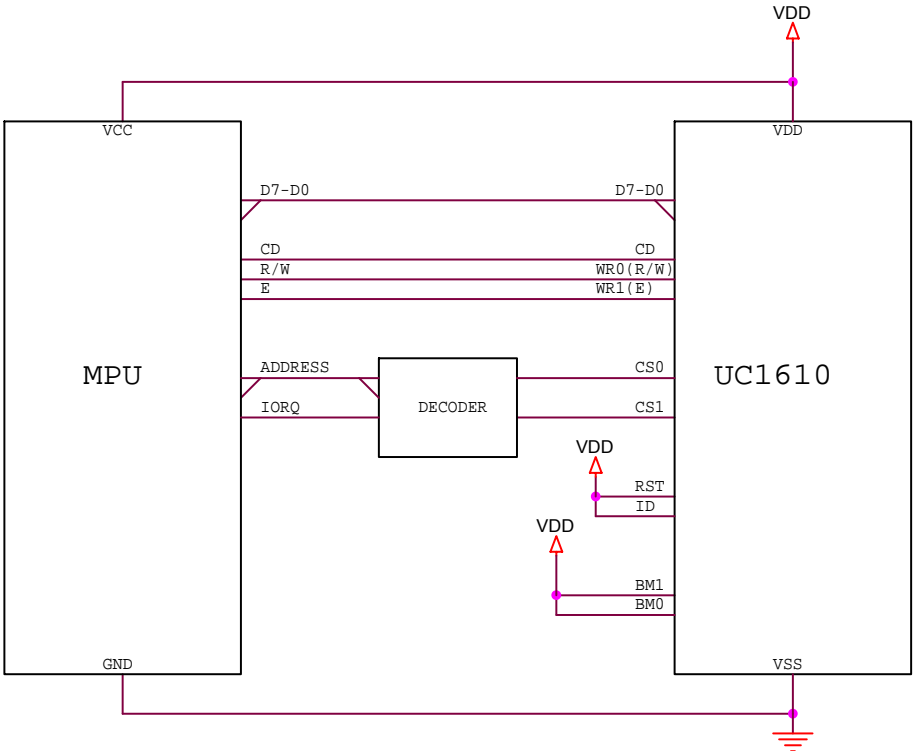


FIGURE 8: 6800/8bit parallel mode reference circuit

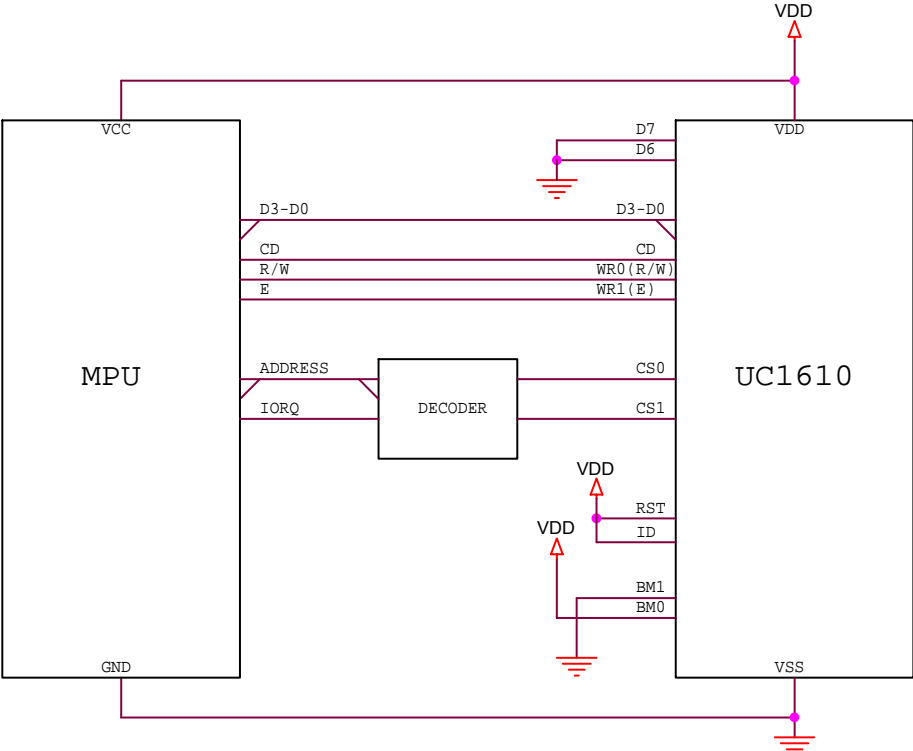


FIGURE 9: 6800/4bit parallel mode reference circuit

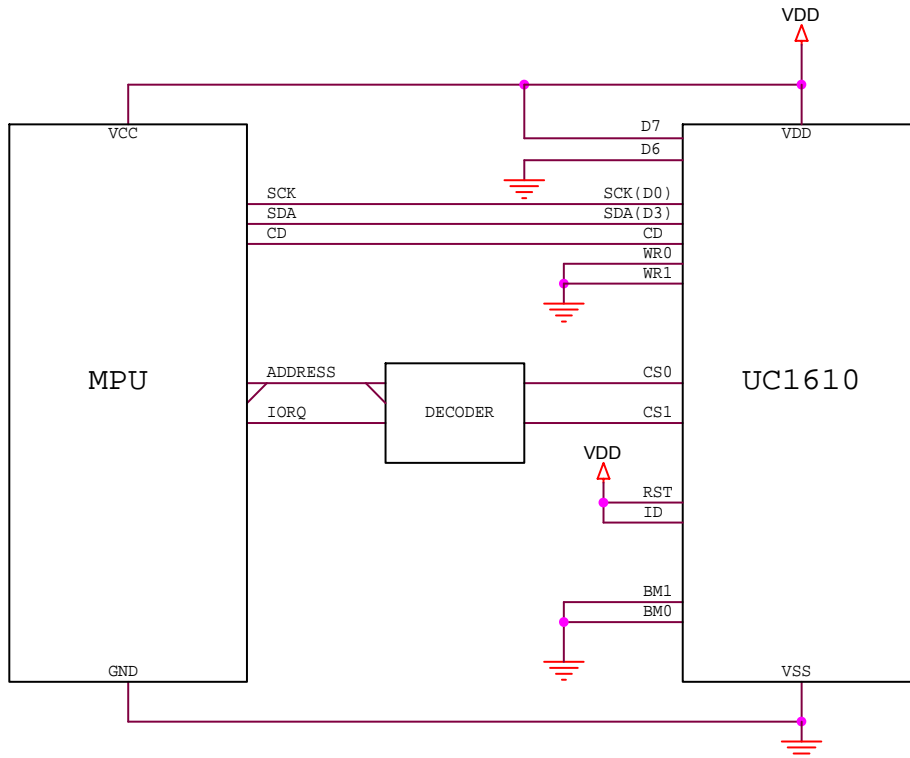


FIGURE 10: 4-Wires SPI (S8) serial mode reference circuit

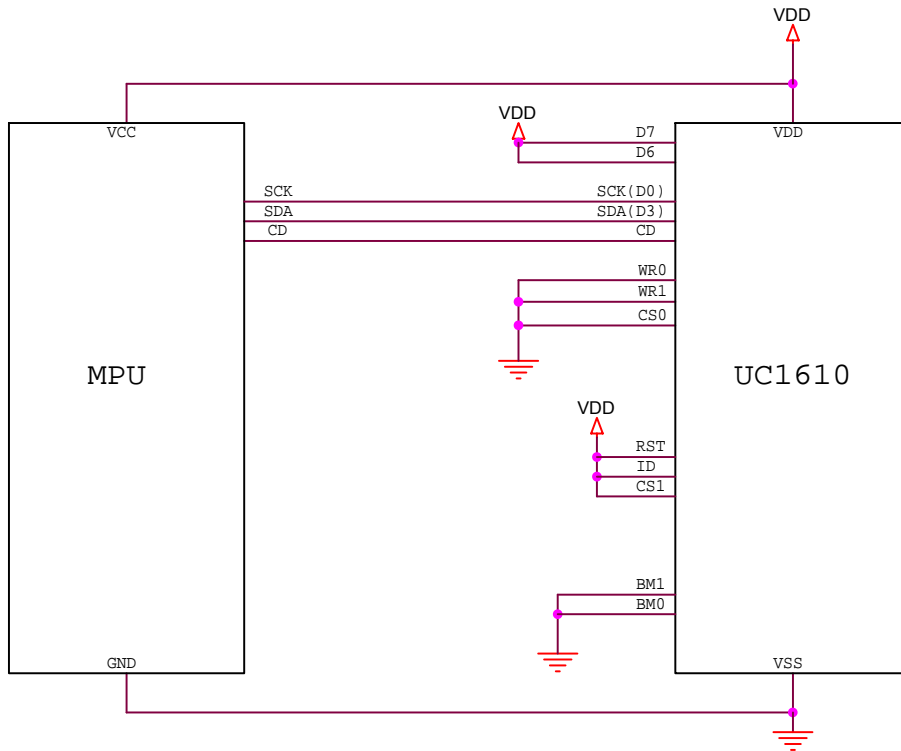


FIGURE 11: 3/4-Wires SPI (S8uc) serial mode reference circuit

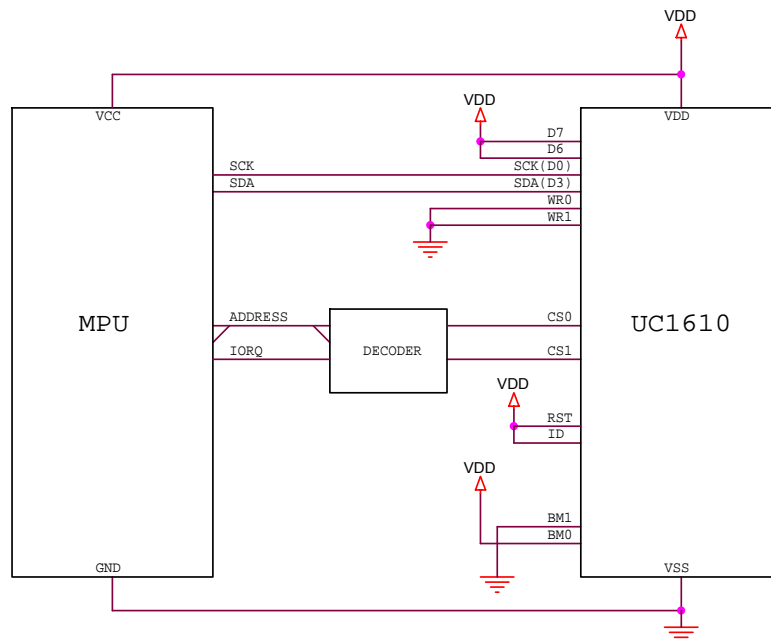


FIGURE 12: 3-Wires SPI (S9) serial mode reference circuit

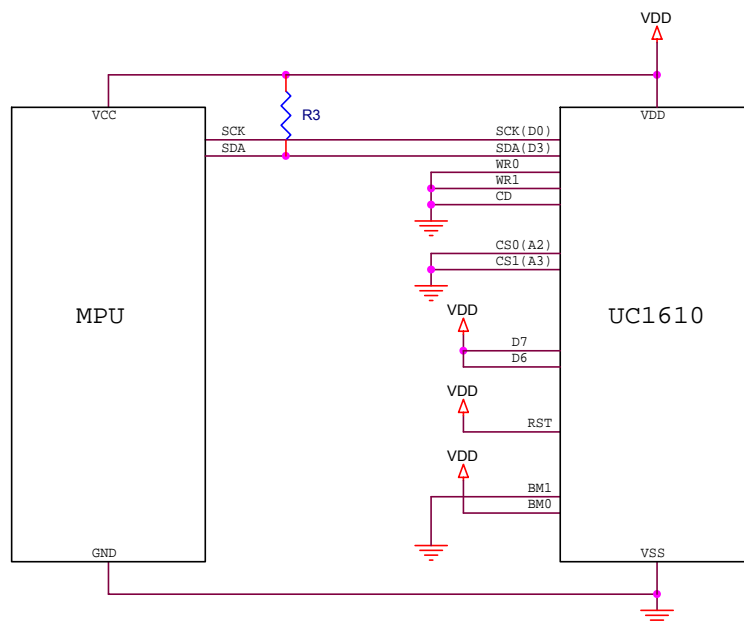


FIGURE 13: I<sup>2</sup>C serial mode reference circuit

**Note**

- ID pin is for production control. The connection will affect the content of D[7] when using *Get Status* command. Connect to V<sub>DD</sub> for “H” or V<sub>SS</sub> for “L”.
- RST pin is optional. When RST pin is not used, connect the pin to V<sub>DD</sub>.
- When using I2C serial mode, CS0/1 are user configurable and affect A[3:2] of device address.
- R3: 2k Ω ~ 10 k Ω, use lower resistor for bus speed up to 4MHz, use higher resistor for lower power.

## DISPLAY DATA RAM

### DATA ORGANIZATION

The input display data is stored to a dual port static RAM (RAM, for Display Data RAM) organized as 128x160x2.

After setting CA and PA, the subsequent data write cycles will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page between the relation of COM, SEG, DDRAM, and various memory control registers.

### DISPLAY DATA RAM ACCESS

The Display RAM is a special purpose dual port RAM which allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

### DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Page Address (PA) and Column Address (CA) by issuing *Set Page Address* and *Set Column Address* commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the end of row (127), and system programmers need to set the values of PA and CA explicitly.

If WA is ON (1), when CA reaches end of page, CA will be reset to 0 and PA will increment or decrement, depending on the setting of row Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 31), PA will be wrapped around to the other end of RAM and continue.

### MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (159-CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect of the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

### ROW MAPPING

COM electrode scanning orders are not affected by Start Line (SL), Fixed Line (FL) or Mirror Y (MY, LC[3]). Visually, register SL having a non-zero value is equivalent to scrolling the LCD display up or down (depends on MY) by SL rows.

### RAM ADDRESS GENERATION

The mapping of the data stored in the display DDRAM and the scanning COM electrodes can be obtained by combining the fixed COM scanning sequence and the following RAM address generation formula.

When FL=0, during the display operation, the RAM line address generation can be mathematically represented as following:

For the 1<sup>st</sup> line period of each field  
 $Line = SL$

Otherwise  
 $Line = Mod(Line+1, 128)$

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to SEG drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produces the "loop around" effect as it effectively resets *Line* to 0 when *Line+1* reaches 128. Effects such as page scrolling, page swapping can be emulated by changing SL dynamically.

### MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between COM electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1<sup>st</sup> line period of each field  
 $Line = Mod(SL + MUX-1, 128)$   
 where MUX = CEN + 1

Otherwise  
 $Line = Mod( Line-1 , 128)$

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM is not affected by MY.



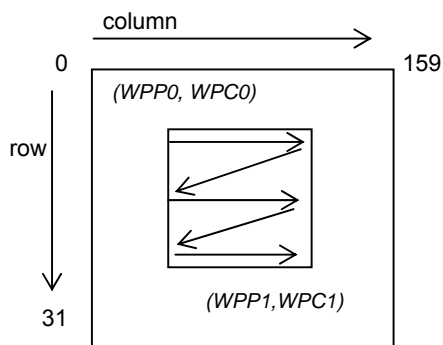
**WINDOW PROGRAM**

Window program is designed for data write in a specified window range of DDRAM address. The procedure should start with window boundary registers setting (*WPP0*, *WPP1*, *WPC0* and *WPC1*) and then enable AC[4]. After AC[4] sets, data can be written to DDRAM within the window address range which is specified by (*WPP0*, *WPC0*) and (*WPP1*, *WPC1*). AC[4] should be cleared after any modification of window boundary registers and then set again in order to initialize another window program.

The data write direction will be determined by AC[2:0] and MX settings. When AC[0]=1, the data write can be consecutive within the range of the specified window. AC[1] will control the data write in either column or row direction. AC[2] will result the data write starting either from row *WPP0* or *WPP1*. MX is for the initial column address either from *WPC0* to *WPC1* or from (*MC-WPC0* to *MC-WPC1*).

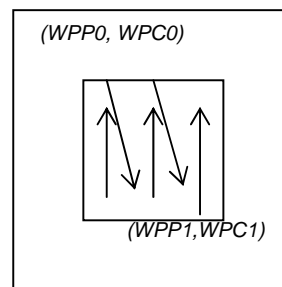
**Example 1:**

AC[2:0] = 001 MX=0



**Example 2:**

AC[2:0] = 111 MX = 0





## RESET & POWER MANAGEMENT

### TYPES OF RESET

UC1610 has two different types of Reset: *Power-ON-Reset* and *System-Reset*.

*Power-ON-Reset* is performed right after  $V_{DD}$  is connected to power. *Power-On-Reset* will first wait for about ~5mS, depending on the time required for  $V_{DD}$  to stabilize, and then trigger the *System Reset*.

*System Reset* can also be activated by software command or by connecting RST pin to ground.

In the following discussions, Reset means *System Reset*.

### RESET STATUS

When UC1610 enters RESET sequence:

- Operation mode will be "Reset"
- System Status bits RS and BZ will stay as "1" until the Reset process is completed. When RS=1, the IC will only respond to *Read Status* command. All other commands are ignored.
- All control registers are reset to default values. Refer to Control Registers for details of their default values.

### OPERATION MODES

UC1610 has three operating modes (OM): Reset, Normal, Sleep.

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	ON	OFF

**Table 4:** Operating Modes

### CHANGING OPERATION MODE

In addition to Power-ON-Reset, two commands will initiate OM transitions:

*Set Display Enable*, and *System Reset*.

When DC[2] is modified by *Set Display Enable*, OM will be updated automatically. There is no other action required to enter Sleep Mode.

OM changes are synchronized with the edges of UC1610 internal clock. To ensure consistent system states, wait at least 10 $\mu$ S after *Set Display Enable* or *System Reset* command.

Action	Mode	OM
Reset command RST_ pin pulled "L" Power ON reset	Reset	00
Set Driver Enable to "0"	Sleep	10
Set Driver Enable to "1"	Normal	11

**Table 5:** OM changes

Both Reset mode and Sleep mode drain the charges stored in the external capacitors  $C_{B0}$ ,  $C_{B1}$ , and  $C_L$ . When entering Reset mode or Sleep mode, the display drivers will be disabled.

The difference between Sleep mode and Reset mode is that, Reset mode clears all control registers and restores them to default values, while Sleep mode retains all the control registers values set by the user.

It is recommended to use Sleep Mode for Display OFF operations as UC1610 consumes very little energy in Sleep mode (typically under 2 $\mu$ A).

### EXITING SLEEP MODE

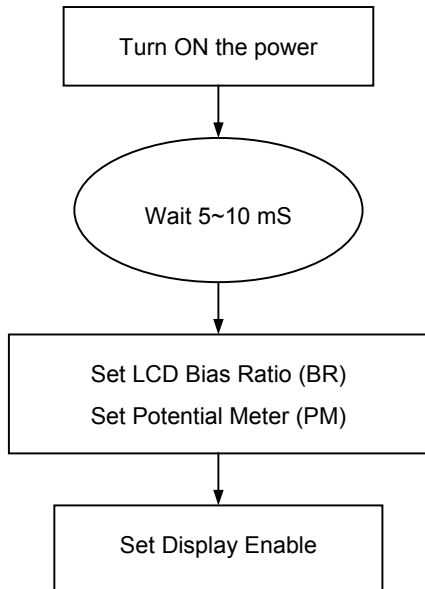
UC1610 contains internal logic to check whether  $V_{LCD}$  and  $V_{BIAS}$  are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset mode, COM and SEG drivers will not be activated until UC1610 internal voltage sources are restored to their proper values.

**POWER-UP SEQUENCE**

UC1610 power-up sequence is simplified by built-in "Power Ready" flags and the automatic invocation of *System-Reset* command after *Power-ON-Reset*.

System programmers are only required to wait 5~10 mS before the CPU starting to issue commands to UC1610. No additional time sequences are required between enabling the charge pump, turning on the display drivers, writing to RAM or any other commands. However, while turning on  $V_{DD}$ ,  $V_{DD2/3}$  should be started not later than  $V_{DD}$ .

Delay allowance between  $V_{DD}$  and  $V_{DD2/3}$  is illustrated as Figure 16.



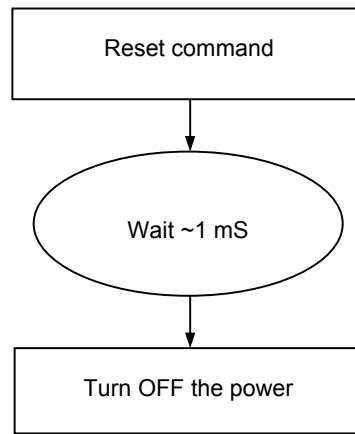
**Figure 14:** Reference Power-Up Sequence

**POWER-DOWN SEQUENCE**

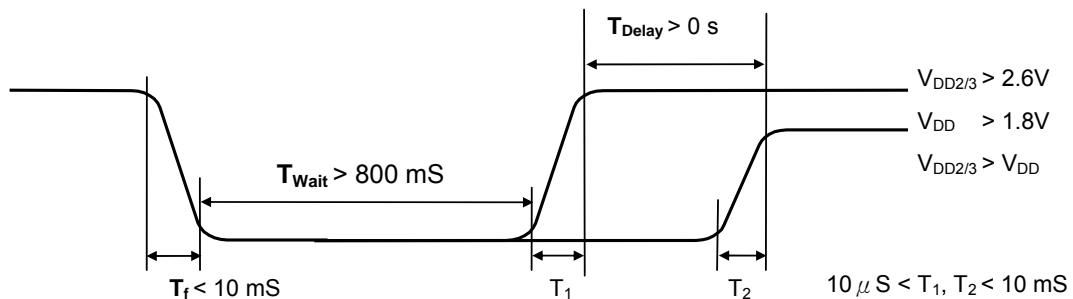
To prevent the charge stored in capacitors  $C_{BX+}$ ,  $C_{BX-}$ , and  $C_L$  from damaging the LCD, when  $V_{DD}$  is switched off, use *Reset* mode to enable the built-in draining circuit and discharge these capacitors.

The draining resistor is 1K Ohm for both  $V_{LCD}$  and  $V_{B+}$ . It is recommended to wait  $3 \times RC$  for  $V_{LCD}$  and  $1.5 \times RC$  for  $V_{B+}$ . For example, if  $C_L$  is 10nF, then the draining time required for  $V_{LCD}$  is 0.5~1mS.

When internal  $V_{LCD}$  is not used, UC1610 will *NOT* drain  $V_{LCD}$  during *RESET*. System designers need to make sure external  $V_{LCD}$  source is properly drained off before turning off  $V_{DD}$ .



**Figure 15:** Reference Power-Down Sequence



**Figure 16:** Delay allowance between  $V_{DD}$  and  $V_{DD2/3}$

**SAMPLE POWER MANAGEMENT COMMAND SEQUENCES**

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "typical, generic" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)

W/R The direction of dataflow of the cycle. It can be either Write (0) or Read (1).

Type Required: These items are required

Customized: These items are not necessary if customer parameters are the same as default

Advanced: We recommend new users to skip these commands and use default values.

Optional: These commands depend on what users want to do.

**POWER-UP**

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	-	-	-	-	-	-	-	-	-	-	Automatic Power-ON Reset.	Wait 5~10mS after V <sub>DD</sub> is ON
C	0	0	0	0	1	0	0	1	#	#	(5) Set Temp. Compensation	Set up LCD format specific parameters, MX, MY, etc.
C	0	0	1	1	0	0	0	#	#	#	(19) Set LCD Mapping	
A	0	0	1	0	1	0	0	0	#	#	(15) Set Line Rate	Fine tune for power, flicker, contrast, and shading.
C	0	0	1	1	0	1	0	1	#	#	(20) Set Gray Shade	
C	0	0	1	1	1	0	1	0	#	#	(24) Set Bias Ratio	
R	0	0	1	0	0	0	0	0	0	1	(11) Set V <sub>BIAS</sub> Potentiometer	LCD specific operating voltage setting
	0	0	#	#	#	#	#	#	#	#		
O	1	0	#	#	#	#	#	#	#	#	Write display RAM	Set up display image
	.	.	.	.	.	.	.	.	.	.		
	1	0	#	#	#	#	#	#	#	#		
R	0	0	1	0	1	0	1	1	1	1	(18) Set Display Enable	

**POWER-DOWN**

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	(21) System Reset	
R	-	-	-	-	-	-	-	-	-	-	Draining capacitor	Wait ~1mS before V <sub>DD</sub> OFF

**DISPLAY-OFF**

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	1	1	1	0	(18) Set Display Disable	
C	1	0	#	#	#	#	#	#	#	#	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the SLEEP state.)
	.	.	.	.	.	.	.	.	.	.		
	1	0	#	#	#	#	#	#	#	#		
R	0	0	1	0	1	0	1	1	1	1	(18) Set Display Enable	

**ESD CONSIDERATION**

1. UC1600 series products are usually provided in bare die format to customers. This makes the product particularly sensitive to ESD damage during handling and manufacturing process. It is therefore highly recommended that LCM makers strictly follow the "JESD 625-A Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices" when manufacturing LCM.

In particular, the following pins in UC1610 require special "ESD Sensitivity" consideration, please refer to Table below.

Pin Name	MM* +V <sub>DD</sub>	MM* +V <sub>SS</sub>	HBM* +V <sub>DD</sub>	HBM* +V <sub>SS</sub>
V <sub>LCDIN</sub>	Pass 150V	Pass 150V	Pass 1000V	Pass 1500V
V <sub>LCDOUT</sub>	Pass 150V	Pass 150V	Pass 1500V	Pass 1500V
C <sub>B</sub>	Pass 100V	Pass 150V	Pass 1500V	Pass 1500V

\* MM: Machine Mode; HBM: Human Body Mode

According to UltraChip's Mass Production experiences, the ESD tolerance conditions are believed to be very stable and can produce high yield in multiple customer sites. However, special care is still required during handling and manufacturing process to avoid unnecessary yield loss due to ESD damages.

2. LCM design suggestions: To minimize potential ESD damages to the finished LCD modules, please consider placing external components (C<sub>B0</sub> and C<sub>B1</sub>) in such a way that they will not be exposed to Machine Mode ESD zap path. For example, place C<sub>B</sub> capacitors on the internal side after folding FPC.

**ABSOLUTE MAXIMUM RATINGS**

In accordance with IEC134, note 1 and 2

Symbol	Parameter	Min.	Max.	Unit
$V_{DD}$	Logic Supply voltage	-0.3	+4.0	V
$V_{DD2}$	LCD Generator Supply voltage	-0.3	+4.0	V
$V_{DD3}$	Analog Circuit Supply voltage	-0.3	+4.0	V
$V_{DD2/3}-V_{DD}$	Voltage difference between $V_{DD}$ and $V_{DD2/3}$	--	1.6	V
$V_{LCD}$	LCD Generated voltage (-30°C ~ +80°C)	-0.3	+18.0	V
$V_{IN}$	Digital input signal	-0.4	$V_{DD} + 0.5$	V
$T_{OPR}$	Operating temperature range	-30	+85	°C
$T_{STR}$	Storage temperature	-55	+125	°C

**Notes**

1.  $V_{DD}$  is based on  $V_{SS} = 0V$
2. Stress beyond ranges listed above may cause permanent damages to the device.

**SPECIFICATIONS**
**DC CHARACTERISTICS**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{DD}$	Supply for digital circuit		1.8		3.3	V
$V_{DD2/3}$	Supply for bias & pump		2.6		3.3	V
$V_{LCD}$	Charge pump output	$V_{DD2/3} \geq 2.6V, 25^{\circ}C$		13.5	15	V
$V_D$	LCD data voltage	$V_{DD2/3} \geq 2.6V, 25^{\circ}C$	0.9		1.5	V
$V_{IL}$	Input logic LOW				$0.2V_{DD}$	V
$V_{IL(Serial)}$	Input logic LOW in serial Mode				$0.15V_{DD}$	
$V_{IH}$	Input logic HIGH		$0.8V_{DD}$			V
$V_{IH(Serial)}$	Input logic HIGH in serial Mode		$0.85V_{DD}$			
$V_{OL}$	Output logic LOW				$0.2V_{DD}$	V
$V_{OH}$	Output logic HIGH		$0.8V_{DD}$			V
$I_{IL}$	Input leakage current				1.5	$\mu A$
$C_{IN}$	Input capacitance			5	10	pF
$C_{OUT}$	Output capacitance			5	10	pF
$R_{ON(SEG)}$	SEG output impedance	$V_{LCD} = 14.7V$		1.2	2.5	$k\Omega$
$R_{ON(COM)}$	COM output impedance	$V_{LCD} = 14.7V$		2.0	4.0	$k\Omega$
$f_{LINE}$	Average Line rate	LC[4:3] = 11b	11.1	12.1	-	kHz

**POWER CONSUMPTION**

$V_{DD} = 2.7$ , Bias Ratio = 10b, PM = 178, Line Rate = 00b,  $P_L = 16 \sim 21nF$ , MR = 128, Bus mode = 6800,  
 $C_L = 0.3\mu F$ ,  $C_B = 2\mu F$ ,  $C_{BIAS} = 0.1\mu F$ . All outputs are open circuit.

Display Pattern	Conditions	Typ. ( $\mu A$ )	Max. ( $\mu A$ )
All-OFF	Bus = idle	617	925
2-pixel checker	Bus = idle	725	1087
-	Bus = idle (standby current)	-	5



## AC CHARACTERISTICS

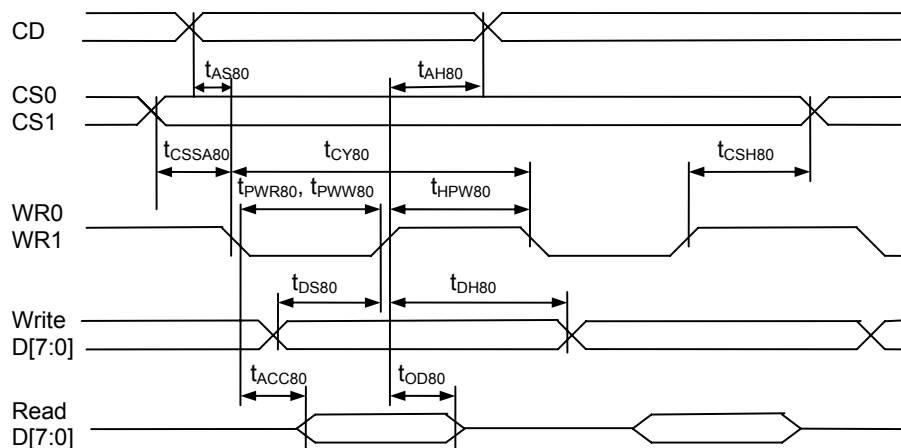


FIGURE 17: Parallel Bus Timing Characteristics (for 8080 MCU)

(2.5V  $\leq$  V<sub>DD</sub> < 3.3V, Ta = -30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t <sub>AS80</sub> t <sub>AH80</sub>	CD	Address setup time Address hold time		5 15	-	nS
t <sub>CY80</sub>		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		140 80 140 80	-	nS
t <sub>PWR80</sub>	WR1	Pulse width 8 bits (read) 4 bits		70 70	-	nS
t <sub>PWW80</sub>	WR0	Pulse width 8 bits (write) 4 bits		40 40	-	nS
t <sub>HPW80</sub>	WR0, WR1	High pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		70 40 70 40	-	nS
t <sub>DS80</sub> t <sub>DH80</sub>	D0~D7	Data setup time Data hold time		30 15	-	nS
t <sub>ACC80</sub> t <sub>OD80</sub>		Read access time Output disable time	C <sub>L</sub> = 100pF	- 25	60	nS
t <sub>CSSA80</sub> t <sub>CSH80</sub>	CS1/CS0	Chip select setup time		5 5		nS

$(1.8V \leq V_{DD} < 2.5V, T_a = -30 \text{ to } +85^\circ\text{C})$ 

Symbol	Signal	Description	Condition	Min.	Max.	Units
$t_{AS80}$ $t_{AH80}$	CD	Address setup time Address hold time		10 30	–	nS
$t_{CY80}$		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		280 160 280 160	–	nS
$t_{PWR80}$	WR1	Pulse width 8 bits (read) 4 bits (read)		140 140	–	nS
$t_{PWW80}$	WR0	Pulse width 8 bits (write) 4 bits (write)		80 80	–	nS
$t_{HPW80}$	WR0, WR1	High pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		140 80 140 80	–	nS
$t_{DS80}$ $t_{DH80}$	D0~D7	Data setup time Data hold time		60 30	–	nS
$t_{ACC80}$ $t_{OD80}$		Read access time Output disable time	$C_L = 100\text{pF}$	- 50		nS
$t_{CSSA80}$ $t_{CSH80}$	CS1/CS0	Chip select setup time		10 10		nS

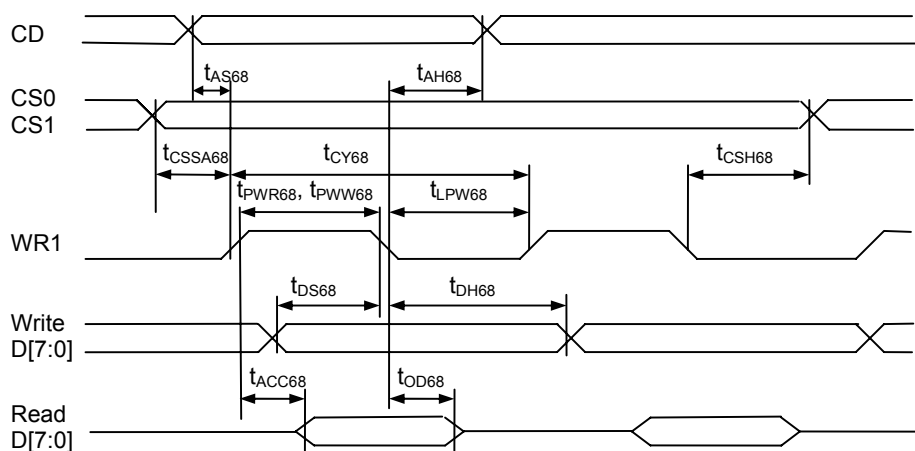


FIGURE 18: Parallel Bus Timing Characteristics (for 6800 MCU)

(2.5V ≤ V<sub>DD</sub> < 3.3V, T<sub>a</sub> = -30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t <sub>AS68</sub> t <sub>AH68</sub>	CD	Address setup time Address hold time		5 15	-	nS
t <sub>CY68</sub>		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		140 80 140 80	-	nS
t <sub>PWR68</sub>	WR1	Pulse width 8 bits (read) 4 bits		70 70	-	nS
t <sub>PWW68</sub>		Pulse width 8 bits (write) 4 bits		40 40	-	nS
t <sub>LPW68</sub>		Low pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		70 40 70 40	-	nS
t <sub>DS68</sub> t <sub>DH68</sub>	D0~D7	Data setup time Data hold time		30 15	-	nS
t <sub>ACC68</sub> t <sub>OD68</sub>		Read access time Output disable time	C <sub>L</sub> = 100pF	- 25	60	nS
t <sub>CSSA68</sub> t <sub>CSH68</sub>	CS1/CS0	Chip select setup time		5 5		nS

(1.8V ≤ V<sub>DD</sub> < 2.5V, Ta= -30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t <sub>AS68</sub> t <sub>AH68</sub>	CD	Address setup time Address hold time		10 30	–	nS
t <sub>CY68</sub>		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		280 160 280 160	–	nS
t <sub>PWR68</sub>	WR1	Pulse width 8 bits (read) 4 bits		140 140	–	nS
t <sub>PWW68</sub>		Pulse width 8 bits (write) 4 bits		80 80	–	nS
t <sub>LPW68</sub>		Low pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		140 80 140 80	–	nS
t <sub>DS68</sub> t <sub>DH68</sub>	D0~D7	Data setup time Data hold time		60 30	–	nS
t <sub>ACC68</sub> t <sub>OD68</sub>		Read access time Output disable time	C <sub>L</sub> = 100pF	- 50		nS
T <sub>CSSA68</sub> T <sub>CSH68</sub>	CS1/CS0	Chip select setup time		10 10		nS

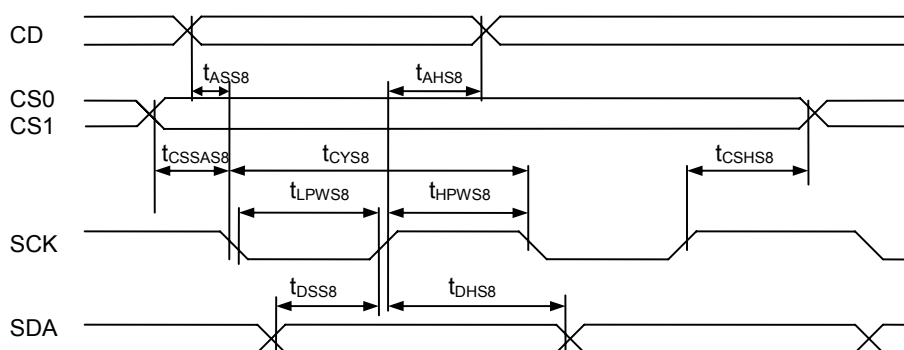


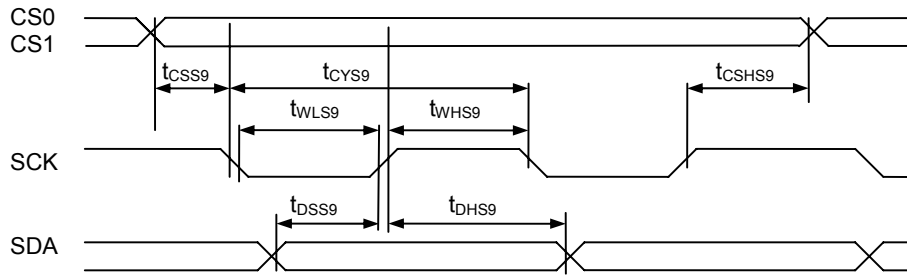
FIGURE 19: Serial Bus Timing Characteristics (for S8 / S8uc)

( $2.5V \leq V_{DD} < 3.3V$ ,  $T_a = -30$  to  $+85^\circ C$ )

Symbol	Signal	Description	Condition	Min.	Max.	Units
$t_{ASS8}$	CD	Address setup time		5	–	nS
$t_{AHS8}$		Address hold time		20	–	nS
$t_{CYS8}$	SCK	System cycle time		125	–	nS
$t_{LPWS8}$		Low pulse width		60	–	nS
$t_{HPWS8}$		High pulse width		60	–	nS
$t_{DSS8}$	SDA	Data setup time		30	–	nS
$t_{DHS8}$		Data hold time		20	–	nS
$t_{CSSAS8}$	CS1/CS0	Chip select setup time		5		nS
$t_{CSHS8}$				15		nS

( $1.8V \leq V_{DD} < 2.5V$ ,  $T_a = -30$  to  $+85^\circ C$ )

Symbol	Signal	Description	Condition	Min.	Max.	Units
$t_{ASS8}$	CD	Address setup time		10	–	nS
$t_{AHS8}$		Address hold time		45	–	nS
$t_{CYS8}$	SCK	System cycle time		250	–	nS
$t_{LPWS8}$		Low pulse width		120	–	nS
$t_{HPWS8}$		High pulse width		120	–	nS
$t_{DSS8}$	SDA	Data setup time		60	–	nS
$t_{DHS8}$		Data hold time		40	–	nS
$t_{CSSAS8}$	CS1/CS0	Chip select setup time		10		nS
$t_{CSHS8}$				30		nS



**FIGURE 20:** Serial Bus Timing Characteristics (for S9)

( $2.5V \leq V_{DD} < 3.3V$ ,  $T_a = -30$  to  $+85^\circ C$ )

Symbol	Signal	Description	Condition	Min.	Max.	Units
$t_{CYS9}$	SCK	System cycle time		80	–	nS
$t_{LPWS9}$		Low pulse width		35	–	nS
$t_{HPWS9}$		High pulse width		35	–	nS
$t_{DSS9}$	SDA	Data setup time		30	–	nS
$t_{DHS9}$		Data hold time		20	–	nS
$t_{CSSAS9}$	CS1/CS0	Chip select setup time		5		nS
$t_{CSHS9}$				5		nS

( $1.8V \leq V_{DD} < 2.5V$ ,  $T_a = -30$  to  $+85^\circ C$ )

Symbol	Signal	Description	Condition	Min.	Max.	Units
$t_{CYS9}$	SCK	System cycle time		160	–	nS
$t_{LPWS9}$		Low pulse width		70	–	nS
$t_{HPWS9}$		High pulse width		70	–	nS
$t_{DSS9}$	SDA	Data setup time		60	–	nS
$t_{DHS9}$		Data hold time		40	–	nS
$t_{CSSAS9}$	CS1/CS0	Chip select setup time		10		nS
$t_{CSHS9}$				10		nS

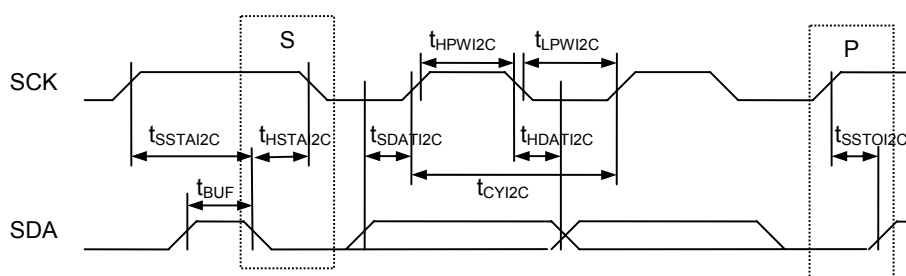


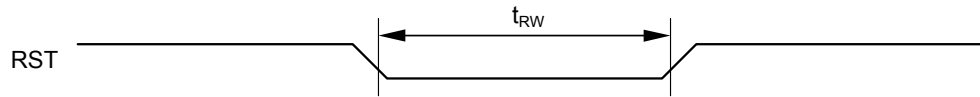
FIGURE 21: Serial bus timing characteristics (for I<sup>2</sup>C)

(2.5V ≤ V<sub>DD</sub> < 3.3V, Ta= -30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t <sub>CYI2C</sub>	SCK	SCK cycle time	tr+tf ≤ 100nS	250	–	nS
t <sub>LPWI2C</sub>		Low pulse width		65	–	nS
t <sub>HPWI2C</sub>		High pulse width		65	–	nS
tr, tf	SCK SDA	Rise time and fall time		–	–	nS
t <sub>SSDAI2C</sub>		Data setup time		25	–	nS
t <sub>HDAI2C</sub>		Data hold time		10	–	nS
t <sub>SSTAI2C</sub>		START Setup time		25	–	nS
t <sub>HSTAI2C</sub>		STAR Hold time		20	–	nS
t <sub>SSTOI2C</sub>		STOP setup time		25	–	nS

(1.8V ≤ V<sub>DD</sub> < 2.5V, Ta= -30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t <sub>CYI2C</sub>	SCK	SCK cycle time	tr+tf ≤ 100ns	300	–	nS
t <sub>LPWI2C</sub>		Low pulse width		100	–	nS
t <sub>HPWI2C</sub>		High pulse width		100	–	nS
tr, tf	SCK SDA	Rise time and fall time		–	–	nS
t <sub>SSDAI2C</sub>		Data setup time		40	–	nS
t <sub>HDAI2C</sub>		Data hold time		10	–	nS
t <sub>SSTAI2C</sub>		START Setup time		25	–	nS
t <sub>HSTAI2C</sub>		STAR Hold time		35	–	nS
t <sub>SSTOI2C</sub>		STOP setup time		25	–	nS



**FIGURE 22: Reset Characteristics**

( $1.8V \leq V_{DD} < 2.5V$ ,  $T_a = -30$  to  $+85^{\circ}C$ )

Symbol	Signal	Description	Condition	Min.	Max.	Units
$t_{RW}$	RST	Reset low pulse width		1	–	$\mu S$



PHYSICAL DIMENSIONS

**DIE SIZE:**  
1.372mm x 11.384mm

**DIE THICKNESS:**  
0.5mm

**BUMP HEIGHT:**  
17 ± 1µM  
H<sub>Max</sub>-H<sub>Min</sub> (within die) < 2µM

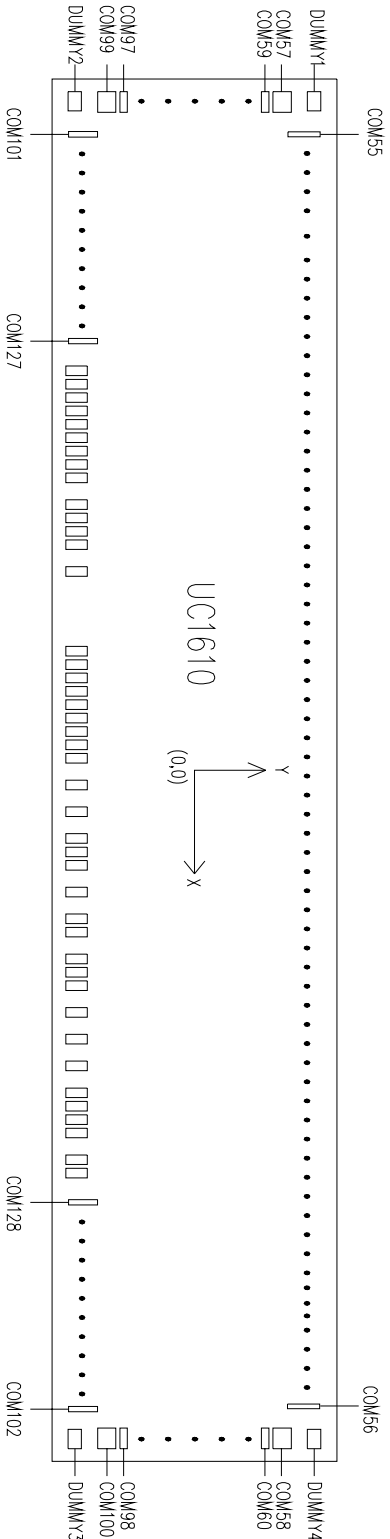
**MINIMUM BUMP PITCH:**  
SEG: 50µM  
COM: 50µM

**MINIMUM BUMP GAP:**  
17µM

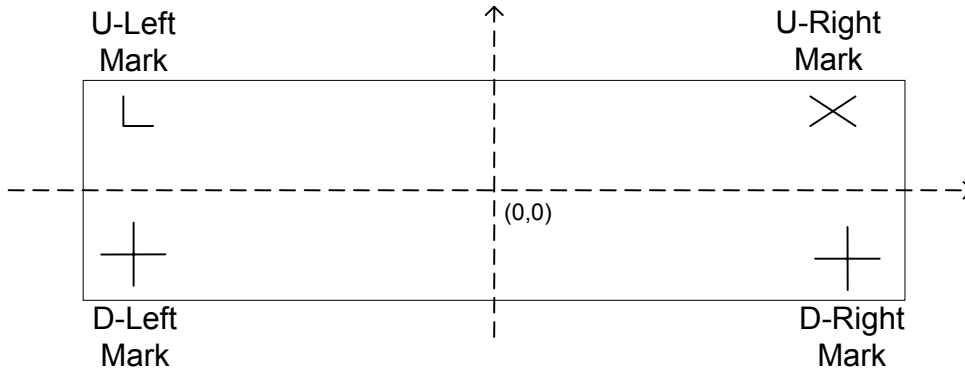
**COORDINATE ORIGIN:**  
Chip center

**PAD REFERENCE:**  
Pad center

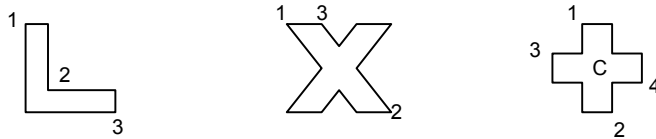
(Drawing and coordinates are for the Circuit/Bump view.)



**ALIGNMENT MARK INFORMATION**



**SHAPE OF THE ALIGNMENT MARK:**



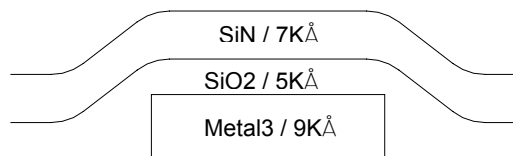
**COORDINATES:**

	U-Left Mark		U-Right Mark	
	X	Y	X	Y
1	-5496.3	623.8	5430.4	625.9
2	-5480.7	591.9	5497.8	578.6
3	-5449.5	576.4	5452.1	625.9

	D-Left Mark		D-Right Mark	
	X	Y	X	Y
1	-5474.3	-591.0	5467.9	-591.0
2	-5463.3	-646.0	5478.9	-646.0
3	-5496.3	-613.0	5445.9	-613.0
4	-5441.3	-624.0	5501.0	-624.0
C	-5468.8	-618.5	5473.4	-618.5

(The values of the x-coordinate and the y-coordinate in the table are after rounded.)

**TOP METAL AND PASSIVATION:**



**FOR NON-OTP PROCESS CROSS-SECTION**

## PAD COORDINATES

#	PAD Name	X	Y	W	H
1	DUMMY	-5588.9	568.6	99	53
2	COM57	-5588.9	508.5	99	33
3	COM59	-5588.9	458.5	99	33
4	COM61	-5588.9	408.5	99	33
5	COM63	-5588.9	358.5	99	33
6	COM65	-5588.9	308.5	99	33
7	COM67	-5588.9	258.5	99	33
8	COM69	-5588.9	208.5	99	33
9	COM71	-5588.9	158.5	99	33
10	COM73	-5588.9	108.5	99	33
11	COM75	-5588.9	58.5	99	33
12	COM77	-5588.9	8.5	99	33
13	COM79	-5588.9	-41.6	99	33
14	COM81	-5588.9	-91.6	99	33
15	COM83	-5588.9	-141.6	99	33
16	COM85	-5588.9	-191.6	99	33
17	COM87	-5588.9	-241.6	99	33
18	COM89	-5588.9	-291.6	99	33
19	COM91	-5588.9	-341.6	99	33
20	COM93	-5588.9	-391.6	99	33
21	COM95	-5588.9	-441.6	99	33
22	COM97	-5588.9	-491.6	99	33
23	COM99	-5588.9	-541.6	99	33
24	DUMMY	-5588.9	-601.4	99	53
25	COM101	-5395.0	-593.0	33	99
26	COM103	-5345.0	-593.0	33	99
27	COM105	-5295.0	-593.0	33	99
28	COM107	-5245.0	-593.0	33	99
29	COM109	-5195.0	-593.0	33	99
30	COM111	-5145.0	-593.0	33	99
31	COM113	-5095.0	-593.0	33	99
32	COM115	-5045.0	-593.0	33	99
33	COM117	-4995.0	-593.0	33	99
34	COM119	-4945.0	-593.0	33	99
35	COM121	-4895.0	-593.0	33	99
36	COM123	-4845.0	-593.0	33	99
37	COM125	-4795.0	-593.0	33	99
38	COM127	-4745.0	-593.0	33	99
39	D0	-4667.5	-600.0	50	80
40	D1	-4597.5	-600.0	50	80
41	D2	-4527.5	-600.0	50	80
42	D3	-4457.5	-600.0	50	80
43	D4	-4387.5	-600.0	50	80
44	D5	-4317.5	-600.0	50	80
45	D6	-4247.5	-600.0	50	80
46	D7	-4177.5	-600.0	50	80
47	RST_	-4105.9	-600.0	50	80
48	CS0	-3846.8	-600.0	50	80
49	VDDX	-3775.9	-600.0	50	80
50	CS1	-3705.2	-600.0	50	80
51	ID	-3450.2	-600.0	50	80
52	CD	-3378.6	-600.0	50	80

#	PAD Name	X	Y	W	H
53	WR0	-3123.6	-600.0	50	80
54	WR1	-3052.0	-600.0	50	80
55	TST4	-2797.0	-600.0	50	80
56	BM0	-2725.4	-600.0	50	80
57	VDDX	-2554.4	-600.0	50	80
58	BM1	-2383.4	-600.0	50	80
59	TST2	-2312.5	-600.0	50	80
60	DUMMY	-2128.4	-600.0	50	80
61	DUMMY	-1868.0	-600.0	50	80
62	VSS	-1797.7	-600.0	50	80
63	VSS	-1727.7	-600.0	50	80
64	VSS	-1657.7	-600.0	50	80
65	VSS	-1587.7	-600.0	50	80
66	VSS	-1517.7	-600.0	50	80
67	VSS	-1447.7	-600.0	50	80
68	VSS2	-1264.3	-600.0	50	80
69	VSS2	-1194.3	-600.0	50	80
70	VSS2	-1124.3	-600.0	50	80
71	VSS2	-1054.3	-600.0	50	80
72	VSS2	-984.3	-600.0	50	80
73	VDD2	-914.3	-600.0	50	80
74	VDD2	-844.3	-600.0	50	80
75	VDD2	-774.3	-600.0	50	80
76	VDD3	-407.6	-600.0	50	80
77	VDD3	-336.4	-600.0	50	80
78	VDD3	-266.4	-600.0	50	80
79	VDD	104.7	-600.0	50	80
80	VDD	174.9	-600.0	50	80
81	VDD	244.9	-600.0	50	80
82	VDD	314.9	-600.0	50	80
83	VDD	384.9	-600.0	50	80
84	DUMMY	558.6	-600.0	50	80
85	DUMMY	628.9	-600.0	50	80
86	DUMMY	889.3	-600.0	50	80
87	VB0-	960.5	-600.0	50	80
88	VB0-	1030.5	-600.0	50	80
89	VB0-	1100.5	-600.0	50	80
90	VB0-	1170.5	-600.0	50	80
91	VB0-	1240.5	-600.0	50	80
92	VB0-	1310.5	-600.0	50	80
93	VB0-	1380.5	-600.0	50	80
94	VB0-	1450.5	-600.0	50	80
95	VB0-	1520.5	-600.0	50	80
96	VB1-	1871.5	-600.0	50	80
97	VB1-	1941.7	-600.0	50	80
98	VB1-	2010.1	-600.0	50	80
99	VB1-	2078.5	-600.0	50	80
100	VB1-	2146.9	-600.0	50	80
101	VB1-	2215.3	-600.0	50	80
102	VB1-	2283.7	-600.0	50	80
103	VB1-	2352.1	-600.0	50	80
104	VB1-	2420.5	-600.0	50	80

#	PAD Name	X	Y	W	H
105	VB1+	2490.5	-600.0	50	80
106	VB1+	2558.9	-600.0	50	80
107	VB1+	2627.3	-600.0	50	80
108	VB1+	2695.7	-600.0	50	80
109	VB1+	2764.1	-600.0	50	80
110	VB1+	2832.5	-600.0	50	80
111	VB1+	2900.9	-600.0	50	80
112	VB1+	2969.3	-600.0	50	80
113	VB1+	3039.3	-600.0	50	80
114	VB0+	3388.3	-600.0	50	80
115	VB0+	3458.6	-600.0	50	80
116	VB0+	3527.0	-600.0	50	80
117	VB0+	3595.4	-600.0	50	80
118	VB0+	3663.8	-600.0	50	80
119	VB0+	3732.2	-600.0	50	80
120	VB0+	3800.6	-600.0	50	80
121	VB0+	3869.0	-600.0	50	80
122	VB0+	3937.4	-600.0	50	80
123	VLCDIN	4007.4	-600.0	50	80
124	VLCDIN	4077.4	-600.0	50	80
125	VLCDOUT	4426.4	-600.0	50	80
126	VLCDOUT	4496.6	-600.0	50	80
127	VBIAS	4566.6	-600.0	50	80
128	COM128	4742.7	-593.0	33	99
129	COM126	4792.7	-593.0	33	99
130	COM124	4842.7	-593.0	33	99
131	COM122	4892.7	-593.0	33	99
132	COM120	4942.7	-593.0	33	99
133	COM118	4992.7	-593.0	33	99
134	COM116	5042.7	-593.0	33	99
135	COM114	5092.7	-593.0	33	99
136	COM112	5142.7	-593.0	33	99
137	COM110	5192.7	-593.0	33	99
138	COM108	5242.7	-593.0	33	99
139	COM106	5292.7	-593.0	33	99
140	COM104	5342.7	-593.0	33	99
141	COM102	5392.7	-593.0	33	99
142	DUMMY	5588.9	-601.4	99	53
143	COM100	5588.9	-541.6	99	33
144	COM98	5588.9	-491.6	99	33
145	COM96	5588.9	-441.6	99	33
146	COM94	5588.9	-391.6	99	33
147	COM92	5588.9	-341.6	99	33
148	COM90	5588.9	-291.6	99	33
149	COM88	5588.9	-241.6	99	33
150	COM86	5588.9	-191.6	99	33
151	COM84	5588.9	-141.6	99	33
152	COM82	5588.9	-91.6	99	33
153	COM80	5588.9	-41.6	99	33
154	COM78	5588.9	8.5	99	33
155	COM76	5588.9	58.5	99	33
156	COM74	5588.9	108.5	99	33
157	COM72	5588.9	158.5	99	33
158	COM70	5588.9	208.5	99	33

#	PAD Name	X	Y	W	H
159	COM68	5588.9	258.5	99	33
160	COM66	5588.9	308.5	99	33
161	COM64	5588.9	358.5	99	33
162	COM62	5588.9	408.5	99	33
163	COM60	5588.9	458.5	99	33
164	COM58	5588.9	508.5	99	33
165	DUMMY	5588.9	568.6	99	53
166	COM56	5375.0	593.0	33	99
167	COM54	5325.0	593.0	33	99
168	COM52	5275.0	593.0	33	99
169	COM50	5225.0	593.0	33	99
170	COM48	5175.0	593.0	33	99
171	COM46	5125.0	593.0	33	99
172	COM44	5075.0	593.0	33	99
173	COM42	5025.0	593.0	33	99
174	COM40	4975.0	593.0	33	99
175	COM38	4925.0	593.0	33	99
176	COM36	4875.0	593.0	33	99
177	COM34	4825.0	593.0	33	99
178	COM32	4775.0	593.0	33	99
179	COM30	4725.0	593.0	33	99
180	COM28	4675.0	593.0	33	99
181	COM26	4625.0	593.0	33	99
182	COM24	4575.0	593.0	33	99
183	COM22	4525.0	593.0	33	99
184	COM20	4475.0	593.0	33	99
185	COM18	4425.0	593.0	33	99
186	COM16	4375.0	593.0	33	99
187	COM14	4325.0	593.0	33	99
188	COM12	4275.0	593.0	33	99
189	COM10	4225.0	593.0	33	99
190	COM8	4175.0	593.0	33	99
191	COM6	4125.0	593.0	33	99
192	COM4	4075.0	593.0	33	99
193	COM2	4025.0	593.0	33	99
194	SEG160	3975.0	593.0	33	99
195	SEG159	3925.0	593.0	33	99
196	SEG158	3875.0	593.0	33	99
197	SEG157	3825.0	593.0	33	99
198	SEG156	3775.0	593.0	33	99
199	SEG155	3725.0	593.0	33	99
200	SEG154	3675.0	593.0	33	99
201	SEG153	3625.0	593.0	33	99
202	SEG152	3575.0	593.0	33	99
203	SEG151	3525.0	593.0	33	99
204	SEG150	3475.0	593.0	33	99
205	SEG149	3425.0	593.0	33	99
206	SEG148	3375.0	593.0	33	99
207	SEG147	3325.0	593.0	33	99
208	SEG146	3275.0	593.0	33	99
209	SEG145	3225.0	593.0	33	99
210	SEG144	3175.0	593.0	33	99
211	SEG143	3125.0	593.0	33	99
212	SEG142	3075.0	593.0	33	99

#	PAD Name	X	Y	W	H
213	SEG141	3025.0	593.0	33	99
214	SEG140	2975.0	593.0	33	99
215	SEG139	2925.0	593.0	33	99
216	SEG138	2875.0	593.0	33	99
217	SEG137	2825.0	593.0	33	99
218	SEG136	2775.0	593.0	33	99
219	SEG135	2725.0	593.0	33	99
220	SEG134	2675.0	593.0	33	99
221	SEG133	2625.0	593.0	33	99
222	SEG132	2575.0	593.0	33	99
223	SEG131	2525.0	593.0	33	99
224	SEG130	2475.0	593.0	33	99
225	SEG129	2425.0	593.0	33	99
226	SEG128	2375.0	593.0	33	99
227	SEG127	2325.0	593.0	33	99
228	SEG126	2275.0	593.0	33	99
229	SEG125	2225.0	593.0	33	99
230	SEG124	2175.0	593.0	33	99
231	SEG123	2125.0	593.0	33	99
232	SEG122	2075.0	593.0	33	99
233	SEG121	2025.0	593.0	33	99
234	SEG120	1975.0	593.0	33	99
235	SEG119	1925.0	593.0	33	99
236	SEG118	1875.0	593.0	33	99
237	SEG117	1825.0	593.0	33	99
238	SEG116	1775.0	593.0	33	99
239	SEG115	1725.0	593.0	33	99
240	SEG114	1675.0	593.0	33	99
241	SEG113	1625.0	593.0	33	99
242	SEG112	1575.0	593.0	33	99
243	SEG111	1525.0	593.0	33	99
244	SEG110	1475.0	593.0	33	99
245	SEG109	1425.0	593.0	33	99
246	SEG108	1375.0	593.0	33	99
247	SEG107	1325.0	593.0	33	99
248	SEG106	1275.0	593.0	33	99
249	SEG105	1225.0	593.0	33	99
250	SEG104	1175.0	593.0	33	99
251	SEG103	1125.0	593.0	33	99
252	SEG102	1075.0	593.0	33	99
253	SEG101	1025.0	593.0	33	99
254	SEG100	975.0	593.0	33	99
255	SEG99	925.0	593.0	33	99
256	SEG98	875.0	593.0	33	99
257	SEG97	825.0	593.0	33	99
258	SEG96	775.0	593.0	33	99
259	SEG95	725.0	593.0	33	99
260	SEG94	675.0	593.0	33	99
261	SEG93	625.0	593.0	33	99
262	SEG92	575.0	593.0	33	99
263	SEG91	525.0	593.0	33	99
264	SEG90	475.0	593.0	33	99
265	SEG89	425.0	593.0	33	99
266	SEG88	375.0	593.0	33	99

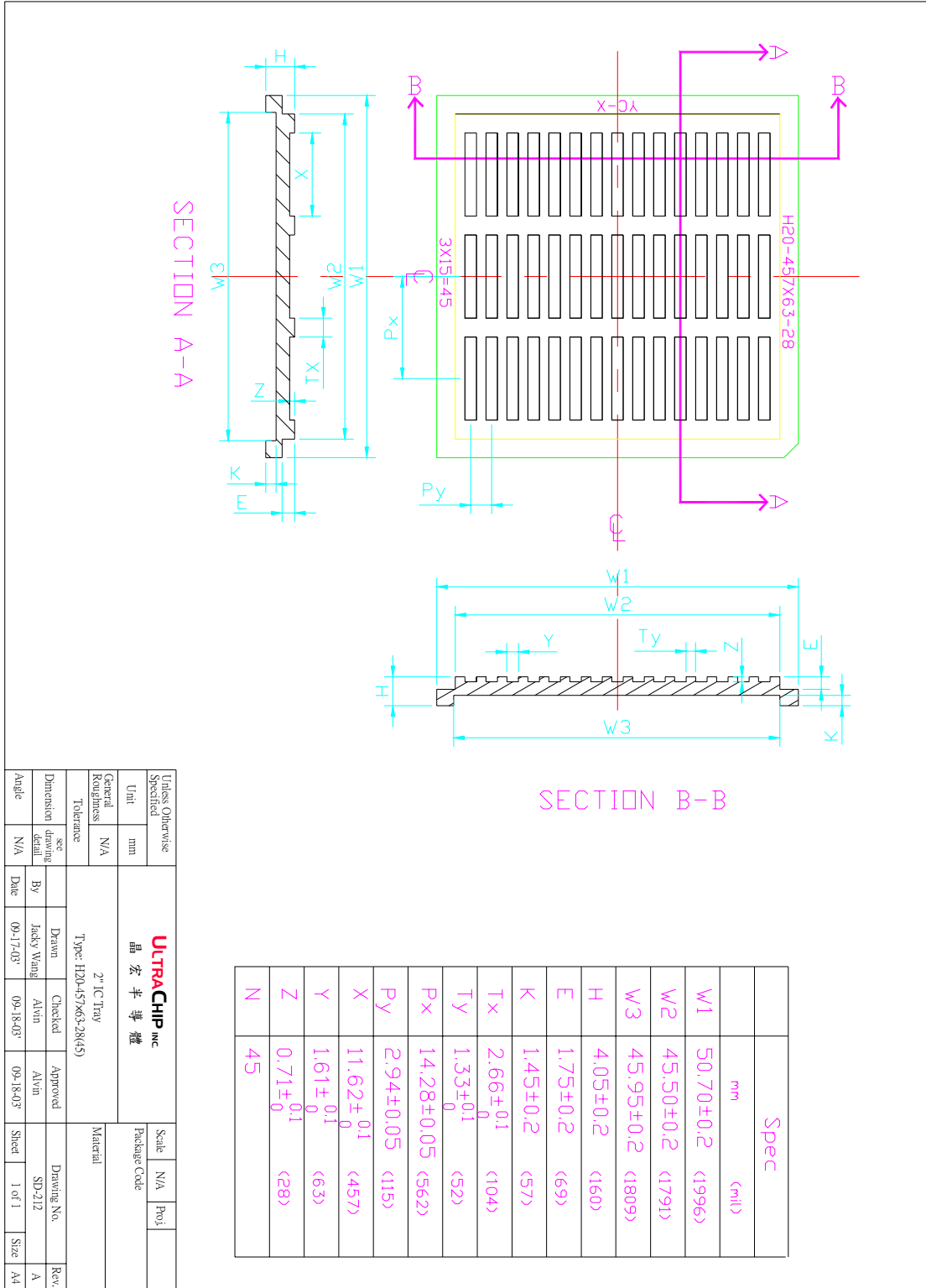
#	PAD Name	X	Y	W	H
267	SEG87	325.0	593.0	33	99
268	SEG86	275.0	593.0	33	99
269	SEG85	225.0	593.0	33	99
270	SEG84	175.0	593.0	33	99
271	SEG83	125.0	593.0	33	99
272	SEG82	75.0	593.0	33	99
273	SEG81	25.0	593.0	33	99
274	SEG80	-25.0	593.0	33	99
275	SEG79	-75.0	593.0	33	99
276	SEG78	-125.0	593.0	33	99
277	SEG77	-175.0	593.0	33	99
278	SEG76	-225.0	593.0	33	99
279	SEG75	-275.0	593.0	33	99
280	SEG74	-325.0	593.0	33	99
281	SEG73	-375.0	593.0	33	99
282	SEG72	-425.0	593.0	33	99
283	SEG71	-475.0	593.0	33	99
284	SEG70	-525.0	593.0	33	99
285	SEG69	-575.0	593.0	33	99
286	SEG68	-625.0	593.0	33	99
287	SEG67	-675.0	593.0	33	99
288	SEG66	-725.0	593.0	33	99
289	SEG65	-775.0	593.0	33	99
290	SEG64	-825.0	593.0	33	99
291	SEG63	-875.0	593.0	33	99
292	SEG62	-925.0	593.0	33	99
293	SEG61	-975.0	593.0	33	99
294	SEG60	-1025.0	593.0	33	99
295	SEG59	-1075.0	593.0	33	99
296	SEG58	-1125.0	593.0	33	99
297	SEG57	-1175.0	593.0	33	99
298	SEG56	-1225.0	593.0	33	99
299	SEG55	-1275.0	593.0	33	99
300	SEG54	-1325.0	593.0	33	99
301	SEG53	-1375.0	593.0	33	99
302	SEG52	-1425.0	593.0	33	99
303	SEG51	-1475.0	593.0	33	99
304	SEG50	-1525.0	593.0	33	99
305	SEG49	-1575.0	593.0	33	99
306	SEG48	-1625.0	593.0	33	99
307	SEG47	-1675.0	593.0	33	99
308	SEG46	-1725.0	593.0	33	99
309	SEG45	-1775.0	593.0	33	99
310	SEG44	-1825.0	593.0	33	99
311	SEG43	-1875.0	593.0	33	99
312	SEG42	-1925.0	593.0	33	99
313	SEG41	-1975.0	593.0	33	99
314	SEG40	-2025.0	593.0	33	99
315	SEG39	-2075.0	593.0	33	99
316	SEG38	-2125.0	593.0	33	99
317	SEG37	-2175.0	593.0	33	99
318	SEG36	-2225.0	593.0	33	99
319	SEG35	-2275.0	593.0	33	99
320	SEG34	-2325.0	593.0	33	99

#	PAD Name	X	Y	W	H
321	SEG33	-2375.0	593.0	33	99
322	SEG32	-2425.0	593.0	33	99
323	SEG31	-2475.0	593.0	33	99
324	SEG30	-2525.0	593.0	33	99
325	SEG29	-2575.0	593.0	33	99
326	SEG28	-2625.0	593.0	33	99
327	SEG27	-2675.0	593.0	33	99
328	SEG26	-2725.0	593.0	33	99
329	SEG25	-2775.0	593.0	33	99
330	SEG24	-2825.0	593.0	33	99
331	SEG23	-2875.0	593.0	33	99
332	SEG22	-2925.0	593.0	33	99
333	SEG21	-2975.0	593.0	33	99
334	SEG20	-3025.0	593.0	33	99
335	SEG19	-3075.0	593.0	33	99
336	SEG18	-3125.0	593.0	33	99
337	SEG17	-3175.0	593.0	33	99
338	SEG16	-3225.0	593.0	33	99
339	SEG15	-3275.0	593.0	33	99
340	SEG14	-3325.0	593.0	33	99
341	SEG13	-3375.0	593.0	33	99
342	SEG12	-3425.0	593.0	33	99
343	SEG11	-3475.0	593.0	33	99
344	SEG10	-3525.0	593.0	33	99
345	SEG9	-3575.0	593.0	33	99
346	SEG8	-3625.0	593.0	33	99
347	SEG7	-3675.0	593.0	33	99
348	SEG6	-3725.0	593.0	33	99
349	SEG5	-3775.0	593.0	33	99
350	SEG4	-3825.0	593.0	33	99
351	SEG3	-3875.0	593.0	33	99
352	SEG2	-3925.0	593.0	33	99
353	SEG1	-3975.0	593.0	33	99
354	COM1	-4025.0	593.0	33	99
355	COM3	-4075.0	593.0	33	99

#	PAD Name	X	Y	W	H
356	COM5	-4125.0	593.0	33	99
357	COM7	-4175.0	593.0	33	99
358	COM9	-4225.0	593.0	33	99
359	COM11	-4275.0	593.0	33	99
360	COM13	-4325.0	593.0	33	99
361	COM15	-4375.0	593.0	33	99
362	COM17	-4425.0	593.0	33	99
363	COM19	-4475.0	593.0	33	99
364	COM21	-4525.0	593.0	33	99
365	COM23	-4575.0	593.0	33	99
366	COM25	-4625.0	593.0	33	99
367	COM27	-4675.0	593.0	33	99
368	COM29	-4725.0	593.0	33	99
369	COM31	-4775.0	593.0	33	99
370	COM33	-4825.0	593.0	33	99
371	COM35	-4875.0	593.0	33	99
372	COM37	-4925.0	593.0	33	99
373	COM39	-4975.0	593.0	33	99
374	COM41	-5025.0	593.0	33	99
375	COM43	-5075.0	593.0	33	99
376	COM45	-5125.0	593.0	33	99
377	COM47	-5175.0	593.0	33	99
378	COM49	-5225.0	593.0	33	99
379	COM51	-5275.0	593.0	33	99
380	COM53	-5325.0	593.0	33	99
381	COM55	-5375.0	593.0	33	99

(The values of the x-coordinate and the y-coordinate in the table are after rounded.)

TRAY INFORMATION



Ululoss Otherwise Specified	mm	<b>ULTRACHIP</b> 晶宏半導體 Type: H20-457x63-28(45)				Scale	N/A	Proj.	
General Roughness	N/A					Package Code			
Tolerance		2" IC Tray				Material			
Dimension	sec drawing detail	Drawn	Checked	Approved	Drawing No				
Angle	N/A	By Jacky Wang	Alvin	Alvin	SD-212				Rev A
		Date 09-17-03	09-18-03	09-18-03	Sheet 1 of 1				Size A4

**REVISION HISTORY**

Version	Contents	Date of Rev.
0.6	Golden release	Aug. 12, 2004
0.61	(1) The table is updated. (Section "ESD Consideration", page 41)	Aug. 16, 2004
0.7	(1) COG section presents. (Section "Recommended COG Layout", page 7) (2) Gray-shade control percentages are updated. LC[6:5] : 20%, 24%, 28%, 32% → 24%, 29%, 36%, 40% (Section "Control Register", page 9; "Command Description", page 15) (3) The condition on V <sub>DD2</sub> is adjusted: 2.5V → 2.7V (Section "LCD Voltage Setting" – Load Driving Strength, page 21) (4) Pad coordination information is updated. (Section "Pad Coordinates", Pp 55 ~ 58)	Nov. 5, 2004
0.71	(1) In the "Operating Mode" table, the status of "Draining Circuit" in Sleep mode is corrected: "OFF" → "ON" (2) Most contents of subsection "Changing Operation Mode" are re-written. (Section "Reset & Power Management", page 38) (3) Subsection "Extended Display OFF" is removed. (4) Subsection "Brief Display OFF" is renamed as "Display OFF". (Section "Reset & Power Management", page 40) (5) COF drawings are removed. (Section "COF Information", Pp 59 ~ 60)	Nov. 9, 2004
0.8	(1) The V <sub>LCD</sub> Formula is updated. (Section "V <sub>LCD</sub> Quick Reference", page 22) (2) A typo error is corrected: "8-shade" → "4-shade" (Section "LCD Display Controls" - Clock & Timing Generator, page 24) (3) In the I <sup>2</sup> C figure (Read Mode), the direction of some acknowledge signals (A) is modified from upward to downward. (Section "Host Interface" – 2-wire Serial Interface (I <sup>2</sup> C), page 30) (4) SEG output impedance, R <sub>ON (SEG)</sub> , COM output impedance, R <sub>ON (COM)</sub> , and Average Line rate, f <sub>LINE</sub> , are adjusted. (Section "Specification" – DC Characteristics, page 44) (5) Experiment data are corrected. (Section "Specification" – Power Consumption, page 44) (6) For 8080, 6800, S8/S8uc, and S9 modes, Chip Select Setup Time t <sub>CSSD80</sub> , t <sub>CSSD68</sub> , t <sub>CSSD88</sub> , t <sub>CSSD89</sub> are removed. (7) Some AC timing data are adjusted. (Section "AC Characteristics", Pp 45 ~ 51)	Nov. 30, 2004
1.0	(1) "COF" related contents are removed. (Overall) (2) V <sub>DD</sub> for COG application is adjusted: 17V → 17.5V (Section "Recommended COG Layout", page 7) (3) The default of APC0~1 is erased. (Section "Control Register", page 9) (4) The content of 2 <sup>nd</sup> byte is corrected. (Section "Command Description" – (31) and (33), page 18) (5) The contents of WR0 and WR1 for serial mode are modified. (Section "Host Interface", page 27)	Feb. 16, 2005



Version	Contents	Date of Rev.
1.0	(6) The RAM table is corrected. (Section "Display Data RAM", page 38)	Feb. 16, 2005
	(7) Point 2 is updated. (Section "ESD Consideration", page 42)	
	(8) Some AC timings are updated. (Section "AC Characteristics", page 49)	
	(9) The presentation of Bump Height is modified. (Section "Physical Dimension", page 53)	
1.01	(1) Figures 14 and 15, for Power Up/Down Sequence, are fixed. (Section "Reset and Power Management", page 40)	Feb. 18, 2005
1.1	(1) Some description for absolute maximum ratings is revised (Section "Absolute Maximum Ratings", page 43)	Mar. 25, 2005
	(2) Serial Mode VIL and VIH are adjusted: $0.2V_{DD}/0.8V_{DD} \rightarrow 0.15V_{DD}/0.85V_{DD}$ (Section "Specifications", page 44)	
	(3) Delete Max Output Disable Time (Section "AC Characteristics", Pp 45 and 47 )	
1.11	(1) Remove without I <sup>2</sup> C interface version	Apr. 13, 2005