AiP31520
61 SEG / 16 COM Driver for Dot Matrix LCD

Product Specification

Specification Revision History：

Version	Data	Description
2010-01-A1	2010-01	New
2012-01-B1	2012-01	Increase in the number and history
2015-03-B2	2015-03	Change block diagram and pin description
2019-11-B3	2019-11	Replace the new template and modify the content
2021-12-B4	2021-12	Add Ordering Information
2022-02-B5	2022-02	Modify Figure 2

1、General Description

The AiP31520 is a dot matrix LCD driver LSI intended for display of characters and graphics. The bit-addressable display data, which is sent from a microcomputer, is stored in a built-in display data RAM and generates the LCD drive signal.

The AiP31520 incorporates innovative circuit design strategies to assure very low current dissipation and a wide range of operating voltages. With these features, the AiP31520 permits the user to implement high-performance handy systems operating from a miniature battery.

In order for the user to adaptively configure his system, the AiP31520 family offers two application forms. One form allows an LCD display of 12 characters 2 lines with an indicator with a single chip. The other is dedicated to driving a total of 80 segments, enabling a medium-size display to be achieved by using a minimum number of drivers.

Features

- Low-power CMOS technology
- Fast CPU 8-bit data interface (80xx, 68xx)
- Built-in display data RAM. . . 2560 bits
- Rich display command setting
- Master/slave operation is supported
- Low power consumption . . . 30uW
- LCD voltage . . . . . 3.5 to 13V
- Single power supply. . . . . 2.4 to 7.0V
- Chip size: 2670×3695 (um×um)
- The IC substrate should be connected to VDD or float in the PCB layout artwork.
- QFP100 or bare chip available

Ordering Information:

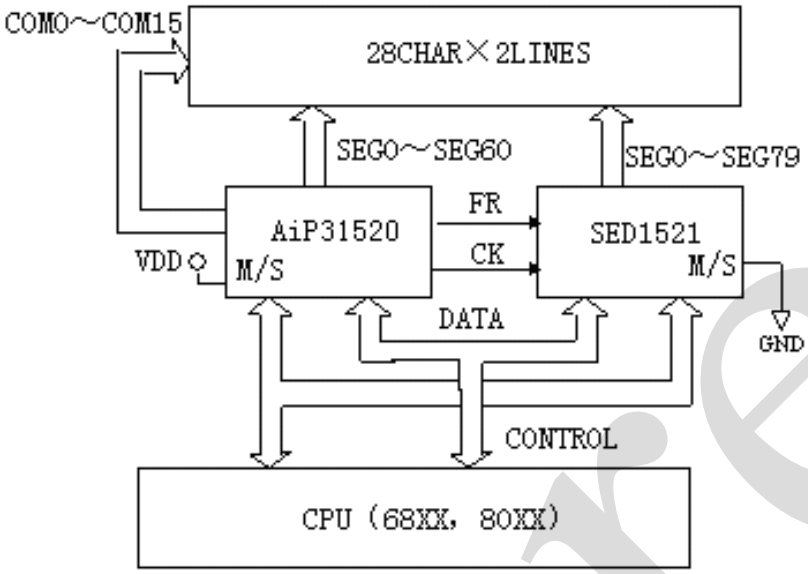
Tube packing specifications:

Type number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP31520NF.TB	QFP100	AiP31520	66 PCS/plate	10 plate/box	660 PCS/box	Dimensions of plastic enclosure: 14.0mm×20.0mm Pin spacing: 0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram



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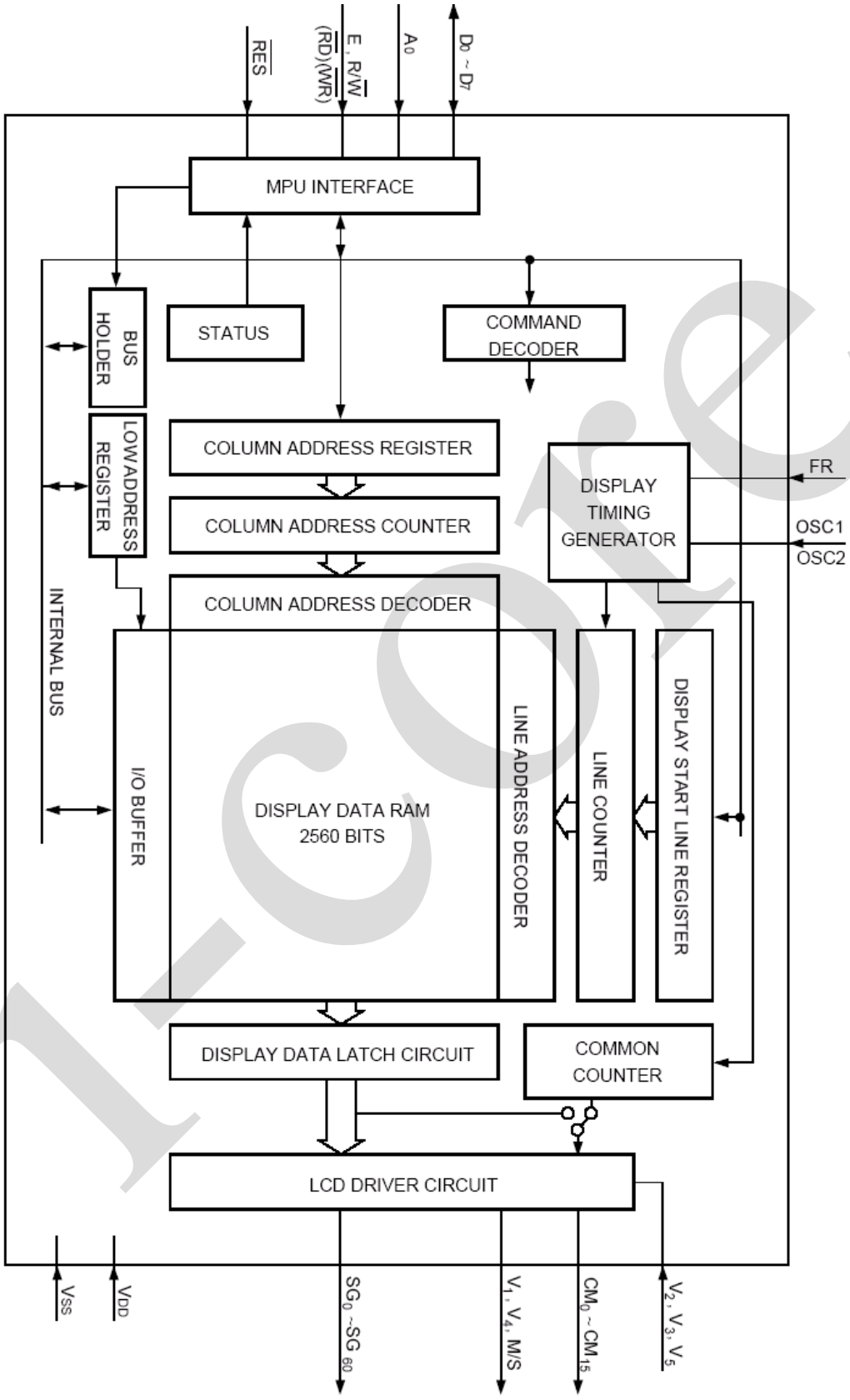
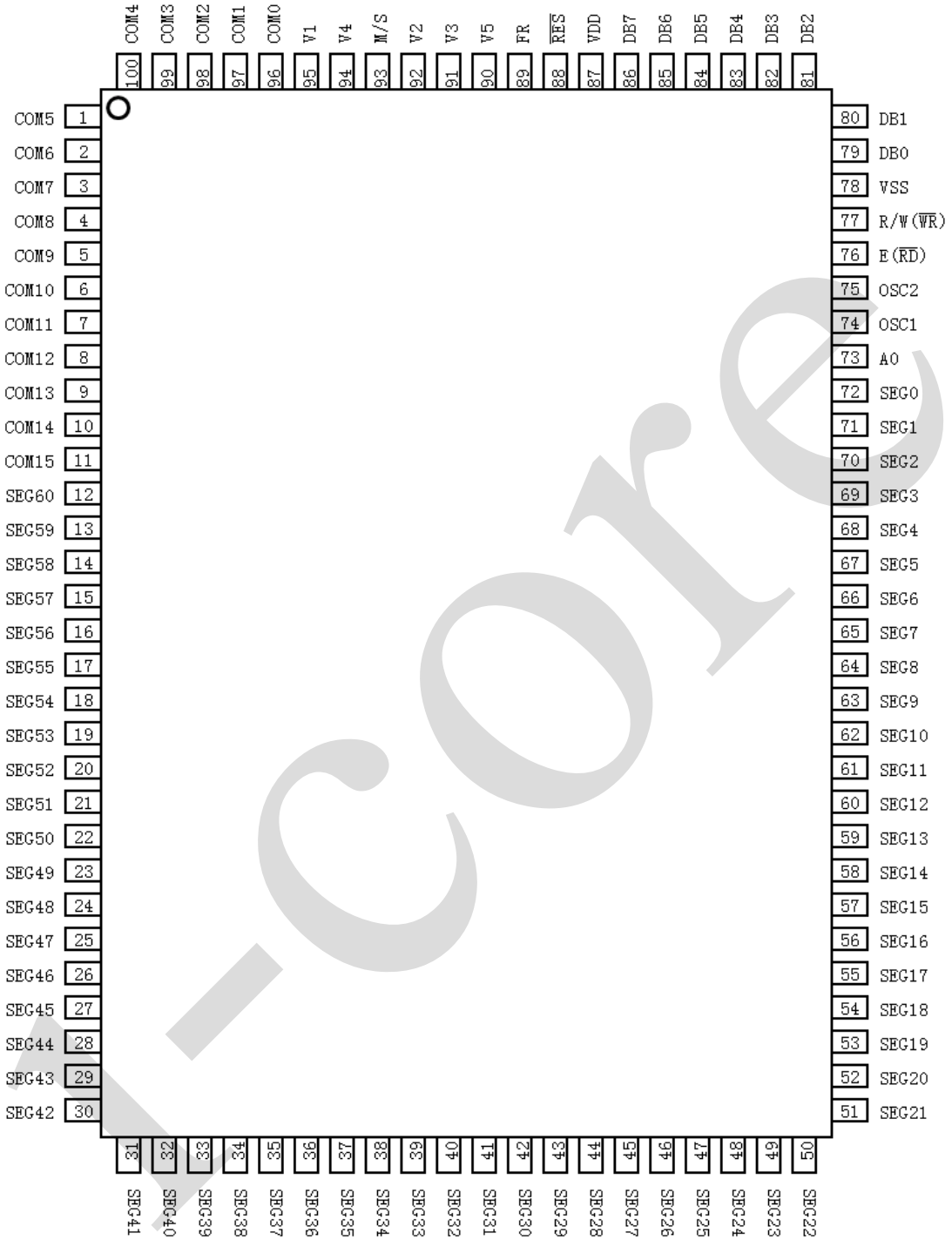

RES
E, R/W
(RD)(WR)
A0
D0 ~ D7
MPU INTERFACE
BUS HOLDER
STATUS
COMMAND DECODER
LOW ADDRESS REGISTER
COLUMN ADDRESS REGISTER
COLUMN ADDRESS COUNTER
COLUMN ADDRESS DECODER
DISPLAY TIMING GENERATOR
FR
OSC1
OSC2
INTERNAL BUS
I/O BUFFER
DISPLAY DATA RAM
2560 BITS
LINE ADDRESS DECODER
LINE COUNTER
DISPLAY START LINE REGISTER
DISPLAY DATA LATCH CIRCUIT
COMMON COUNTER
LCD DRIVER CIRCUIT
VSS
VDD
SG0 ~SG60
V1, V4, M/S
CM0 ~ CM15
V2, V3, V5

2.2、Pin Configurations



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2.3、Pin Description

Pin No.	Pin Name	Description
87	VDD	Connected to +5V power. Common to MPU power pin VCC.
78	VSS	0V, connected to system GND.
95~94 90~92	V1~V5	Multi-level power used to drive LCDs. Voltage specified to each LCD cell is divided by resistors or impedance-converted by an operational amplifier before being applied. Each voltage to be applied must be based on VDD, while fulfilling the following conditions: VDD≥V1≥V2 ≥V3≥V4≥V5
79~86	D7~D0	8–bit, tri-state, bi-directional I/O bus. Normally, connected to the data bus of an 8–/16–bit standard microcomputer.
73	A0	Input pin. Normally, the LSB of the MPU address bus is connected to this input pin to provide data/command selection. 0: Display control data on D7–D0 1: Display data on D7–D0
88	$\overline{RES}$	Input pin. The AiP31520 can be reset or initialized by setting RES to low level (if it is interfaced with a 68 family MPU) or high level (if with an 80 family MPU). This reset operation occurs when an edge of the RES signal is sensed. The level input selects the type of interface with the 68 or 80 family MPU: High level: Interface with 68 family MPU Low level: Interface with 80 family MPU
74	OSC1	An oscillation amplifier input pin to which an oscillation resistor (R_f) is connected.
76	E($\overline{RD}$)	Chip interfaced with 68 family MPU: Enable Clock signal input for the 68 family MPU. Chip interfaced with 80 family MPU: “L” Active input pin to which the 80 family MPU $\overline{RD}$ signal is connected. With this signal held at “L”, the AiP31520 data bus works as output.
77	R/W($\overline{WR}$)	Chip interface with 68 family MPU: Read/Write control signal input pin. R/W = “H”:Read R/W = “L”:Write Chip interfaced with 80 family MPU: “L” Active input pin to which the 80 family $\overline{WR}$ is connected. The signal on the data bus is fetched by the leading edge of $\overline{WR}$.
75	OSC2	For a chip containing an oscillator, this pin works as the oscillation amplifier output pin to which an oscillation resistor (R_f) is connected.
89	FR	LCD AC signal I/O pin. Connected to pin M of the common driver. I/O selection: Chip containing commons M/S = 1:Output M/S = 0:Input

<table>
<tr><td>12~72</td><td>SEG0~SEG60</td><td>LCD column (segment) driving output. One of the VDD, V2, V3 and V5 levels is selected by a combination of the content of display RAM and the FR signal. Fig 1</td></tr>
<tr><td>96~100
1~11</td><td>COM0~COM15</td><td>LCD common (row) driving output. One of the VDD, V1, V4 and V5 levels is selected by a combination of the output of the common counter and the FR. Fig 2</td></tr>
<tr><td>93</td><td>M/S</td><td>Input signal which selects the master or slave LSI. Connected to VDD or VSS.
M/S = VDD:Master
M/S = VSS:Slave
M/S selection changes the function of pins FR, COM0–COM15, OSC1 (CS) and OSC2 (CL):
<table>
<tr><th>M/S</th><th>FR</th><th>COM Output</th><th>OSC1</th><th>OSC2</th></tr>
<tr><td>VDD</td><td>Output</td><td>COM0~COM15</td><td>Input</td><td>Output</td></tr>
<tr><td>VSS</td><td>Input</td><td>COM31~COM16</td><td>NC</td><td>Input</td></tr>
</table>
</td></tr>
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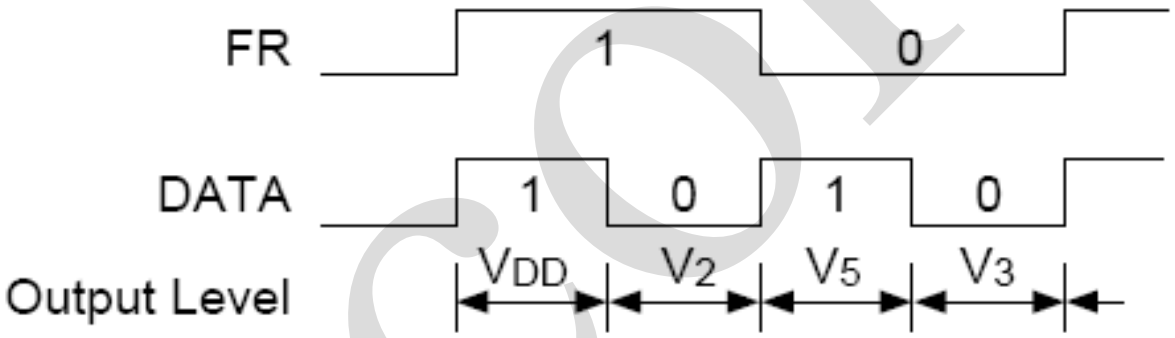

Fig.1 LCD Column (Segment) Driving Output Timing

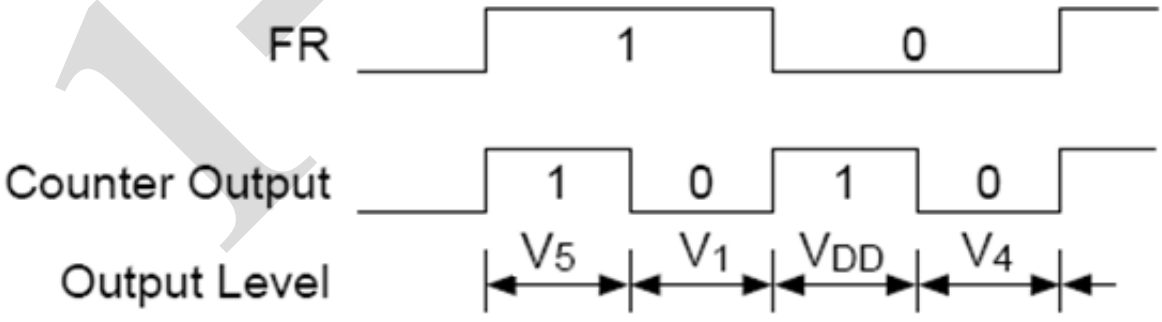

Fig.2 LCD Common (row) driving output

3、Electrical Parameter

3.1、Absolute Maximum Ratings

Characteristic	Symbol	Conditions	Value	Unit
Supply voltage (1)	VSS	-	-8~+0.3	V
Supply voltage (2)	V5	-	-16.5~+0.3	V
Supply voltage (3)	V1, V2, V3, V4	-	V5~+0.3	V
Input voltage	V_{IN}	-	VSS-0.3~+0.3	V
Output voltage	V_{OUT}	-	VSS-0.3~+0.3	V
Allowable loss	P_D	-	250	mW
Ambient temperature	T_{amb}	-	-40~+85	℃
Storage temperature	T_{stg}	-	-65~+150	℃
Soldering temperature	T_L	10s	250	℃

Note:

1. All voltages are based on VDD = 0V.
2. The following condition must always hold true with voltages V1, V2, V3, V4 and V5:
   VDD≥ V1≥ V2 ≥V3≥V4 ≥V5
3. The LSI may be permanently damaged if used with any value in excess of the absolute maximum ratings. During normal operation, the LSI should preferably be used within the specified electrical characteristics. Failure to meet them can cause the LSI to malfunction or lose its reliability.
4. Generally, flat package LSIs may have moisture resistance lowered when solder dipped. In mounting LSIs on a board, it is recommended to use a method which is least unlikely to give thermal stress on the package resin.

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3.2、Electrical Characteristics

3.2.1、DC Characteristics 1

(VDD=0V, T_{amb}=+25℃, unless otherwise specified.)

Parameter		Symbol	Condition		Min.	Typ.	Max.	Unit	Applicable pin
Operating voltage (1)*1	Recommended	VSS	-		-5.5	-5.0	-4.5	V	VSS
	Allowable		-		-7.0	-	-2.4		
Operating voltage (2)	Recommended	V5	-		-13.0	-	-3.5	V	V5*10
	Allowable		-		-13.0	-	-		
	Allowable	V1,V2	-		0.6×V5	-	VDD	V	V1,V2
	Allowable	V3,V4	-		V5	-	0.4×V5	V	V3,V4
High level input voltage		V_{IHT}	-		VSS+2.0	-	VDD	V	*2 *3
		V_{IHC}	-		0.2×VSS	-	VDD		
Low level input voltage		V_{ILT}	-		VSS	-	VSS+0.8	V	*2 *3
		V_{ILC}	-		VSS	-	0.8×VSS		
High level output voltage		V_{OHT}	I_{OH}= -3.0mA		VSS+2.4	-	-	V	*4 *5 OSC2
		V_{OHC1}	I_{OH}= -2.0mA		VSS+2.4	-	-		
		V_{OHC2}	I_{OH}= -120uA		0.2×VSS	-	-		
Low level output voltage		V_{OLT}	I_{OL}= 3.0mA		-	-	VSS+0.4	V	*4 *5 OSC2
		V_{OLC1}	I_{OL}= 2.0mA		-	-	VSS+0.4		
		V_{OLC2}	I_{OL}= 120uA		-	-	0.8×VSS		
Input leakage current		I_{LI}	-		-1.0	-	1.0	uA	*6
Output leakage current		I_{LO}	-		-3.0	-	3.0	uA	*7
LCD driver ON resistor		R_{ON}	T_{amb}=25℃	V5= -5.0V	-	5.0	7.5	kΩ	SEG0~60 *11 COM0~15
				V5= -3.5V	-	10.0	50.0		
Static current dissipation		I_{DDQ}	$\overline{CS}$=CL=VDD		-	0.05	1.0	uA	VDD
Dynamic current dissipation		$I_{DD(1)}$	During display V5=-5.0V	f_{CL}=2kHz	-	2.0	5.0	uA	VDD
				R_f=1MΩ	-	9.5	15.0		
				f_{CL}=18kHz	-	5.0	10.0		
		$I_{DD(2)}$	During access t_{CYC}=200kHz		-	300	500	uA	*8
Input pin capacitance		C_{IN}	T_{amb}=25℃ f=1MHz		-	5.0	8.0	pF	All input pins
Oscillation frequency		f_{OSC}	R_f=1.0MΩ± 2% VSS=-5.0V		15	18	21	kHz	*9
			R_f=1.0MΩ±2% VSS=-3.0V		11	16	21		

Reset time	t_R	-	1.0	-	1000	us	$\overline{RES}$

Note:

*1. Operation over a wide range of voltages is guaranteed except where a sudden voltage change occurs during access.

*2. Pins A0,D0~D7,E($\overline{RD}$),R/W($\overline{WR}$)and$\overline{CS}$.

*3. Pins CL,FR,M/S and$\overline{RES}$

*4. Pins D0~D7

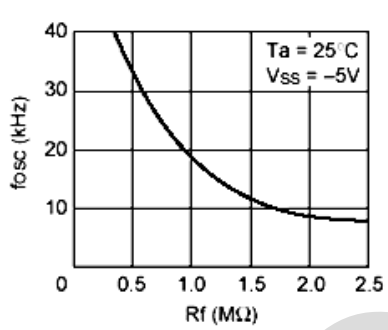
*5. Pins FR

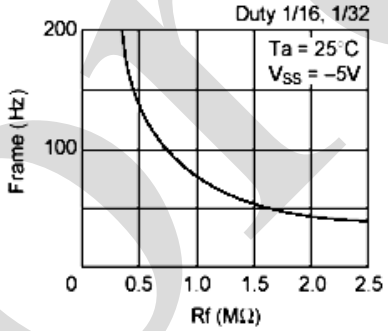
*6. Pins A0, E($\overline{RD}$),R/W($\overline{WR}$),$\overline{CS}$,CL and$\overline{RES}$

*7. Applicable when pins D0-D7 and FR are at high impedance.

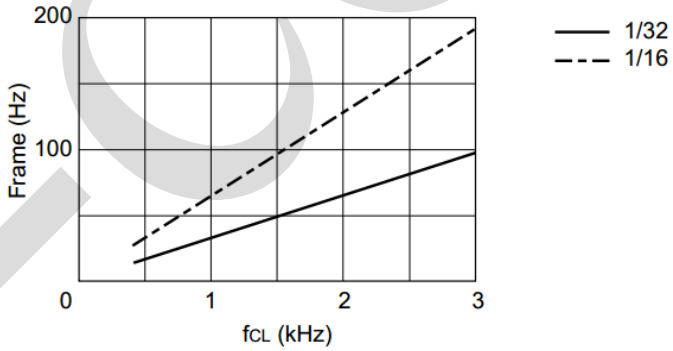
*8. This value is current consumption when a vertical stripe pattern is written at t_{CYC}.
Current consumption during access is nearly proportionate to access frequency (t_{CYC}). Only TDD (1) is consumed while no access is made.

*9. Relationship between oscillation frequency, frame and R_f

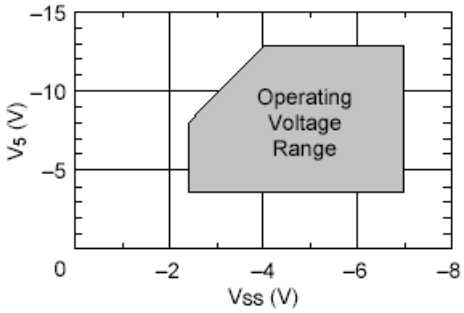




Relationship between external clock (f_{CL}) and frame



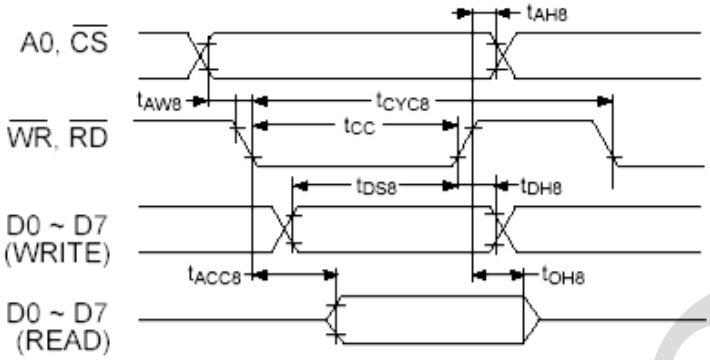
*10. Operating voltage ranges of VSS and V5



*11. Resistance with a voltage of 0.1V applied between the output pin (SEG, COM) and each power pin (V1, V2, V3, V4). It is specified within the operating voltage range.

3.2.2、AC Characteristics

● **System Bus Read/Write I (80 Family MPU)**



(T_{amb}=+25℃,VSS=-5.0V±10%)

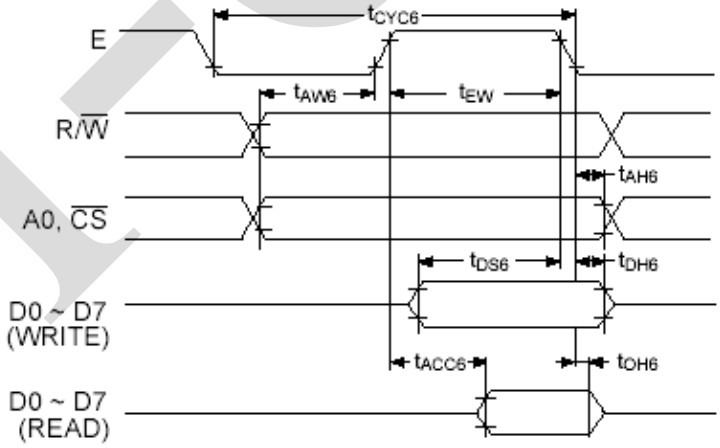
Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time Address setup time	A0, $\overline{CS}$	t_{AH8} t_{AW8}	-	10 20	-	ns
System cycle time Control pulse width	$\overline{WR}$, $\overline{RD}$	t_{CYC8} t_{CC}		1000 200	-	ns
Data setup time Data hold time $\overline{RD}$ access time Output disable time	D0~D7	t_{DS8} t_{DH8} t_{ACC8} t_{OH8}	C_L=100pF	80 10 - 10	- - 90 60	ns

Note:

*1. Each of the values where VSS=-3.0V is about 200% of that where VSS=-5.0V

*2. The rise or fall time of input signals should be less than 15ns.

● **System Bus Read/Write II (68 Family MPU)**



(T_{amb}=+25℃,VSS=-5.0V±10%)

Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time Address setup time Address hold time		A0, $\overline{CS}$ R/$\overline{W}$	t_{CYC6} *1 t_{AW6} t_{AH8}	-	1000 20 10	- -	ns
Data setup time Data hold time Output disable time Access time		D0~D7	t_{DS6} t_{DH6} t_{OH6} t_{ACC6}	- - C_L=100pF -	80 10 10 -	- - 60 90	ns
Enable pulse width	Read	E	t_{EW}	-	100	-	ns
	Write				80	-	ns

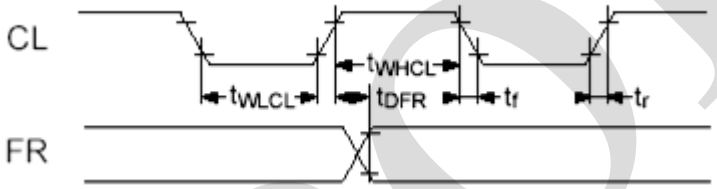
Note:

*1. t_{CYC6} indicates the cycle time during which CS•E = "H". It does not mean the cycle time of signal E.

*2. Each of the values where VSS=-3.0V is about 200% of that where VSS =-5.0V

*3. The rise or fall time of input signals should be less than 15ns.

● Display Control Timing



● Input Timing

(T_{amb}=+25℃,VSS=-5.0V±10%)

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Low level pulse width	CL	t_{WLCL}	-	35	-	-	us
High level pulse width		t_{WHCL}	-	35	-	-	us
Rise time		t_r	-	-	30	150	ns
Fall time		t_f	-	-	30	150	ns
FR delay time	FR	t_{DFR}	-	-2.0	0.2	2.0	us

● Output Timing

(T_{amb}=+25℃,VSS=-5.0V±10%)

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
FR delay time	FR	t_{DFR}	C_L=100pF	-	0.2	0.4	us

Note:

*1. The listed FR input delay time applies to the SED1521 and AiP31520 (slave).
The listed FR output delay time applies to the AiP31520 (master).

*2. Each of the values where VSS=-3.0V is about 200% of that where VSS=-5.0V.

4、Function Description

4.1、Description Of Circuit Blocks

4.1.1、MPU Interface

- **Selection of Interface Type**

The AiP31520 Series uses 8 bits of bi-directional data bus (D0–D7) to transfer data. The reset pin is capable of selecting MPU interface; setting the polarity of $\overline{RES}$ to either "H" or "L" can provide direct interface of the AiP31520 with a 68 or 80 family MPU (see Table 1 below).

Table 1

Polarity of $\overline{RES}$	Type	A0	E	R/W	$\overline{CS}$	D0~D7
H	68 MPU	↑	↑	↑	↑	↑
L	80 MPU	↑	$\overline{RD}$	$\overline{WR}$	↑	↑

- **Identification of Data Bus Signals**

The AiP31520 uses a combination of A0, E, R/W, ($\overline{RD}$, $\overline{WR}$) to identify a data bus signal.

Table 2

Common	68 MPU	80 MPU		Function
A0	R/W	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Read display data
1	0	1	0	Write display data
0	1	0	1	Read status
0	0	1	0	Write to internal register (command)

- **Access to Display Data RAM and Internal Register**

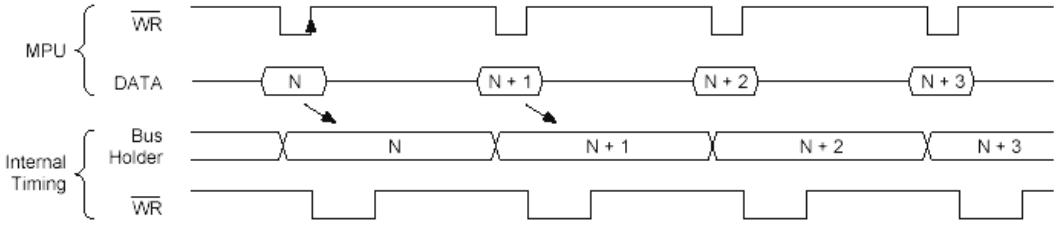
In order to make matching of operating frequencies between the MPU and the display data RAM or internal register, the AiP31520 performs a sort of LSI–LSI pipelining via the bus holder attached to the internal data bus.

Consider the case where the MPU reads the content of the display data RAM. In the first data read cycle (dummy), the data is stored on the bus holder. In the next data read cycle, the data is read from the bus holder to the system bus.

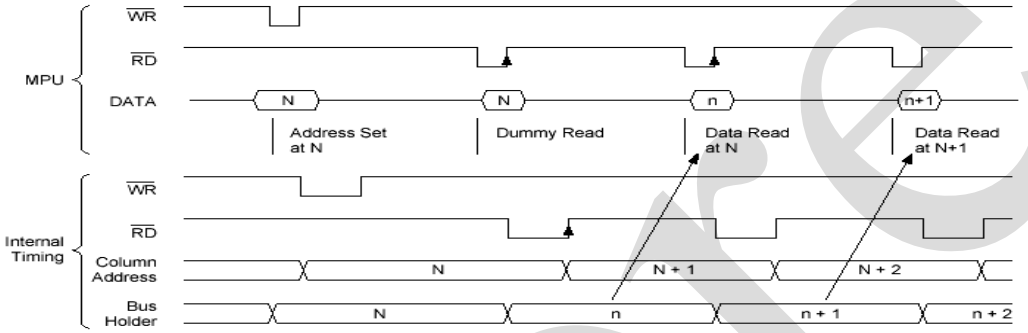
Also, consider the case where the MPU writes data to the display data RAM. In the first data write cycle, the data is held on the bus holder. The data is written to the display data RAM before the next data write cycle begins.

Therefore, MPU's access to the AiP31520 is affected not by display data RAM access time (t_{ACC},t_{DS}) but by cycle time (t_{CYC}). This leads to faster transfer of data to and from the MPU. If the cycle time requirement is not met, the MPU has only to execute the NOP instruction and this is apparently equivalent to execution of a waiting operation. However, there is a restriction on the read sequence of the display data RAM; when an address is set, its data is output not to the first read instruction (immediately following the address setting operation) but to the second read instruction. Thus, one dummy read cycle is necessary after an address set or write cycle. This relation is shown in Figures a) and b).

a) Write Timing Diagram



b) Read Timing Diagram



4.1.2、Busy Flag

Busy flag being "1" means that the AiP31520 is performing its internal operation and any instruction other than Read Status is disabled. The busy flag is output to pin D7 by a Read Status instruction. As long as the cycle time (t_{CYC}) requirement is met, the flag need not be checked before each command and this dramatically improves the MPU performance.

4.1.3、Display Start Line Register

This register is a pointer which determines the start line corresponding to COM0 (normally, the uppermost line of display) for display of data in the display data RAM. It is used for scrolling the display or changing the page from one to another. Executing the Set Display Start Line command sets 5 bits of display start address in this register. Its content is preset in the line counter at each timing the FR signal changes. The line counter is incremented synchronously to a CL input, thus generating a line address for sequential reading of 80 bits of data from the display data RAM to the LCD driver circuit.

4.1.4、Column Address Counter

The column address counter is a 7–bit presettable counter which gives column addresses of the display data RAM as shown in Fig.4.When a Read/Write Display Data command comes in, the counter is incremented by 1. For any nonexisting address over 50H, the counter is locked and not incremented.
The column address counter is independent from the page register.

4.1.5、Page Register

This register gives a page address of the display data RAM as shown in Fig.4. The Set Page Address command permits the MPU to access a new page of the display data RAM.

4.1.6、Display Data RAM

Dot data for display is stored in this RAM. Since the MPU and LCD driver circuit operate independently of each other, data can be changed asynchronously without adverse effect on the display.

One bit of the display data RAM is assigned to one bit of LCD:

LCD on= “1”

LCD off= “0”

The ADC command inverts the assignment relationship between a display data RAM column address and a segment output (see Fig.4).

4.1.7、Common Timing Generator

This circuit generates common timing and frame (FR) signals from the basic clock (CL). The Select Duty command selects a duty of 1/16 or 1/32. The 1/32 duty is achieved by a two-chip (master and slave) configuration (common multi-chip system).

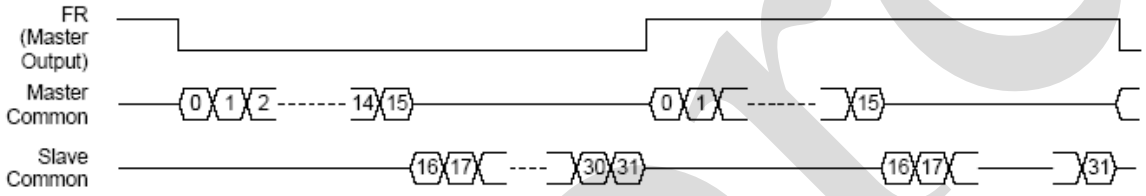


Fig.3 Common Timing Diagram

4.1.8、Display Data Latch Circuit

The display data latch circuit temporarily stores the data which will be output from the display data RAM to the LCD driver circuit at one-common intervals. The display ON/OFF and Static Driver ON/OFF commands control the latched data so that the data in the display data RAM remains unchanged.

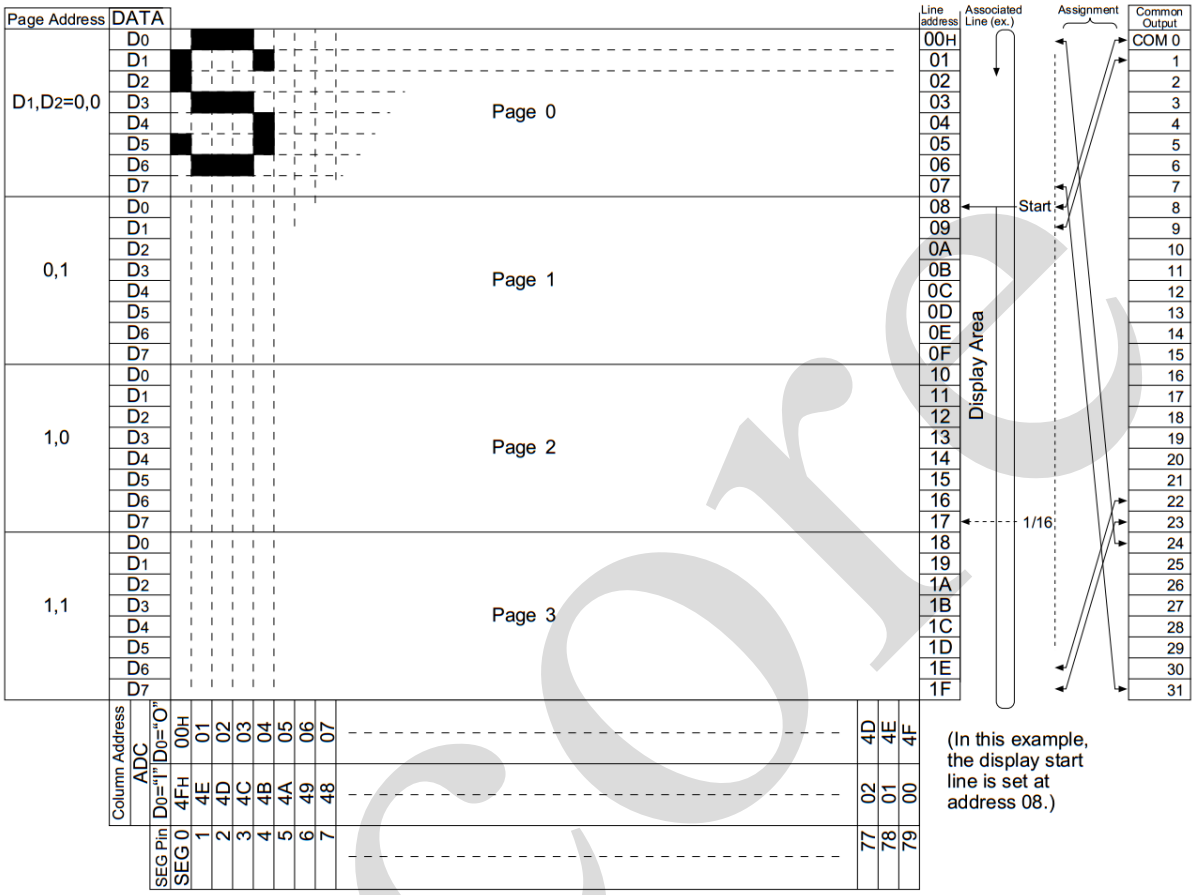


Fig.4 Relationship between Display Data RAM Locations and Addresses (Display Start Line:08)

4.1.9、LCD Driver Circuit

This circuit generates 80 sets of multiplexer that generate quartet levels for LCD driving. Display data in the display data latch, common timing generator output and FR signal are combined to output an LCD driving waveform.

4.1.10、Display Timing Generator

This circuit generates an internal display timing signal from the basic clock (CL) and frame signal (FR).

The frame signal FR makes the LCD driver circuit generate a dual frame AC driving waveform (type B) to drive LCD, while making both the line counter and common timing generator synchronized to the FR signal output LSI (dedicated common driver or the AiP31520 master LSI). To achieve these functions, the FR signal must be a clock with a duty of 50% which is synchronized to the frame period.

The clock CL is a clock used to operate the line counter. For a system in which both the AiP31520 and SED1521F coexist, they should be of LSI types having the same clock frequency to be applied to pin CL.

4.1.11、Oscillation Circuit

This circuit is a low-power CR oscillator which uses an oscillation resistor Rf alone to adjust the oscillation frequency. It generates display timing signals. The AiP31520 is available in two LSI types if classified by oscillation: one LSI type contains an oscillation circuit and the other uses an externally provided clock.

The oscillation resistor Rf is connected as shown below. Where an LSI containing an oscillation circuit is operated with an external clock, it is necessary to input the clock with the same phase as OSC2 of the master LSI to OSC2 of the slave LSI.

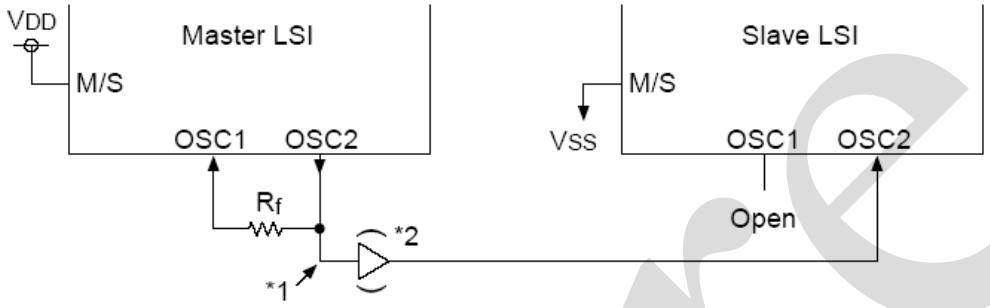


Fig.5 LSI Containing Oscillator

Note:

1.As the parasitic capacitance in this portion increases, the oscillation frequency will shift to a lower level. The R_f musthave a smaller value than the specification.

2. For a system having two or more slave LSIs, a CMOS buffer is necessary.

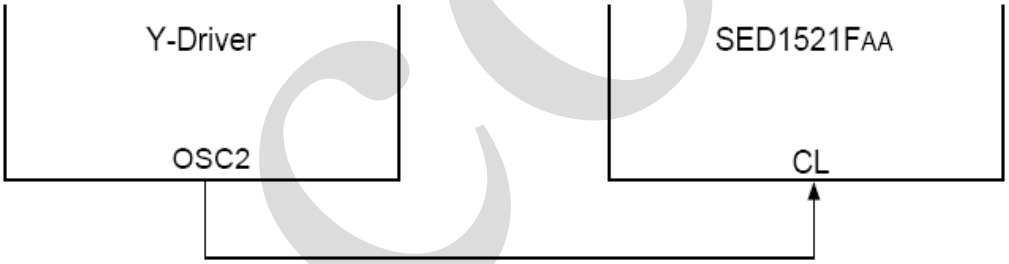


Fig.6 LSI Operating with External Clock

4.1.12、Reset Circuit

This circuit senses the leading edge or trailing edge of $\overline{RES}$ and initializes the system when its power is switched on.

Initialization:

(a) Display off

(b) Display start line register:First line

(c) Static drive off

(d) Column address counter:Address 0

(e) Page address register:Page 0

(f) Select duty:1/32

(g) Select ADC:Forward (ADC command D0="0", ADC status flag="1")

(h) Read modify write off

The input at pin $\overline{RES}$ is level-sensed to select an MPU interface mode as shown in Table 1. For interfacing with an 80 family MPU, an "H" active reset signal is input to pin $\overline{RES}$. For interfacing with a 68 family MPU, an "L" active reset signal is input to the pin.

As exemplified in section 6 "MPU Interface", pin RES is connected to the MPU reset pin. Thus the AiP31520 and the MPU are initialized at the same time. If system is initialized by pin $\overline{RES}$ at power on, it may no longer be reset.

The Reset command causes initialization (b), (d) and (e).

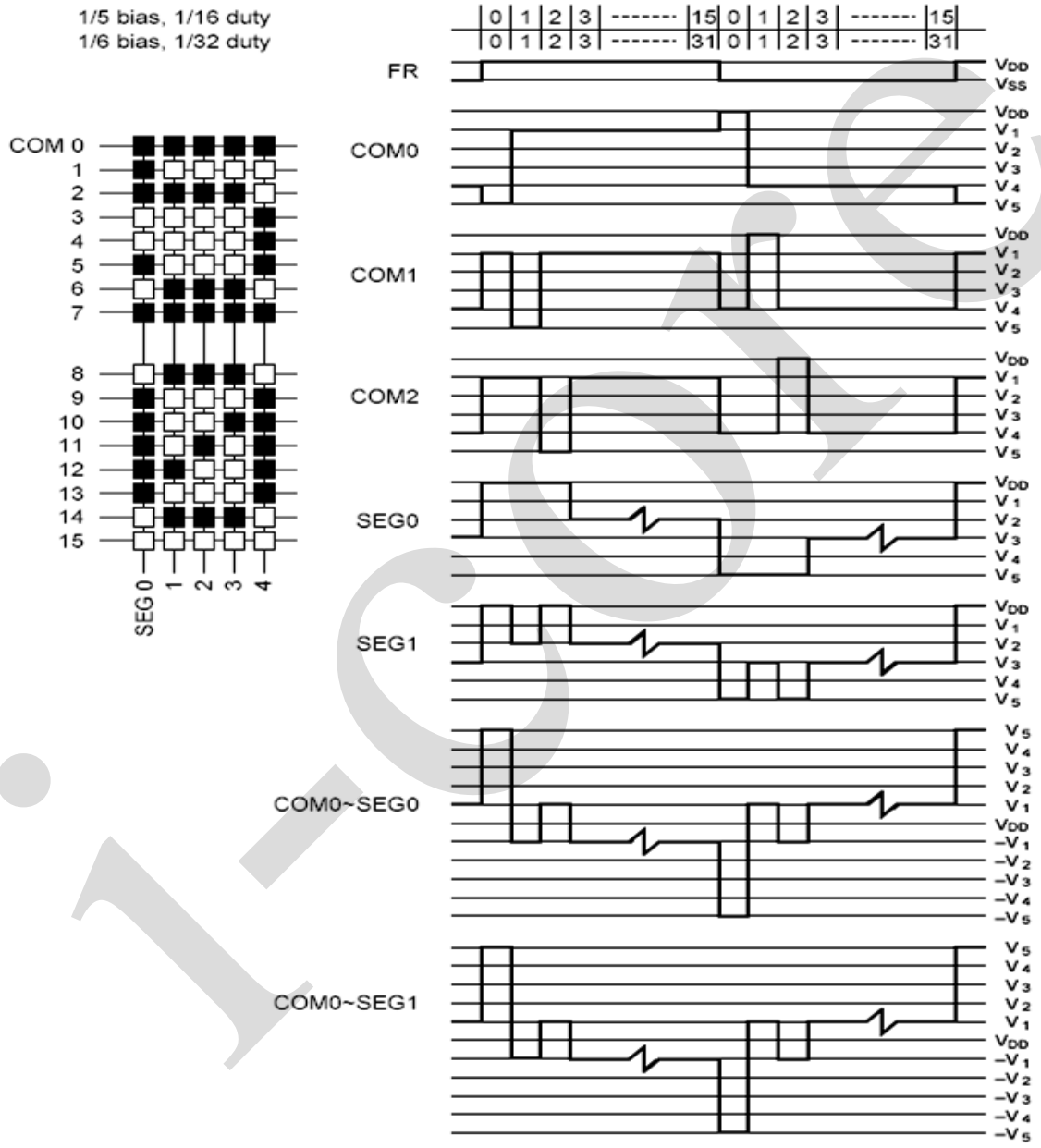


Fig.7 Example of LCD Driving Waveform

4.2、Commands

Table 3 lists the commands used with the AiP31520. This LSI uses a combination of A0, R/W ($\overline{RD}$, $\overline{WR}$) to identify a data bus signal. Interpretation and execution of a command depends not on external clock but on internal timing alone. Therefore, a command can be executed so fast that no busy check is needed.
A detailed description of commands follows.

- **Display ON/OFF**

This command forces all display to turn on or off.

A0	R/W $\overline{RD}$	R/W $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

D =0:Display OFF
D =1:Display ON

- **Display Start Line**

This command specifies a line address thus marking the display line that corresponds to COM0. Display begins with the specified line address and covers as many lines as match the display duty in address ascending order. Dynamic line address change with the Display Start Line command enables column-wise scrolling or page change.

A0	R/W $\overline{RD}$	R/W $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	A4	A3	A2	A1	A0

A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0
0	0	0	0	1	1
		-			-
		-			-
1	1	1	1	1	31

- **Set Page Address**

This command is used to specify a page address equivalent to a row address for MPU access to the display data RAM. A required bit of the display data RAM can be accessed by specifying its page address and column address. Changing the page address causes no change in display.

		R/W							
A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	1	0	A1	A0

A1	A0	Page
0	0	0
0	1	1
1	0	2
1	1	3

- **Column Address**

This command specifies a display data RAM column address. The column address is incremented by 1 each time the MPU accesses from the set address to the display data RAM. Thus, it is possible for the MPU to gain continuous access to only the data. This incrementing stops with address 80; the page address is not continuously changed.

		R/W							
A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	A6	A5	A4	A3	A2	A1	A0

A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			-				-
			-				-
1	0	0	1	1	1	1	79

- **Read Status**

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY: BUSY being “1” means that system is performing an internal operation or is reset. No command is accepted before BUSY = “0”. As long as the cycle time requirement is met, no BUSY check is needed.

ADC: Indicates assignment of column addresses to segment drivers.

0: Inverted (column address 79-n↔segment driver n)

1: Forward (column address n↔segment driver n)

ON/OFF: Indicates display on or off.

0: Display on

1: Display off

This bit has polarity reverse to the Display ON/OFF command.

RESET: Indicates that system is being initialized by the REST signal or the Reset command.

0: Display mode

1: Being reset

- **Write Display Data**

This command allows the MPU to write 8 bits of data into the display data RAM. Once the data is written, the column address is automatically incremented by 1; this enables the MPU to write multiword data continuously.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

- **Read Display Data**

This command allows the MPU to read 8 bits of data from the display data RAM location specified by a column address and a page address. Once the data is read, the column address is automatically incremented by 1; this enables the MPU to read multi-word data continuously.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

- **Select ADC**

This command inverts the relation of assignment between display data RAM column addresses and segment driver outputs. In other words, the Select ADC command can software-invert the order of segment driver output pins, reducing the restrictions on the configuration of ICs at LCD module assembly. For details, see Fig. 4.

Incrementing the column address by 1, which takes place after the MPU writing or reading display data, follows the sequence of column addresses specified in Fig. 4.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

D = 0: Clockwise output (forward)

D = 1: Counterclockwise output (reverse)

- **Static Drive ON/OFF**

This command forces all display to be on and, at the same time, all common output to be selected.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

D = 0: Static drive off

D = 1: Static drive on

- **Select Duty**

This command is used to select the duty (degree of multiplexity) of LCD driving. It is valid for the AiP31520 (actively operating LSI) only, not valid for the SED1521F (passively operating LSI).The SED1521F operates with any duty determined by the FR signal.

A0	R/W $\overline{RD}$	R/W $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	0	D

D = 0: Duty 1/16

D = 1: Duty 1/32

- **Read Modify Write**

This command is used with the End command in a pair. Once it has been entered, the column address will be incremented not by the Read Display Data command but by the Write Display Data command only. This mode will stay until the End command is entered.

Entry of the End command causes the column address to return to the address which was valid when the Read Modify Write command was entered. This function lessens the load of the MPU when the data in a specific display area are repeatedly updated.

A0	R/W $\overline{RD}$	R/W $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Even in the Read Modify Write mode, any command other than Read/Write Data and Set Column Address may be used.

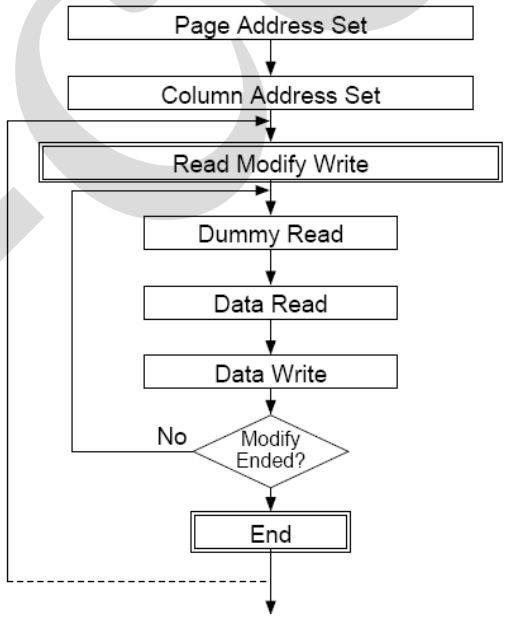


Fig.8 Cursor Blinking Sequence

- **END**

This command cancels the Read Modify Write command, returning the column address to the initial mode address. See Fig.8 and Fig.9

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

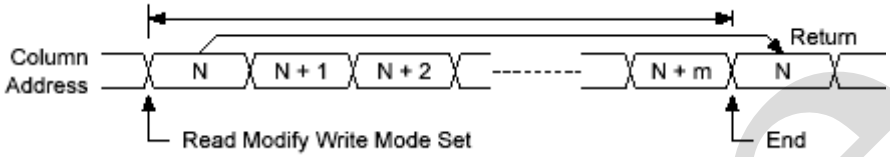


Fig.9 End Timing

- **RESET**

This command initializes the display start line register, column address counter, and page address counter without any effect on the display data RAM.

		R/W								
A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

Initialization at power-on is performed not by the Reset command but by a reset signal applied to the $\overline{RES}$ pin.

- **Save Power(Combined Command)**

Static drive going on with display off invokes power-saving mode, reducing current consumption to nearly static current level. During this mode, the AiP31520 holds the following conditions:

(a) It stops driving the LCD; the segment and common driver outputs are at VDD level.

(b) Oscillation and external clock input are disabled; OSC2 is in floating condition.

(c) The display data and operational mode are held.

The power-saving mode is cancelled by display on or static drive off.

If an external resistor division circuit is used to give LCD driving voltage level, the current flowing into the resistors must be cut off by the power-save signal.

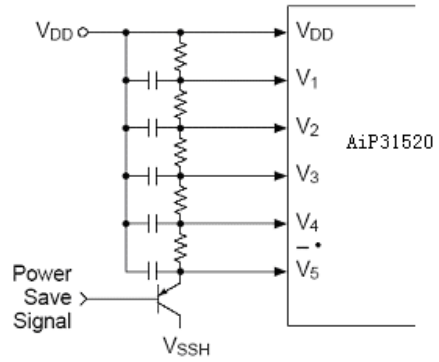


Fig.10 External Resistor Division Circuit

Table3 Command

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0/1	Turns all display on or off, independently of display RAM data or internal status. 1:ON 0:OFF
Display start line	0	1	0	1	1	0	Display Start Address (0~31)					Specifies RAM line corresponding to uppermost line (COM0) of display.
Set page address	0	1	0	1	0	1	1	1	0	Page (0~3)		Sets display RAM page in page address register.
Set column address	0	1	0	0	Column Address（0～79）							Sets display RAM column address in column address register.
Read status	0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0	Reads the following status: BUSY 1: Internal operation 0: Ready ADC 1: CW output(forward) 0: CCW output (reverse) ON/OFF 1: Display off 0: Display on RESET 1: Being reset 0: Normal
Write data	1	1	0	Write Data								Writes data from data bus into display RAM.
Read data	1	0	1	Read Data								Reads data from display RAM onto data bus.
Select ADC	0	1	0	1	0	1	0	0	0	0	0/1	Used to invert relationship of assignment between display RAM column addresses and segment

												driver outputs. 0:CW output (forward) 1:CCW output (reverse)
Static drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Selects normal display or static driving operation. 1: Static drive (power-saving mode) 0: Normal driving
Select duty	0	1	0	1	0	1	0	1	0	0	0/1	Selects LCD cell driving duty. 1:1/32 0:1/16
Read modify write	0	1	0	1	1	1	0	0	0	0	0	Increments column address counter by 1 when display data is written. (This is not done when data is read.)
END	0	1	0	1	1	1	0	1	1	1	0	Clears read modify write mode.
RESET	0	1	0	1	1	1	0	0	0	1	0	Sets display start line register on the first line. Also sets column address counter and page address counter to 0.

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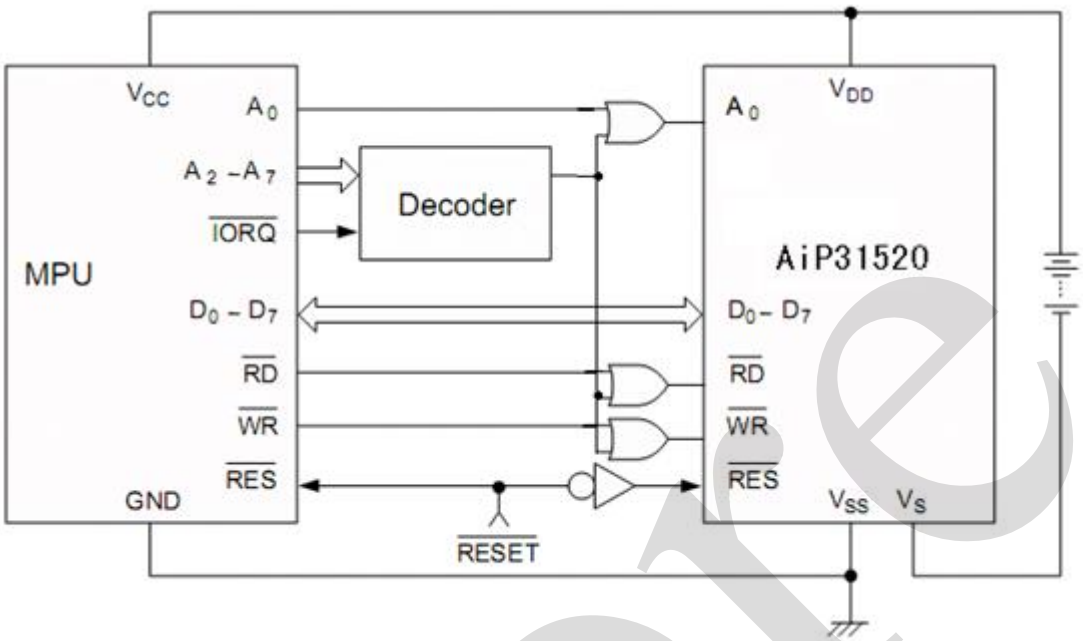
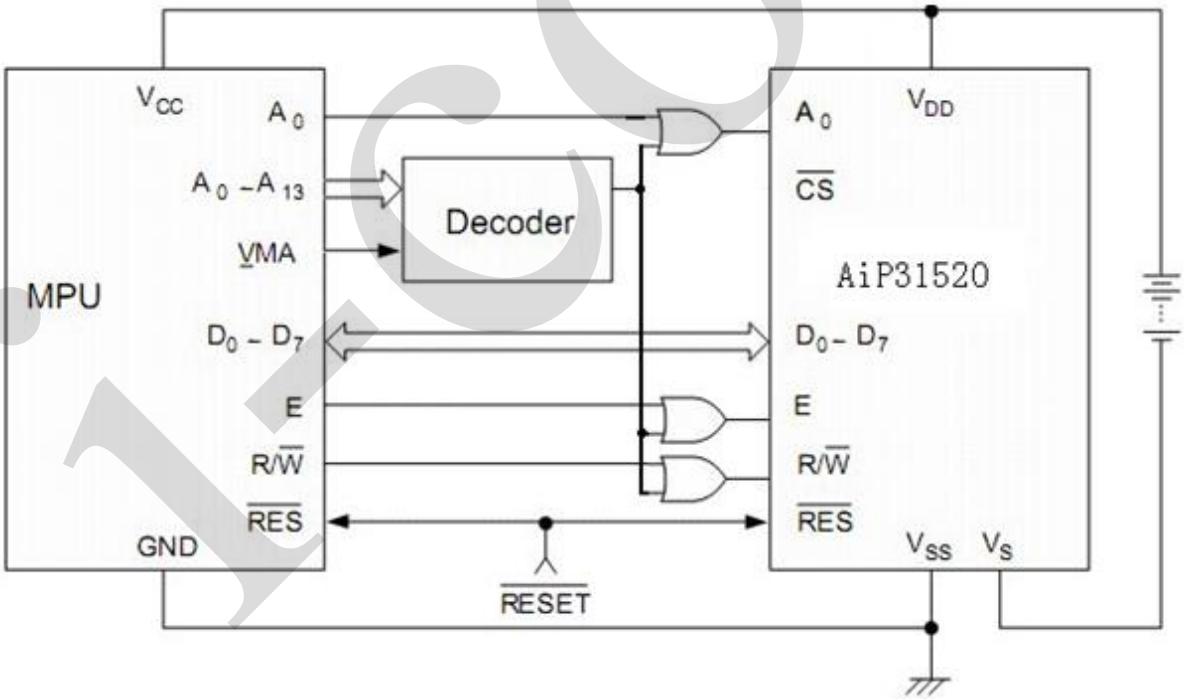
4.3、The MPU Interface

4.3.1、80 Family MPU

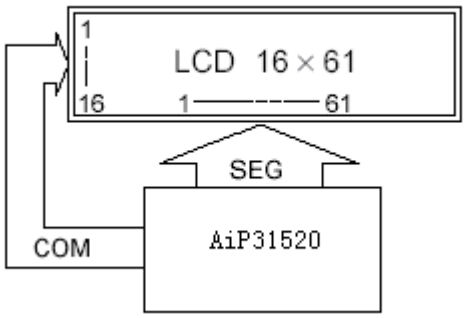


4.3.2、68 Family MPU

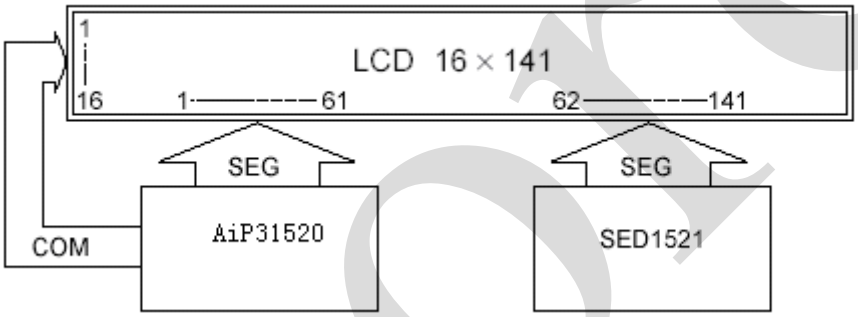


4.4、Typical Connections With LCD Panel

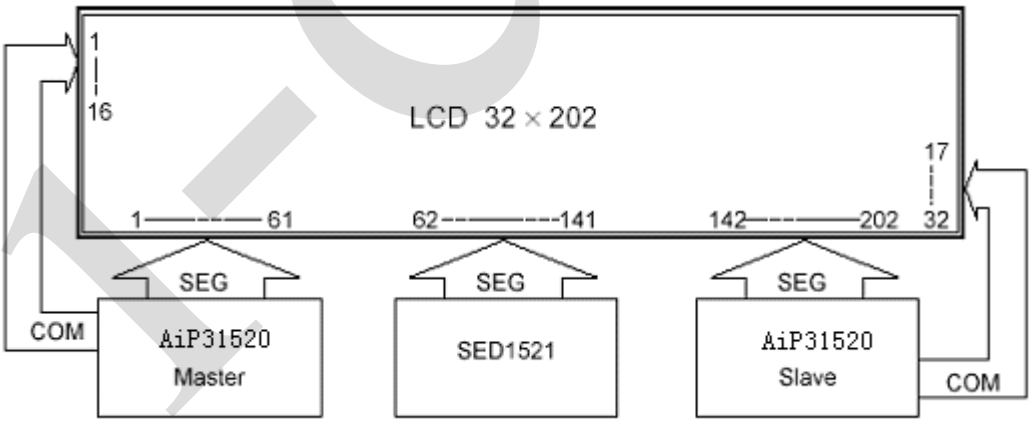
- **Duty 1/16, 10 Characters ×2 Lines(1 character=6×8dots)**



- **Duty 1/16, 23 Characters ×2 Lines(1 character=6×8dots)**

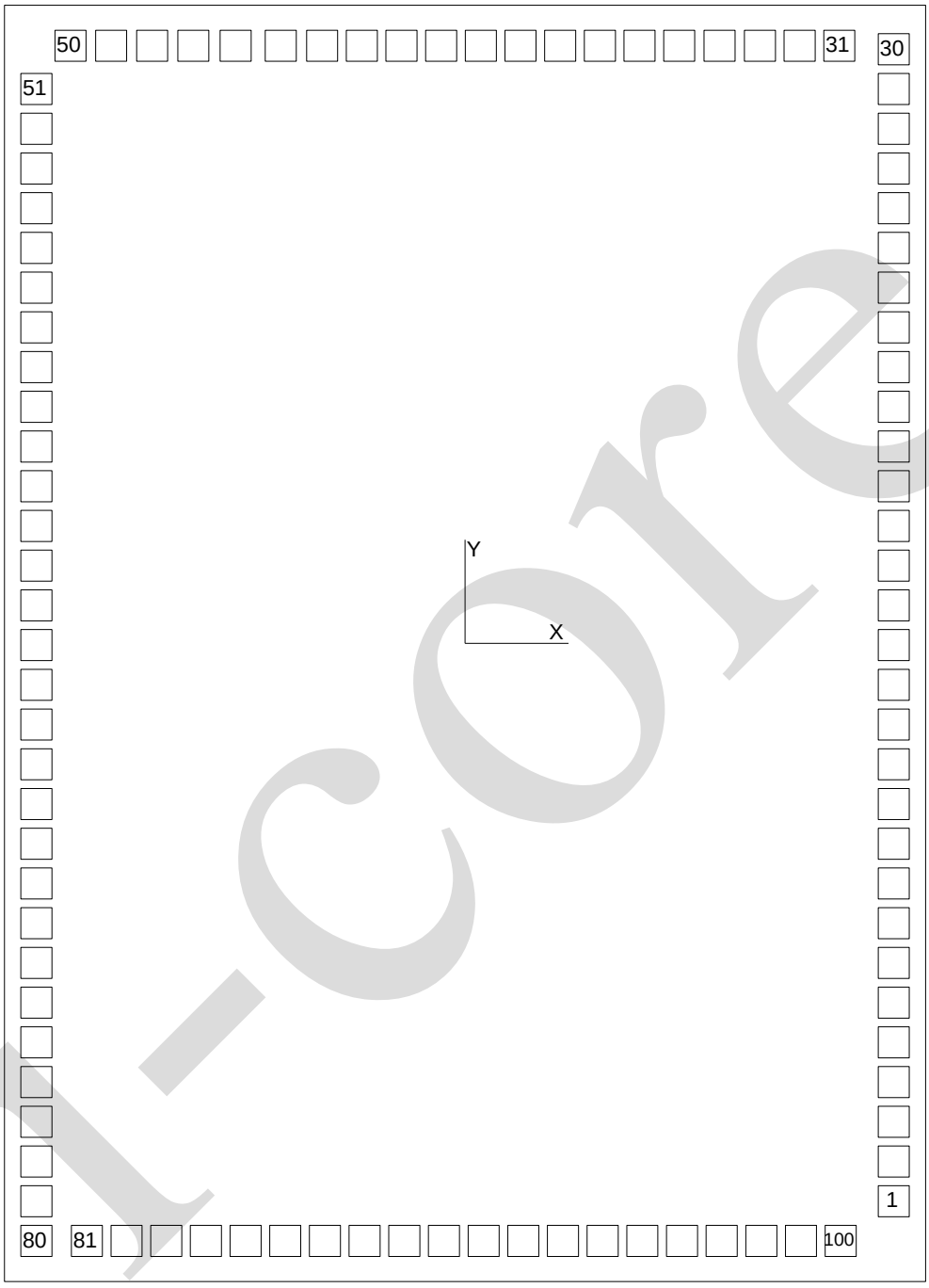


- **Duty 1/32, 33 Characters ×4 Lines(1 character=6×8dots)**



5、PAD Diagram And PAD Location

5.1、PAD Diagram



Chip Size: 2670×3695 (um×um)

PAD Size: 90×90(um×um)

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5.2、PAD Location

PAD No.	Pin Name	X	Y	PAD No.	Pin Name	X	Y
1	COM5	1242.6	-1615.05	**51**	SEG21	-1242.6	1604.95
2	COM6	1242.6	-1500.05	**52**	SEG20	-1242.6	1489.95
3	COM7	1242.6	-1385.05	**53**	SEG19	-1242.6	1374.95
4	COM8	1242.6	-1270.05	**54**	SEG18	-1242.6	1259.95
5	COM9	1242.6	-1155.05	**55**	SEG17	-1242.6	1144.95
6	COM10	1242.6	-1040.05	**56**	SEG16	-1242.6	1029.95
7	COM11	1242.6	-925.05	**57**	SEG15	-1242.6	914.95
8	COM12	1242.6	-810.05	**58**	SEG14	-1242.6	799.95
9	COM13	1242.6	-695.05	**59**	SEG13	-1242.6	684.95
10	COM14	1242.6	-580.05	**60**	SEG12	-1242.6	569.95
11	COM15	1242.6	-465.05	**61**	SEG11	-1242.6	454.95
12	SEG60	1242.6	-350.05	**62**	SEG10	-1242.6	339.95
13	SEG59	1242.6	-235.05	**63**	SEG9	-1242.6	224.95
14	SEG58	1242.6	-120.05	**64**	SEG8	-1242.6	109.95
15	SEG57	1242.6	-5.05	**65**	SEG7	-1242.6	-5.05
16	SEG56	1242.6	109.95	**66**	SEG6	-1242.6	-120.05
17	SEG55	1242.6	224.95	**67**	SEG5	-1242.6	-235.05
18	SEG54	1242.6	339.95	**68**	SEG4	-1242.6	-350.05
19	SEG53	1242.6	454.95	**69**	SEG3	-1242.6	-465.05
20	SEG52	1242.6	569.95	**70**	SEG2	-1242.6	-580.05
21	SEG51	1242.6	684.95	**71**	SEG1	-1242.6	-695.05
22	SEG50	1242.6	799.95	**72**	SEG0	-1242.6	-810.05
23	SEG49	1242.6	914.95	**73**	A0	-1242.6	-925.05
24	SEG48	1242.6	1029.95	**74**	OSC1	-1242.6	-1040.05
25	SEG47	1242.6	1144.95	**75**	OSC2	-1242.6	-1155.05
26	SEG46	1242.6	1259.95	**76**	E($\overline{\text{RD}}$)	-1242.6	-1270.05
27	SEG45	1242.6	1374.95	**77**	R/W($\overline{\text{WR}}$)	-1242.6	-1385.05
28	SEG44	1242.6	1489.95	**78**	VSS	-1242.6	-1500.05
29	SEG43	1242.6	1604.95	**79**	DB0	-1242.6	-1615.05
30	SEG42	1242.6	1719.95	**80**	DB1	-1242.6	-1730.05
31	SEG41	1084.8	1730.05	**81**	DB2	-1096.2	-1730.05
32	SEG40	969.8	1730.05	**82**	DB3	-981.2	-1730.05
33	SEG39	854.8	1730.05	**83**	DB4	-866.2	-1730.05
34	SEG38	737.6	1730.05	**84**	DB5	-751.2	-1730.05
35	SEG37	620.7	1730.05	**85**	DB6	-636.2	-1730.05
36	SEG36	505.7	1730.05	**86**	DB7	-521.2	-1730.05
37	SEG35	390.7	1730.05	**87**	VDD	-406.2	-1730.05
38	SEG34	275.7	1730.05	**88**	$\overline{\text{RES}}$	-291.2	-1730.05
39	SEG33	160.7	1730.05	**89**	FR	-176.2	-1730.05
40	SEG32	45.7	1730.05	**90**	V5	-61.2	-1730.05

41	SEG31	-69.3	1730.05	**91**	V3	53.8	-1730.05
42	SEG30	-184.3	1730.05	**92**	V2	168.8	-1730.05
43	SEG29	-299.3	1730.05	**93**	M/S	283.8	-1730.05
44	SEG28	-414.3	1730.05	**94**	V4	398.8	-1730.05
45	SEG27	-534.2	1730.05	**95**	V1	513.8	-1730.05
46	SEG26	-665	1730.05	**96**	COM0	628.8	-1730.05
47	SEG25	-787.7	1730.05	**97**	COM1	743.8	-1730.05
48	SEG24	-907.1	1730.05	**98**	COM2	858.8	-1730.05
49	SEG23	-1025.8	1730.05	**99**	COM3	973.8	-1730.05
50	SEG22	-1143.8	1730.05	**100**	COM4	1088.8	-1730.05

Unit:um

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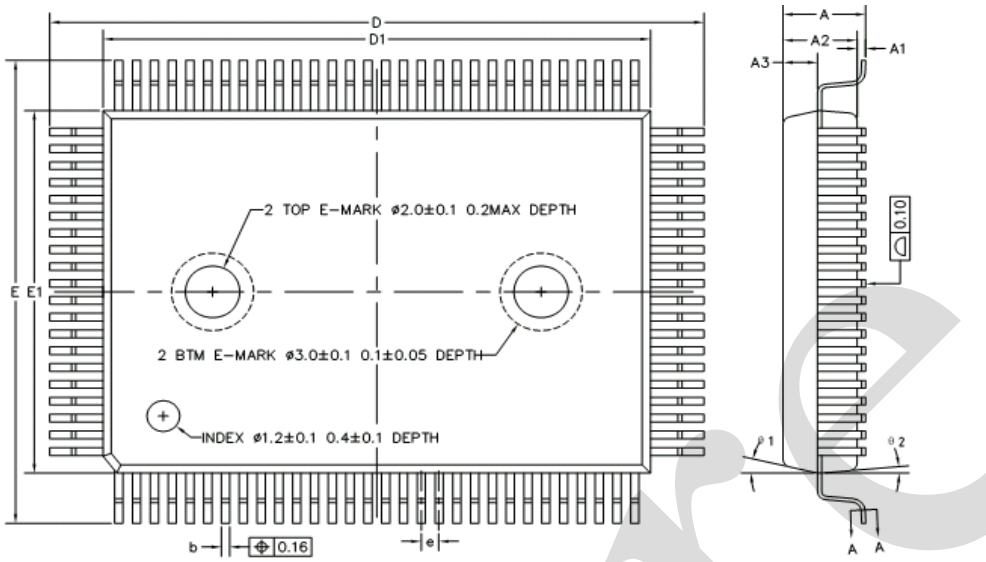
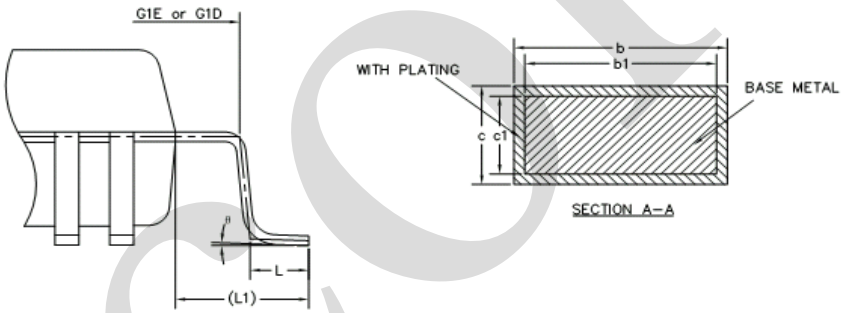
6、Package Information

6.1、QFP100-14×20-0.65





COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	3.30
A1	0.10	–	0.40
A2	2.65	2.75	2.85
A3	1.20	1.30	1.40
b	0.27	–	0.37
b1	0.27	0.30	0.33
c	0.14	–	0.20
c1	0.14	0.15	0.16
D	23.60	23.90	24.20
D1	19.90	20.00	20.10
E	17.60	17.90	18.20
E1	13.90	14.00	14.10
e	0.55	0.65	0.75
G1D	22.00REF		
G1E	16.00REF		
L	0.60	0.80	1.00
L1	1.95REF		
θ	0°	2°	8°
θ 1	11°	13°	15°
θ 2	3°	5°	7°

7、Statements And Notes

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

7.2、Notion

Recommended carefully reading this information before the use of this product；

The information in this document are subject to change without notice；

This information is using to the reference only, the company is not responsible for any loss；

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