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AX6120 / AX6121
(Dot Matrix LCD Drivers)

DATA SHEET

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AX6120 / AX6121
Dot Matrix LCD Drivers

Preliminary functional specification

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OVERVIEW FEATURES

The AX6120 family of dot matrix LCD drivers are designed for the display of characters and graphics. The drivers generate LCD drive signals derived from bit mapped data stored in an internal RAM.

The drivers are available in two configurations

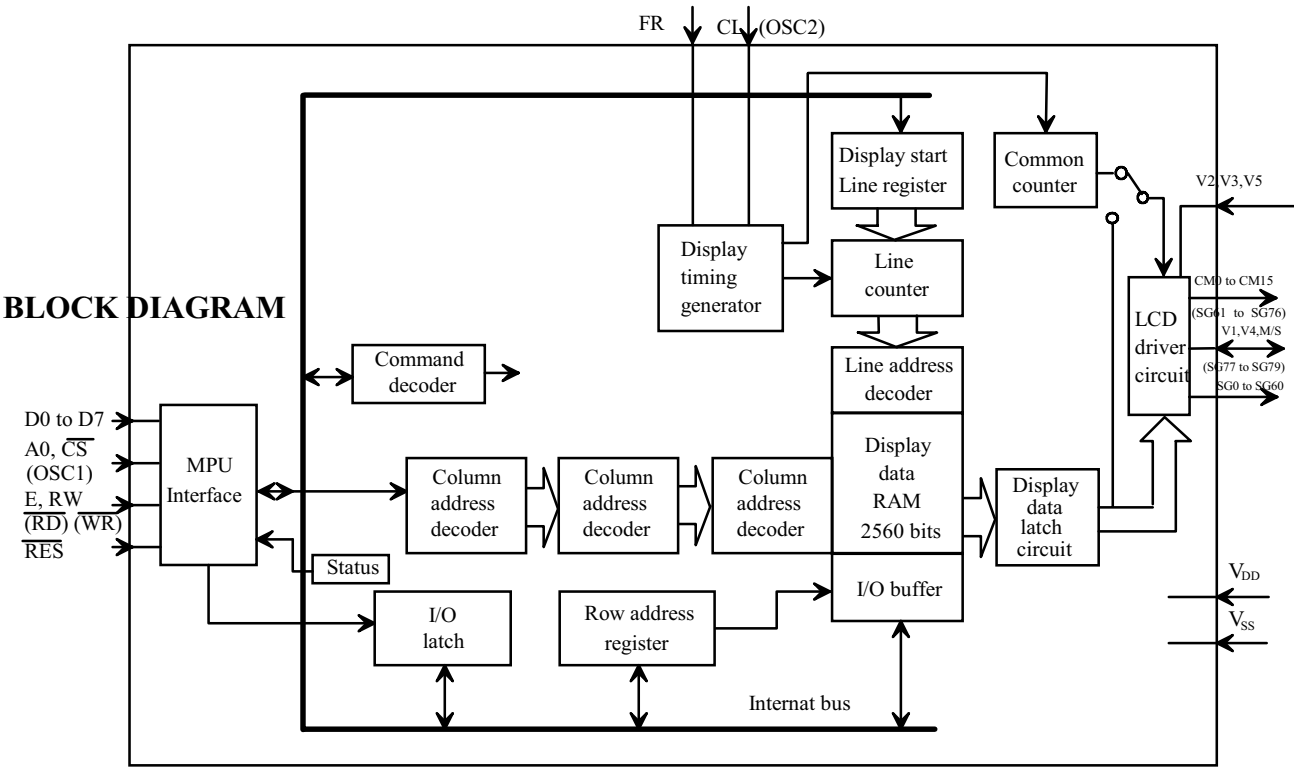
- The AX6120 which is able to drive two lines of twelve characters each.
- The AX6120 which is able to drive 80 segments

The AX6120 family drivers incorporate innovative circuit design strategies to achieve very low power dissipation at a wide range of operating voltages. These features give the designer a flexible means of implementing small to medium size LCD displays for compact, low power systems.

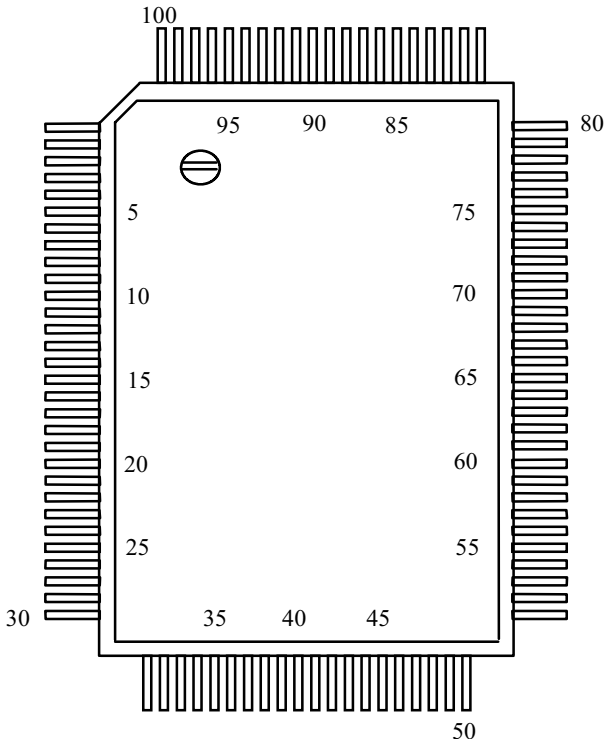
- Fast 8-bit MPU interface compatible with 80- and 68-family microcomputers
- Rich command set
- 80 (segment + common) drive sets
- Low power -- 30 μ W at 2kHz external clock
- Wide range of supply voltages
  V_{DD} - V_{SS} : -2.4 to -7.0V
  V_{DD} - V5 : -3.5 to -13.0
- Low-power CMOS
- Packages :
  100-pin QFP : AX6120F / AX6121F
  Al pad chip : AX6120D_{AA} / AX6121D_{AA}
  Au bump pad chip : AX6120D_{AB} / AX6121D_{AB}

Product Name	Clock Frequency		Applicable Driver	Number of SEG Drivers	Number of CMOS Drivers
	On-Chip	External			
AX6120F_{OA}	18kHz	18kHz	AX6120F_{OA}, AX6121F_{OA}	61	16
AX6121F_{OA}	--	18kHz		80	0
AX6120F_{AA}	--	2kHz	AX6120F_{AA}, AX6121F_{AA}	61	16
AX6121F_{AA}	--	2kHz		80	0

BLOCK DIAGRAM



PACKAGE OUTLINE



PIN OUT

AX6120FOA

Number	Name	Number	Name	Number	Name	Number	Name
1	COM5	26	SEG46	51	SEG21	76	E(RD)
2	COM6	27	SEG45	52	SEG20	77	R/W(WR)
3	COM7	28	SEG44	53	SEG19	78	Vss
4	COM8	29	SEG43	54	SEG18	79	DB0
5	COM9	30	SEG42	55	SEG17	80	DB1
6	COM10	31	SEG41	56	SEG16	81	DB2
7	COM11	32	SEG40	57	SEG15	82	DB3
8	COM12	33	SEG39	58	SEG14	83	DB4
9	COM13	34	SEG38	59	SEG13	84	DB5
10	COM14	35	SEG37	60	SEG12	85	DB6
11	COM15	36	SEG36	61	SEG11	86	DB7
12	SEG60	37	SEG35	62	SEG10	87	VDD
13	SEG59	38	SEG34	63	SEG9	88	RES
14	SEG58	39	SEG33	64	SEG8	89	FR
15	SEG57	40	SEG32	65	SEG7	90	V5
16	SEG56	41	SEG31	66	SEG6	91	V3
17	SEG55	42	SEG30	67	SEG5	92	V2
18	SEG54	43	SEG29	68	SEG4	93	M/S
19	SEG53	44	SEG28	69	SEG3	94	V4
20	SEG52	45	SEG27	70	SEG2	95	V1
21	SEG51	46	SEG26	71	SEG1	96	COM0
22	SEG50	47	SEG25	72	SEG0	97	COM1
23	SEG49	48	SEG24	73	A0	98	COM2
24	SEG48	49	SEG23	74	OSC1	99	COM3
25	SEG47	50	SEG22	75	OSC2	100	COM4

Family Variation

Product Name	Pin/Pad Number					
	74	**75**	**96 to 100, 1 to 11**	**93**	**94**	**95**
AX6120FOA	OSC1	OSC2	COM0 to COM15	M/S	V4	V1
AX6120FAA	CS	CL	COM0 to COM15	M/S	V4	V1
AX6121FOA	OSC1	OSC2	SEG76 to SEG61	SEG79	SEG78	SEG77
AX6121FAA	CS	CL	SEG76 to SEG61	SEG79	SEG78	SEG77
AX6120DOA	OSC1	OSC2	COM0 to COM15	M/S	V4	V1
AX6121DAA	CS	CL	SEG76 to SEG61	SEG79	SEG78	SEG77

PIN DESCRIPTION

System Bus Interface

D0 - D7 :

8-bits, tri-state, bi-directional I/O bus

A0 :

Data/command select input

- A0=0 : Display control data on D0 - D7
- A0=1 : Display data D0 - D7

RES :

Reset and interface configuration input. The driver is reset on any edge of RES.

- Display off
- Display start line register : line 1
- Static drive off
- Column address counter : 0

Page address register : 3

- Duty : 1/32
- ADC : Forward (ADC : D0= "0")
- Read-modify-write off

In addition if the interface is configured by the level of RES as given in the table below.

RES	Interface	A0	E	R/W	CS	D0 to D7
High	68MPU	↑	↑	↑	↑	↑
Low	80 MPU	↑	RD	WR	↑	↑

$\overline{CS}$:

(See note 1)

Active low chip select input

E or $\overline{RD}$:

- RES= 1 :E , Enable clock input
  For AX6120OA RES must be high.
- RES= 0 :$\overline{RD}$, Active low read input. Taking the $\overline{RD}$ inputs of an AX6120FOA low causes the driver to drive the MPU bus. Taking both $\overline{CS}$ and $\overline{RD}$ inputs of an AX6120FAA/AX6121FOA/ AX6121FAA low causes the driver to drive the MPU bus.

R/$\overline{W}$ or $\overline{WR}$:

- RES= 1 :R/$\overline{W}$ input
- RES= 0 :$\overline{WR}$ Active low write strobe.

Data is latched into the driver on the driver on the falling edge of $\overline{WR}$.

LCD Interface

M/$\overline{S}$:

(See note 2)

Master/stave driver select input.

- M/$\overline{S}$= 1 : Master
- M/$\overline{S}$= 0 : Slave

The operation of some signals are different in master and slave mode as given in the table below.

M/S	FR	COM output	OSC1	OSC2
VDD	Output	COM0 to COM15	Input	Output
Vss	Input	COM31 to COM16	NC	Input

Note : The order in which the common signals are scanned for a master is the reverse of that for a slave.

FR :

LCD AC drive signal input/output. This pin is configured by M/S as given in the table below.

M/S	6120xx	6121xx
1	Output	Input
0	Input	Input

SEG0 to SEG60 :

LCD segment (column) drive outputs. The levels of these pins are given in the table below.

FR	Data	
	1	0
1	VDD	V2
0	V5	V3

SEG61 to SEG79 :

(See note 3)

See SEG0 to SEG60

COM0 to COM15 :

(See note 2)

LCD common (row) drive outputs. The output level of these pins depend on FR and the output into of the common counter and are given in the table below.

FR	Common	
	1	**0**
1	V5	V1
0	VDD	V4

When M/S=0 COM0 to COM15 become COM31 to COM16.

Oscillator

CL :
(See note 1)
Clock input
OSC 1 :
(See note 4)

- M/S= 1 : Connect the internal oscillator feedback resistor, Rf, to this pin.
- M/S= 0 : Leave open.

OSC 2 :
(See note 4)

- M/S= 1 : Connect the internal oscillator feedback resistor, Rf, to this pin.
- M/S= 0 : Clock input.

Power Supply

VDD
0 V ground
VSS :
-5V input
V1 to V5 :
LCD drive power supply. These voltages must conform to the following relation.
VDD≧V1≧V2≧V3≧V4≧V5

Notes : 1. AX6120F$_{AA}$, AX6121F$_{OA}$ and AX6121F series only.
2. AX6120F series only.
3. AX6121F series only.
4. AX6120F$_{OA}$ only.

BLOCK DESCRIPTION

System Bus

Data transfer

The AX6120 and AX6121 drivers use the A0.E (or RD) and R/W (or WR) signals to transfer data between the system MPU and internal registers. The combinations used are given in the table blow. In order to match the timing requirements of the MPU with those of the display data RAM and control registers all data is latched into and out of the driver. This introduces a one cycle delay between a read request for data and the arriving. For example when the MPU executes a read cycle to access display RAM the current contents of the latch are placed on the system data bus while the desired contents of the display RAM are moved into the latch.

This means that a dummy read cycle has to be executed at the start of every series of reads. See Figure 1. No dummy cycle is required at the start of a series of writes as data is transferred automatically from the input latch to its destination.

Common	68MPU	80MPU		Function
A0	R/W	RD	WR	
1	1	0	1	Read display data
1	0	1	0	Write display data
0	1	0	1	Read status
0	0	1	0	Write to internal register (command)

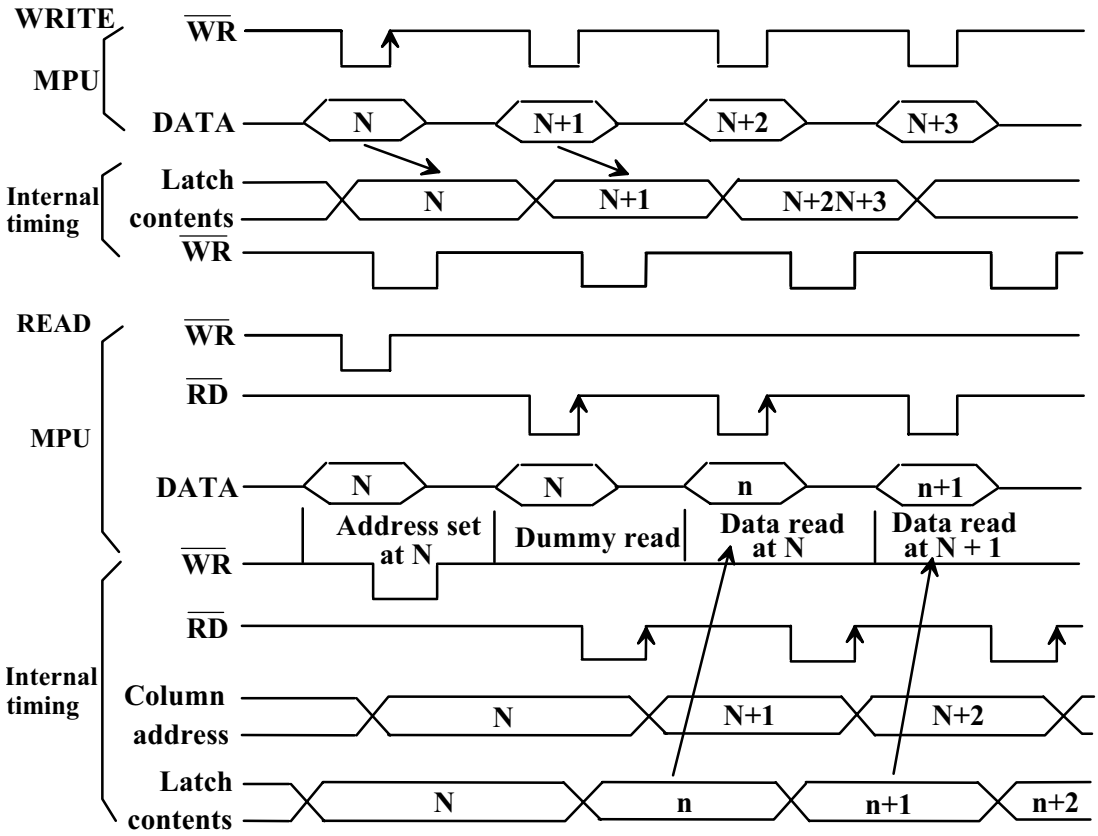


Figure 1 Bus Buffer Delay

Display Start Line and Line Count Registers

The contents of this regiter form a pointer to a line of data in display data RAM corresponding to the first line of the display (COM0), and are set by the Display Start Line command. See section 3.
The contents of the display start line register are copied into the line count register at the start of every frame, that is on each edge of FR. The line count register is incremented by the CL clock once for every display line, thus generating a pointer to the current line of data, in display data RAM, beging transferred to the segment driver circuits.

Column Address Counter

The column address counter is a 7-bit presettable counter that supplies the column address for MPU access to the display data RAM. See Figure 2. The counter is incremented by one every time the driver receives a Read or Write Display Data command. Addresses above 50H are invalid, and the counter will not increment past this value. The contents of the column address counter are set with the Set Column Address command.

Page Resiter

The page resiter is a 2-bit register that supplies the page address for MPU access to the display data RAM. See Figure 2. The contents of the page register are set by the Set Page Register command.

Display Data RAM

The display data RAM stores the LCD display data, on a 1-bit per pixel basis. The relation-ship between display data, display address and the display is shown in Figure 2.

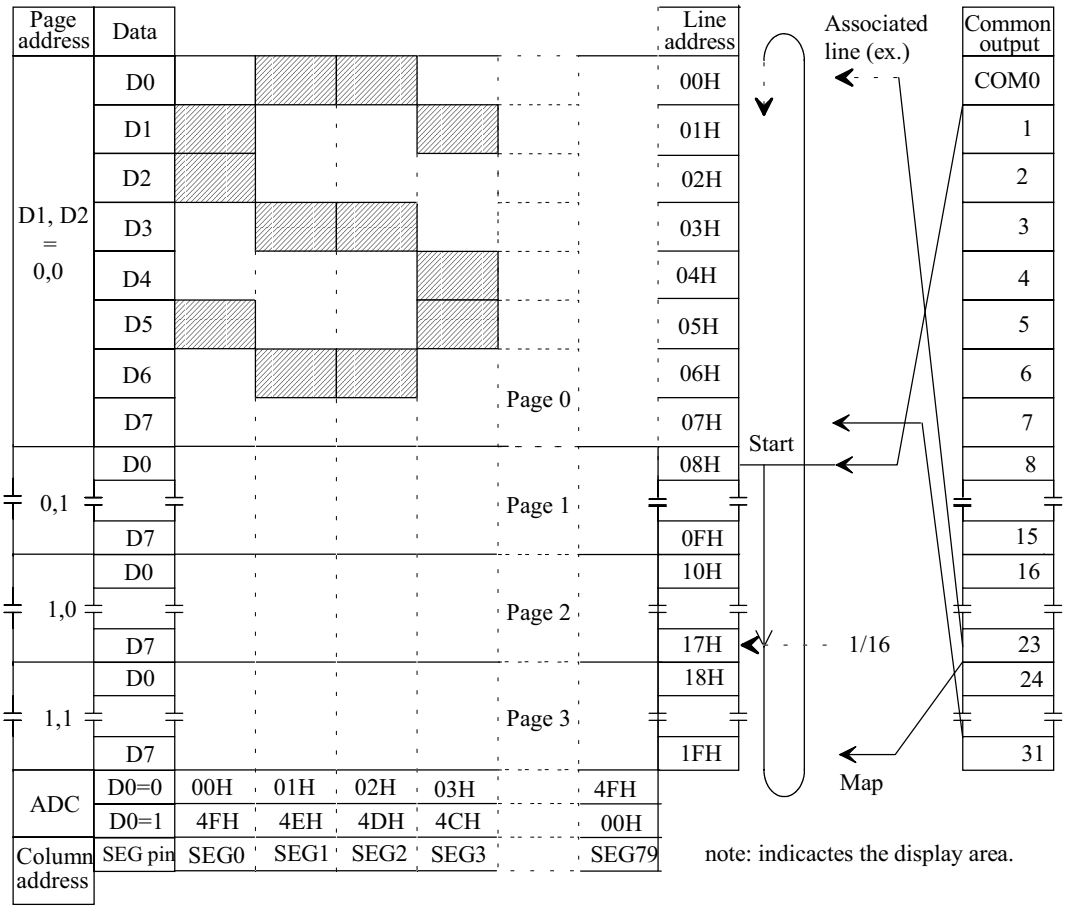


Figure 2 Display Data RAM Addressing

Common Timing Generator
This circuit generates common timing and frame, FR, signals from the basic clock, CL.

Display Data Latch Circuit
This latch stores one line of display data for use by the LCD driver interface circuitry. The output of this latch is controlled by the Display ON/OFF and Static Drive ON/OFF commands

LCD Driver Circuit
The LCD driver circuitry generates the 80 4-level signals used to drive the LCD panel, using output from the display data latch and the common timing generator circuitry.

Display Timing Generator
This circuit generates the internal display timing signal using the basic clock, CL, and the frame signals, FR. FR is used to generate the dual frame AC-drive wave-form (type B drive) and to lock the line counter and common timing generator to the system frame rate.
CL is used to lock the line counter to the system line scan rate. If a system uses both AX6120s and AX6121s they must have the same CL frequency rating.

Oscillator Circuit (AX6120F$_{OA}$ Only)
The oscillator is a low power CR oscillator whose frequency of oscillation is determined by the value of the feedback resistor Rf. For details see section 6.1.

Reset Circuit
This circuit senses both the edge and the level of the signal at the RES pin and uses this information to

- reset the driver.
- configure the system bus interface.

For details see section 1.

COMMANDS

Summary

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
Display On/Off	0	1	0	1	0	1	0	1	1	1	0/1	Turns display on or off. 1 : ON, 0 : OFF
Display start line	0	1	0	1	1	0	Display start address (0 to 31)					Specifies RAM line corresponding to top line of display.
Set page address	0	1	0	1	0	1	1	1	0	Page (0 to 3)		Sets display RAM page in page address register.
Set column (segment) address	0	1	0	0	Column address (0 to 79)							Sets display RAM column address in column address registser.
Read status	0	0	1	Busy	ADC	ON/OFF	Reset	0	0	0	0	Reads the following status : BUSY 1 : Busy 0 : Ready ADC 1 : CW output 0 : CCW output ON/OFF 1 : Display off 0 : Display on RESET 1 : Being reset 0 : Normal
Write display data	1	1	0	Write data								Writes data from data bus into display RAM.
Read display data	1	0	1	Read data								Reads data from display RAM onto data bus.
Select ADC	0	1	0	1	0	1	0	0	0	0	0/1	0 : CW output, 1 : CCW output
Statis drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Selects static driving operation. 1 : Static drive, 0 : Normal driving
Select duty	0	1	0	1	0	1	0	1	0	0	0/1	Selects LCD duty cycle 1 : 1/32, 0 : 1/16
Read-Modify -Write	0	1	0	1	1	1	0	0	0	0	0	Read-modify-write ON
End	0	1	0	1	1	1	0	1	1	1	0	Read-modify-write OFF
Reset	0	1	0	1	1	1	0	0	0	1	0	Software reset

Command Description
Display ON/OFF

A0	RD	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	1	1	1	D	AEH, AFH

This command turns the display on and off.
- D= 1 : Display ON
- D= 0 : Display OFF

Display Start Line

A0	RD	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	A4	A3	A2	A1	A0	C0H to DFH

This command loads the display start line register.

A4	A3	A2	A1	A0	Line Address
0	0	0	0	0	0
0	0	0	0	1	1
		:			:
		:			:
1	1	1	1	1	31

See Figure 2.

Set Page Address

A0	RD	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	1	1	0	A1	A0	B8H to BBH

This command loads the page address register.

A1	A0	Page
0	0	0
0	1	1
1	0	2
1	1	3

See Figure 2.

A0	RD	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	A6	A5	A4	A3	A2	A1	A0	00H to 4FH

Set Column Address

This command loads the column address register.

A6	A5	A4	A3	A1	A0	Column Address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
			:			:
			:			:
1	0	0	1	1	1	79

Read Status

A0	RD	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Reading the command I/O register (A0=0) yields system status information.
- The busy bit indicates whether the driver will accept a command or not.

Busy=1 : The driver is currently executing a command or is resetting. No new command will be accepted.
Busy=0 : The driver will accept a new command.
- The ADC bit indicates the way column addresses are assigned to segment drivers.

ADC=1 : Normal. Column address n → segment driver n.
ADC=0 : Inverted. Column address 79-u → segment driver u.
- The ON/OFF bit indicates the current status of the display.

ON/OFF=1 : Display OFF
ON/OFF=0 : Display ON
- The RESET bit indicates whether the driver is executing a hardware or software reset or if it is in normal operating mode.

RESET=1 : Currently executing reset command.
RESET=0 : Normal operation

Write Display Data

A0	RD	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

Writes 8-bits of data into the display data RAM, at a location specified by the contents of the column address and page address registers and then increments the column address register by one.

Read Display Data

A0	RD	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

Reads 8-bits of data from the data I/O latch, updates the contents of the I/O latch with display data from the display data RAM location specified by the contents of the column address and page address registers and then increments the column address register.
After loding a new address into the column address register one dummy read is required before valid data is obtained.

Select ADC

A0	RD	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	0	0	0	D	A0H, A1H

This command selects the relationship between display data RAM column addresses and segment drivers.
D=1 : SEG0 ← column address 4FH, ... (inverted)
D=0 : SEG0 ← column address 00h, ... (normal)
This command is provided to reduce restrictions on the placement of driver ICs and routing of traces during printed circuit board design. See Figure 2 for a table of segments and column addresses for the two values of D.

Static Drive ON/OFF

A0	RD	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	0	1	0	D	A4H, A5H

Forces display on and all common outputs to be selected.
D=1 : Static drive on
D=0 : Static drive off

Select Duty

A0	RD	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	1	0	0	D	A8H, A9H

This command sets the duty cycle of the LCD drive and is only valid for the AX6120F. The duty cycle of the AX6121F is determined by the externally generated FR signal.
D=1 : 1/32 duty cycle
D=0 : 1/16 duty cycle

Read-Modify-Write

A0	RD	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	0	0	0	D	E0H

This command defeats column address register auto-increment after data reads. The current conetents of the column address register are saved. This mode remains active until an End command is received.

End

A0	RD	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	1	1	1	0	EEH

This command cancels read-modify-write mode and restores the contents of the column address register to their value prior to the receipt of the Read-Modify-Write command.

Reset

A0	RD	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	0	0	1	0	E2H

This command clears
- the display start line register.
- column address counter.
- and set page address register to 3 page.

  It does not affect the contents of the display data RAM.

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage (1)	Vss	-8.0 to +0.3	V
Supply voltage (2)	V5	-16.5 to +0.3	V
Supply voltage (3)	V1, V4, V2, V3	V5 to +0.3	V
Input voltage	VIN	Vss -0.3 to +0.3	V
Output voltage	VO	Vss -0.3 to +0.3	V
Power dissipation	PD	250	mW
Operating temperature	Topr	-30 to +85	deg. C
Storage temperature	Tstg	-65 to +150	deg. C
Soldering temperature time at lead	Tsol	260, 10	deg. C, s

Notes : 1. All voltages are specified relative to VDD= 0 V.
2. The following relation must be always hold
VDD≧V2≧V3≧V4≧V5
3. Exceeding the absolute maximum ratings may cause permanent damage to the device. Functional operation under these conditions is not implied.
4. Moisture resistance of flat packages can be reduced by the soldering process, so care should be taken to avoid thermally stressing the package during board assembly.

Electrical Specifications

DC Characteristics

Ta= -20 to 75 deg. C, V_{DD}= 0 V unless stated otherwise

Parameter		Symbol	Condition	Rating			unit	Applicable Pin
				min	typ	max		
Operating voltage (1) See note 1.	Recommended	Vss		-5.5	-5	-4.5	V	VSS
	Allowable			-7	--	-3		
Operating voltage (2)	Recommended	V5		-12	--	-3.5	V	V5 See note 10.
	Allowable				--	--		
	Allowable	V1, V2		0.6xV5	--	VDD	V	V1, V2
	Allowable	V3, V4		V5	--	0.4xV5	V	V3, V4
High-level input voltage		VIHT		Vss+2.0	--	VDD	V	See note 2 & 3.
		VIHC		0.2xVss	--	VDD		
Low-level input voltage		VILT		Vss	--	VSS+0.8	V	See note 2 & 3.
		VILC		Vss	--	0.8xVss		

(continued)

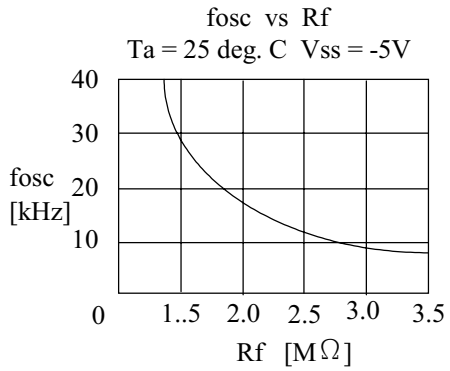
DC Characteristics (Cont'd)

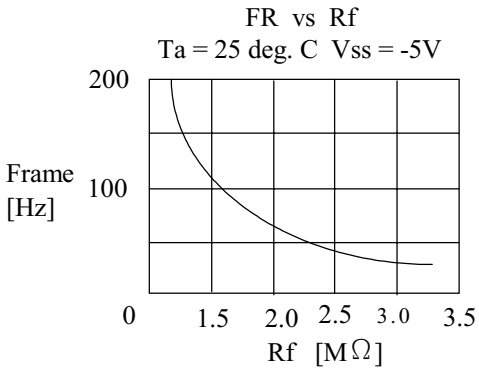
Ta= -20 to 75 deg. C, VDD= 0 V unless stated otherwise

Parameter	Symbol	Condition		Rating			Unit	Applicable Pin
				min	typ	max		
High-level output voltage	VOHT	IOH=-3.0 mA		Vss+2.4	--	--	V	OSC2 See note 4 & 5.
	VOHC1	IOH=-2.0mA		Vss+2.4	--	--		
	VOHC2	IOH=-120 μ		0.2xVss	--	--		
Low-level output voltage	VOLT	IOL=3.0mA		--	--	Vss+0.4	V	OSC2 See note 4 & 5.
	VOLC1	IOL=2.0mA		--	--	Vss+0.4		
	VOLC2	IOL=120 μ A		--	--	0.8xVss		
Input leakage current	ILI			-1	--	1	μ A	See note 6.
Output leakage current	ILO			-3	--	3	μ A	See note 7.
LCD driver ON resistance	Ron	Ta=25 deg. C	V5= -5.0V	--	5	7.5	kΩ	SEG0 to 79, COM0 to 15, See note 11
			V5= -3.5V	--	10	50		
Static current dissipation	IDD0	CS = CL = VDD		--	0.05	1	μ A	VDD
Dynamic current dissipation	IDD (1)	During display V5= -5.0V	fCL=2kHz	--	2	5	μ A	VDD See note 12, 13 & 14.
			Rf= 2 MΩ	--	9.5	15		
			fCL= 18kHz	--	5	10		
	IDD (2)	During access tcyc=200kHz		--	300	500	μ A	See note 8.
Input pin capacitance	CIN	Ta= 25 deg. C, f= 1MHz		--	5	8	pF	All input pins
Oscillation frequency	fOSC	Rf= 2.0 MΩ± 2% Vss= -5.0V		15	18	21	kHz	See note 9.
		Rf= 2.0 MΩ± 2% Vss= -3.0V		11	18	21		
Reset time	tR			1	--	1,000	μ S	RES

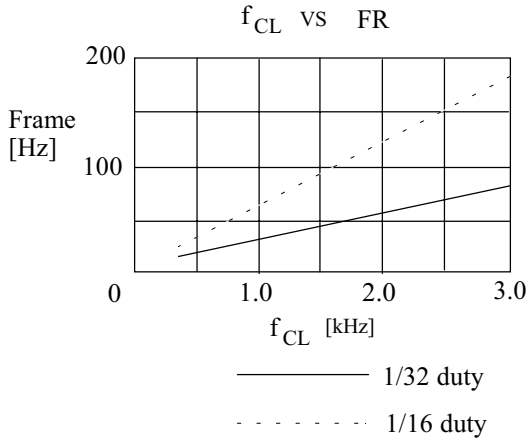
Note : 1. Operation over the specified voltage range is guaranteed, except where the supply voltage changes suddenly during CPU access.
2. A0, D0 to D7, E (or RD), R/W (or WR) and CS.
3. CL, FR, M/S and RES.
4. D0 to D7.
5. FR
6. A0, E (or RD), R/W (or WR), CS, CL, M/S and RES.
7. When D0 to D7 and FR are high impedance.
8. During continual write accss at a frequency of teye. Current consumption during access is effectively proportional to the access frequency.
9. See figure below for details
10. See figure below for detais
11. For a voltage differential of 0.1 V between input (V1, ... V4) and output (COM, SEG) pins. All voltages within specifed operating voltage range.
12. AX6120FAA and AX6121FAA only. Does not include transient currents due to stray and panel capacitances.
13. AX6120FOA only. Does not include transient currents due to stray and panel capacitances.
14. AX6121FOA only. Does not includle transient currents due to stray and panel capacitances.

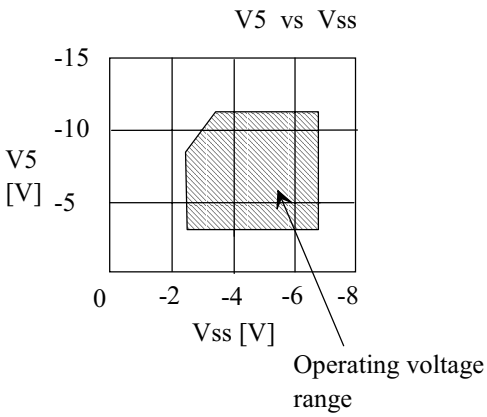
Relationship between fossc, fFR and Rf, and operating bounds on Vss and V5





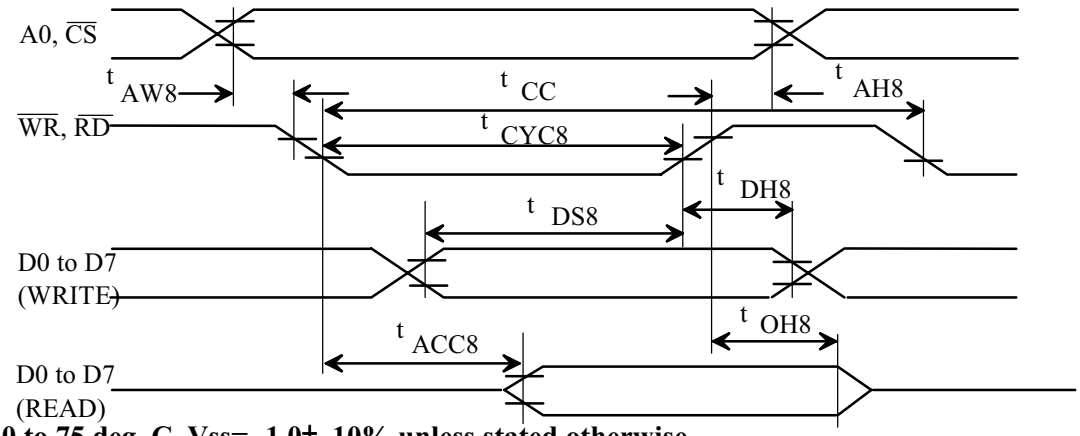
Duty 1/16, 1/32





AC Characteristics

- MPU Bus Read/Write i (80-family MPU)



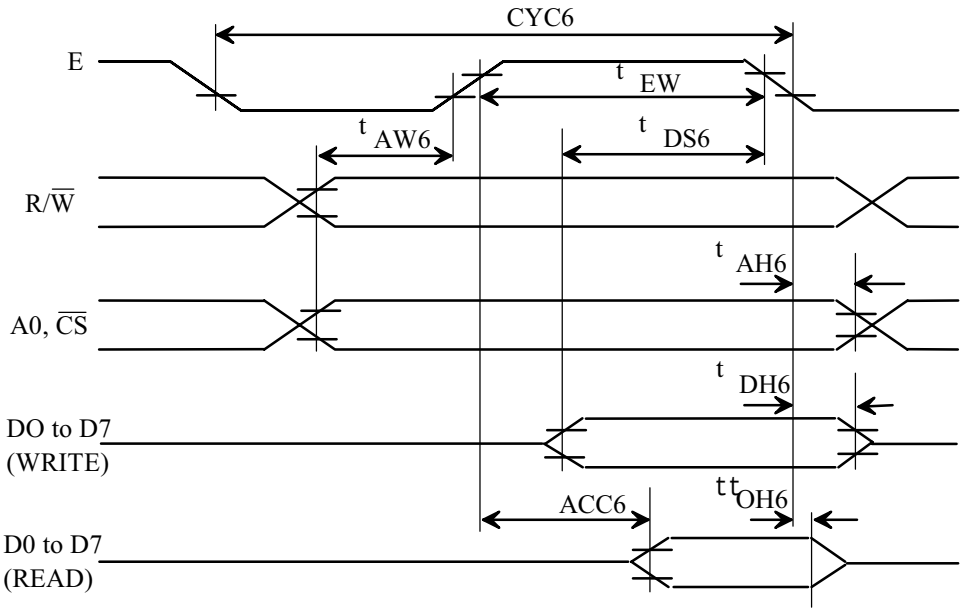
Ta= -20 to 75 deg. C, Vss= -1.0± 10% unless stated otherwise

Parameter	Symbol	Condition	Rating		Unit	Signal
			min	max		
Address hold time	tAH8		10	--	ns	A0, CS
Address setup time	tAW8		20	--	ns	
System cycle time	tCYC8		1,000	--	ns	WR, RD
Control pulsewidth	tcc		200	--	ns	
Data setup time	tDS8		80	--	ns	DO to D7
Data hold time	tDH8		10	--	ns	
RD access time	tACC8	CL= 100pF	--	90	ns	
Output disable time	tCH8		10	60	ns	

Notes : 1. Increase parameter values by 200% when Vss= -3.0V.

2. All inputs must have a rise and fall time of less than 15 ns.

- **MPU Bus Read/Write II (68-family MPU)**

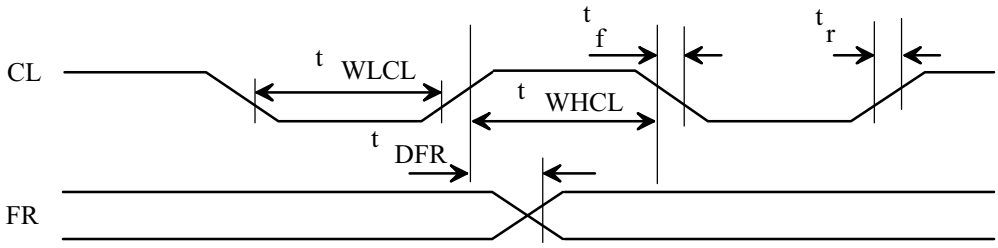


Ta= -20 to 75 deg. C. Vss= -5V ± 10 unless stated otherwise

Parameter		Symbol	Condition	Rating		Unit	Signal
				min	max		
System cycle time		tCYC6		1,000	--	ns	A0, $\overline{CS}$, R/$\overline{W}$
Address setup time		tAW6		20	--	ns	
Address hold time		tAH6		10	--	ns	
Data setup time		tDS6		80	--	ns	D0 to D7
Data hold time		tDH6		10	--	ns	
Output disable time		tOH6	CL= 100pF	10	60	ns	
Access time		tACC6		--	90	ns	
Enable pulsewidth	Read	tEW		100	--	ns	E
	Write			8	--	ns	

Notes : 1. tCYC6 is the cycle time of $\overline{CS}$. E=H. not the cycle time of E.
2. Increase parameter values by 200% when Vss= -3.0V.
3. all inputs must have a rise and fall time of less than 15 ns.

• Display Control Signal Timing



Input

Ta= -20 to 75 deg. C, Vss= -5.0V ± 10% unless stated otherwise

Parameter	Symbol	Condition	Rating			Unit	Signal
			min	typ	max		
Low-level pulse width	tWLCL		35	--	--	μs	CL
High-level pulse width	tWHCL		35	--	--	μs	
Rise time	tr		--	30	150	μs	
Fall time	tf		--	30	150	μs	
FR delay time	tDFR		-2	0.2	2	μs	FR

Note : The listed input tDFR applies to the AX6120 and AX6121 in slave mode.

Output

Ta= -20 to 75 deg, C, Vss= -5.0V ± 10% unless stated otherwise

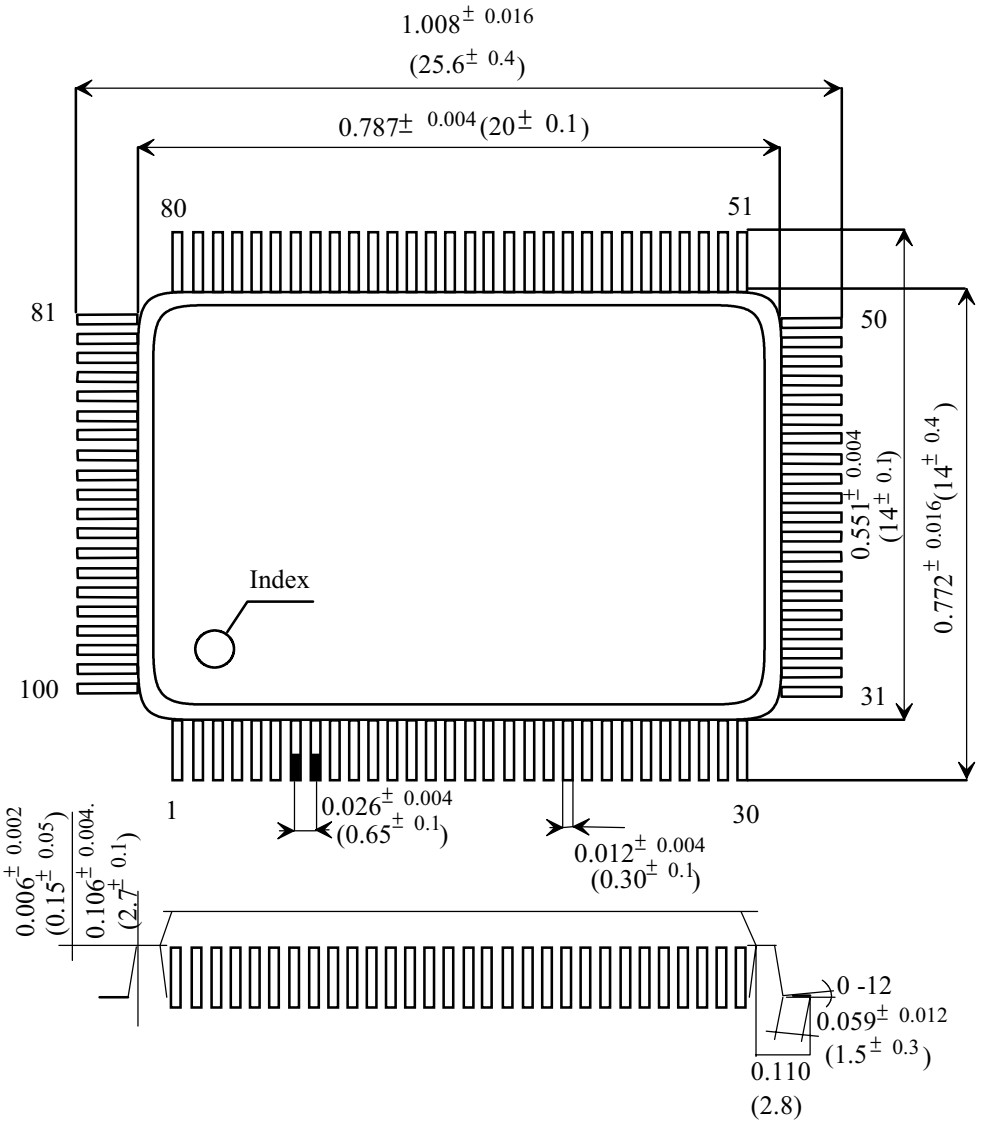
Parameter	Symbol	Condition	Rating			Unit	Signal
			min	typ	max		
FR delay time	tDFR	CL= 100pF	--	0.2	0.4	μs	FR

Notes : 1. The listed output tDFR applies to the AX6120 in master mode.
2. Increase parameter values by 200% when Vss= -3.0V.

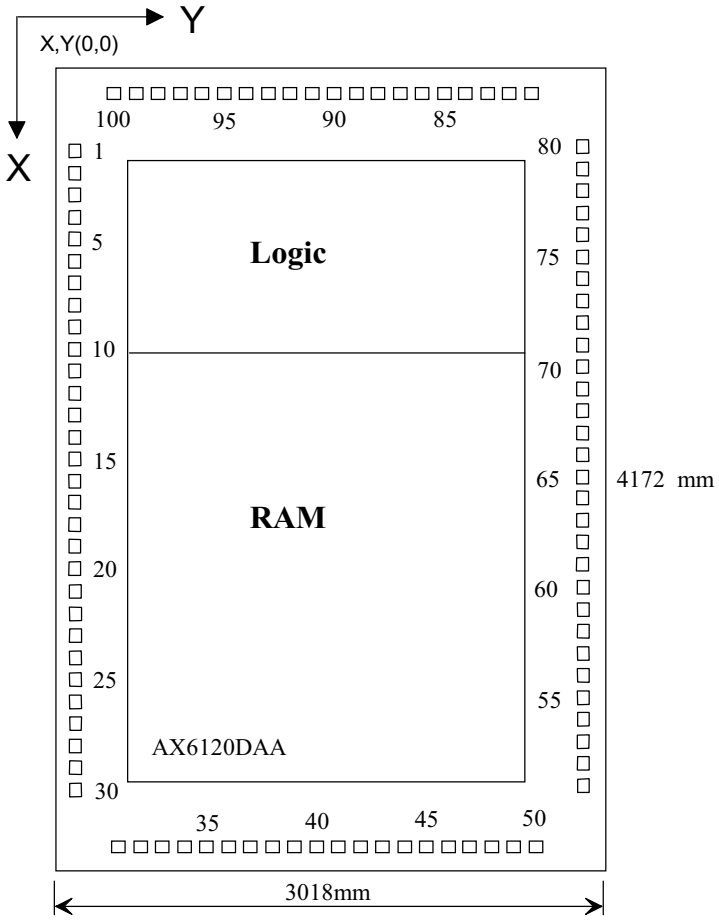
Package Dimensions

- AX6120F / AX6121F

Dimensions : inches (mm)



- AX6120D / AX6121D



Chip Size : 4.172 * 3.018 mm

-- AX6120DAB pad coordinates

Pad		x	y	Pad		x	y	Pad		x	y
Number	Name			Number	Name			Number	Name		
1	COM5	215	55	35	SEG37	4,077	826	69	SEG3	1,532	2,923
2	COM6	348	55	36	SEG36	4,077	961	70	SEG2	1,400	2,923
3	COM7	481	55	37	SEG35	4,077	1,096	71	SEG1	1,268	2,923
4	COM8	614	55	38	SEG34	4,077	1,231	72	SEG0	1,136	2,923
5	COM9	747	55	39	SEG33	4,077	1,366	73	A0	1,004	2,923
6	COM10	880	55	40	SEG32	4,077	1,501	74	CS	872	2,923
7	COM11	1,013	55	41	SEG31	4,077	1,636	75	CL	740	2,923
8	COM12	1,146	55	42	SEG30	4,077	1,771	76	E(RD)	608	2,923
9	COM13	1,279	55	43	SEG29	4,077	1,906	77	R/W(WR)	476	2,923
10	COM14	1,412	55	44	SEG28	4,077	2,041	78	VSS	344	2,923
11	COM15	1,545	55	45	SEG27	4,077	2,176	79	DB0	212	2,923
12	SEG60	1,678	55	46	SEG26	4,077	2,311	80	DB1	80	2,923
13	SEG59	1,811	55	47	SEG25	4,077	2,446	81	DB2	55	2,744
14	SEG58	1,944	55	48	SEG24	4,077	2,581	82	DB3	55	2,612
15	SEG57	2,077	55	49	SEG23	4,077	2,716	83	DB4	55	2,477
16	SEG56	2,210	55	50	SEG22	4,077	2,851	84	DB5	55	2,340
17	SEG55	2,343	55	51	SEG21	3,908	2,923	85	DB6	55	2,203
18	SEG54	2,476	55	52	SEG20	3,776	2,923	86	DB7	55	2,065
19	SEG53	2,609	55	53	SEG19	3,644	2,923	87	VDD	55	1,926
20	SEG52	2,742	55	54	SEG18	3,512	2,923	88	RES	55	1,780
21	SEG51	2,875	55	55	SEG17	3,380	2,923	89	FR	55	1,636
22	SEG50	3,008	55	56	SEG16	3,248	2,923	90	V5	55	1,491
23	SEG49	3,141	55	57	SEG15	3,116	2,923	91	V3	55	1,349
24	SEG48	3,274	55	58	SEG14	2,984	2,923	92	V2	55	1,210
25	SEG47	3,407	55	59	SEG13	2,852	2,923	93	M/S	55	1,071
26	SEG46	3,540	55	60	SEG12	2,720	2,923	94	V4	55	941
27	SEG45	3,673	55	61	SEG11	2,588	2,923	95	V1	55	769
28	SEG44	3,806	55	62	SEG10	2,456	2,923	96	COM0	55	639
29	SEG43	3,939	55	63	SEG9	2,324	2,923	97	COM1	55	509
30	SEG42	4,072	55	64	SEG8	2,192	2,923	98	COM2	55	379
31	SEG41	4,077	286	65	SEG7	2,060	2,923	99	COM3	55	249
32	SEG40	4,077	421	66	SEG6	1,928	2,923	100	COM4	55	59
33	SEG39	4,077	556	67	SEG5	1,796	2,923				
34	SEG38	4,077	691	68	SEG4	1,664	2,923				

Driver RAM Access Rates
When using the MPU data bus to access the display data RAM, access timing is determined by the driver cycle time, tcyc, not by the RAM access time. In general this strategy leads to faster data transfers between the driver and the MPU.
If the MPU access frequency is likely to exceed 1/tcyc then the designer has the choice of inserting NOPs into the access loop or polling the driver, by reading the busy flag, to see if it will accept new data or instructions.

Selecting Duty Cycle
The select duty cycle command selects a duty cycle of either 1/16 or 1/32. The 1/32 duty cycle is used for a two driver, master-slave, system
The common outputs for the two drivers are selected as shown in figure 3.

Stand-By Mode
If static drive is selected and the display turned off the current consumption of the system can be reduced to almost static (quiescent) levels. When the driver is in this state.
1. the segment and common driver outputs are to VDD.
2. the oscillator is halted and OSC2 goes tri-state or the external clock input, CL, goes tri-state.
3. display data and operating set-up are saved.
Stand-by mode is canceled by deselecting static drive or turning the display on.
Note that if the LCD drive voltages are derived from a resistive divider network, minimum power consumption will only be achieved if the current flowing in the network is cutoff in stand-by mode.

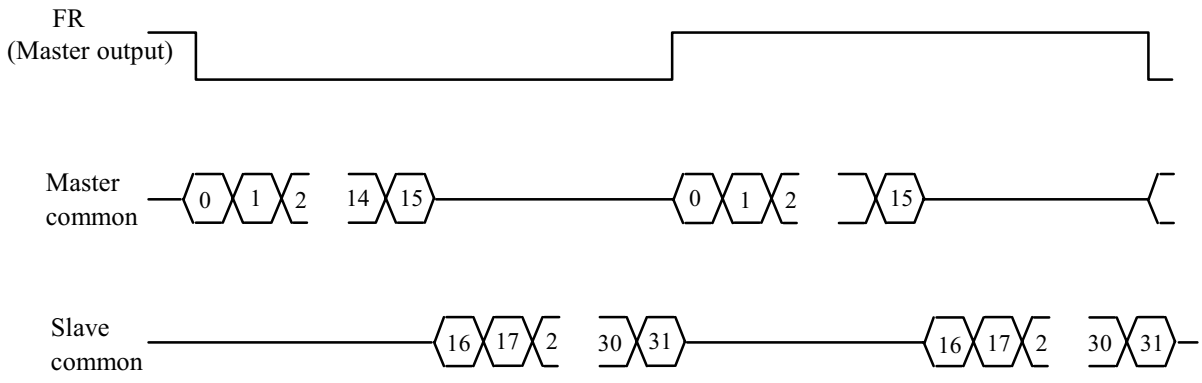
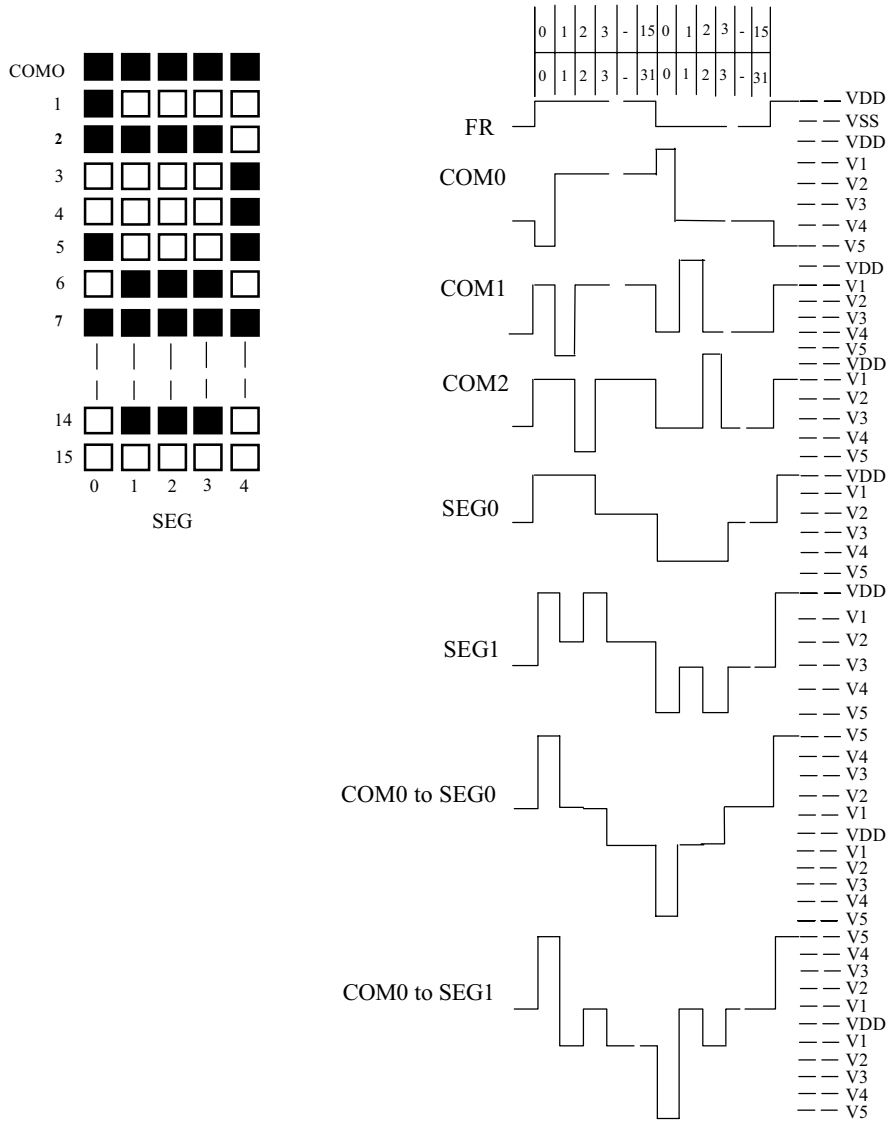


Figure 3 Common Outputs at 1/32 Duty Cycle

Example Drive Waveforms



APPLICATION NOTES

The Oscillator : AX6120FOA Only

The external feedback resistor, Rf, is connected as shown in Figure 4.

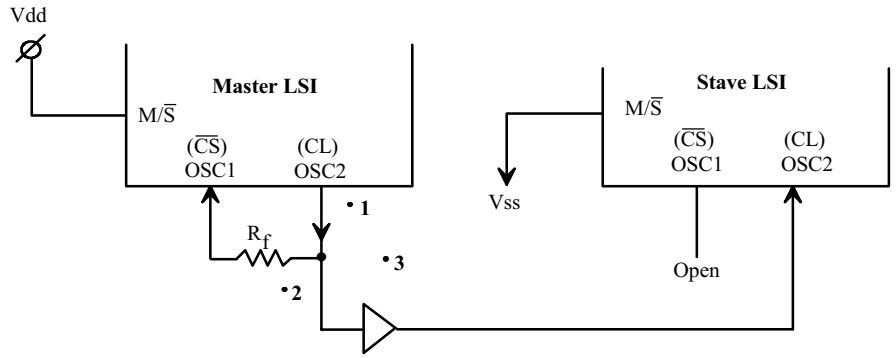


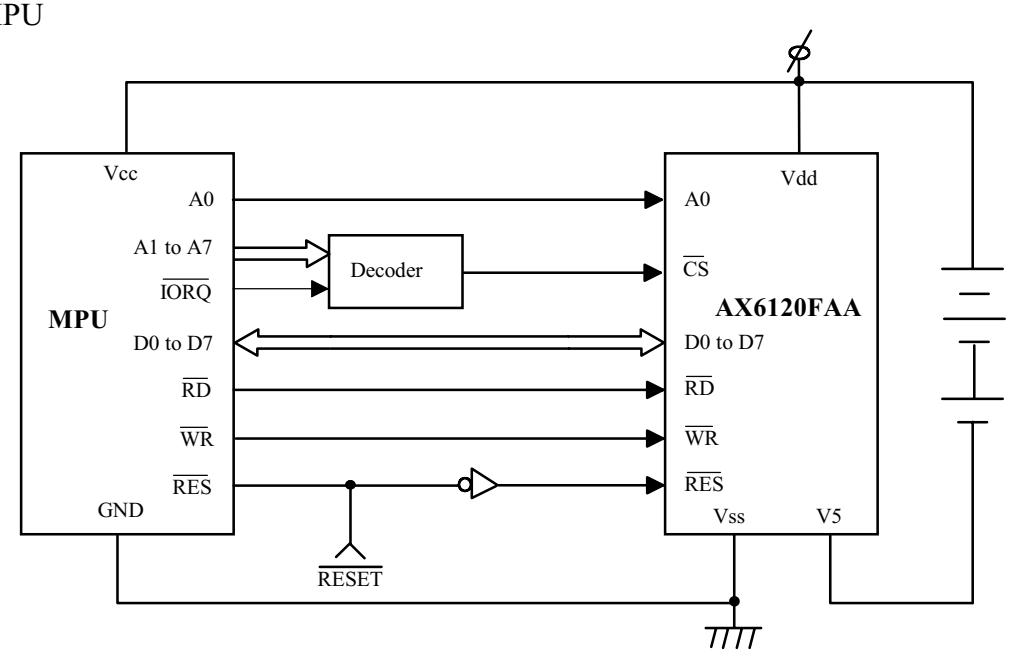
Figure 4 External Rf Connection

Notes : 1. If a slave AX6120FOA is driven with an external clock, the input clock to the slave must be in phase with the signal at the masters OSC2 output.

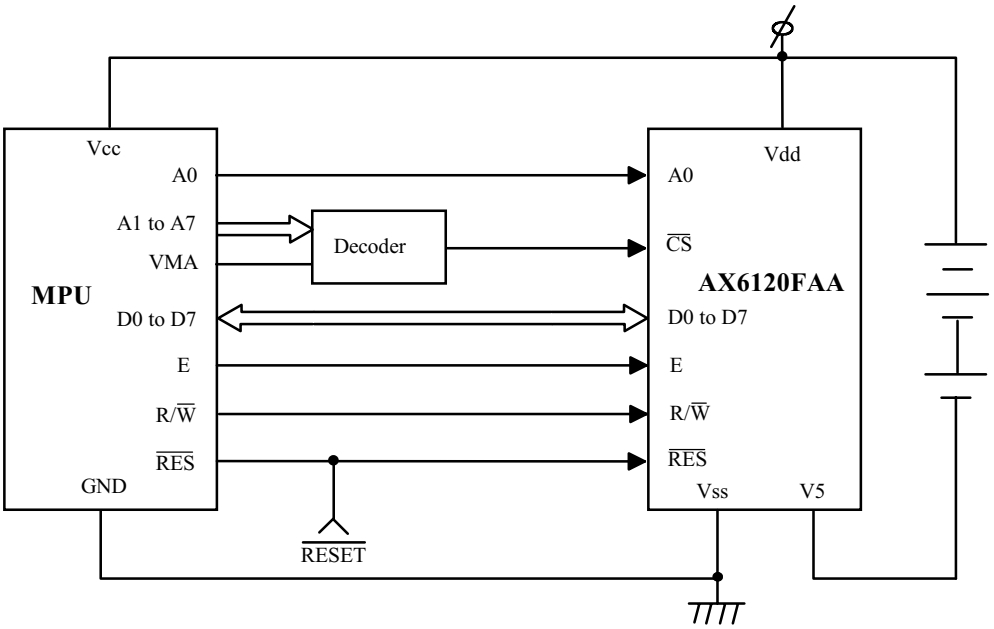
2. Parasitic capacitance in the feedback loop will decrease fosc. The leads of the feedback resistor, Rf, must be kept as short as possible. It may be necessary to reduce Rf to keep fosc within specified limits.
3. If a system has two or more slave drivers a CMOS buffer will be required.

MPU Interface Configuration

80 Family MPU



68 Family MPU



Notes : 1. These examples also apply to the AX6121FOA and AX6121FAA.
2. The AX6120FOA does not have a CS pin. A0, RD (or E) and WR (or R/W) should be gated with CS externally. See Figure 5.

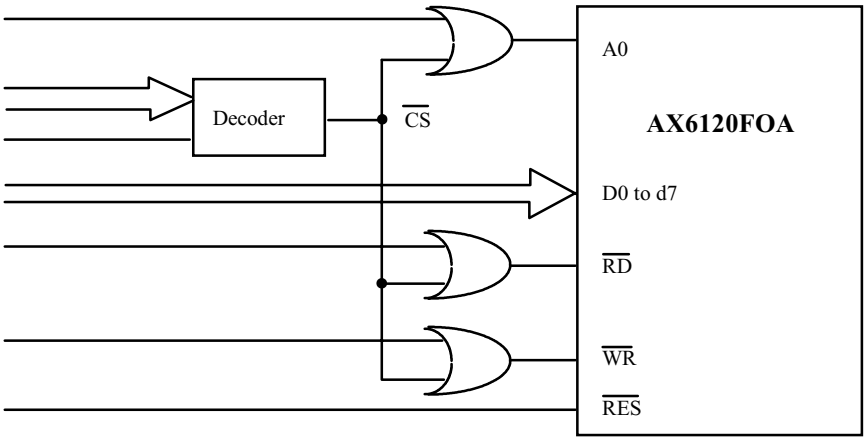
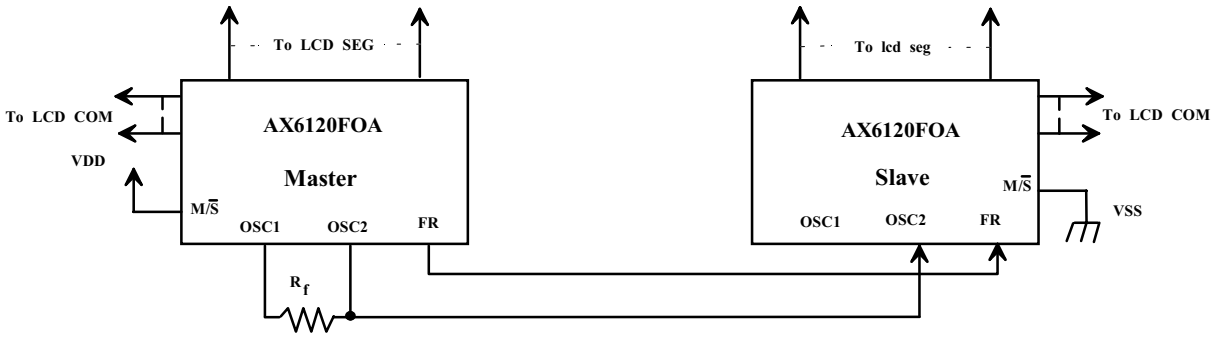
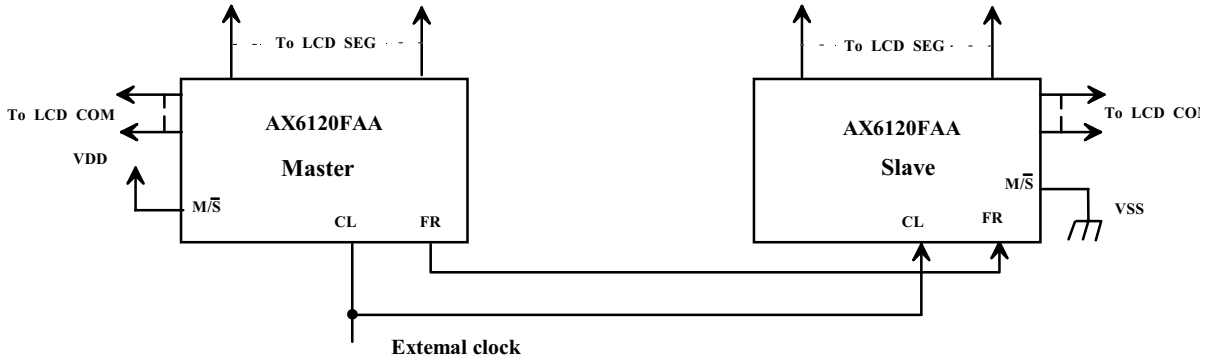


Figure 5 Generating Control Signals for the AX6120FOA

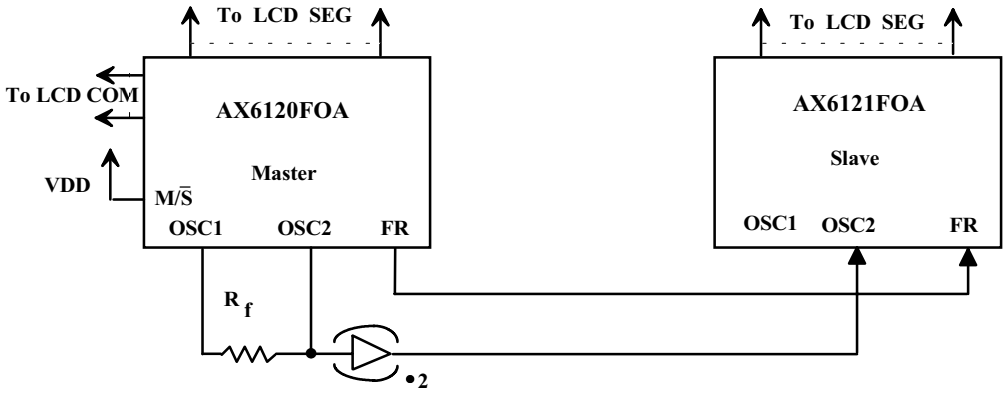
AX6120F$_{OA}$



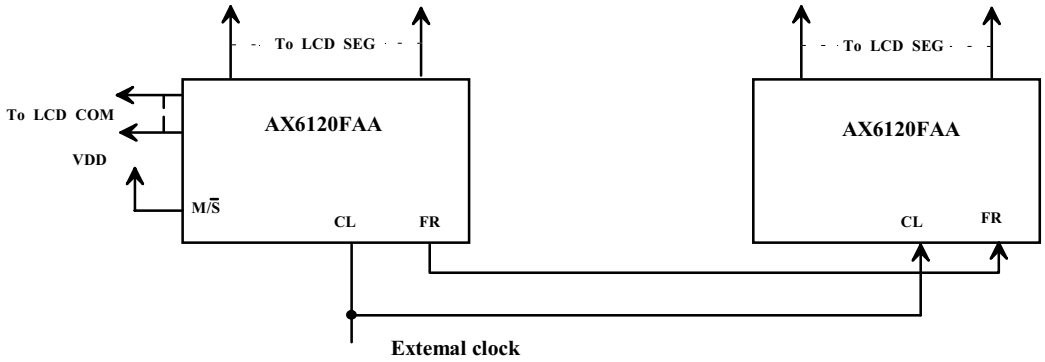
A
X6120F$_{AA}$ - AX6120F$_{AA}$



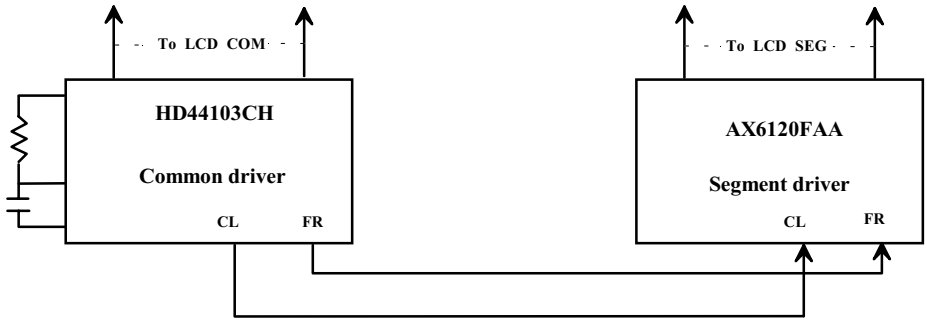
AX6120F$_{OA}$ - AX6121F$_{OA}$ (See note 1)



AX6120F$_{AA}$ - AX6121F$_{AA}$



HD44103CH - AX6121F$_{AA}$

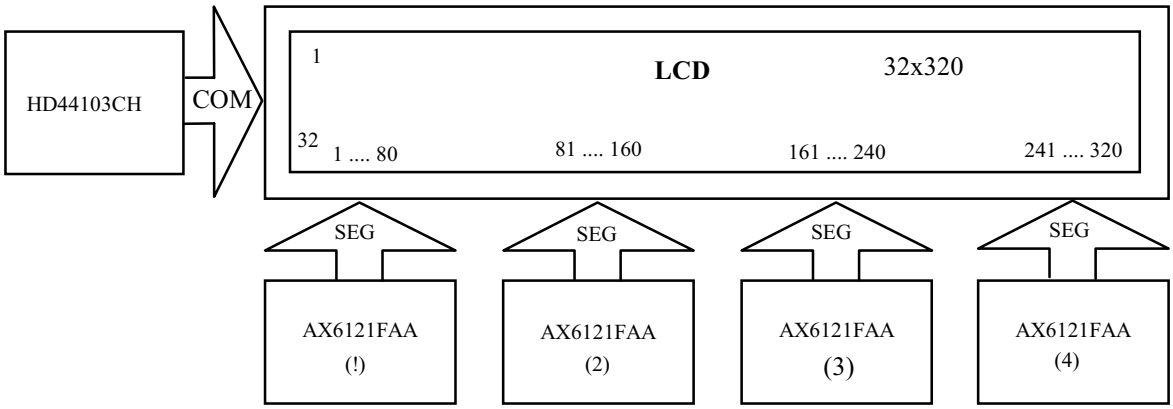


Notes : 1. The duty cycle of the slave must be the same as that for the master.
2. If a system has two or more slave drivers a CMOS buffer will be required.

Panel Interface Configuration

1/32 Duty Cycle, Single Screen

- 20 Sino-Japanese kanji characters (16x16pixels) per line
- 2 lines



1/32 Duty Cycle, Dual Screen

- 20 Sino-Japanese kanji charaeters (16x16 pixels) per line
- 4 lines

