芯颖科技有限公司
CHIP WEALTH TECHNOLOGY LTD.

CH13620

368RGB x 448 dot

AMOLED Mobile Single Chip Driver

1 DESCRIPTION

The CH13620 device is a single-chip solution for LTPS AMOLED that incorporates gate drivers and is capable of 368RGBx448, 360RGBx360, 320RGBx360, 320RGBx320, 320RGBx290, 300RGBx300, 272RGBx340, 264RGBx296, 240RGBx240, 240RGBx320, 180RGBx360, with internal GRAM. It includes a 1,978,368 bits internal memory, a timing controller with glass interface level-shifters and a glass power supply circuit.

The CH13620 supports serial peripheral interfaces (SPI), dual serial peripheral interfaces (Dual-SPI) and quad serial peripheral interfaces (Quad-SPI). The specified window area can be updated selectively, so that moving pictures can be displayed simultaneously independent of the still picture area.

The CH13620 is also able to make gamma correction settings separately for RGB dots to allow benign adjustments to panel characteristics, resulting in higher display qualities. The IC possesses internal GRAM that stores 368-RGB x 448-dot 16.77M-color images. A deep standby mode is also supported for lower power consumption. This LSI is suitable for wearable device applications, including I-watch and smart band.

2 Features

■ Single chip AMOLED Controller/driver.

■ 186 channels source driver.

■ Display Resolutions

- 368RGB x (100+2NL)
- 360RGB x (100+2NL)
- 320RGB x (100+2NL)
- 300RGB x (100+2NL)
- 272RGB x (100+2NL)
- 264RGB x (100+2NL)
- 240RGB x (100+2NL)
- 180RGB x (100+2NL)

■ Display data frame memory

- RAM size: 1,978,368 bits (368 x 448 x 24 bits*1/2)

■ Display mode (Color mode)

- Full color mode: 16.7M colors
- Reduce color mode: 262K colors
- Reduce color mode: 65K colors
- Reduce color mode: 4096 colors
- Idle mode: 16.7M colors, 262K colors , 65K colors , 4096 colors , 8 colors

■ Interface

- Serial peripheral interface (SPI)
- Dual serial peripheral interface (Dual-SPI)
- Quad serial peripheral interface (Quad-SPI)

■ Display features:

- Built-in digital R/G/B separate gamma correct circuit
- Source output mirror function
- Source support MUX1:6,1:9
- Partial display function
- Deep standby function

■ Supply voltage range

- Regulator and I/O power supply for VDDIO,VDDR: 1.65 ~ 3.6V
- Analog power supply for VDDA,VDDB: 2.7 ~ 3.6V

■ Output voltage range

- Step-up output voltage range for AVDD:4.5 ~ 6.5V(2*VDDB,3*VDDB)
- Step-up output voltage range for AVEE: -1*VDDB,-2*VDDB
- gamma highest voltage range for VGM: 2.0V ~ 6.3V (10mV/step,max:AVDD-0.2)
- gamma lowest voltage range for VGS: 0,0.2V ~ 4.5V(10mV/step)
- Positive gate driver voltage range for VGH: AVDD, AVDD+VDDB,2AVDD
- Negative gate driver voltage range for VGL: AVEE,AVEE-VDDB,AVEE-AVDD
- Positive gate driver voltage range for VGHO : 3.0V ~ 10V(0.5V/step)
- Negative gate driver voltage range for VGLO: -10V ~ -3.0V (0.5V/step)
- Pixel reset voltage range for VREFP: 0.5V ~ 5.0V (0.1V/step, max:AVDD-0.2)
- Pixel reset voltage range for VREFN: -5.0V ~ -0.2V(0.1V/step, max:AVEE+0.2)
- Step-up output positive voltage for ELVDD(VEP): 2.0V~5V(0.1V/step)
- Step-up output negative voltage for ELVSS(VEN):0,-0.2V~-5V(0.1V/step)

■ On chip:

- Brightness control
- Support HBM function(High brightness mode)
- Support Sunlight Readability enhancement function
- Support circular edge optimization algorithm
- Support oblique line optimization algorithm
- Support notch algorithm
- Support AOD function
- Support Dynamic ELVSS
- Support gate control signals to gate driver on the panel
- Internal oscillator for display clock
- Support OTP for adjusting gamma/timing parameters

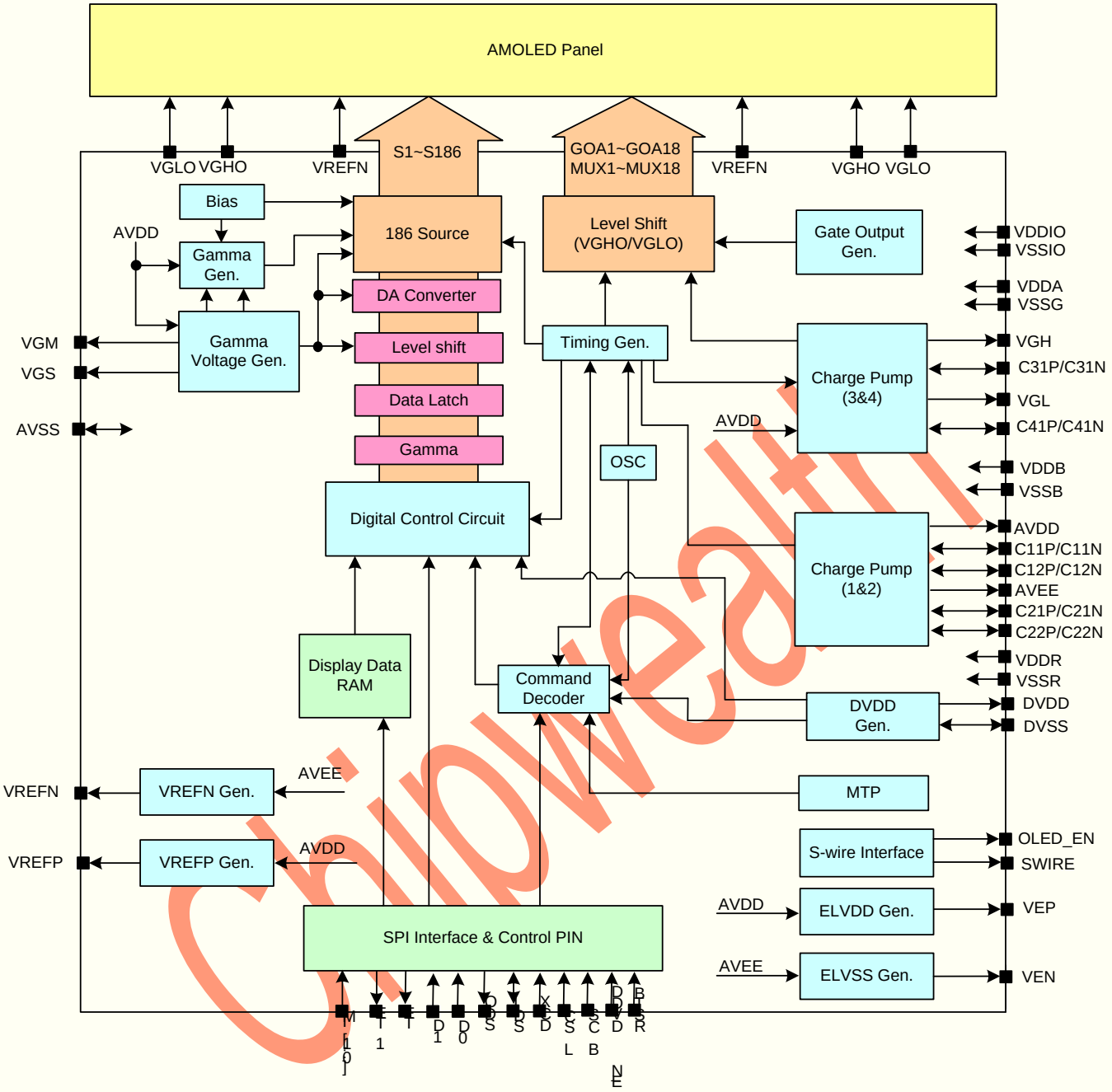
■ PKG

- COF/COG

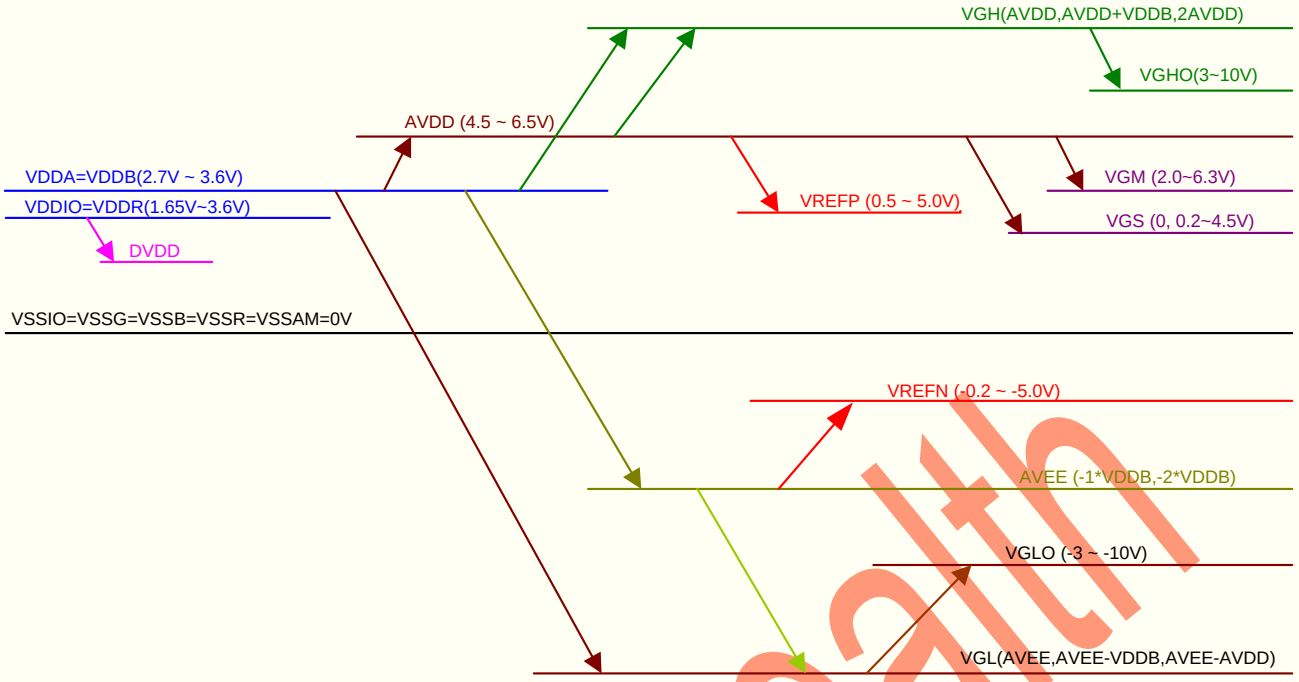
■ Chip size: 12000um x 850um

3 Device Over View

3.1 Block Diagram



3.2 POWER GENERATION CIRCUIT



3.3 EXTERNAL COMPONENTS CONNECTION

Pad Name	Connection	Typical Value
VDDIO/ VDDR	Connect to Capacitor (Max 6V): VDDIO/ VDDR ------||------ GND	2.2μF
VDDA/ VDDB	Connect to Capacitor (Max 6V): VDDA/ VDDB ------||------ GND	2.2μF
DVDD	Connect to Capacitor (Max 6V): DVDD------||------ GND	2.2μF
VSSIO	Interface ground(Connect to GND)	-
VSSR	Regulator ground(Connect to GND)	-
VSSB	Pump ground (Connect to GND)	-
DVSS	Digital logic ground (Connect to GND)	-
VSSG	Analog gray ground (Connect to GND)	-
AVSS	Source OP ground (Connect to GND)	-
C11P, C11N	Connect to Capacitor (Max 10V): C11P ------||------ C11N	1.0μF
C12P, C12N	Connect to Capacitor (Max 10V): C12P ------||------ C12N	1.0μF
C21P, C21N	Connect to Capacitor (Max 10V): C21P------||------ C21N	1.0μF
C22P, C22N	Connect to Capacitor (Max 10V): C22P ------||------ C22N	1.0μF
C31P, C31N	Connect to Capacitor (Max 16V): V31P ------||------ C31N	1.0μF
C41P, C41N	Connect to Capacitor (Max 16V): V41P ------||------ C41N	1.0μF
AVDD	Connect to Capacitor (Max 10V): AVDD ------||------ GND	4.7μF
AVEE	Connect to Capacitor (Max 10V): AVEE ------||------ GND	2.2μF
VGH	Connect to Capacitor (Max 16V): VGH ------||------ GND	1.0μF
VGL	Connect to Capacitor (Max 16V): VGL ------||------ GND └----►|------ GND	2.2μF D1(Note 1)
VREFP	Connect to Capacitor (Max 10V): VREFP ------||------ GND	2.2μF(Note 2)
VREFN	Connect to Capacitor (Max 10V): VREFN ------||------ GND	2.2μF
VEP	Connect to Capacitor (Max 10V): VEP ------||------ GND	2.2uF(Note 2)
VEN	Connect to Capacitor (Max 10V): VEN ------||------ GND	2.2μF(Note 2)
VGHO	Connect to Capacitor (Max 16V): VGHO ------||------ GND	1.0μF
VGLO	Connect to Capacitor (Max 16V): VGLO ------||------ GND	1.0μF
VREF	Connect to Capacitor (Max 6V): VREF ------||------ GND	2.2μF
VGM	No Capacitor is needed	-
VGS	No Capacitor is needed	-

Note 1: The recommended component: Schottky RB521CS-30 (VF=0.35V@10mA and VR=30V).
Note 2: Leave VREFP/VEP/VEN open if this voltage is not in use.

3.4 MAXIMUM SERIES RESISTANCE

The driver will operate in “Chip on Glass” applications with series Resistances (due to ITO track Resistance). Voltages are specified at module I/O assuming maximum values as in below table.

Name	Type	Maximum Series Resistance	Unit
VDDIO	Power supply	20	Ω
VDDR	Power supply	5	Ω
VDDA	Power supply	15	Ω
VDDB	Power supply	5	Ω
VSSIO	Power supply	20	Ω
VSSR	Power supply	5	Ω
VSSB	Power supply	5	Ω
VSSG	Power supply	15	Ω
AVSS	Power supply	10	Ω
DVSS	Power supply	5	Ω
IM[1:0]	Input	30	Ω
DVDD_EN	Input	30	Ω
RSTB, CSB,SCL,DCX,D[1:0]	Input	30	Ω
SDI	Input/Output	30	Ω
SDO, OLED_EN,SWIRE	Output	30	Ω
DVDD	Power output	5	Ω
VREF	Power output	15	Ω
VGM,VGS,VEP,VEN,VREFP,VREFN	Power output	15	Ω
AVDD,AVEE	Power output	5	Ω
C11P/N,C12P/N,C21P/N,C22P/N	Capacitor connection	5	Ω
C31P/N, C41P/N	Capacitor connection	10	Ω
VGH,VGL,VGHO,VGLO	Power output	10	Ω

4 Pin description

Symbol	Name	Description
Power Supply Pins		
VDDIO	I/O Power	Power supply for interface system except MIPI interface.
VDDR	Regulator Power	Power supply for regulator system.
VDDA	Analog Power	Power supply for analog system.
VDDB	Analog Power	Power supply for DC/DC converter.
VSSIO	I/O GND	System ground for interface system.
VSSR	Regulator GND	System ground for regulator.
VSSB	Pump GND	System ground for pump circuit system.
VSSG	Analog gray GND	System ground for analog gray system.
AVSS	Source OP GND	System ground for source OP.
DVSS	Digital GND	System ground for digital circuit system.
DC/DC Converter Pins		
AVDD	O	Output voltage from step-up circuit 1.generated from VDDB. Connect a capacitor for stabilization.
AVEE	O	Output voltage from internal step-up circuit 2, generated from VDDB. Connect a capacitor for stabilization.
VGH	O	Output voltage from step-up circuit 3. Connect a capacitor for stabilization.
VGL	O	Output voltage from step-up circuit 4. Connect a capacitor for stabilization.
C11P,C11N C12P,C12N	O	Capacitor connection pins for the step-up circuit which generate AVDD. Connect capacitor as requirement. When not in used, please open these pins.
C21P,C21N C22P,C22N	O	Capacitor connection pins for the step-up circuit which generate AVEE. Connect capacitor as requirement.
C31P,C31N	O	Capacitor connection pins for the step-up circuit which generate VGH. Connect capacitors as required, if not used open these pins.
C41P,C41N	O	Capacitor connection pins for the step-up circuit which generate VGL. Connect capacitors as required, if not used open these pins.
VGM	O	Output voltage generated from AVDD. LDO output for gamma's highest reference voltage.
VGS	O	Output voltage generated from AVDD. LDO output for gamma's lowest reference voltage.
VEP	O	Output voltage generated from AVDD. LDO output positive voltage for panel ELVDD.
VEN	O	Output voltage generated from AVEE. LDO output negative voltage for panel ELVSS.
VREF	O	Regulator output for internal reference voltage, Connect a capacitor for stabilization.
DVDD	O	Regulator output for logic system power, Connect a capacitor for stabilization.

Symbol	I/O	Description
SPI Interface Pins connect with Host		
CSB	I	Chip select input pin in SPI I/F. If not used, please connect to VDDIO.
SCL	I	Synchronous clock signal in SPI I/F. If not used, please connect to VSSIO.
DCX	I	Display data/command selection in 8 bit SPI I/F. DCX = “0” : Command; DCX = “1” : Display data or Parameter; If not used, please connect to VSSIO.
SDI	I/O	Serial input signal in SPI I/F. The data is input on the rising edge of the SCL signal. If not used, please open this pin.
SDO	O	Serial outputs signal in SPI I/F. The data is output on the edge of the SCL signal. If the host places the SDI line into high-impedance state during the read interval, the SDI and SDO can be tied together. If not used, please open this pin.
D0,D1	I	Serial input signal in SPI I/F. The data is input on the rising edge of the SCL signal. If not used, please connect to VSSIO.

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">Interface Logic Pins</td></tr>
<tr><td>RSTB</td><td>I</td><td>This signal will reset the device and must be applied to properly initialize the chip.
Signal is active low.</td></tr>
<tr><td>IM[1:0]</td><td>I</td><td>Interface type selection.
<table>
<tr><th>IM[1:0]</th><th>Display Data</th><th>Command</th></tr>
<tr><td>00</td><td>9 bit SPI</td><td>9 bit SPI</td></tr>
<tr><td>01</td><td>8 bit SPI</td><td>8 bit SPI</td></tr>
<tr><td>10</td><td>Quad-SPI</td><td>Quad-SPI</td></tr>
<tr><td>11</td><td>/</td><td>16 bit rising SPI</td></tr>
</table>
Please connect to VDDIO or VSSIO.</td></tr>
<tr><td>TE</td><td>O</td><td>Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command.
When this pin is not activated, this pin is output low.
If not used, please open this pin.</td></tr>
<tr><td>TE1</td><td>O</td><td>This signal is used for noise sensing of TP and generated per scan line.
The output voltage level of TE1 pin is determined by VDDIO.
The TE1 pin can select to output other control signals via register setting as well.
If not used, please open this pin.</td></tr>
<tr><td>DVDD_EN</td><td>I</td><td>Set generation of DVDD.
DVDD_EN=0, disable generation of DVDD.
DVDD_EN=1, enable generation of DVDD.
This pin internal pull high.</td></tr>
</table>

Symbol	I/O	Description
Output Driver Pins		
S1~ S186	O	Pixel electrode driving output.
GOA1~GOA18 MUX1~MUX28	O	Gate driver output pins. The swing voltage level is VGHO to VGLO.
VGHO	O	High voltage level for gate control signals and gate circuit of panel.
VGLO	O	Low voltage level for gate control signals and gate circuit of panel.
VREFP	O	Pixel Reset Voltage. Connect a capacitor for stabilization. If not used, please open this pin.
VREFN	O	Pixel Reset Voltage. Connect a capacitor for stabilization. If not used, please open this pin.
External Power Control Pins		
OLED_EN	O	Power IC enable control pin. If not used, please open this pin.
SWIRE	O	S-wire protocol setting pin of power IC. If not used, please open this pin.
Test Pins		
DUMMY	-	-These pins are dummy with Hi-Z in driver IC (not have any function inside). -Signal traces can pass through on glass under these pads.
ATN ATP	O	Test pins, not accessible to user. If not used, please open this pin.
DTEST1[4:0],DTEST2	I/O	Test pins, not accessible to user. Please connect to VSSIO.
DTEST3[6:0] DTEST4[1:0]	I/O	Test pins, not accessible to user.

5 Command Description

User Command set list

Instr.	ACT	R/W	Address		Parameter								Function
			MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
NOP	Dir	W	00h	0000h	No Argument								No Operation
SWRESET	Dir	W	01h	0100h	No Argument								Software Reset
RDDID	Dir	R	04h	0400h	ID1[7:0]								Read display ID
				0401h	ID2[7:0]								
				0402h	ID3[7:0]								
RDDPM	Dir	R	0Ah	0A00h	D7	D6	D5	D4	D3	D2	-	-	Read display power mode
RDDMADCTR	Dir	R	0Bh	0B00h	MY	MX	MV	ML	RGB	-	RSMX	RSMY	Read display MADCTR
RDDCOLMO	Dir	R	0Ch	0C00h	-	-	-	-	-	IFPF[2:0]			Read display pixel format
RDDIM	Dir	R	0Dh	0D00h	-	-	D5	D4	D3	-	-	-	Read display image mode
RDDSM	Dir	R	0Eh	0E00h	D7	D6	D5	-	-	-	-	D0	Read display signal mode
RDDSDR	Dir	R	0Fh	0F00h	-	-	-	-	-	D2	D1	D0	Read display Self-diagnostic
SLPIN	DVS	W	10h	1000h	No Argument								Sleep in & booster off
SLPOUT	Dir	W	11h	1100h	No Argument								Sleep out & booster on
PTLON	DVS	W	12h	1200h	No Argument								Partial display mode on
NORON	DVS	W	13h	1300h	No Argument								Normal display mode on
INVOFF	DVS	W	20h	2000h	No Argument								Display inversion off (normal)
INVON	DVS	W	21h	2100h	No Argument								Display inversion on
ALLPOFF	DVS	W	22h	2200h	No Argument								All pixel off (black)
ALLPON	DVS	W	23h	2300h	No Argument								All pixel on (white)
DISPOFF	DVS	W	28h	2800h	No Argument								Display off
DISPON	DVS	W	29h	2900h	No Argument								Display on
CASET	Dir	R/W	2Ah	2A00h	-	-	-	-	-	-	-	SC8	Set column start address
				2A01h	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	
				2A02h	-	-	-	-	-	-	-	EC8	
				2A03h	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	
RASET	Dir	R/W	2Bh	2B00h	-	-	-	-	-	-	SP9	SP8	Set row start address
				2B01h	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	
				2B02h	-	-	-	-	-	-	EP9	EP8	
				2B03h	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	
RAMW	Dir	W	2Ch	2C00h	D7	D6	D5	D4	D3	D2	D1	D0	Write RAM start
				2C01h	D7	D6	D5	D4	D3	D2	D1	D0	

				2C02h	D7	D6	D5	D4	D3	D2	D1	D0	
				:	:	:	:	:	:	:	:	:	
RAMR	Dir	R	2Eh	2E00h	D7	D6	D5	D4	D3	D2	D1	D0	Read RAM start
				2E01h	D7	D6	D5	D4	D3	D2	D1	D0	
				2E02h	D7	D6	D5	D4	D3	D2	D1	D0	
				:	:	:	:	:	:	:	:	:	
HPTLAR	DVS	R/W	30h	3000h	-	-	-	-	-	-	PSR[9]	PSR[8]	Horizontal Partial area
				3001h	PSR[7]	PSR[6]	PSR[5]	PSR[4]	PSR[3]	PSR[2]	PSR[1]	PSR[0]	
				3002h	-	-	-	-	-	-	PER[9]	PER[8]	
				3003h	PER[7]	PER[6]	PER[5]	PER[4]	PER[3]	PER[2]	PER[1]	PER[0]	
VPTLAR	DVS	R/W	31h	3100h	-	-	-	-	-	-	-	PSC[8]	Vertical Partial area
				3101h	PSC[7]	PSC[6]	PSC[5]	PSC[4]	PSC[3]	PSC[2]	PSC[1]	PSC[0]	
				3102h	-	-	-	-	-	-	-	PEC[8]	
				3103h	PEC[7]	PEC[6]	PEC[5]	PEC[4]	PEC[3]	PEC[2]	PEC[1]	PEC[0]	
TEOFF	DVS	W	34h	3400h	No Argument								Tearing effect line off
TEON	DVS	W	35h	3500h	-	-	-	-	-	-	TE_M	TELOM	Tearing effect mode set & on
SDC	Dir	R/W	36h	3600h	MY	MX	MV	ML	RGB	-	RSMX	RSMY	Scan direction control
IDMOFF	DVS	W	38h	3800h	No Argument								Idle mode off
IDMON	DVS	W	39h	3900h	No Argument								Idle mode on
IPF	Dir	R/W	3Ah	3A00h	-	-	-	-	-	IFPF[2:0]			Interface Pixel Format
RAMWC	Dir	W	3Ch	3C00h	D7	D6	D5	D4	D3	D2	D1	D0	Write RAM Continuous
				3C01h	D7	D6	D5	D4	D3	D2	D1	D0	
				3C02h	D7	D6	D5	D4	D3	D2	D1	D0	
				:	:	:	:	:	:	:	:	:	
RAMRDC	Dir	R	3Eh	3E00h	D7	D6	D5	D4	D3	D2	D1	D0	Read RAM Continuous
				3E01h	D7	D6	D5	D4	D3	D2	D1	D0	
				3E02h	D7	D6	D5	D4	D3	D2	D1	D0	
				:	:	:	:	:	:	:	:	:	
STESL	DVS	W	44h	4400h	N15	N14	N13	N12	N11	N10	N9	N8	Set tearing effect scan line
				4401h	N7	N6	N5	N4	N3	N2	N1	N0	
GSL	Dir	R	45h	4500h	N15	N14	N13	N12	N11	N10	N9	N8	Get scan line
				4501h	N7	N6	N5	N4	N3	N2	N1	N0	
DSTBON	Dir	W	4Fh	4F00h	-	-	-	-	-	-	-	DSTB	Deep standby mode on
WDB	DVS	W	51h	5100h	DBV[7:0]								Write display brightness
RDB	DVS	R	52h	5200h	DBV[7:0]								read display brightness
HBMSEL	DVS	W	53h	5300h	HBM_EN[7:0]								Select HBM mode
RHBM	Dir	R	54h	5400h	HBM_EN[7:0]								Read HBM mode

NEM	DVS	R/W	55h	5500h	NOR_WIDTH[7:0]								Set EM Width for Normal mode
IEM	DVS	R/W	56h	5600h	IDLE_WIDTH[7:0]								Set EM Width for Idle mode
HEM	DVS	R/W	57h	5700h	HBM_WIDTH[7:0]								Set EM Width for HBM mode
BACTR	Dir	R/W	60h	6000h	EM_M	EM_DIM_EN	HMS_DIM_EN	IMS_DIM_EN	-	BC_LINEAR	BC_DIM_M	BC_DIM_EN	Dimming Control
DECTR	DVS	R/W	62h	6200h	-	-	-	D_DIM_EN	-	IDLE_DELVSS_EN	DELVSSM[1:0]		Dynamic ELVSS Function Control
SRECTR	DVS	R/W	63h	6300h	-	-	-	SRE_EN	-	-	SRE_SIZE[1:0]		SRE Mode Control
GACMSET	DVS	R/W	64h	6400h	-	-	GAM_HBM[1:0]		GAM_IDLE[1:0]		GAM_NOR[1:0]		Gamma and Color Mode set
SPIRDC	Dir	W	65h	6500h	SPI_CNT[7:0]								SPI read manufacture
CICEN	DVS	R/W	67h	6700h	-	-	UD_POS[1:0]		-	-	-	R_O_EN	circular edgeenable
OLOAEN	DVS	R/W	68h	6800h	-	-	OBL_Y	OBL_X	-	-	-	OBL_EN	Oblique Lineenable
NOTCHEN	DVS	R/W	69h	6900h	-	-	-	-	-	-	-	Notch_EN	Notch algorithm enable
INCIREN	DVS	R/W	6Ah	6A00h	-	-	-	-	-	-	-	R_I_EN	Inside CircularAlgorithm Enable
SWIREMANU	DVS	R/W	6Ch	6C00h	SMANU_CTL[7:0]								Swire Manual Control
SPIRDC	Dir	W	6Dh	6D00h	-	-	-	-	-	-	-	SPI_READ_EN	SPI read manufacture command Enable
RDID1	Dir	R	DAh	DA00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read ID1
RDID2	Dir	R	DBh	DB00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	Read ID2
RDID3	Dir	R	DCh	DC00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	Read ID3

Notes:
1. The following description is indicates the executing time of instructions.

No.	Symbol	Executing time
1	Dir (Direct)	At the received a completed instruction and parameter
2	DVS (Display Vertical Sync.)	Synchronized with the next frame

2. The 8-bit Command code in above table and following command description means QSPI.

NOP(0000h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
00h	0000h	No Argument								N/A
Description		This command is empty command. It does not have effect on the display module. However it can be used to terminate parameter write commands.								
Restriction		-								

SWRESET: Software Reset (0100h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
01h	0100h	No Argument								N/A
Description		When the software reset command is written, it causes software reset. It resets the commands and parameters to their S/W reset default values. (See default tables in each command description). The display is blank immediately.								
Restriction		It will be necessary to wait 5 msec before sending new command following software reset. The display module loads all display suppliers factory default values to the registers during this 5 msec. If software reset is applied during sleep out mode, it will be necessary to wait 120 msec before sending sleep out command. Software reset command cannot be sent during sleep out sequence.								

RDDID: Read Display ID (0400h~0402h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
04h	0400h	ID1[7:0]								00h
	0401h	ID2[7:0]								80h
	0402h	ID3[7:0]								00h
Description		This read byte returns 24-bit display identification information. The 1st parameter (ID1): the module's manufacture ID. The 2nd parameter (ID2): the module/driver version ID. The 3rd parameter (ID3): the module/driver ID. Note: Commands RDID1/2/3 (DAh, DBh, DCh) read data correspond to the parameter 1, 2, 3 of the command 04h, respectively								
Restriction		-								

RDDPM: Read display power mode (0A00h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>0Ah</td><td>0A00h</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>-</td><td>-</td><td>08h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>Booster Voltage Status</td><td>“1”=Booster On, “0”=Booster Off</td></tr>
<tr><td>D6</td><td>Idle Mode On/Off</td><td>“1”=Idle Mode On, “0”= Idle Mode Off</td></tr>
<tr><td>D5</td><td>Partial mode On/Off</td><td>“1”=Partial Mode On, “0”= Partial Mode Off</td></tr>
<tr><td>D4</td><td>Sleep In/Out</td><td>“1”=Sleep Out Mode, “0”=Sleep In Mode</td></tr>
<tr><td>D3</td><td>Display Normal Mode On/Off</td><td>“1”=Display Normal On, “0”=Display Normal Off</td></tr>
<tr><td>D2</td><td>Display On/Off</td><td>“1”=Display On, “0”=Display Off</td></tr>
</table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

RDDMADCTR: Read Display MADCTR (0B00h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>0Bh</td><td>0B00h</td><td>MY</td><td>MX</td><td>MV</td><td>ML</td><td>RGB</td><td>-</td><td>RSMX</td><td>RSMY</td><td>00h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">This command indicates the current status of the display as described in the table below.
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>MY</td><td>Row Address Increment</td><td>“0” = Increasing in vertical;
“1” = Decreasing in vertical</td></tr>
<tr><td>MX</td><td>Column Address Increment</td><td>“0” = Increasing in horizontal;
“1” = Decreasing in horizontal</td></tr>
<tr><td>MV</td><td>Row/Column Order</td><td>“0” =Normal;
“1” = Row/column exchange</td></tr>
<tr><td>ML</td><td>Vertical Refresh Order</td><td>“0” =Panel Refresh Top to Bottom;
“1” = Panel Refresh Bottom to Top;</td></tr>
<tr><td>RGB</td><td>RGB/BGR Order</td><td>“0” =RGB;
“1” = BGR</td></tr>
<tr><td>RSMX</td><td>Horizontal Flip</td><td>“0” =Normaldisplay;
“1” = Flipped display</td></tr>
<tr><td>RSMY</td><td>Vertical Flip</td><td>“0” =Normaldisplay;
“1” = Flipped display</td></tr>
</table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

RDDCOLMOD: Read Display Pixel Format (0C00h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>0Ch</td><td>0C00h</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td colspan="3">IFPF[2:0]</td><td>07h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>IFPF[2:0]</th><th>DBI pixel format</th></tr>
<tr><td>001</td><td>SPI 1-1-1</td></tr>
<tr><td>010</td><td>SPI 8bit/pixel(256 colors);SPI 3-3-2</td></tr>
<tr><td>011</td><td>SPI 8bit/pixel(256 colors);SPI 256Gray</td></tr>
<tr><td>101</td><td>16bit/pixel(65,536 colors)</td></tr>
<tr><td>110</td><td>18bit/pixel(262,144 colors)</td></tr>
<tr><td>111</td><td>24bit/pixel(16.7M colors)</td></tr>
<tr><td>Others</td><td>reserved</td></tr>
</table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

RDDIM: Read Display Image Mode (0D00h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>0Dh</td><td>0D00h</td><td>-</td><td>-</td><td>D5</td><td>D4</td><td>D3</td><td>-</td><td>-</td><td>-</td><td>00h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D5</td><td>Inversion On/Off</td><td>“1” = Inversion On, “0” = Inversion Off</td></tr>
<tr><td>D4</td><td>All Pixel On</td><td>“1” = White display, “0” = Normal display</td></tr>
<tr><td>D3</td><td>All Pixel Off</td><td>“1” = Black display, “0” = Normal display</td></tr>
</table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

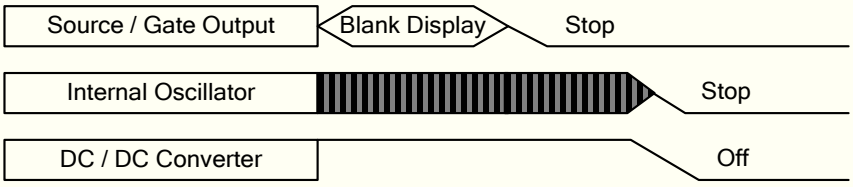
RDDSM: Read Display Signal Mode (0E00h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>0Eh</td><td>0E00h</td><td>D7</td><td>D6</td><td>D5</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>00h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>Tearing Effect Line On/Off</td><td>“1” = On, “0” = Off</td></tr>
<tr><td>D6</td><td>Tearing Effect Mask Mode</td><td>“1” = TE Mask Mode
“0” = TE Non-mask Mode</td></tr>
<tr><td>D5</td><td>Tearing Effect Line Mode</td><td>“1” = V-Blanking & H-Blinking Mode
“0” = V-Blanking Mode</td></tr>
</table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

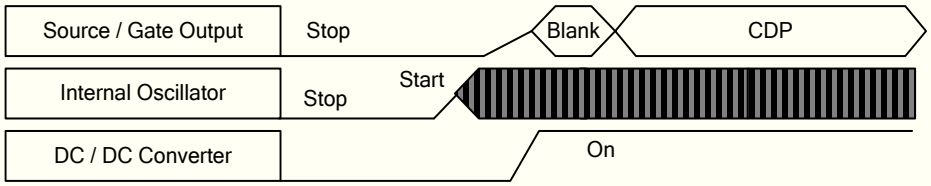
RDDSDR: Read Display Self-Diagnostic Result (0F00h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>0Fh</td><td>0F00h</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>D2</td><td>-</td><td>D0</td><td>00h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>value</th></tr>
<tr><td>D2</td><td>fill ok flag反馈标志位</td><td>“1”=fill ok flag, “0”=not fill ok flag</td></tr>
<tr><td>D0</td><td>Checksum Status</td><td>“1”=Checksum abnormal, “0”= Checksum normal</td></tr>
</table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

SLPIN: Sleep In (1000h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
10h	1000h	No Argument								Sleep in mode
Description		This command causes the AMOLED module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, internal display oscillator is stopped, and panel scanning is stopped.  Control Interface, display data and registers are still working. User can send RGB Timing for blank display after Sleep In command and this information is invalid during 2 frames after Sleep In command if there is used Normal Mode On in Sleep Out-mode. Dimming function does not work when there is changing mode from Sleep Out to Sleep In.								
Restriction		This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.								

SLPOUT: Sleep Out (1100h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
11h	1100h	No Argument								Sleep out mode
Description		This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.  User can start to send RGB Timing before Sleep Out command driver IC will do sequence control about gate control signals when sleep out.								
Restriction		Sleep Out Mode can only be exit by the Sleep In Command (10h), S/W Reset command (01h) or H/W Reset. It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. Driver IC loads all default values of extended and test command to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if those default and register values are same when this load is done and when the driver IC is already Sleep Out mode. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.								

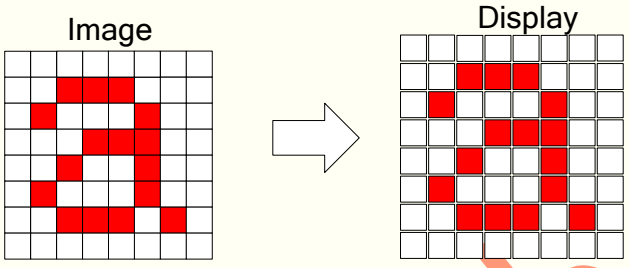
PTLON: Partial Display Mode On(1200h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
12h	1200h	No Argument								Partial Mode On
Description		This command causes the display module to enter the Partial Display Mode. The Partial Display Mode window is described by the Partial Area (30h/31h) command. To leave Partial Display Mode, the Normal Display Mode On (13h) command should be written. The host processor continues to send PCLK, HS and VS information to display modules for two frames after this command is sent when the display module is in Normal Display Mode.								
Restriction		This command has no effect when Partial Display Mode is active.								

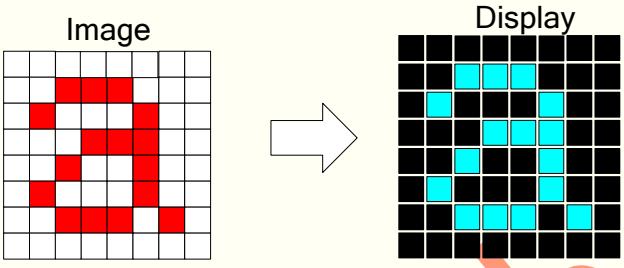
NORON: Normal Display Mode on (1300h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
13h	1300h	No Argument								Normal Mode On
Description		This command returns the display to normal mode.								
Restriction		This command has no effect when Normal Display Mode is active.								

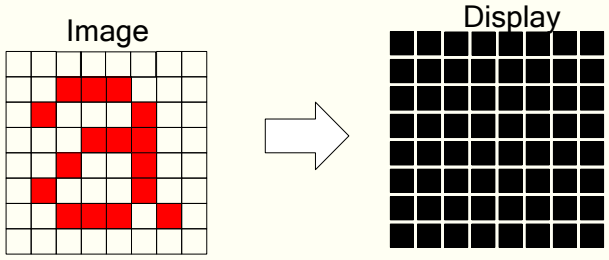
INVOFF: Display Inversion Off (2000h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
20h	2000h	No Argument								Display inversion off
Description		This command is used to recover from display inversion mode. This command does not change any other status. Example: 								
Restriction		This command has no effect when module is already in inversion off mode.								

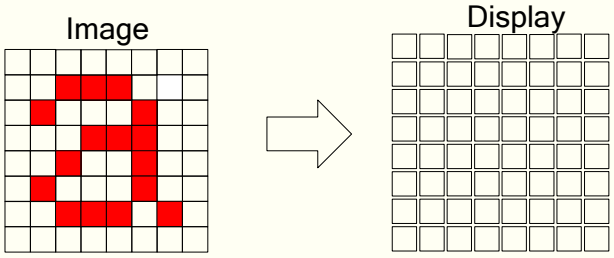
INVON: Display Inversion On (2100h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
21h	2100h	No Argument								Display inversion on
Description		This command is used to enter display inversion mode. This command does not change any other status. To exit from Display Inversion On, the Display Inversion Off command (20h) should be written. Example:  …								
Restriction		This command has no effect when module is already in Inversion On mode.								

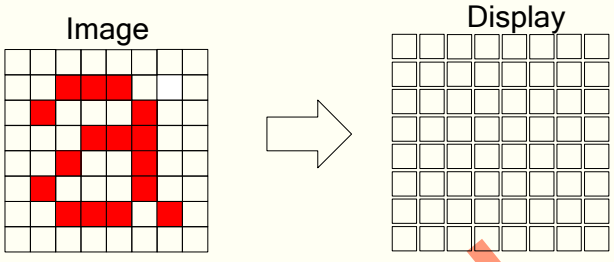
ALLPOFF: All Pixel Off (2200h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
22h	2200h	No Argument								All pixel off
Description		This command turns the display panel black in Sleep Out mode and a status of the Display On/Off register can be on or off. This command does not change any other status. Example:  "All Pixels On" or "Normal Display Mode On" commands are used to leave this mode. The display panel shows the display data after "Normal Display On" command.								
Restriction		This command has no effect when module is already in All Pixel Off mode.								

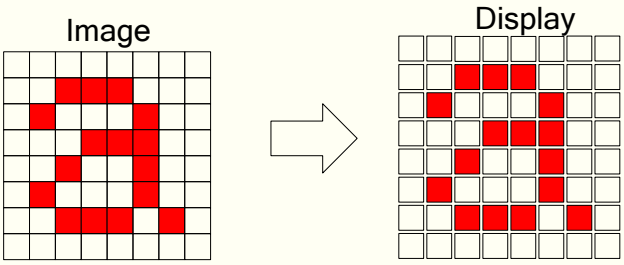
ALLPON: All Pixel On (2300h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
23h	2300h	No Argument								All pixel on
Description		This command turns the display panel white in Sleep Out mode and a status of the Display On/Off register can be on or off. This command does not change any other status. Example:  "All Pixels Off" or "Normal Display Mode On" commands are used to leave this mode. The display panel is showing the display data after "Normal Display On" command.								
Restriction		This command has no effect when module is already in All Pixel ON mode.								

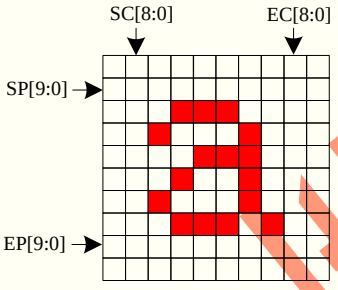
DISPOFF: Display Off (2800h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
28h	2800h	No Argument								Display off
Description		This command is used to enter into Display Off mode. In this mode, the display data is disabled and the blank page is inserted. This command does not change any other status. There will be no abnormal visible effect on the display. Example:  …								
Restriction		This command has no effect when module is already in display off mode.								

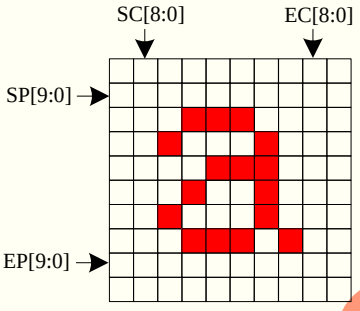
DISPON: Display On (2900h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
29h	2900h	No Argument								Display on
Description		This command is used to recover from DISPLAY OFF mode. Output from display data is enabled. This command does not change any other status. Example:  …								
Restriction		This command has no effect when module is already in Display On mode.								

CASET: Set Column Start Address(2A00h~2A03h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
2Ah	2A00h	-	-	-	-	-	-	-	SC8	00h
	2A01h	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	00h
	2A02h	-	-	-	-	-	-	-	EC8	01h
	2A03h	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	6Fh
Description		This command defines the column extent of the frame memory accessed by the host processor with the write_memory_continue and read_memory_continue command. This command makes no change on theother driver status. The values of SC[8:0] and EC[8:0] are referred when RAMWR command comes.  								
Restriction		When partial update,The SC[8:0] and EC[8:0]-SC[8:0]+1 must can be divisible by 2.								

RASET: Set Row Start Address(2B00h~2B03h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
2Bh	2B00h	-	-	-	-	-	-	SP9	SP8	00h
	2B01h	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	00h
	2B02h	-	-	-	-	-	-	EP9	EP8	01h
	2B03h	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	BFh
Description		This command defines the page extent of the frame memory accessed by the host processor with the write_memory_continue and read_memory_continue command. This command makes no change on theother driver status. The values of SP[9:0] and EP[9:0] are referred when RAMWR command comes.  								
Restriction		When partial update,The SP[9:0] and EC[9:0]-SC[9:0]+1 must can be divisible by 2.								

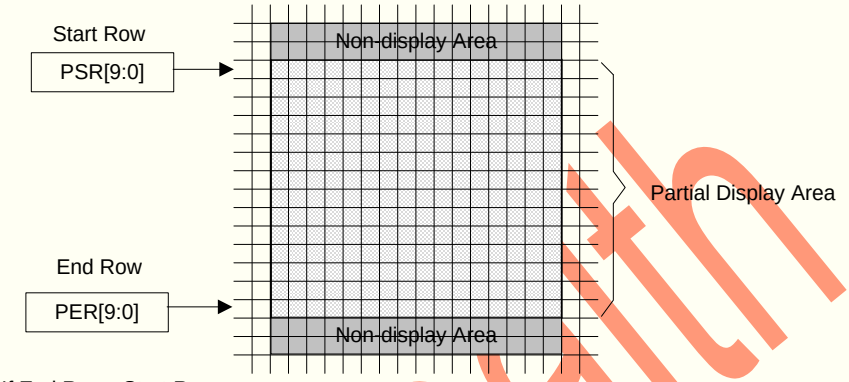
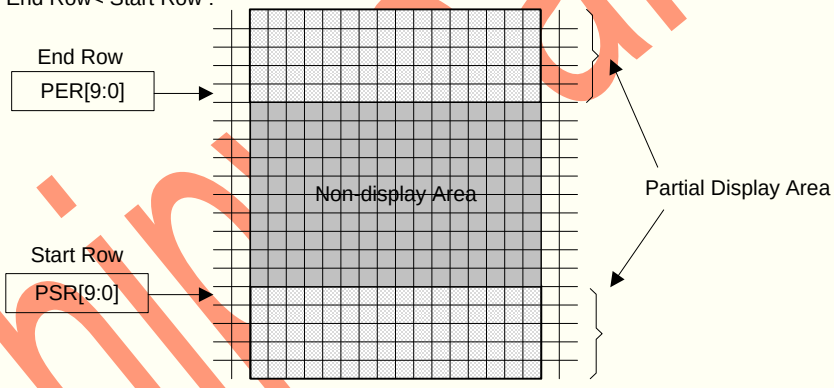
RAMW: Write memory Start (2Ch)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
2Ch	2C00h	D7	D6	D5	D4	D3	D2	D1	D0	Contents of memory is set randomly
	2C01h	D7	D6	D5	D4	D3	D2	D1	D0	
	2C02h	D7	D6	D5	D4	D3	D2	D1	D0	
	:	:	:	:	:	:	:	:	:	
Description		This command transfers image data from the host processor to the display module's frame memory starting at the pixel location specified by preceding CASET (2Ah) and RASET (2Bh) commands. Please use MIPI HS format to write image data. If MV(36h-B5) = 0: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If MV(36h-B5) = 1: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command.								
Restriction		A Memory Write should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMWR(2Ch) and any following RAMWRC(3Ch) commands is written to undefined locations.								

RAMR: Read memory (2Eh)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
2Eh	2E00h	D7	D6	D5	D4	D3	D2	D1	D0	Contents of memory is set randomly
	2E01h	D7	D6	D5	D4	D3	D2	D1	D0	
	2E02h	D7	D6	D5	D4	D3	D2	D1	D0	
	:	:	:	:	:	:	:	:	:	
Description		This command transfers image data from the display module's frame memory to the host processor starting at the pixel location specified by preceding CASET (2Ah) and RASET (2Bh) commands. If MV(36h-B5) = 0: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If MV(36h-B5) = 1: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.								
Restriction		There is no restriction on length of parameters.								

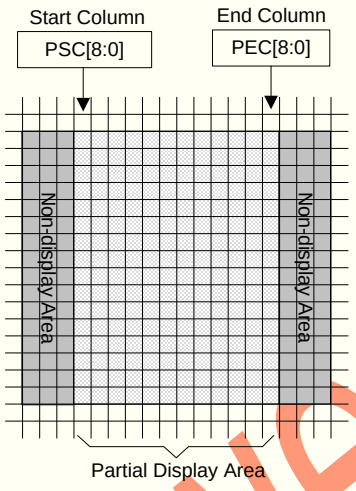
HPTLAR: Horizontal Partial Area (3000h~3003h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
30h	3000h	-	-	-	-	-	-	PSR[9]	PSR[8]	00h
	3001h	PSR[7]	PSR[6]	PSR[5]	PSR[4]	PSR[3]	PSR[2]	PSR[1]	PSR[0]	00h
	3002h	-	-	-	-	-	-	PER[9]	PER[8]	01h
	3003h	PER[7]	PER[6]	PER[5]	PER[4]	PER[3]	PER[2]	PER[1]	PER[0]	6Fh
Description		This command defines the Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the following figure. If End Row> Start Row:  If End Row< Start Row :  If End Row = Start Row Then the Partial Area will be one row deep.								
Restriction		PSR[9:0] and PER[9:0] settings should be within max available Display Area.								

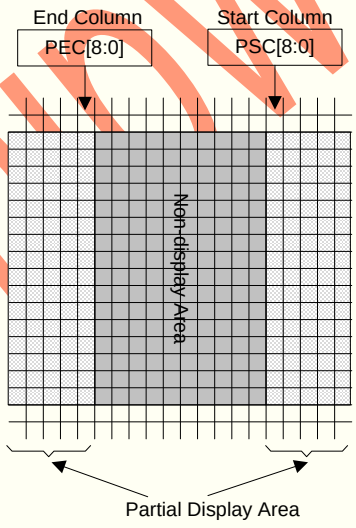
VPTLAR:Vertical Partial Area (3100h~3101h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
31h	3100h	-	-	-	-	-	-	-	PSC[8]	00h
	3101h	PSC[7]	PSC[6]	PSC[5]	PSC[4]	PSC[3]	PSC[2]	PSC[1]	PSC[0]	00h
	3102h	-	-	-	-	-	-	-	PEC[8]	01h
	3103h	PEC[7]	PEC[6]	PEC[5]	PEC[4]	PEC[3]	PEC[2]	PEC[1]	PEC[0]	BFh
Description		This command defines the Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Column (SC) and the second the End Column (EC), as illustrated in the following figure.								
Restriction		PSC[8:0] and PEC[8:0] settings should be within max available Display Area.								

If End Column> Start Column:



If End Column< Start Column:



If End Column = Start Column then the partial Area will be one column deep.

TEOFF: TE Signal OFF (3400h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
34h	3400h	No Argument								TE off
Description		This command is used to turn OFF (Active Low) the output signal from the TE signal line.								
Restriction		This command has no effect when TE output is already OFF.								

TEON: TE Signal ON (3500h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
35h	3500h	-	-	-	-	-	-	TE_M	TELOM	TE on

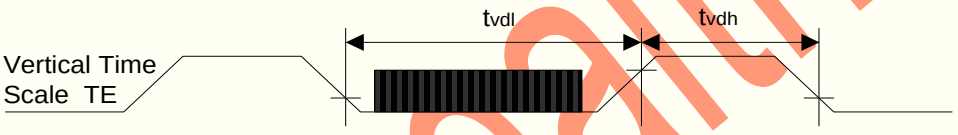
Description

This command is used to turn ON the output signal from the TE signal line. The TE On has one parameter, which describes the mode of Output Line. ("-"means don't care).

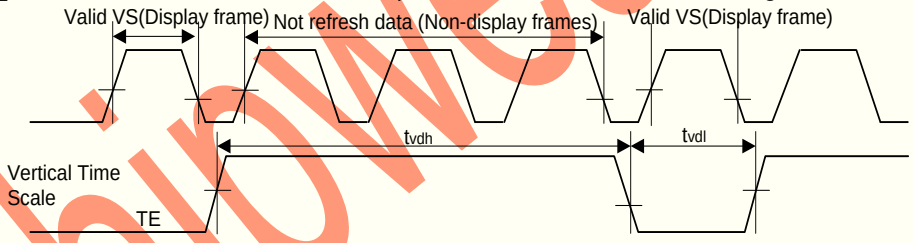
TE_M	Function
0	Output mode of TE signal set
1	Output mode of TE signal set (Mask TE signal during non-display Frame)

When TE_M = "0" & TELOM = "0": The TE Output line consists of V-Blanking information only.

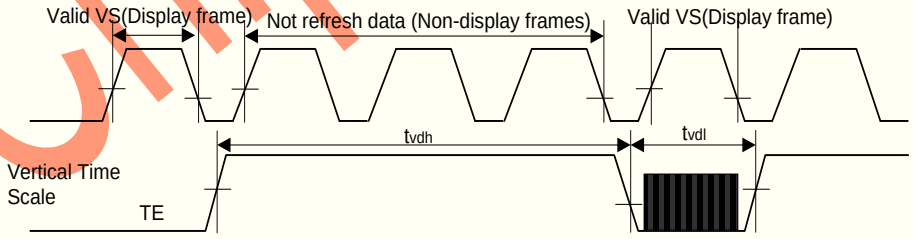
When TE_M = "0" & TELOM = "1": The TE Output line consists of both V-Blanking and H-Blinking information.



When TE_M = "1" & TELOM = "0": The TE Output line consists of Valid V-Blanking information.



When TE_M = "1" & TELOM = "1": The TE Output line consists of Valid V-Blanking information.



Note: 1. During Sleep In Mode with TE Line On, TE Output pin will be active Low.
2. When 35h=01h, TE output high during non-display frame.

Restriction	This command has no effect when Tearing Effect output is already ON.

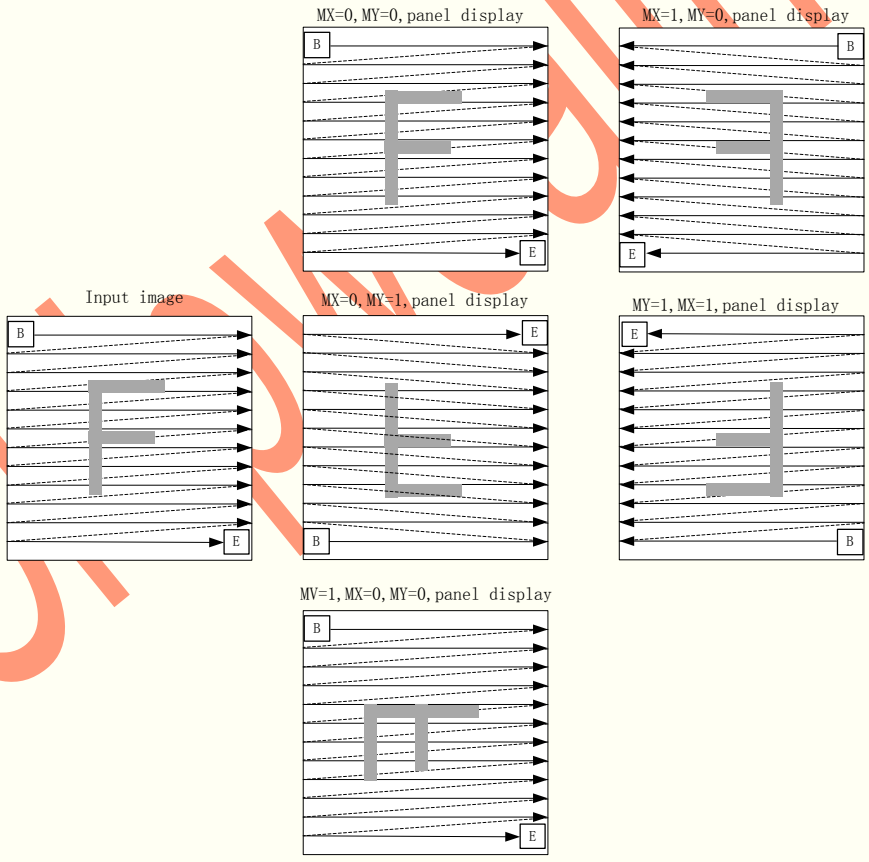
SDC: ScanDirectionControl (3600h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
36h	3600h	MY	MX	MV	ML	RGB	-	RSMX	RSMY	00h

Description

This command defines the scan direction of Source and Gate Driver. This command makes no change on the other driver status.

Bit	Description	Value
MY	Row Address Increment	“0” = Increasing in vertical “1” = Decreasing in vertical
MX	Column Address Increment	“0” = Increasing in horizontal “1” = Decreasing in horizontal
MV	Row/Column Order	“0” = Normal “1” = Row/column exchange
ML	Vertical Refresh Order	“0” = Panel Refresh Top to Bottom “1” = Panel Refresh Bottom to Top
RGB	RGB/BGR Order	“0” = RGB “1” = BGR
RSMX	Horizontal Flip	“0” = Normaldisplay “1” = Flipped display
RSMY	Vertical Flip	“0” = Normaldisplay “1” = Flipped display



Note:1:MV转置功能设计只保证需要转置的图片在panel的有效显示区域内，转置后出现部分画面转出屏体的case设计不做特殊处理
2:其中MY/MX/MV/RGB为Dir，ML/RSMX/RSMY为DVS

Restriction	-

IDMOFF: Idle Mode Off (3800h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
38h	3800h	No Argument								Idle Mode off
Description		This command is used to recover from idle mode on. In the idle off mode, display panel can display maximum 16.7M colors.								
Restriction		This command has no effect when module is already in Idle Off Mode.								

IDMON: Idle mode On (3900h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
39h	3900h	No Argument								Idle Mode on

Description

This command is used to enter into Idle mode on.
In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G, and B, 8 color depth data is displayed.

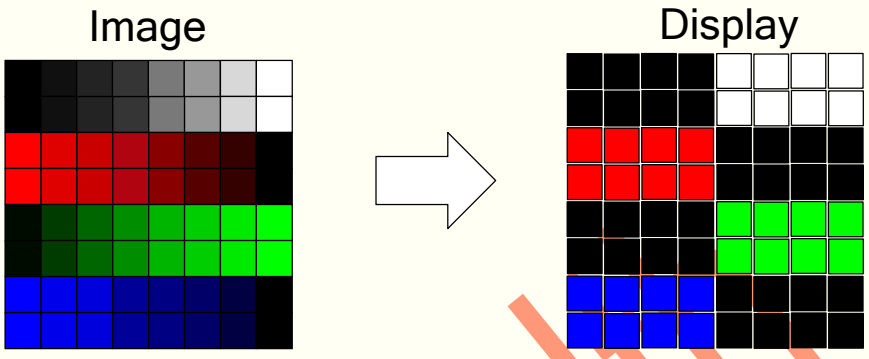


Image Contents VS. Display Colors			
	R7R6R5R4R3R2R1R0	G7G6G5G4G3G2G1G0	B7B6B5B4B3B2B1B0
Black	0XXXXXXX	0 XXXXXXX	0 XXXXXXX
Blue	0 XXXXXXX	0 XXXXXXX	1 XXXXXXX
Red	1 XXXXXXX	0 XXXXXXX	0 XXXXXXX
Magenta	1 XXXXXXX	0 XXXXXXX	1 XXXXXXX
Green	0 XXXXXXX	1 XXXXXXX	0 XXXXXXX
Cyan	0 XXXXXXX	1 XXXXXXX	1 XXXXXXX
Yellow	1 XXXXXXX	1 XXXXXXX	0 XXXXXXX
White	1 XXXXXXX	1 XXXXXXX	1 XXXXXXX

Restriction	This command has no effect when module is already in Idle On Mode.

IPF: Interface Pixel Format(3A00h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
3Ah	3A00h	-	-	-	-	-	IFPF[2:0]			07h

Description

This command sets the pixel format for the RGB image data used by the interface.
IFPF[2:0] : Pixel Format Definition.
If not used DPI interface, then the corresponding bits in the parameter are ignored.

IFPF[2:0]	Control Interface Color Format
001	SPI 1-1-1
010	SPI 8bit/pixel(256 colors);SPI 3-3-2
011	SPI 8bit/pixel(256 colors);SPI 256Gray
101	16bit/pixel(65,536 colors)
110	18bit/pixel(262,144 colors)
111	24bit/pixel(16.7M colors)
Others	reserved

SPI 1-1-1

RGB 1-1-1 bit	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	0	0	0	0	0	0	0x2C for GRAM Write
1,2RAMD Data Write	1	x	x	P1[2]	P1[1]	P1[0]	P2[2]	P2[1]	P2[0]	1,2pixel Data Write
3,4RAMD Data Write	1	x	x	P3[2]	P3[1]	P3[0]	P4[2]	P4[1]	P4[0]	3,4pixel Data Write
5,6RAMD Data Write	1	x	x	P5[2]	P5[1]	P5[0]	P6[2]	P6[1]	P6[0]	5,6pixel Data Write
So on…										

RGB 1-1-1 bit	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	0	0	0	0	0	0	0x2C for GRAM Write
1,2RAMD Data Write	1	x	P1[2]	P1[1]	P1[0]	x	P2[2]	P2[1]	P2[0]	1,2pixel Data Write
3,4RAMD Data Write	1	x	P3[2]	P3[1]	P3[0]	x	P4[2]	P4[1]	P4[0]	3,4pixel Data Write
5,6RAMD Data Write	1	x	P5[2]	P5[1]	P5[0]	x	P6[2]	P6[1]	P6[0]	5,6pixel Data Write
So on…										

RGB 1-1-1 bit	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	0	0	0	0	0	0	0x2C for

										GRAM Write
1,2RAMD Data Write	1	P1[3]	P1[2]	P1[1]	P1[0]	P2[3]	P2[2]	P2[1]	P2[0]	1,2pixel Data Write
3,4RAMD Data Write	1	P3[3]	P3[2]	P3[1]	P3[0]	P4[3]	P4[2]	P4[1]	P4[0]	3,4pixel Data Write
5,6RAMD Data Write	1	P5[3]	P5[2]	P5[1]	P5[0]	P6[3]	P6[2]	P6[1]	P6[0]	5,6pixel Data Write
So on…										

SPI 3-3-2

RGB 3-3-2 bit	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	0	0	0	0	0	0	0x2C for GRAM Write
1st RAMD Data Write	1	R1[2]	R1[1]	R1[0]	G1[2]	G1[1]	G1[0]	B1[1]	B1[0]	1st pixel Data Write
2st RAMD Data Write	1	R2[2]	R2[1]	R2[0]	G2[2]	G2[1]	G2[0]	B2[1]	B2[0]	2st pixel Data Write
3st RAMD Data Write	1	R3[2]	R3[1]	R3[0]	G3[2]	G3[1]	G3[0]	B3[1]	B3[0]	3st pixel Data Write
So on…										

SPI 3-3-2 SPI 256 Gray

RGB 3-3-2 bit	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	0	0	0	0	0	0	0x2C for GRAM Write
1st RAMD Data Write	1	P1[7]	P1[6]	P1[5]	P1[4]	P1[3]	P12]	P1[1]	P1[0]	1st pixel Data Write
2st RAMD Data Write	1	P2[7]	P2[6]	P2[5]	P2[4]	P2[3]	P2[2]	P2[1]	P2[0]	2st pixel Data Write
3st RAMD Data Write	1	P3[7]	P3[6]	P3[5]	P3[4]	P3[3]	P3[2]	P3[1]	P3[0]	3st pixel Data Write
So on…										

Restriction	-

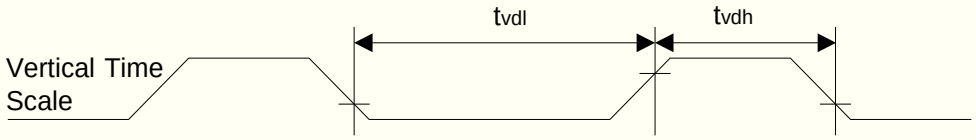
RAMWC: Write memory Continue (3Ch)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
3Ch	3C00h	D7	D6	D5	D4	D3	D2	D1	D0	Contents of memory is set randomly
	3C01h	D7	D6	D5	D4	D3	D2	D1	D0	
	3C02h	D7	D6	D5	D4	D3	D2	D1	D0	
	:	:	:	:	:	:	:	:	:	
Description		This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. Please use QSPI format to write image data. If MV(36h-B5) = 0: Data is written continuing from the pixel location after the write range of the previous RAMWR(2Ch) or RAMWRC(3Ch). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored. If MV(36h-B5) = 1: Data is written continuing from the pixel location after the write range of the previous RAMWR(2Ch) or RAMWRC(3Ch). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored. Frame Memory Access and Interface setting (B3h), WEMODE=0 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.								
Restriction		A Memory Write should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMWR(2Ch) and any following RAMWRC(3Ch) commands is written to undefined locations.								

RAMRDC: Memory Continuous Read (3Eh)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
3Eh	3E00h	D7	D6	D5	D4	D3	D2	D1	D0	Contents of memory is set randomly
	3E01h	D7	D6	D5	D4	D3	D2	D1	D0	
	3E02h	D7	D6	D5	D4	D3	D2	D1	D0	
	:	:	:	:	:	:	:	:	:	
Description		This command transfers image data from the display module's frame memory to the host processor starting at the pixel location specified by preceding CASET (2Ah) and RASET (2Bh) commands. If MV(36h-B5) = 0: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If MV(36h-B5) = 1: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.								
Restriction		There is no restriction on length of parameters.								

STESL: Set tearing effect scan line (4400h~4401h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
44h	4400h	N15	N14	N13	N12	N11	N10	N9	N8	00h
	4401h	N7	N6	N5	N4	N3	N2	N1	N0	00h
Description		This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N. The Tearing Effect Line On has parameter, which describes the mode of the Tearing Effect Output Line Mode. The Tearing Effect Output line consists of V-Blanking information only.  Note that STESL with N[15:0]="0000h" is equivalent to TEON with M="0" The Tearing Effect Output line shall be active low when the display module is in sleep in mode. This command takes effect on the frame following the current frame. Therefore, if the TE output is already on, the TE output shall continue to operate as programmed by the previous "TEON(35h)" or "STESL(44h) command" until the end of the frame.								
Restriction		-								

GSL: Get Scan Line (4500h~4501h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
45h	4500h	N15	N14	N13	N12	N11	N10	N9	N8	00h
	4501h	N7	N6	N5	N4	N3	N2	N1	N0	00h
Description		This command returns the current scan line, N, used to update the display module. The total number of scan lines on display is defined as VSYNC+VBP+VADR+VFP. The first scan line is defined as the first line of V Sync and is denoted as Line 0. When in Sleep in mode, the returned value is undefined.								
Restriction		-								

DSTBON: Deep Standby Mode On (4F00h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
4Fh	4F00h	-	-	-	-	-	-	-	DSTB	00h
Description		This command is used to enter deep standby mode. DSTB="1", enter deep standby mode. Notes: 1. Before setting this command, enter Sleep In Mode (10h) and Display Off (28h) first. User cannot write this register in Sleep-Out and Display-On mode. 2. It cannot exit Deep Standby Mode while setting bit DSTB from "1" to "0". 3. To exit Deep Standby Mode, input low pulse more than 1 msec to pin RSTB. 4. When Driver IC in Deep Standby Mode, the lane status of DSI must keep to LP-00.								
Restriction		-								

WDB: Write Display Brightness (5100h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
51h	5100h	DBV[7:0]								FFh
Description		This command is used to adjust brightness value. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.								
Restriction		-								

RDB: Read Display Brightness (5200h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
52h	5200h	DBV[7:0]								FFh
Description		This command is used to return the brightness value. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.								
Restriction		-								

HBMSEL: High Brightness Mode Selection (5300h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
53h	5300h	HBM_EN[7:0]								5Ah
Description		This command is used to select high brightness mode. HBM_EN:used to enable or disablehigh brightness mode.								
Restriction		-								

HBM_EN	Function
5Ah	Disable HBM
A5h	Enable HBM

RHBM: Read High Brightness Mode (5400h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
54h	5400h	HBM_EN[7:0]								5Ah
Description		This command is used to select high brightness mode. HBM_EN: the status of high brightness mode.								
Restriction		-								

HBM_EN	Function
5Ah	Disable HBM
A5h	Enable HBM

NEM: Emission Width for Normal Mode (5500h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>55h</td><td>5500h</td><td colspan="8">NOR_WIDTH[7:0]</td><td>05h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">This command is used to configure the emission for Normal mode.
NOR_WIDTH[7:0]: the initial EM width for idle mode.

<table>
<tr><th>NOR_WIDTH[7:0]</th><th>Function</th></tr>
<tr><td>00h</td><td>0 h-syncs</td></tr>
<tr><td>01h</td><td>1 h-syncs</td></tr>
<tr><td>02h</td><td>2 h-syncs</td></tr>
<tr><td>…</td><td>1 h-sync/step</td></tr>
<tr><td>05h</td><td>5 h-syncs</td></tr>
<tr><td>…</td><td>1 h-sync/step</td></tr>
<tr><td>FFh</td><td>255 h-syncs</td></tr>
</table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

Note:检测写动作，即写了此寄存器后，待DVS生效时，将55h寄存器值写入或将值的作用体现在GOA的STE信号

IEM: Emission Width for Idle mode (5600h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>56h</td><td>5600h</td><td colspan="8">IDLE_WIDTH[7:0]</td><td>05h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">This command is used to configure the emission for Idle mode.
IDLE_WIDTH[7:0]: the initial EM width for idle mode.

<table>
<tr><th>IDLE_WIDTH[7:0]</th><th>Function</th></tr>
<tr><td>00h</td><td>0 h-syncs</td></tr>
<tr><td>01h</td><td>1 h-syncs</td></tr>
<tr><td>02h</td><td>2 h-syncs</td></tr>
<tr><td>…</td><td>1 h-sync/step</td></tr>
<tr><td>05h</td><td>5 h-syncs</td></tr>
<tr><td>…</td><td>1 h-sync/step</td></tr>
<tr><td>FFh</td><td>255 h-syncs</td></tr>
</table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

Note:检测写动作，即写了此寄存器后，待DVS生效时，将56h寄存器值写入或将值的作用体现在GOA的STE信号上

HEM: Emission Width for HBM mode (5700h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>57h</td><td>5700h</td><td colspan="8">HBM_WIDTH[7:0]</td><td>05h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">This command is used to configure the emission for HBM mode.
HBM_WIDTH[7:0]: the initial EM width for HBM mode.

<table><tr><th>HBM_WIDTH[7:0]</th><th>Function</th></tr><tr><td>00h</td><td>0 h-syncs</td></tr><tr><td>01h</td><td>1 h-syncs</td></tr><tr><td>02h</td><td>2 h-syncs</td></tr><tr><td>…</td><td>1 h-sync/step</td></tr><tr><td>05h</td><td>5 h-syncs</td></tr><tr><td>…</td><td>1 h-sync/step</td></tr><tr><td>FFh</td><td>255 h-syncs</td></tr></table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

Note:检测写动作，即写了此寄存器后，待DVS生效时，将57h寄存器值写入或将值的作用体现在GOA的STE信号上

BACTR: Brightness Adjustment Control (6000h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>60h</td><td>6000h</td><td>EM_M</td><td>EM_DIM_EN</td><td>HMS_DIM_EN</td><td>IMS_DIM_EN</td><td>-</td><td>BC_LINEAR</td><td>BC_DIM_M</td><td>BC_DIM_EN</td><td>01h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">
This command is used to configure the dimming for 51h and mode switch.
BC_DIM_EN: enable or disable the 51h dimming.
<table>
<tr><th>BC_DIM_EN</th><th>Function</th></tr>
<tr><td>0</td><td>Disable 51h dimming</td></tr>
<tr><td>1</td><td>Enable 51h dimming</td></tr>
</table>
BC_DIM_M: set the 51h dimming mode.
<table>
<tr><th>BC_DIM_M</th><th>Function</th></tr>
<tr><td>0</td><td>fixed time</td></tr>
<tr><td>1</td><td>fixed step</td></tr>
</table>
BC_LINEAR: set the brightness curve trend.
<table>
<tr><th>BC_LINEAR</th><th>Function</th></tr>
<tr><td>0</td><td>2.2</td></tr>
<tr><td>1</td><td>1.0</td></tr>
</table>
IMS_DIM_EN/HBM_DIM_EN: enable or disable the dimming of mode switch.
<table>
<tr><th>IMS_DIM_EN/HMS_DIM_EN</th><th>Function</th></tr>
<tr><td>0</td><td>Disable mode switch dimming</td></tr>
<tr><td>1</td><td>Enable mode switch dimming</td></tr>
</table>
EM_DIM_EN: enable or disable the dimming for changing emission ratio.
<table>
<tr><th>EM_DIM_EN</th><th>Function</th></tr>
<tr><td>0</td><td>Disable change emission ratio dimming</td></tr>
<tr><td>1</td><td>Enable change emission ratio dimming</td></tr>
</table>
EM_M: select the mode of Emission width.
<table>
<tr><th>EM_M</th><th>Function</th></tr>
<tr><td>0</td><td>Reference emission width from STV1</td></tr>
<tr><td>1</td><td>Reference emission width from 55h</td></tr>
</table>
</td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

Note1: Idle和HBM dimming mode独立使能原因为：如果DGC调节Normal和Idle，高亮可能不调节DGC，通过STE实现；
Note2: BC_LINEAR通过Data Ratio查找表或51h设定的值转换为对应的Data Ratio实现线性1.0和2.2。
Note3: EM_DIM_EN控制的dimming参数详见Page4B1h寄存器

DECTR: Dynamic ELVSS Function Control (6200h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th colspan="2">D1 D0</th></tr>
<tr><td>62h</td><td>6200h</td><td>-</td><td>-</td><td>-</td><td>D_DIM_EN</td><td>-</td><td>IDLE_DELVSS_EN</td><td colspan="2">DELVSSM[1:0]</td><td>04h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">This command is used to select the dynamic elvss(VEN) level.
DELVSSM [1:0]: different level.
<table><tr><th>DELVSSM[1:0]</th><th>Function</th></tr><tr><td>00</td><td>Close Dynamic Elvss</td></tr><tr><td>01</td><td>Mode1</td></tr><tr><td>10</td><td>Mode2</td></tr><tr><td>11</td><td>Mode3</td></tr></table>
IDLE_DELVSS_EN: Enable or Disable Dynamic ELVSS function in idle mode.
<table><tr><th>IDLE_DELVSS_EN</th><th>Function</th></tr><tr><td>0</td><td>Close Dynamic ELVSS</td></tr><tr><td>1</td><td>Same to normal mode</td></tr></table>
D_DIM_EN: Enable or Disable Dynamic ELVSS Dimming function.
<table><tr><th>D_DIM_EN</th><th>Function</th></tr><tr><td>0</td><td>Dimming function disable</td></tr><tr><td>1</td><td>Dimming function enable</td></tr></table>
Note: Mode1: DBV+AVR ; Mode2:DBV ; Mode3:AVR</td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

SRECTR:Sunlight Readable Enhance Function Control (6300h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>63h</td><td>6300h</td><td>-</td><td>-</td><td>-</td><td>SRE_EN</td><td>-</td><td>-</td><td colspan="2">SRE_SIZE[1:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to set the SRE function.
SRE_EN: Sunlight Readable Enhance functions enable control.
<table>
<tr><th>SRE_EN</th><th>Function</th></tr>
<tr><td>0</td><td>SRE function disable</td></tr>
<tr><td>1</td><td>SRE function enable</td></tr>
</table>
SRE_SIZE[1:0]: Sunlight Readable Enhance function level set, while level0 is the lowest and level2 is the highest.
<table>
<tr><th>SRE_SIZE[1:0]</th><th>Function</th></tr>
<tr><td>00</td><td>SRE level0</td></tr>
<tr><td>01</td><td>SRE level1</td></tr>
<tr><td>10</td><td>SRE level2</td></tr>
<tr><td>11</td><td>SRE level0</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

GACMSET: Gamma Set and Color ModeSet (6400h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>64h</td><td>6400h</td><td>-</td><td>-</td><td colspan="2">GAM_HBM[1:0]</td><td colspan="2">GAM_IDLE[1:0]</td><td colspan="2">GAM_NOR[1:0]</td><td>00h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">This command is used to select the Gamma and Color Mode.
GAM_HBM[1:0]/ GAM_IDLE[1:0]/ GAM_NOR[1:0]: select the gamma for HBM/Idle/normal mode.

<table><tr><th>GAM_HBM[1:0]/ GAM_IDLE[1:0]/ GAM_NOR[1:0]</th><th>Gamma</th></tr><tr><td>00h</td><td>Gamma1</td></tr><tr><td>01h</td><td>Gamma2</td></tr><tr><td>10h</td><td>Gamma3</td></tr><tr><td>11h</td><td>Gamma1</td></tr></table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

SPIRDC:SPI read manufacture command control (6500h)

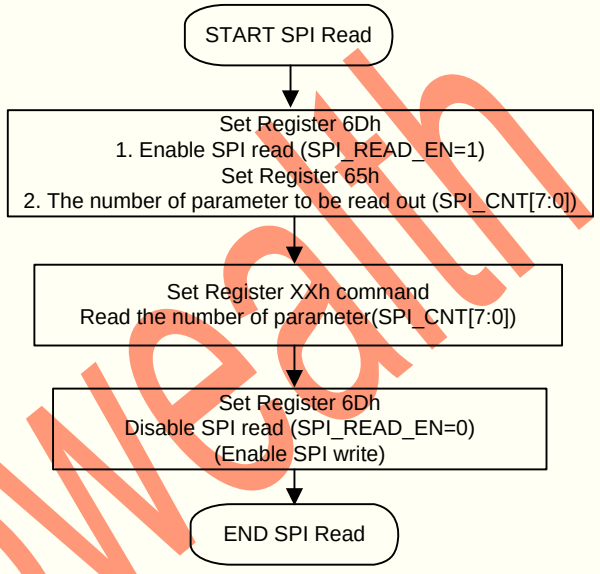
Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
65h	6500h	SPI_CNT[7:0]								00h

Description

This command is used to set the number of parameter to be read out from R/W command in SPI interface.
It must set SPI_READ_EN is enable(6Dh) before reading command.

SPI_CNT[7:0]	The number of parameter to be read out
00h	1
01h	2
:	:
FFh	256

SPI_CNT[7:0]: The number of parameter to be read out



Restriction	Note:65h only support SPI write

CICEN: Circular Edge Optimization Algorithm Enable(6700h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>67h</td><td>6700h</td><td>-</td><td>-</td><td colspan="2">UD_POS[1:0]</td><td>-</td><td>-</td><td>-</td><td>R_O_EN</td><td>00h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">R_O_EN:Out circular edge optimization algorithm enable.
<table>
<tr><th>R_O_EN</th><th>function</th></tr>
<tr><td>0</td><td>disable</td></tr>
<tr><td>1</td><td>enable</td></tr>
</table>
UD_POS[1:0]:The mode config of out circular.
<table>
<tr><th>UD_POS[1:0]</th><th>Mode config</th></tr>
<tr><td>00</td><td>Both big circle</td></tr>
<tr><td>01</td><td>UP big，Down small</td></tr>
<tr><td>10</td><td>UP small，Down big</td></tr>
<tr><td>11</td><td>Both small circle</td></tr>
</table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

OLOAEN: Oblique Line Optimization Algorithm Enable (6800h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
68h	6800h	-	-	OBL_Y	OBL_X	-	-	-	OBL_EN	01h

Description

OBL_EN：The Oblique Line Optimization Algorithm Enable.

OBL_EN	function
0	“0”=disable
1	“1”= enable

OBL_X/ OBL_Y:Mirror select.

OBL_X	OBL_Y	function
0	0	normal
1	0	X Mirror
0	1	Y Mirror
1	1	180 degreereversal

Restriction

NOTCHEN: Notch AlgorithmEnable(6900h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>69h</td><td>6900h</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>Notch_EN</td><td>00h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">Notch_EN:Notch algorithm enable.
<table>
<tr><th>Notch_EN</th><th>function</th></tr>
<tr><td>0</td><td>disable</td></tr>
<tr><td>1</td><td>enable</td></tr>
</table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9"></td></tr>
</table>

INCIREN: Inside CircularAlgorithmEnable(6A00h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
6Ah	6A00h	-	-	-	-	-	-	-	R_I_EN	00h
Description		R_I_EN:Inside circular edge optimization algorithm enable.								
Restriction										

R_I_EN	function
0	disable
1	enable

SWIREMANU: SWIRE manual control (6C00h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>6Ch</td><td>6C00h</td><td colspan="8">SMANU_CTL[7:0]</td><td>5Ah</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">SMANU_CTL [7:0]:SWIRE Manual control
<table><tr><th>SMANU_CTL[7:0]</th><th>SWIRE manual control</th></tr><tr><td>5Ah</td><td>ELVDD/ELVSS power Off</td></tr><tr><td>A5h</td><td>ELVDD/ELVSS power On</td></tr><tr><td>Others</td><td>ELVDD/ELVSS power Off</td></tr></table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

SPIRDC:SPI read manufacture command Enable (6D00h)

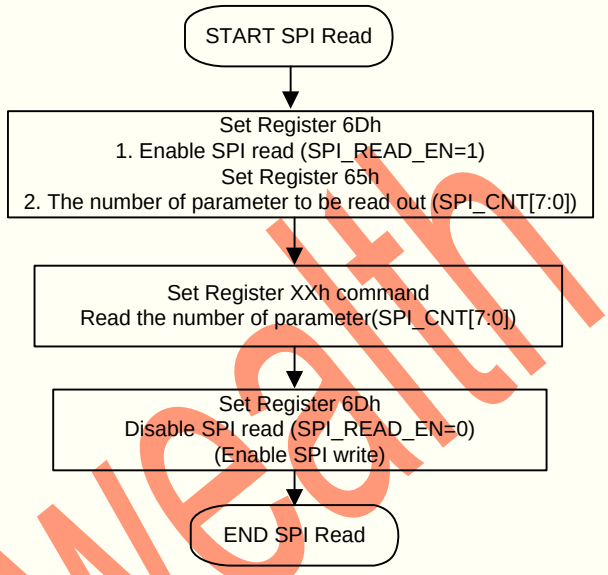
Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
6Dh	6D00h	-	-	-	-	-	-	-	SPI_READ_EN	00h

Description

This command is used to enable/disable SPI read R/W command
SPI_READ_EN: 8bit/9bit/Quad SPI read R/W command enable

SPI_READ_EN	Function
0	8bit/9bit/Quad SPI read R/W command Disable
1	8bit/9bit/Quad SPI read R/W command Enable

SPI_CNT[7:0]: The number of parameter to be read out



Restriction	Note:6Dh only support SPI write

RDID1: Read ID1 Value (DA00h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
DAh	DA00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	00h
Description		This read byte identifies the AMOLED module's manufacture ID.								
Restriction		-								

RDID2: Read ID2 Value (DB00h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
DBh	DB00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	80h
Description		This read byte is used to track the AMOLED module/driver version. It is defined by module maker and changes each time a revision is made to the display, material or construction specifications.								
Restriction		-								

RDID3: Read ID3 Value (DC00h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
DCh	DC00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	00h
Description		This read byte identifies the AMOLED module's manufacture ID.								
Restriction		-								

6 Interface

The CH13620 supports serial peripheral interfaces (SPI).
The interface type can be selected by setting IM1, IM0 pins as shown below:

Table Interface Type Selection

IM[1:0]	Display Data	Command
00	9 bit SPI	9 bit SPI
01	8 bit SPI	8 bit SPI
10	Quad-SPI	Quad-SPI
11	/	16 bit rising SPI

6.1 Serial Interface connect with Host

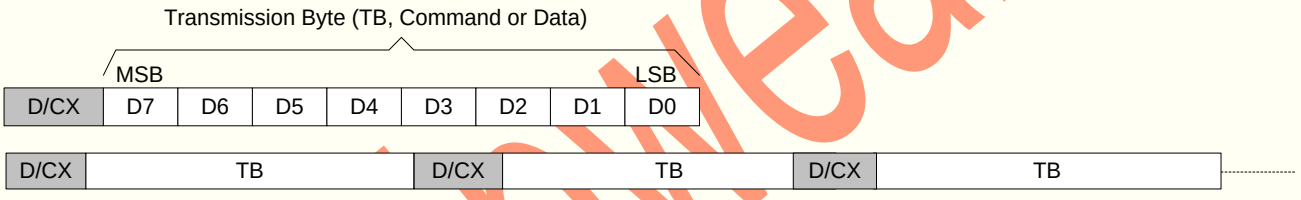
6.1.1 8/9 bit Serial Interface

The 8-bit SPI (4-pin) use CSB (chip select), DCX (data/command select), SCL (serial clock) and SDI/SDO (serial data input/output).
The 9-bit SPI (3-pin) use CSB, SCL and SDI/SDO. SCL is used for interface with MPU only, so it can be stopped when no communication is necessary. If the host places the SDI line into high-impedance state during the read intervals, then the SDI and SDO can be tied together.

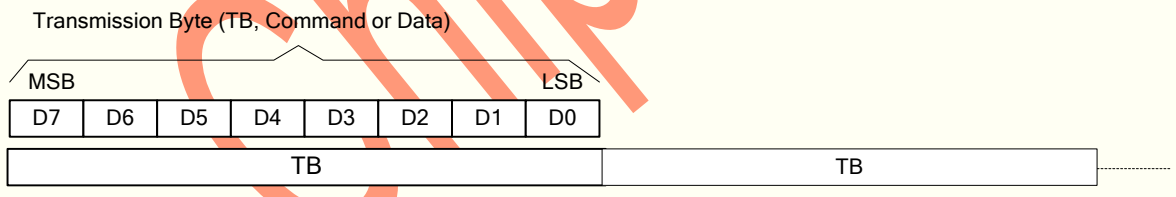
Write Mode

The write mode of the interface means the micro controller writes commands and data to the CH13620. 9-bit serial data packet contains a control bit D/CX and a transmission byte, in 8-bit serial case, data packet contains just transmission byte and control bit D/CX is transferred by D/CX pin. If D/CX is low, the transmission byte is interpreted as command byte. If D/CX is high, the transmission byte is stored in command register as parameter.
The MSB is transmitted first. The serial interface is initialized when CSB is high. In this state, SCL clock pulse or SDI/SDO data have no effect. A falling edge on CSB enables the serial interface and indicates the start of data transmission.

3 wire Serial Data Stream Format

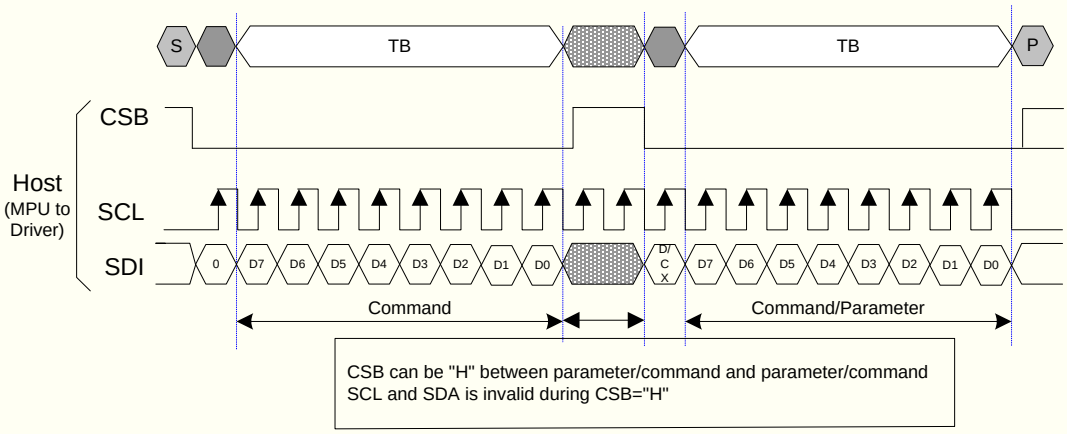


4 wire Serial Data Stream Format

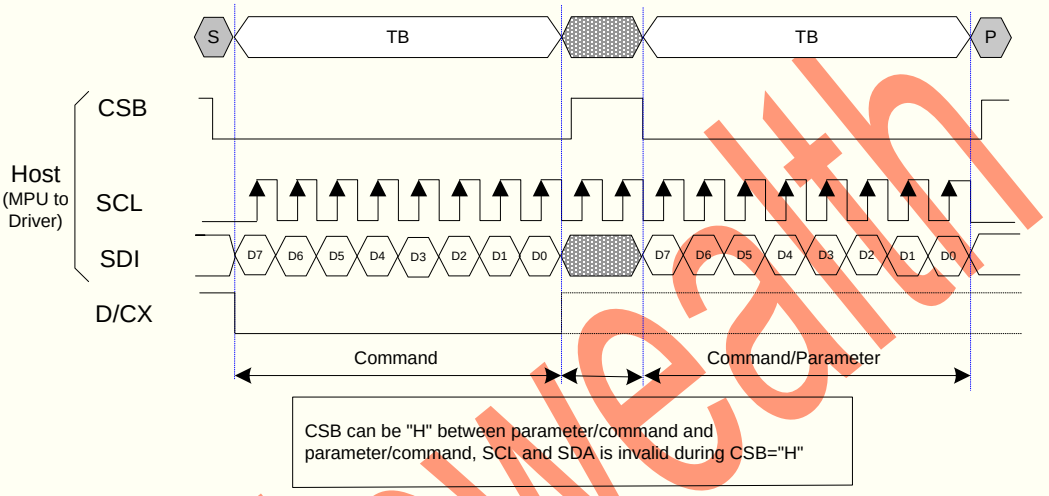


When CSB is high, SCL clock is ignored. During the high time of CSB the serial interface is initialized. At the falling CSB edge, SCL can be high or low (see below figure). SDI/SDO is sampled at the rising edge of SCL. D/CX indicates whether the byte is command code (D/CX=0) or parameter (D/CX=1). It is sampled when first rising SCL edge (3-line serial interface) or 8th rising SCLK edge (4-line serial interface). If CSB stays low after the last bit of command/data byte, the serial interface expects the D/CX bit (3-line serial interface) or D7 (4-line serial interface) of the next byte at the next rising edge of SCL.

1) 3-Pin Serial Interface Protocol for Register Write



2) 4-Pin Serial Interface Protocol for Register Write

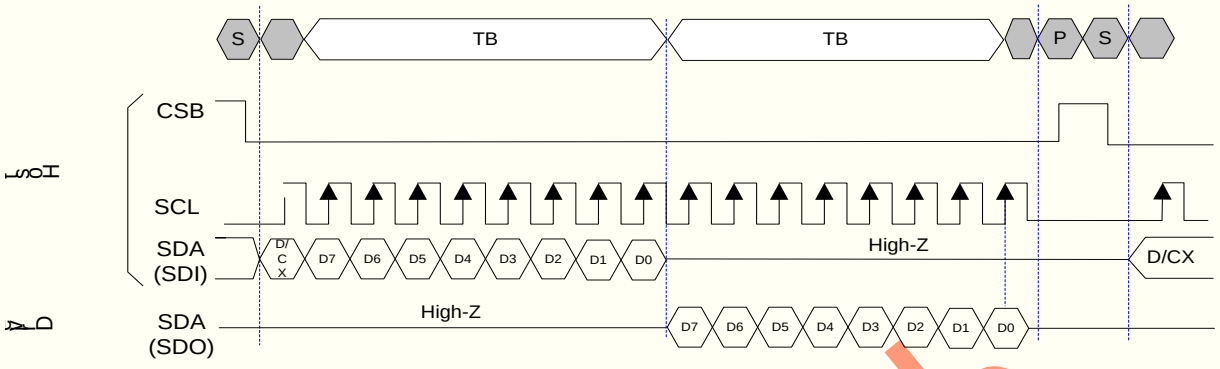


Serial bus protocol for register write mode

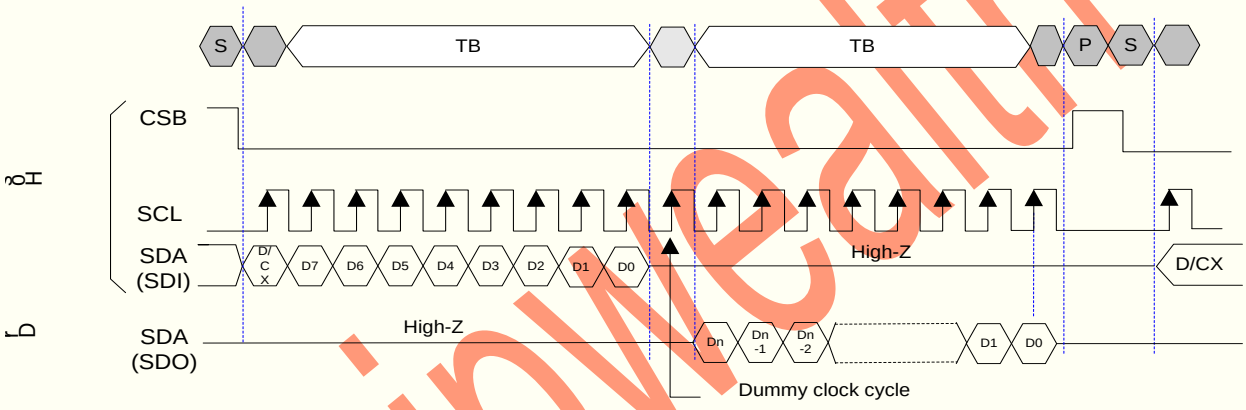
Read Mode

The read mode of the interface means that the micro controller reads register value from the CH13620. To do so the micro controller first has to send a command (Read ID or Read Register command) and then the following byte is transmitted in the opposite direction. After that CSB is required to go high before a new command is send. The CH13620 samples the SDI (input data) at the rising edges, but shifts SDO (output data) at the falling SCL edges. Thus the micro controller is supported to read data at the rising SCL edges. After the read status command has been sent, the SDI line must be set to tri-state no later than at the falling SCL edge of the last bit.

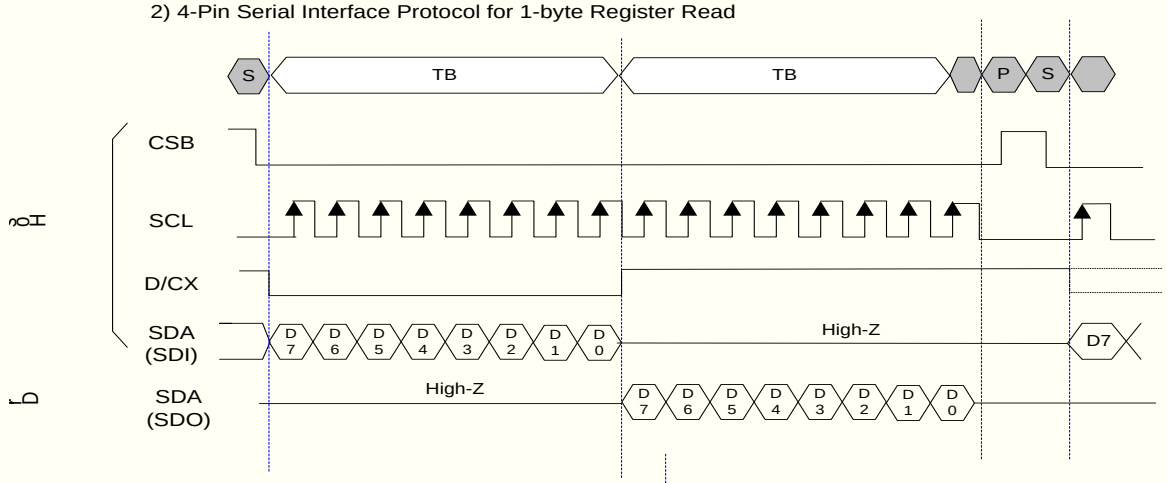
1) 3-Pin Serial Interface Protocol for 1-byte Register Read



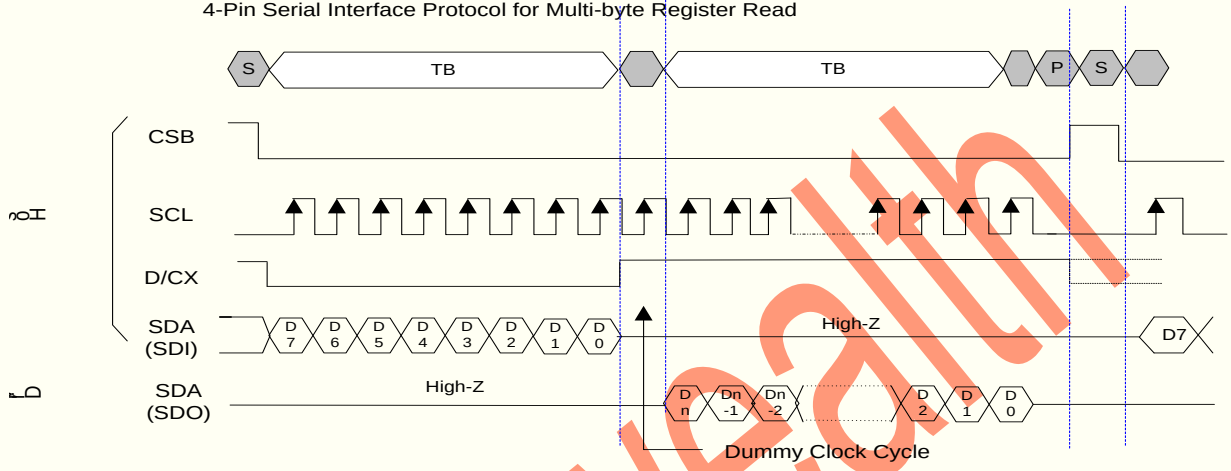
3-Pin Serial Interface Protocol for Multi-byte Register Read



2) 4-Pin Serial Interface Protocol for 1-byte Register Read



4-Pin Serial Interface Protocol for Multi-byte Register Read



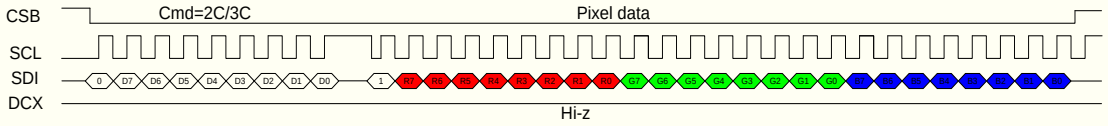
Serial bus protocol for register read mod

Dual-SPI Write RAM mode

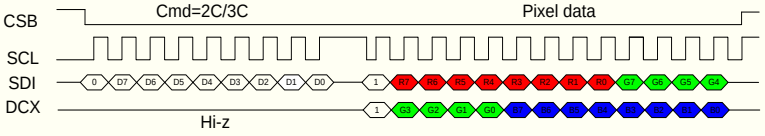
SPI_WRAM=1, Enable SPI Write RAM. DSPI_EN=1, Enable Dual-SPI interface. All 3-kinds of pixel format can be available during Dual-SPI interface (selected by the IPF command (3Ah): IFPF[2:0]).

SPI_WRAM	DSPI_EN	DSPI_CFG [1:0]	IM[1:0]	Pixel format
1	1	00:1P1T 1wire	00:9bit SPI	RGB888
				RGB666
				RGB565
			01:8bit SPI	RGB888
				RGB666
				RGB565
		01:1P1T 2wire	00:9bit SPI	RGB888
				RGB666
				RGB565
			01:8bit SPI	RGB888
				RGB666
				RGB565
		10:2P3T 2wire	00:9bit SPI	RGB888
				RGB666
			01:8bit SPI	RGB888
				RGB666
0	0	/	/	Not support write RAM

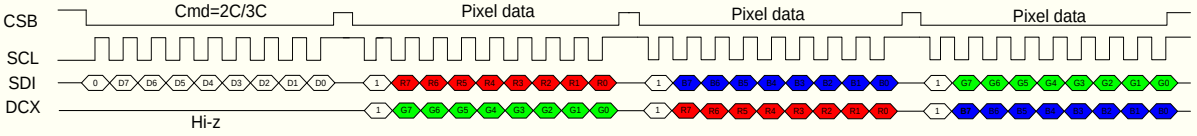
9bit-1P1T 1wire,RGB888



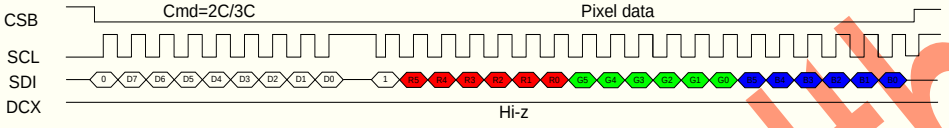
9bit-1P1T 2wire,RGB888



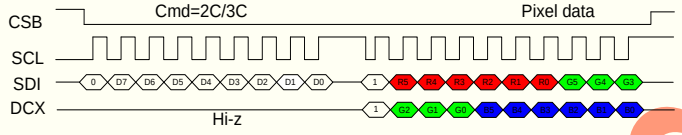
9bit-2P3T 2wire,RGB888



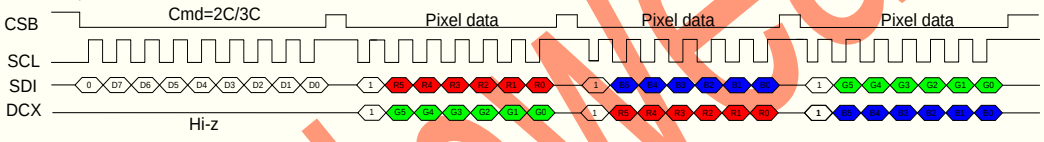
9bit-1P1T 1wire,RGB666



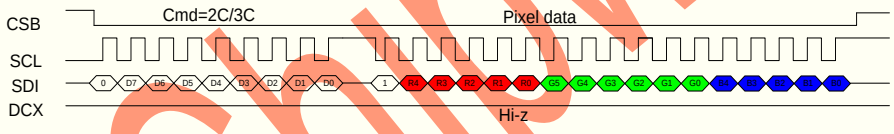
9bit-1P1T 2wire,RGB666



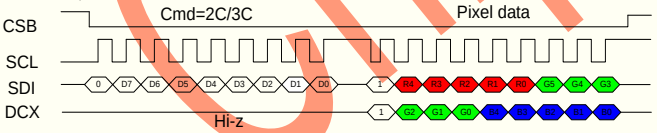
9bit-2P3T 2wire,RGB666



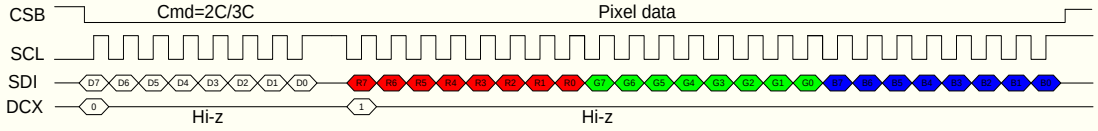
9bit-1P1T 1wire,RGB565



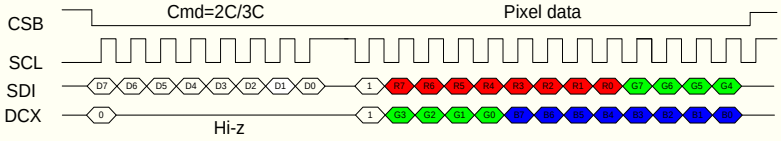
9bit-1P1T 2wire,RGB565



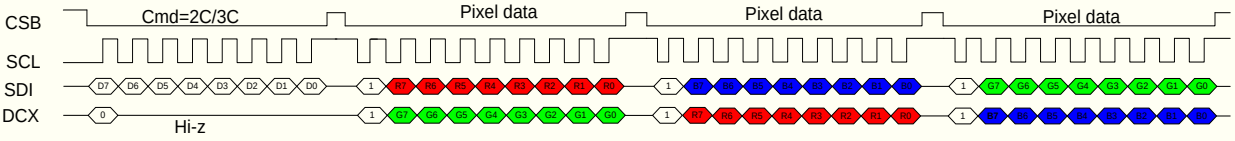
8bit-1P1T 1wire,RGB888



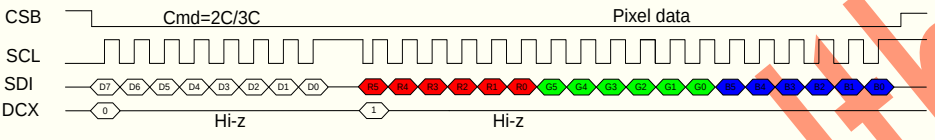
8bit-1P1T 2wire,RGB888



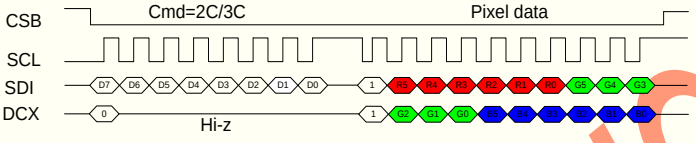
8bit-2P3T 2wire,RGB888



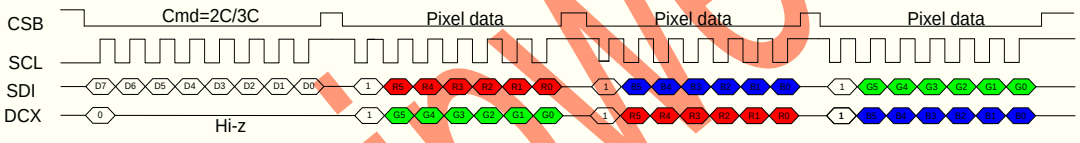
8bit-1P1T 1wire,RGB666



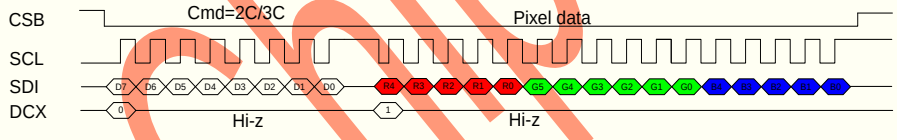
8bit-1P1T 2wire,RGB666



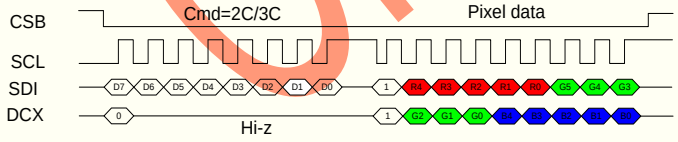
8bit-2P3T 2wire,RGB666



8bit-1P1T 1wire,RGB565



8bit-1P1T 2wire,RGB565



6.1.2 Quad-SPI Interface

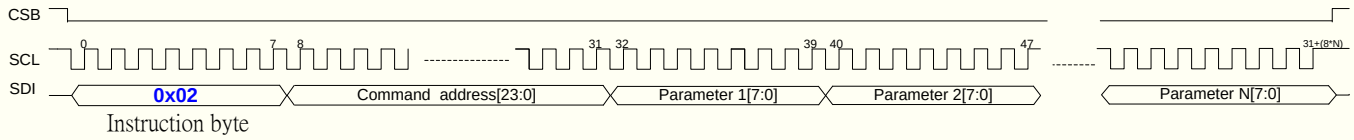
The Quad-SPI interface consists of CSB (chip select), SCL (serial clock), SDI / DCX / D0 / D1 (serial data input) and SDO (serial data output).

Quad-SPI Write mode

The write mode of the interface means the micro controller writes commands and data to the CH13620. Quad-SPI data packet contains an instruction byte. This byte specifies which type of data to be transferred.

Write Command Mode

QSPI Write Command – Instruction byte = 0x02 (Command – 1 wire / Parameter – 1 wire))

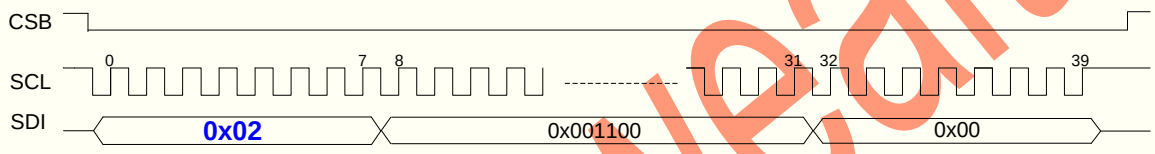


For example:

SLPOUT: Sleep Out (1100h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
11h	1100h	No argument								Sleep in mode

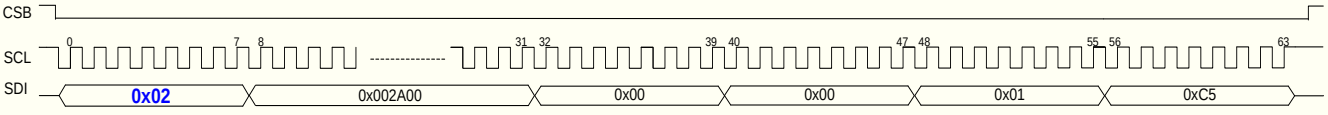
QSPI Write Command



CASET: Set Column Start Address (2A00h~2A03h)

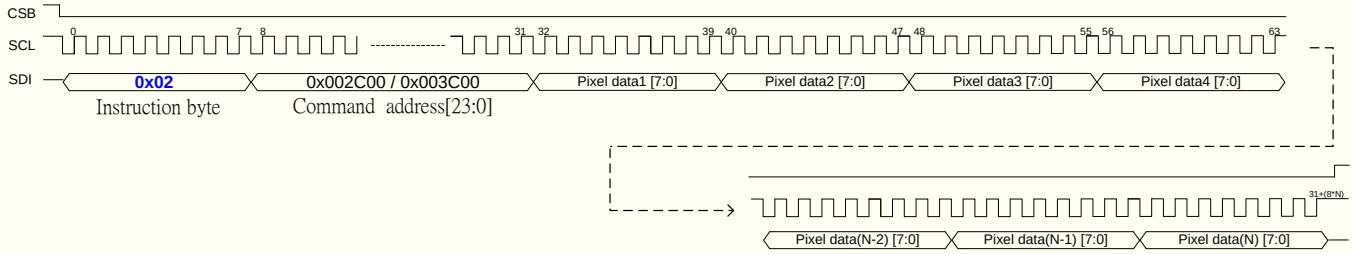
Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
2Ah	2A00h	-	-	-	-	-	-	-	SC8	00h
	2A01h	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	00h
	2A02h	-	-	-	-	-	-	-	EC8	01h
	2A03h	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	C5h

QSPI Write Command

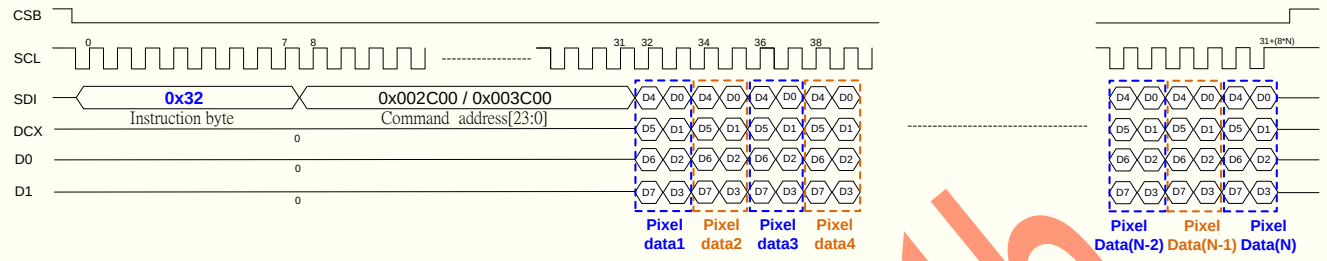


Write RAM mode

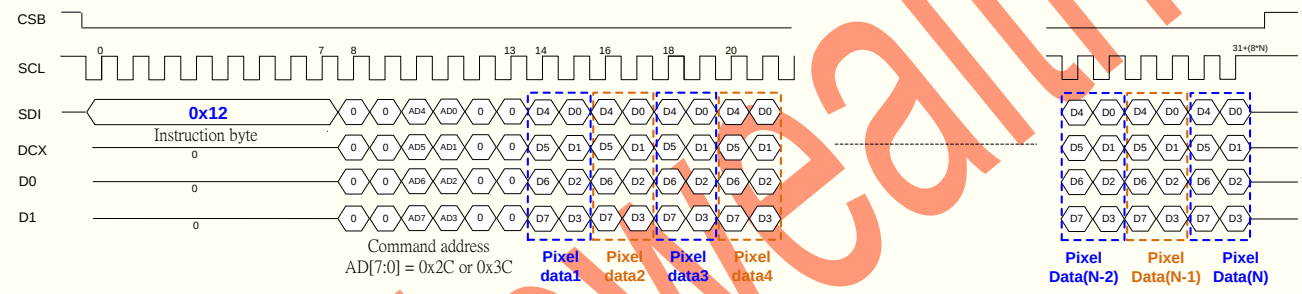
QSPI Write Ram – Instruction byte = 0x02 (Command – 1 wire / Data – 1 wire)



QSPI Write Ram – Instruction byte = 0x32 (Command – 1 wire / Data – 4 wire)



QSPI Write Ram – Instruction byte = 0x12 (Command – 4 wire / Data – 4 wire)



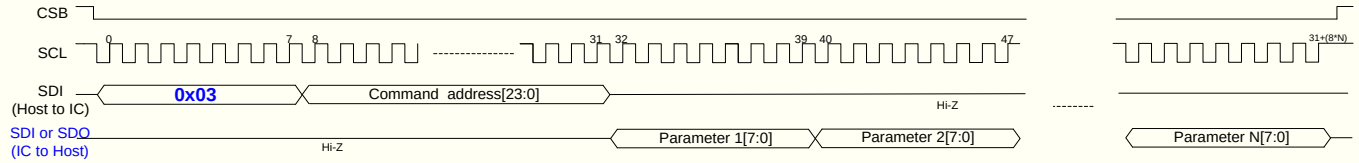
SPI_WRAM=1, Enable SPI Write RAM. IM[1:0]=10, Enable Quad-SPI interface. All 3-kinds of pixel format can be available during Quad-SPI interface (selected by the IPF command (3Ah): IFPF[2:0]).

SPI_WRAM	IM[1:0]	Pixel format
1	10: Quad-SPI	RGB888
		RGB666
		RGB565
		RGB332
		RGB111
		Gray256
0	/	Not support write RAM

Note. To avoid tearing effect, it is recommended to synchronize the TE signal when writing ram.

Quad-SPI Read Command/Ram – Instruction byte = 0x03

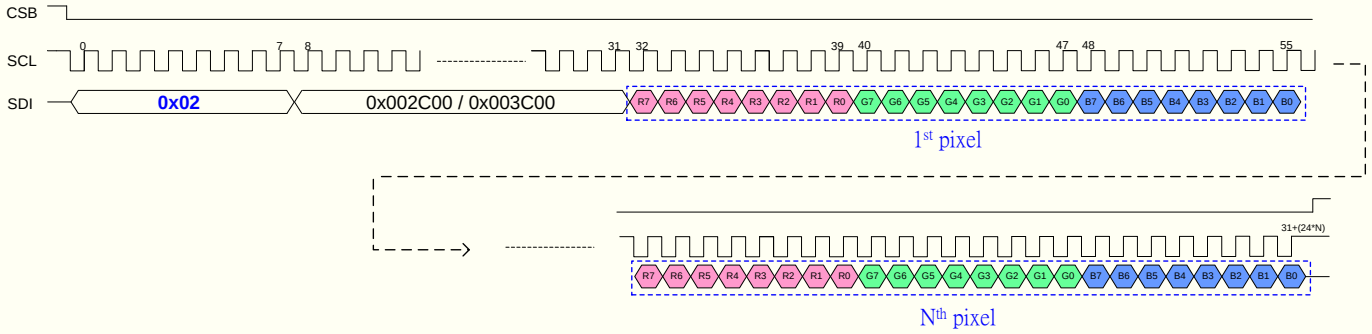
QSPI Read



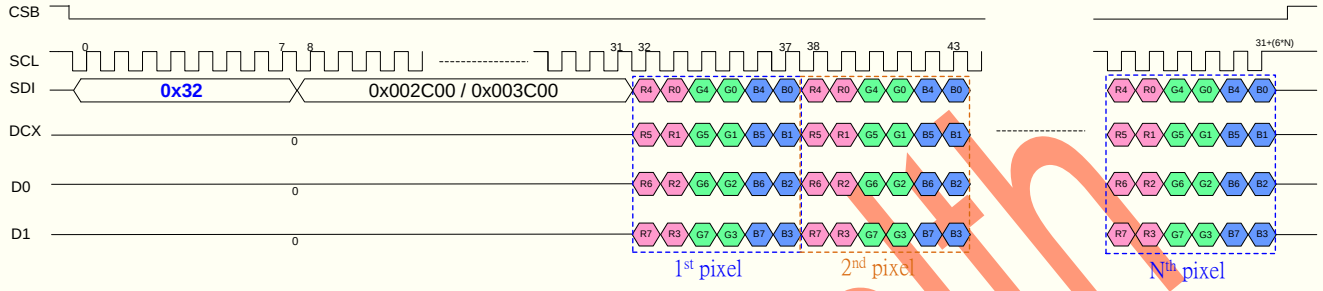
Note. The 1st read parameter is dummy packet in read ram.

Quad SPI – RGB888

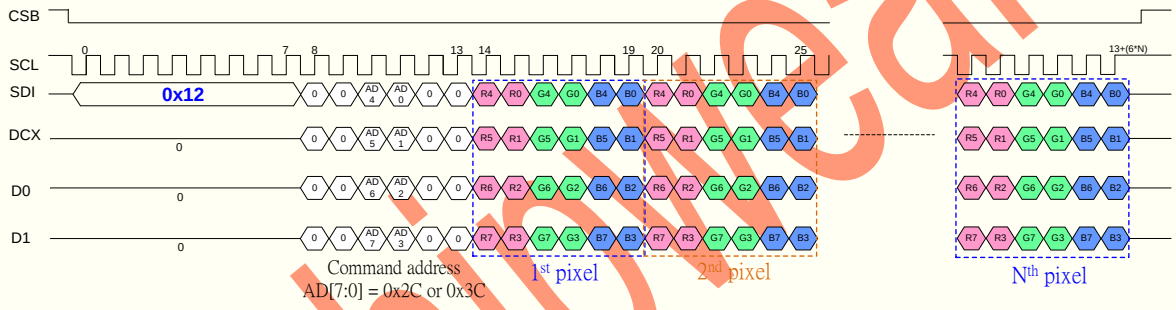
QSPI RGB888 – Instruction byte = 0x02



QSPI RGB888 – Instruction byte = 0x32

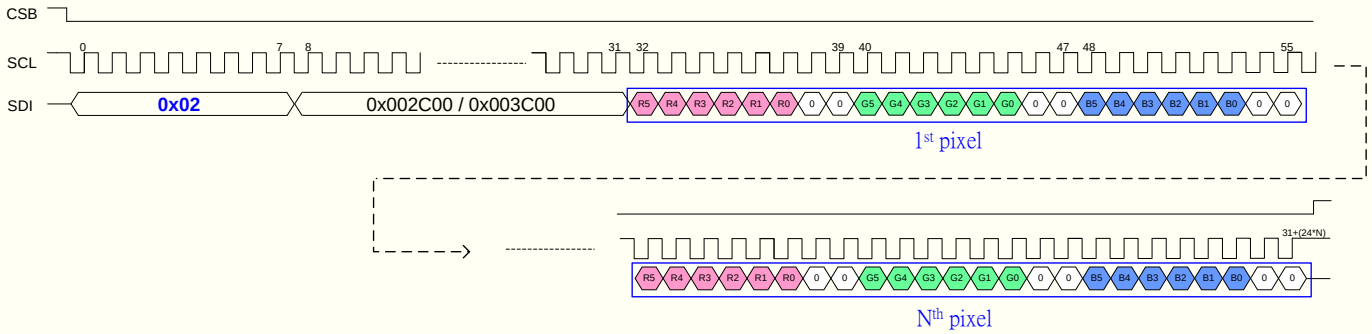


QSPI RGB888 – Instruction byte = 0x12

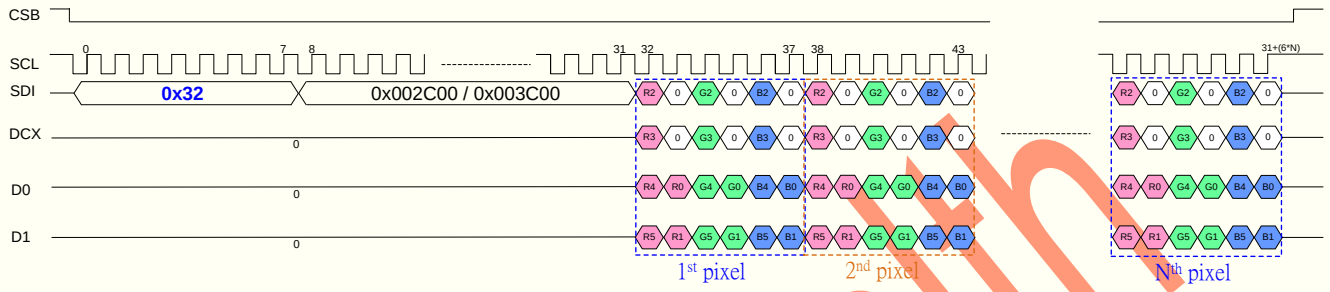


Quad SPI – RGB666

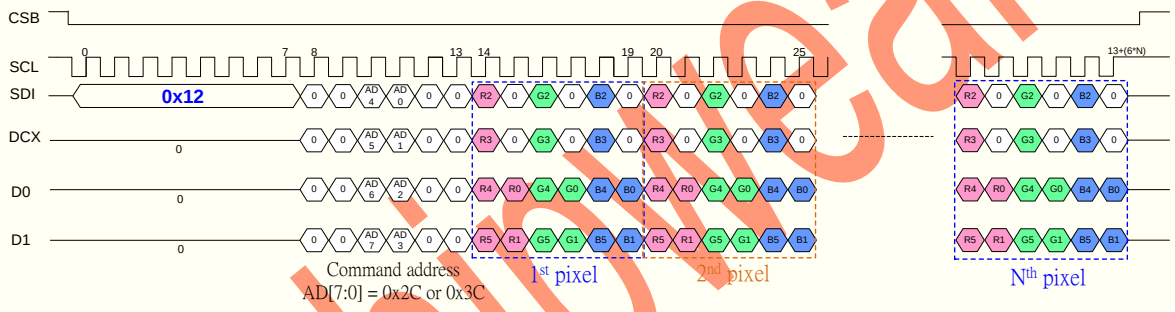
QSPI RGB666 – Instruction byte = 0x02



QSPI RGB666 – Instruction byte = 0x32

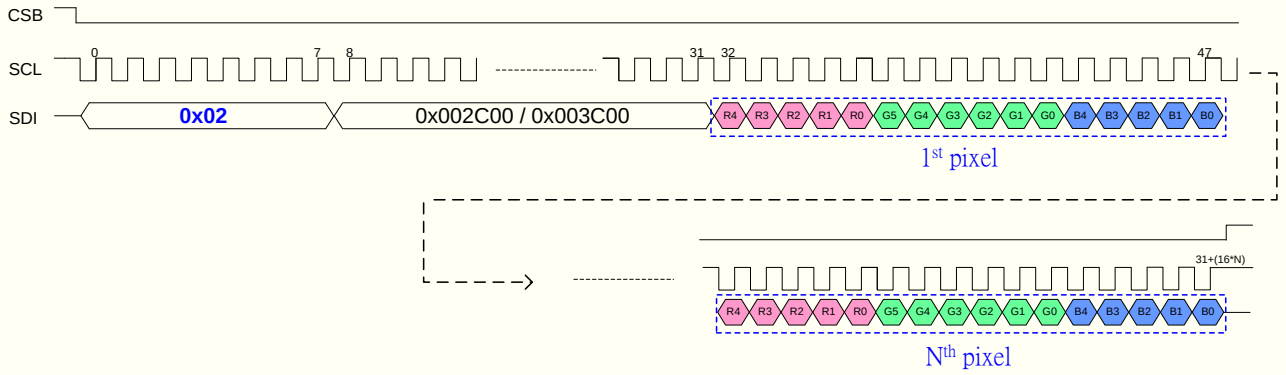


QSPI RGB666 – Instruction byte = 0x12

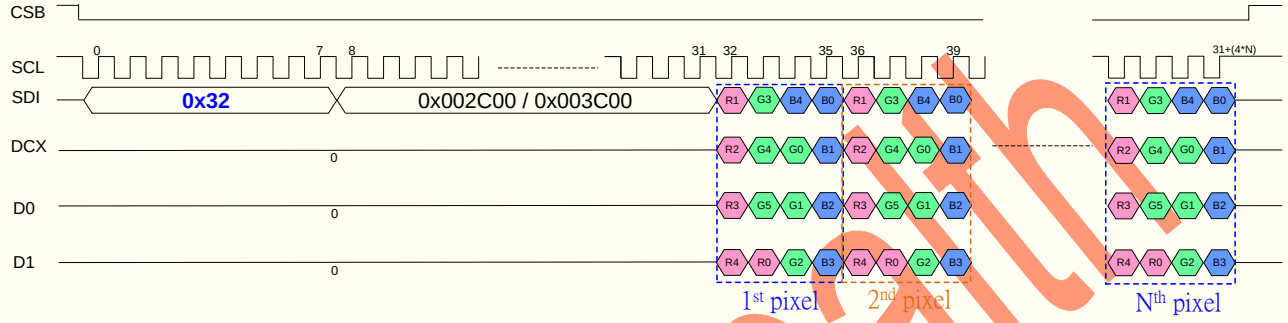


Quad SPI – RGB565

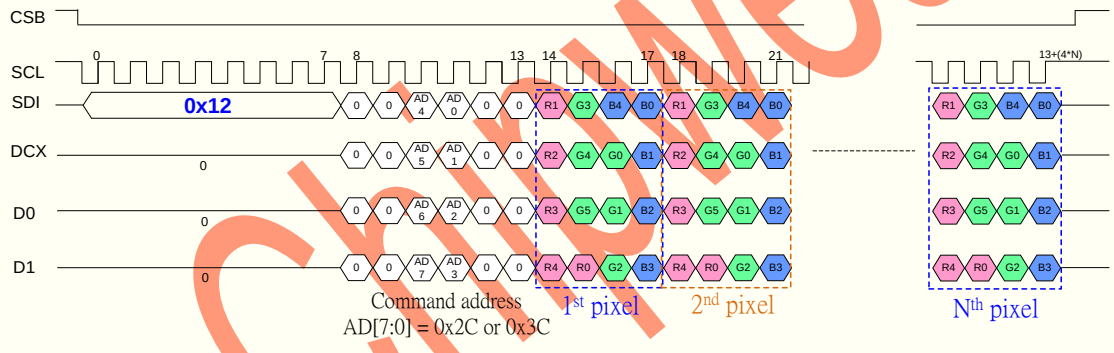
QSPI RGB565 – Instruction byte = 0x02



QSPI RGB565 – Instruction byte = 0x32

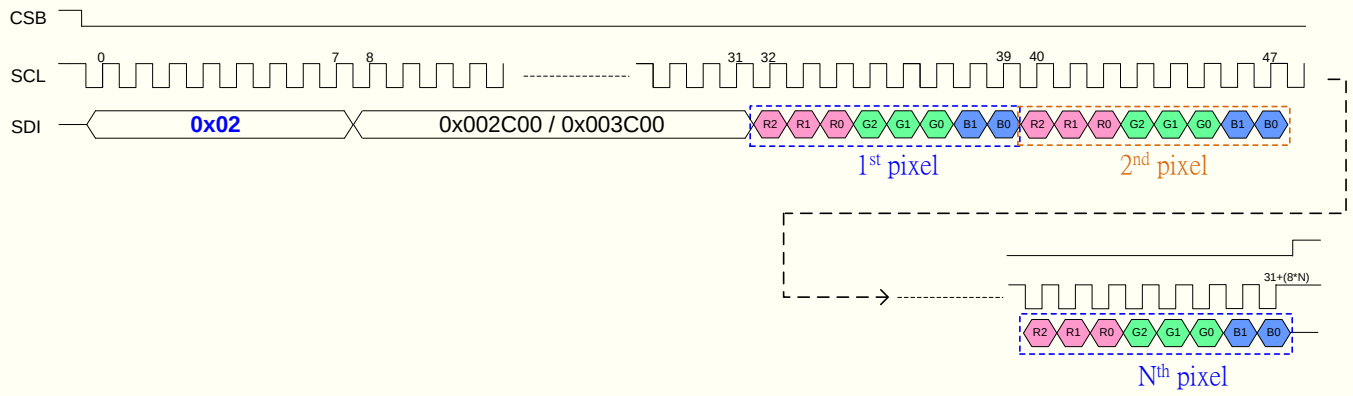


QSPI RGB565 – Instruction byte = 0x12

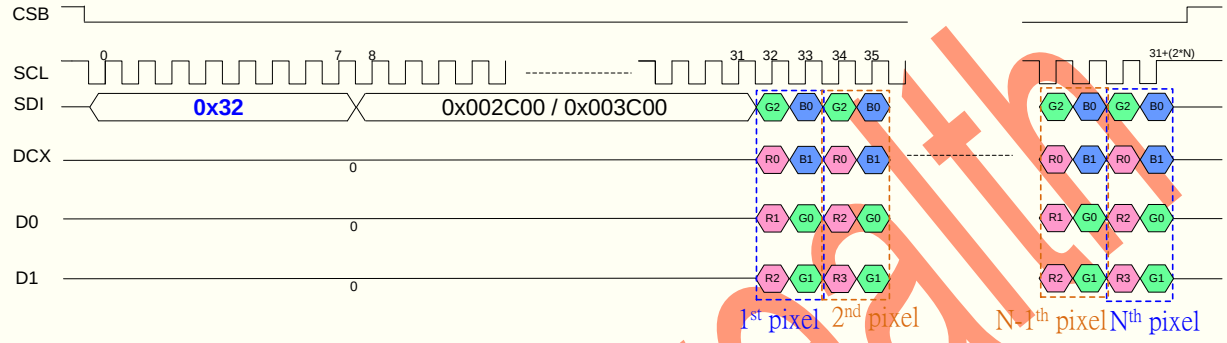


Quad SPI – RGB332

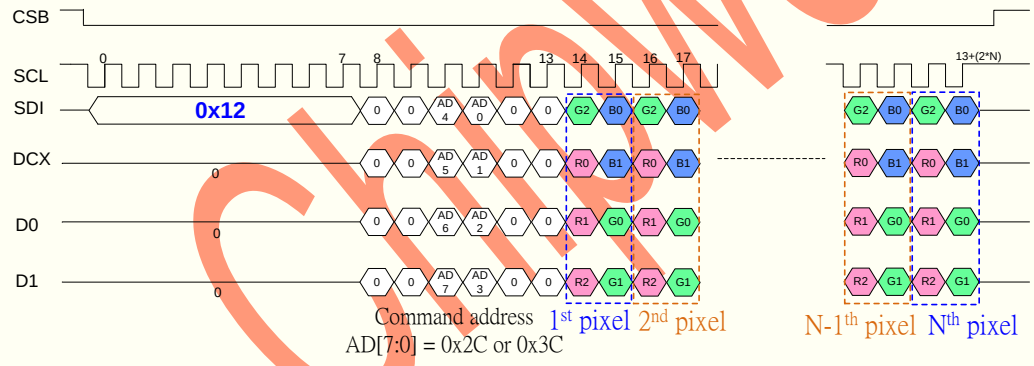
QSPI RGB332 – Instruction byte = 0x02



QSPI RGB332 – Instruction byte = 0x32

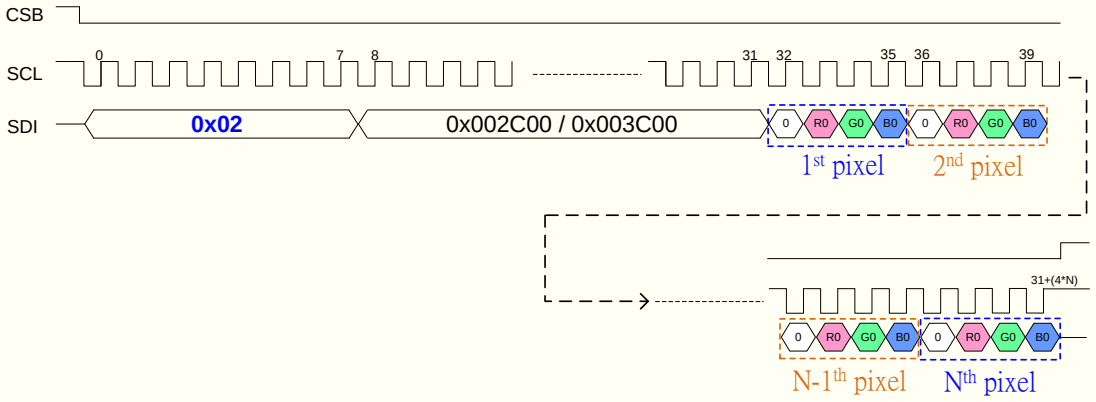


QSPI RGB332 – Instruction byte = 0x12

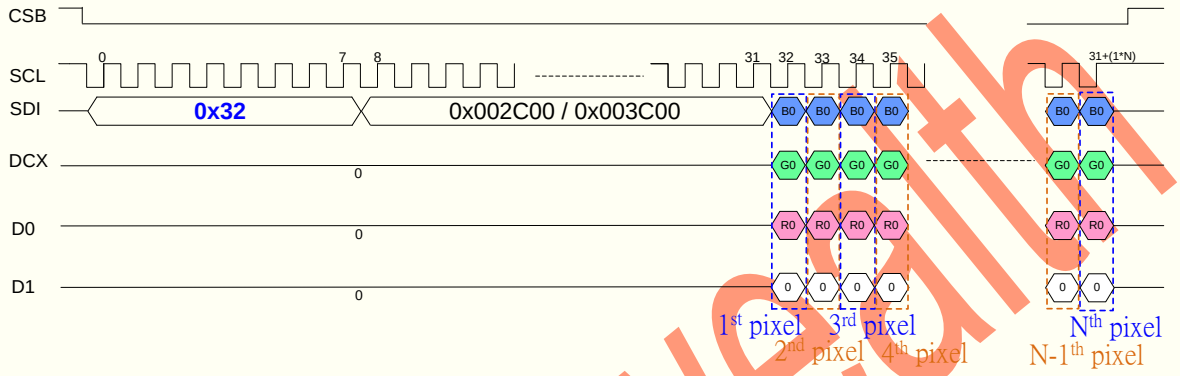


Quad SPI – RGB111

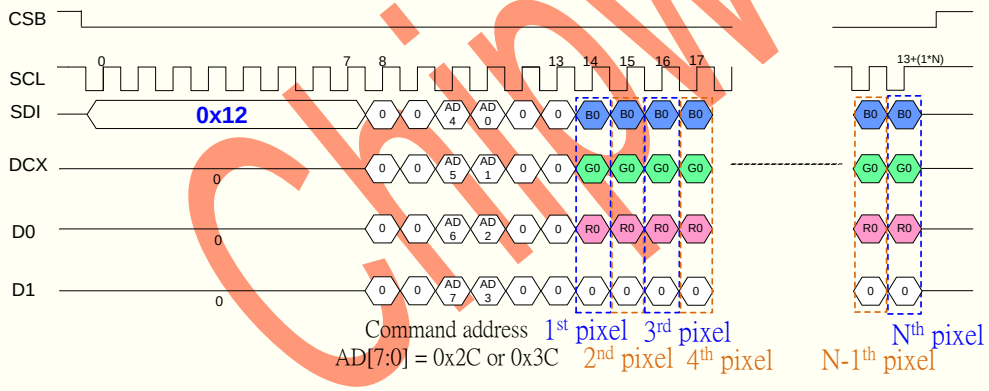
QSPI RGB111 – Instruction byte = 0x02



QSPI RGB111 – Instruction byte = 0x32

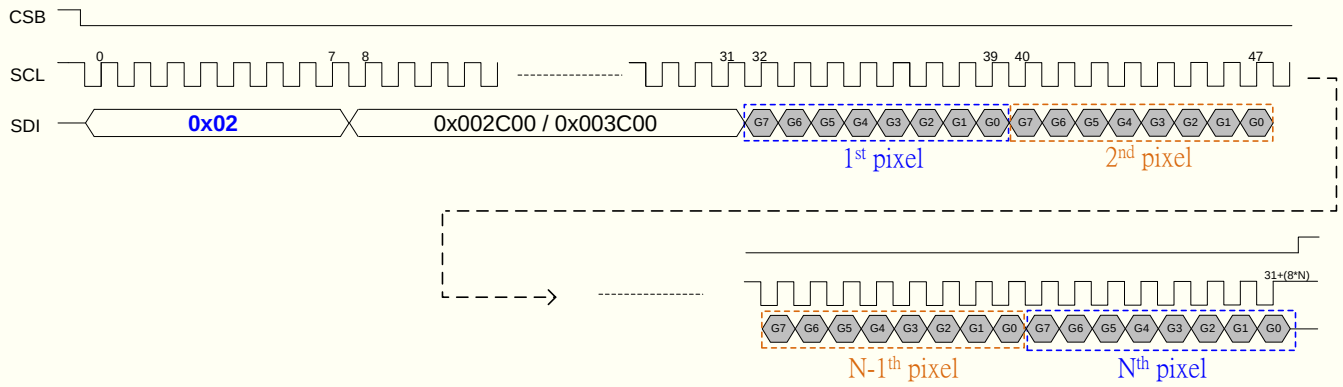


QSPI RGB111 – Instruction byte = 0x12

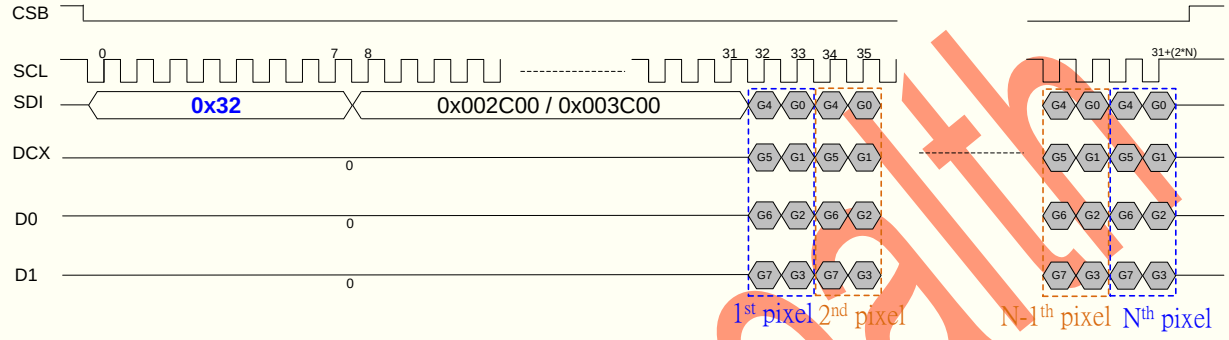


Quad SPI – Gray256

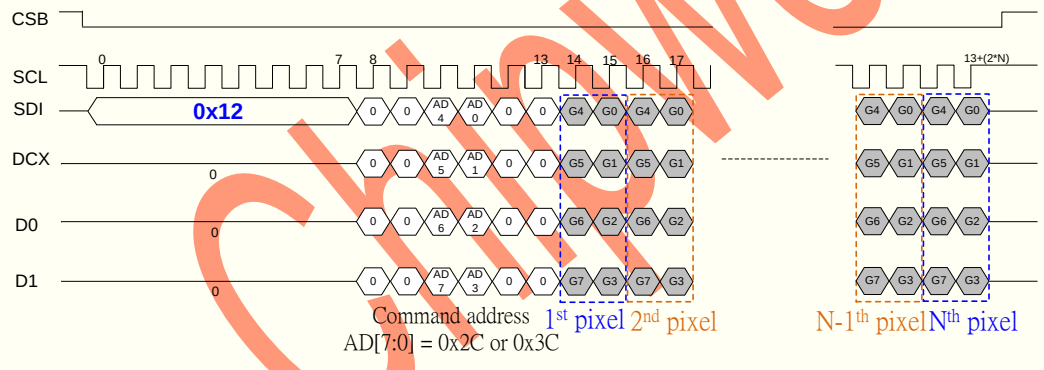
QSPI Gray256 – Instruction byte = 0x02



QSPI Gray256 – Instruction byte = 0x32

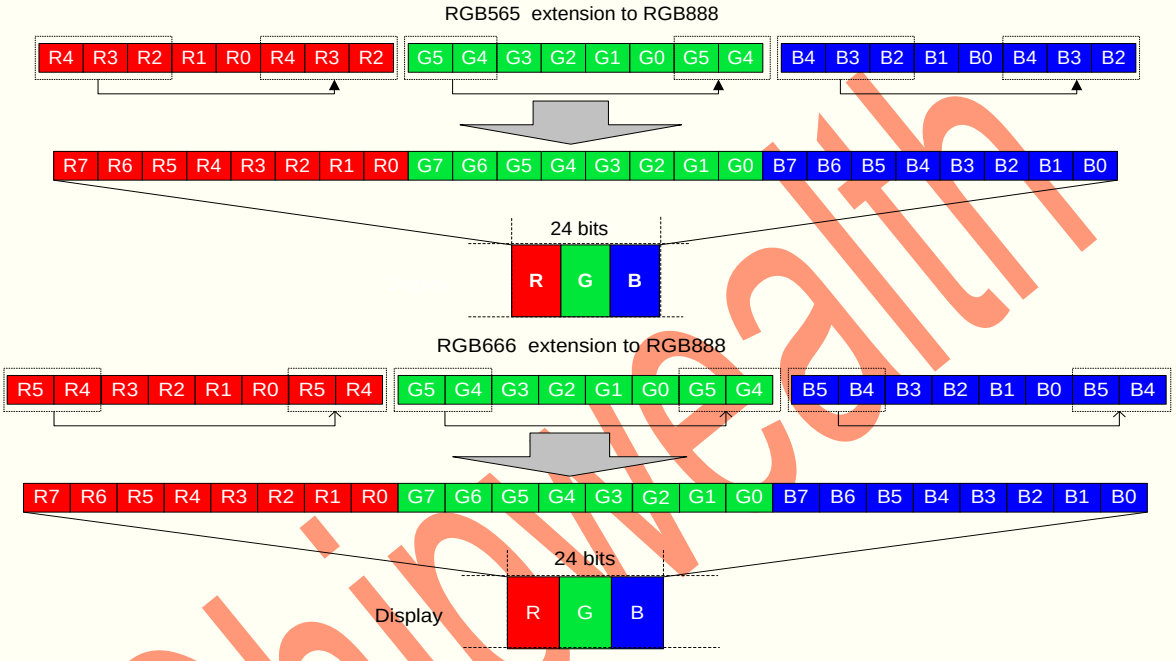


QSPI Gray256 – Instruction byte = 0x12



Quad-SPI support maximum frequency:

Quad SPI write/read		1-wire	4-wire
Write command		50 MHz	Not support
Write pixel data	RGB 888	50 MHz	50 MHz
	RGB 666	50 MHz	50 MHz
	RGB 565	50 MHz	50 MHz
	RGB 332	50 MHz	30 MHz
	RGB 111	50 MHz	15 MHz
	Gray 256	50 MHz	30 MHz
Read		10 MHz	Not support



6.1.3 16 bit Serial Interface

The serial interface can select IM[1:0] to decide the trigger edge is rising edge. The serial interface is used to communication between the micro controller and the driver chip. It contains CSB (chip select), SCL (serial clock), SDI (serial data input) and SDO (serial data output). Serial clock (SCL) is used for interface with MPU only, so it can be stopped when no communication is necessary. If the host places the SDI line into high-impedance state during the read intervals, then the SDI and SDO can be tied together.

Write Mode

The write mode of the interface means the micro controller writes commands and data to the IC. When CSB is high, SCL clock is ignored. During the high time of CSB the serial interface is initialized. At the falling CSB edge, SCL can be high or low. SDI/SDO is sampled at the rising(falling) edge of SCL. R/W indicates, whether the byte is read command (R/W = '1') or write command (R/W = '0'). It is sampled when first rising(falling) SCL edge. If CSB stays low after the last bit of command/data byte, the serial interface expects the R/W bit of the next byte at the next rising(falling) edge of SCL.

Serial bus protocol for register write mode

Read Mode

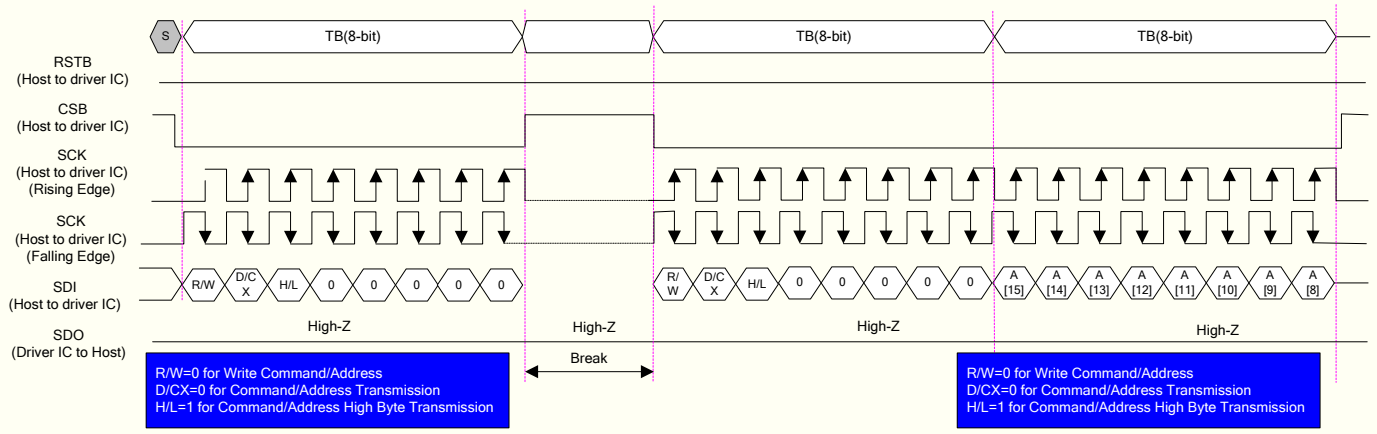
The read mode of the interface means that the micro controller reads register value from the IC. To do so the micro controller first has to send a command and then the following byte is transmitted in the opposite direction. After that CSB is required to go high before a new command is send. The IC samples the SDI (input data) at the rising(falling) edges, but shifts SDO (output data) at the falling(rising) SCL edges. Thus the micro controller is supported to read data at the rising(falling) SCL edges. After the read status command has been sent, the SDI line must be set to tri-state no later than at the falling SCL edge of the last bit. It doesn't need any dummy clock when execute the command data read.

Serial bus protocol for register read mode

6.2 Data transfer break and recovery

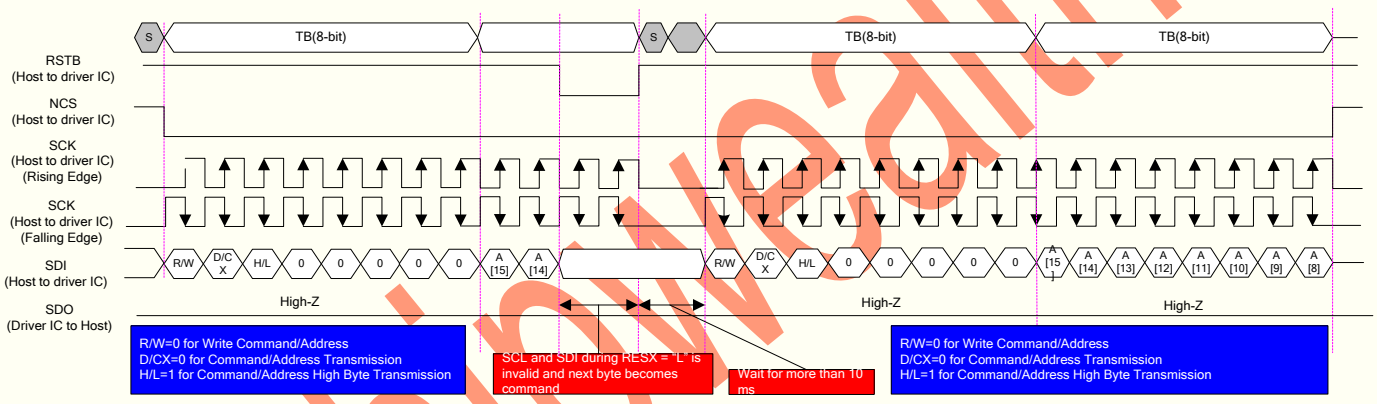
If there is a break in data transmission by CSB pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have Reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSB) is next activated after.

16-bit SPI



If there is a break in data transmission by RSTB pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have Reset the interface such that it will be ready to receive command data again when the chip select pin (CSB) is activated after RSTB have been in high state.

16-bit SPI



Serial bus protocol, write mode-interrupted by RSTB

6.3 Interface Pause

16-bit SPI Interface Pause
16-bit SPI interface does not support “Pause Mode”.

7 Function Description

7.1 Power On/Off Sequence

During power off, if AMOLED is in the Sleep Out mode, VDDA/VDDB/VDDIO/VDDR must be powered down minimum 5 frames after RSTB has been released.
During power off, if AMOLED is in the Sleep In mode, VDDA/VDDB/VDDIO/VDDR can be powered down minimum 0msec after RSTB has been released.
Notes:
1. There will be no damage to the display module if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
4. If RSTB line is not held stable by host during Power On Sequence as defined in section “power Level Mode”, then it will be necessary to apply a Hardware Reset (RSTB) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.
5. There is not a limit for Rise/Fall time on VDDA/VDDB/VDDIO/VDDR.
6. VDDA/VDDB/VDDIO/VDDR are applied and H/W Reset is not active (5ms is as same as the Reset Cancel Time).

Power on sequence

The Power on sequence has been applied following Fig1, otherwise correct functionality is not guaranteed.

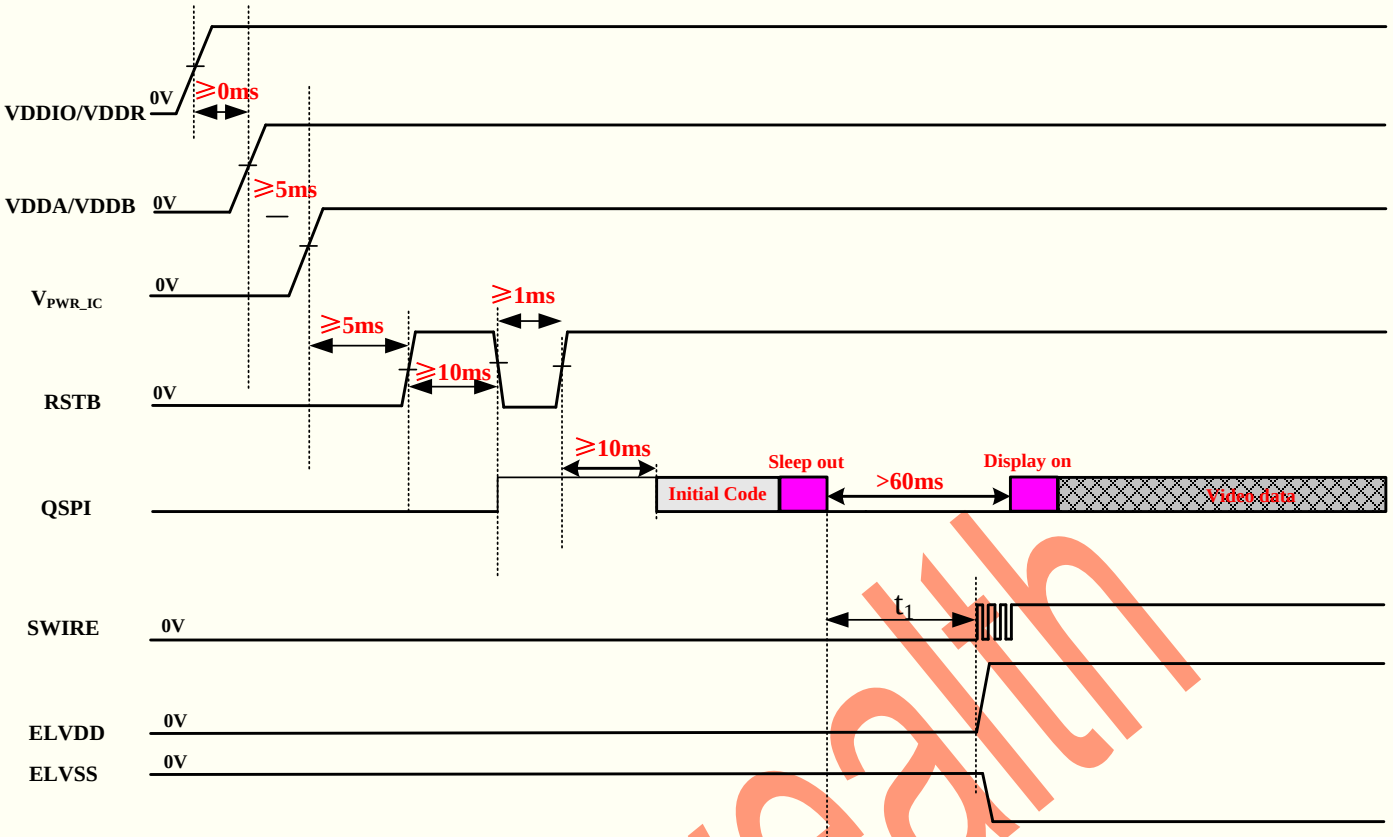


Fig 1 Power on sequence

Note1: t1 is ELVDD/ELVSS set up time, is controlled by SWIRE_ONF[5:0];
Note3: V_{PWR_IC} is the power of Power IC for ELVDD/ELVSS;

Power off sequence

The Power off sequence have been applied following Fig2, otherwise correct functionality is not guaranteed.

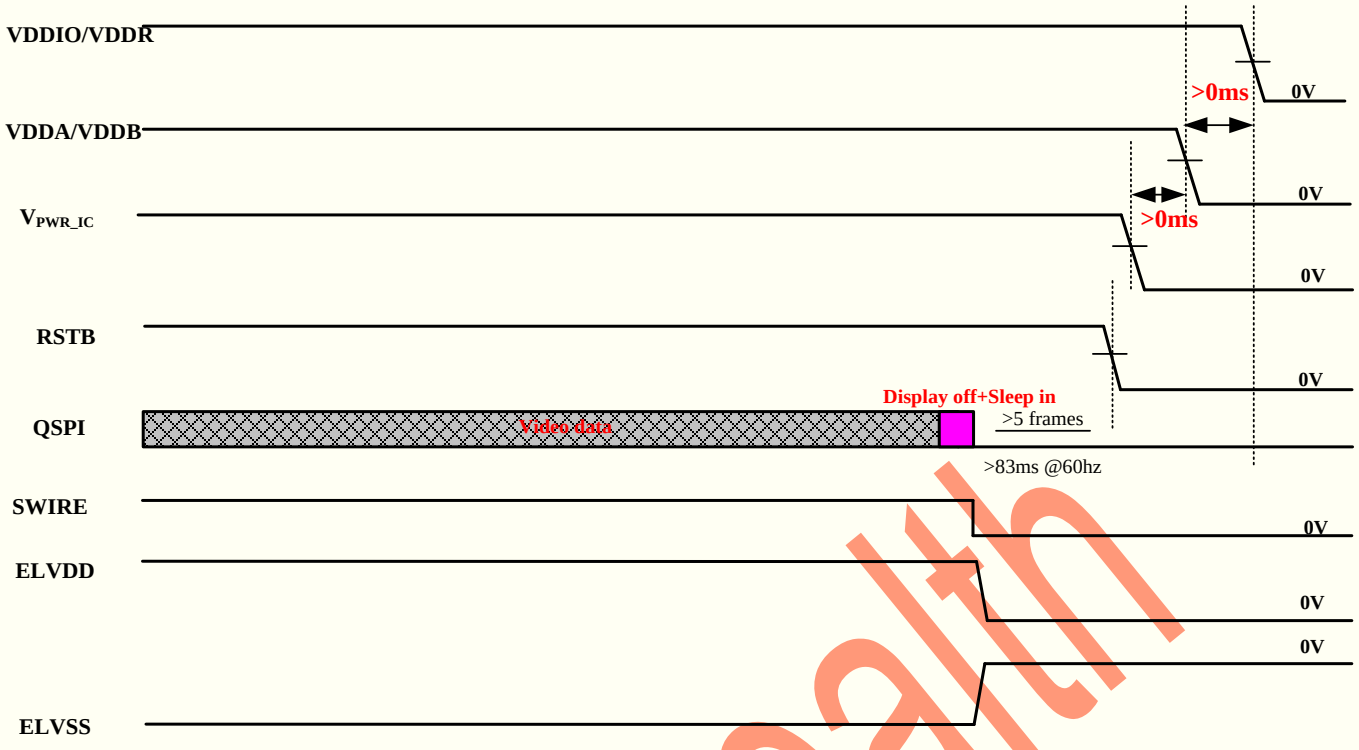


Fig 2 Power off sequence

Note1: V_{PWR_IC} is the power of Power IC for ELVDD/ELVSS;

Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until “Power On Sequence” powers it up.

7.2 Power Level Modes

Definition

Four level modes are defined they are in order of maximum power consumption to minimum power consumption:

Normal Mode On (full display), Sleep Out.
In this mode, the display is able to show maximum 16.7M colors.

Normal Mode On, Idle Mode On, Sleep Out
In this mode, the display is able to show maximum 16.7M colors (include 8 colors).

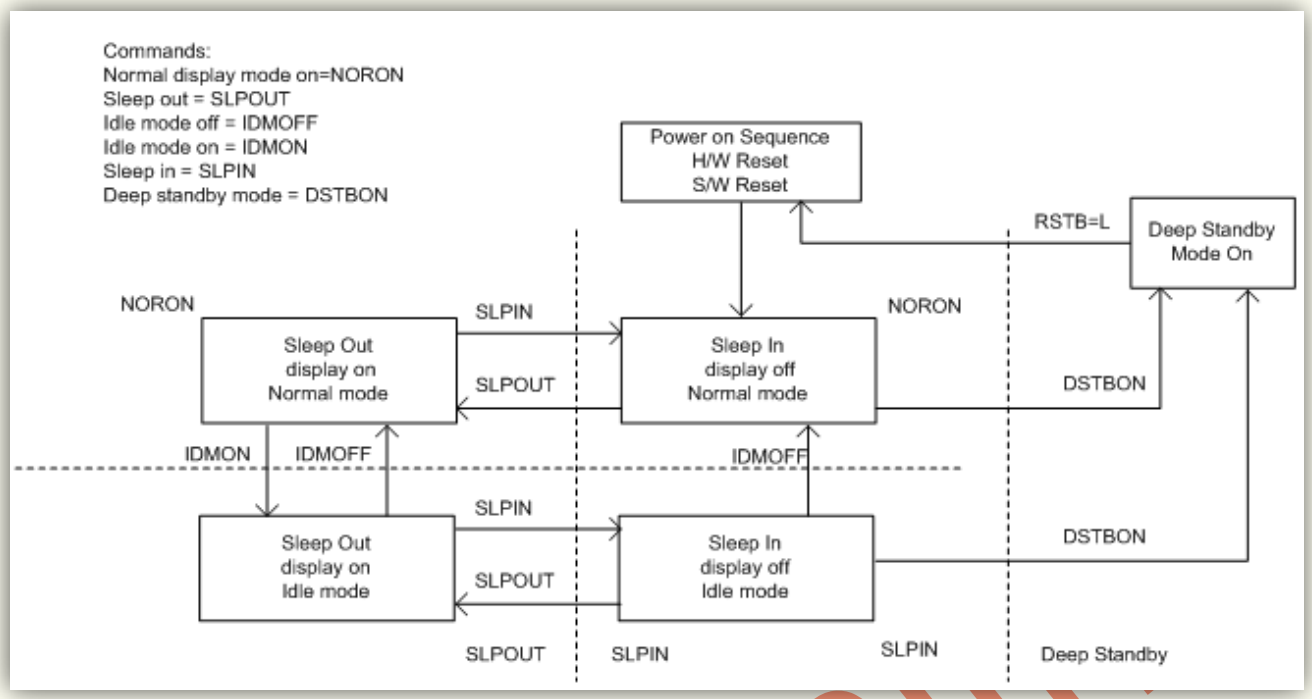
Sleep In Mode.
In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. Only the QSPI interface and registers are working with VDDIO power supply.

Deep Standby Mode.
In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. The QSPI interface and registers are not working.

Power Off Mode
In this mode, VDDIO/VDDR and VDDA/VDDB are removed.

NOTE: Mode 4 is entered for power saving with both power supplies for I/O and analog circuits and can be exited by hardware reset only (RSTB=L). Mode 4 is entered only when both power supplies for I/O and analog circuits are removed.

Power Level Mode Flow Chart



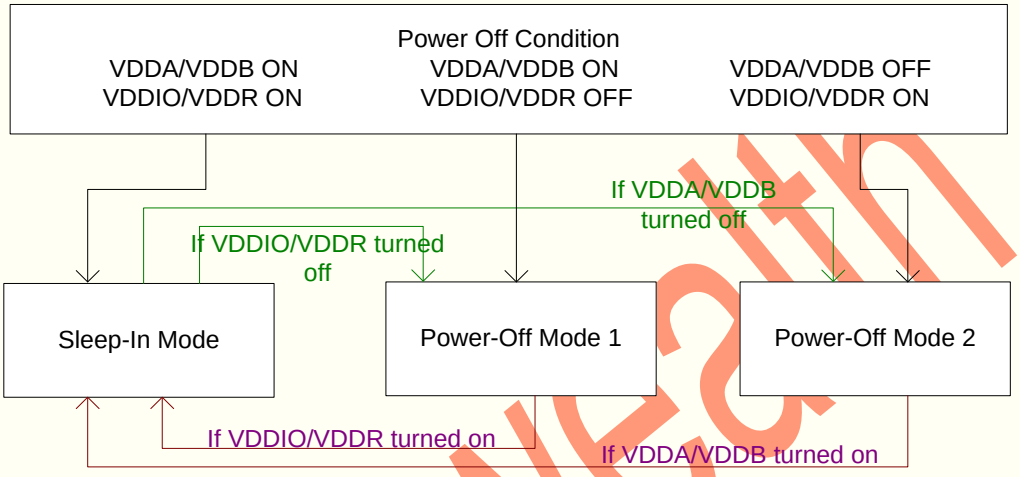
NOTES:
1) There is not any abnormal visual effect when there is changing from one power mode to another power mode.
2) There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode

The following table represents the registers its mode state.

Mode	Register	Control	
		Enter	Exit
Sleep in mode	Keep	Command	
Deep-standby mode	Loss	Command	RSTB pin
RSTB=L	Default Value	Reset(H/W)	

The condition for irregular power off mode is shown below:

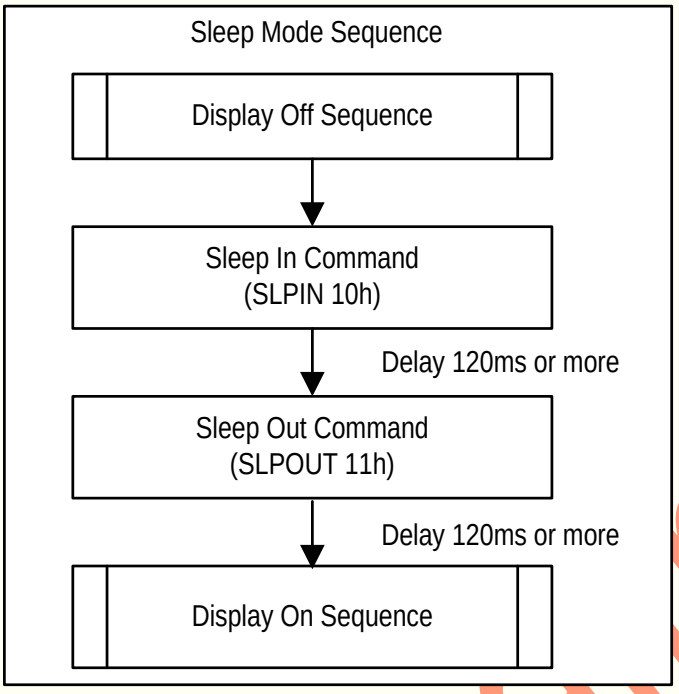
Power Off Mode	VDDA/VDDB	VDDIO/VDDR	RSTB	I/O
Mode 1	ON	OFF	H or L	L
Mode 2	OFF	ON	H or L	L



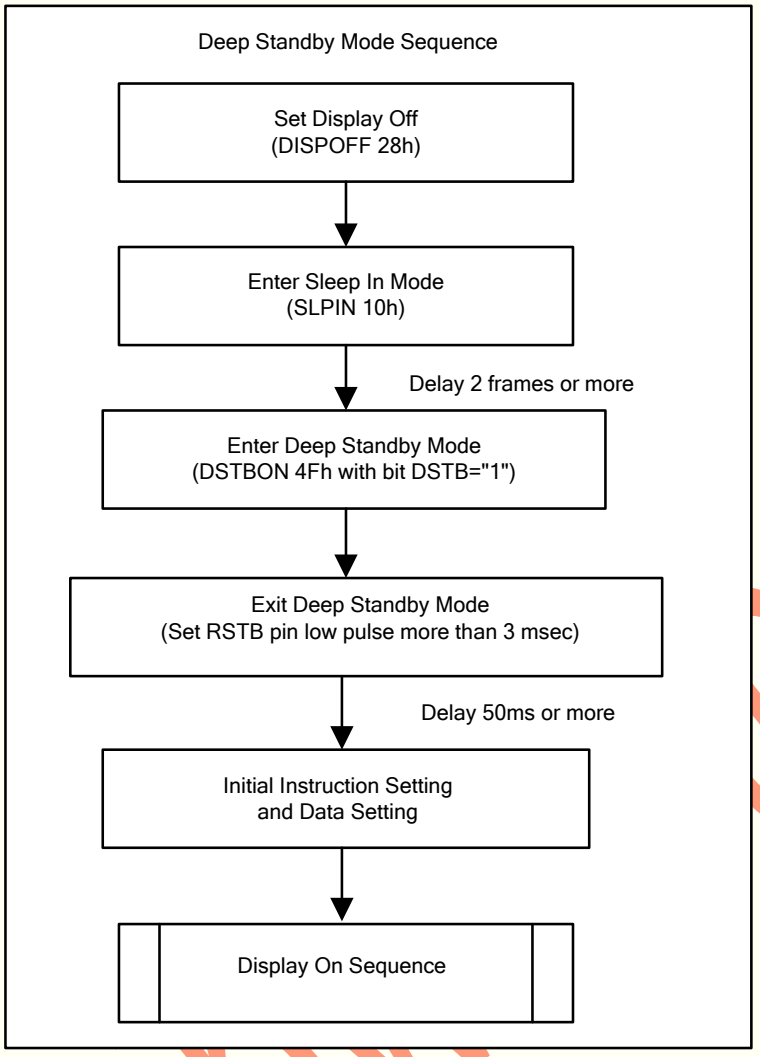
7.3 Instruction Setting Sequence

When setting instruction to the CH13620, the sequences shown in below figure must be followed to complete the instruction setting.

Sleep In/Out Sequence

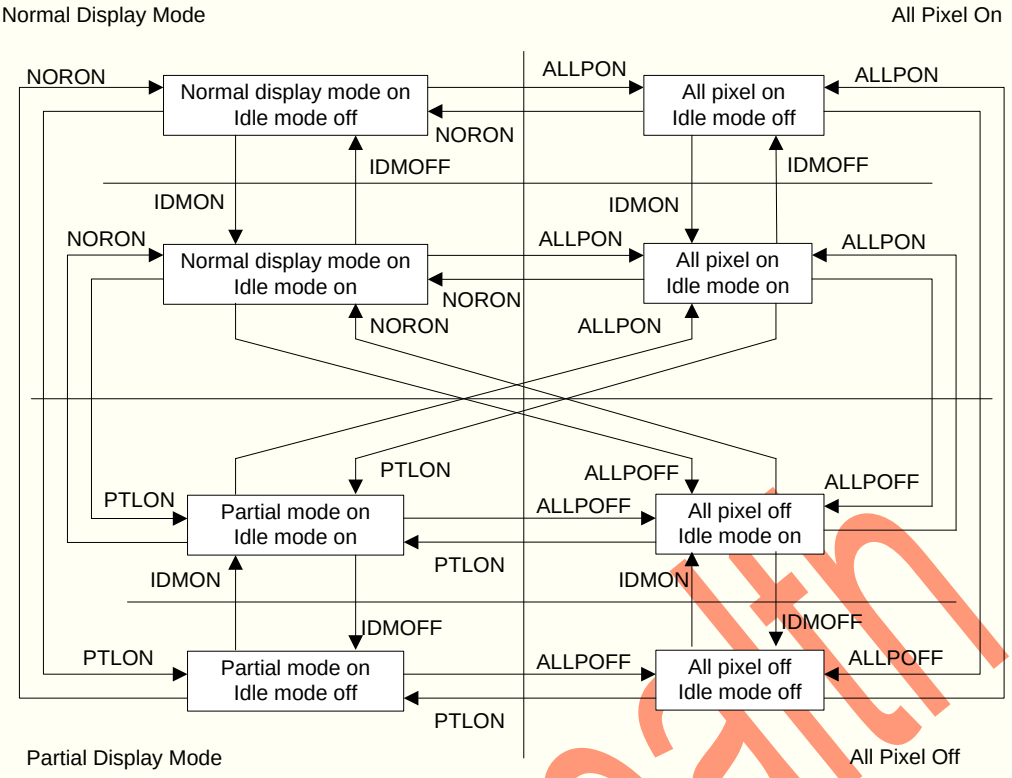


Deep Standby Mode Enter/Exit Sequence



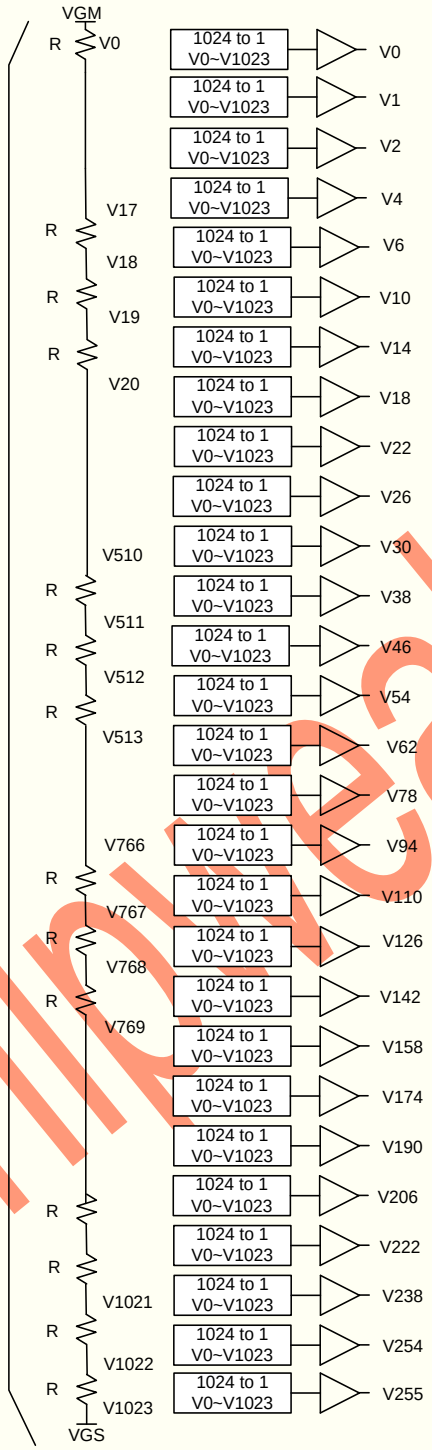
7.4 Basic Display Mode

The CH13620 has some basic operation modes which are Normal Display Mode, Idle Mode, All Pixel On and All Pixel Off for panel display. User can change these display modes for each other is illustrated below.

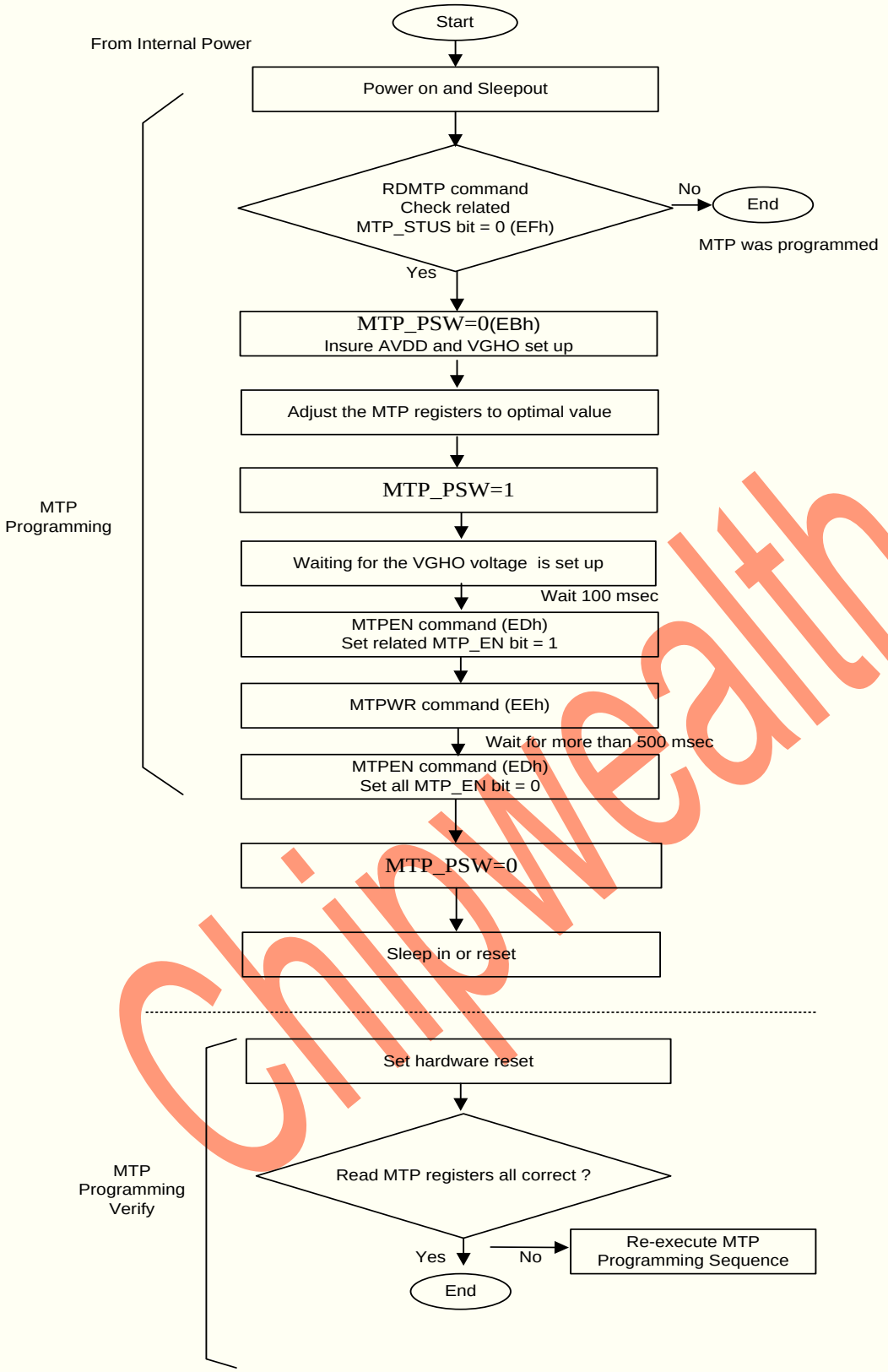


7.5 Gamma characteristic correction function

The structure of grayscale amplifier is shown as below. The 1024 voltage levels between VGM and VGS are determined by the reference adjustment register, the amplitude adjustment register and the micro-adjustment register.
There are 28 key point for Gamma correction.

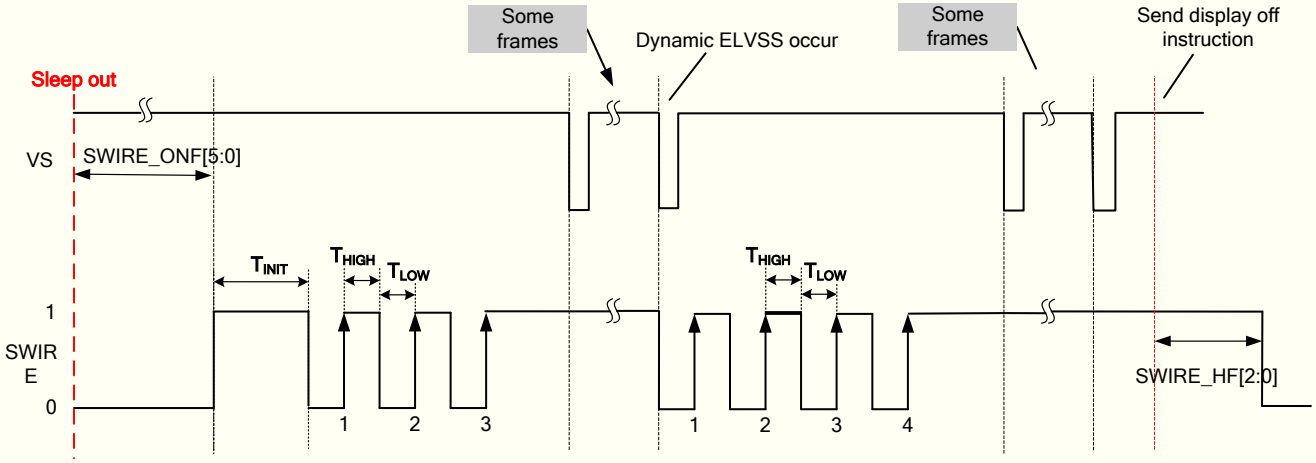


7.6 MTP Write Sequence



7.7 S-Wire Timing Control

S-wire interface is used to digitally communicate over a single cable with single-wire components. The CH13620 has a s-wire interface which allows programming the positive and negative output voltage of AMOLED panel power IC.



Parameter	Symbol	min.	typ.	max.	Unit
Power IC setup time	T_{INIT}	1	5	16	ms
SWIRE high time	T_{HIGH}	4	10	18	us
SWIRE low time	T_{LOW}	4	10	18	us

Note: The parameters of SWIRE pulse can be adjusted by SWIRECTR register.

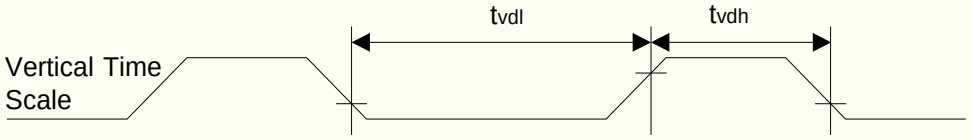
7.8 Tearing Effect information

7.8.1 Tear Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

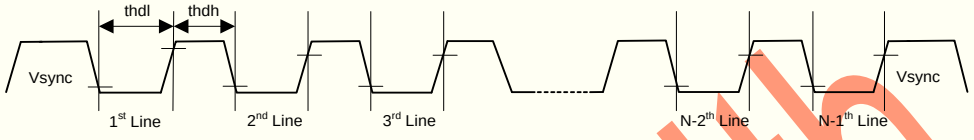
7.8.2 Tearing Effect Line Modes

VS output1: The Tearing Effect Output signal consists of V-Blanking Information only:



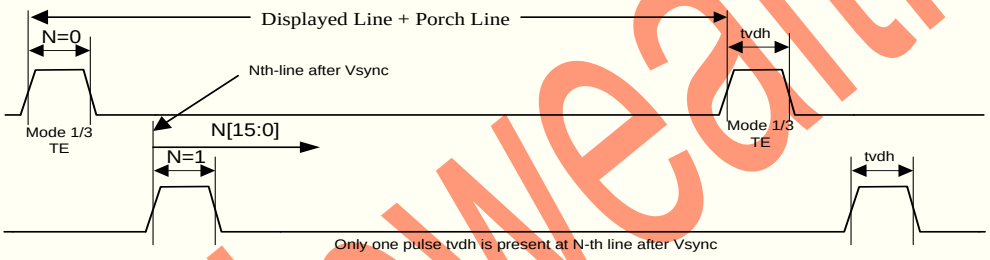
Tvdh = The LCD display is not updated from the Frame Memory
Tvdl = The LCD display is updated from the Frame Memory(except Invisible Line –see below)

HS output: The Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one Vsync and H-sync pulses per field.



Thdh = The LCD display is not updated from the Frame Memory
Thdl = The LCD display is updated from the Frame Memory(except Invisible Line-see above)

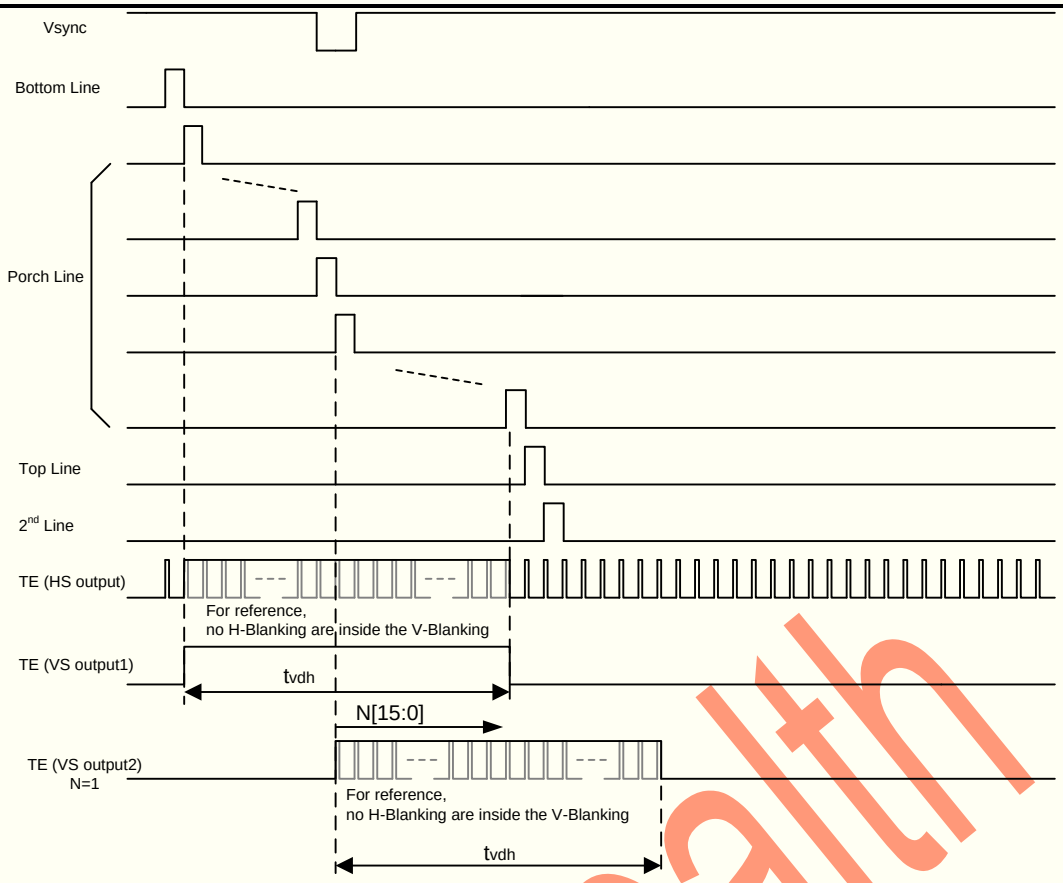
VS output2: This mode turn on the Tearing Effect output signal at line N after Vsync.



N = The N-th line, which set by register N[15:0] of command STESE(44h) after Vsyn.

The TE mode selection is described as below table

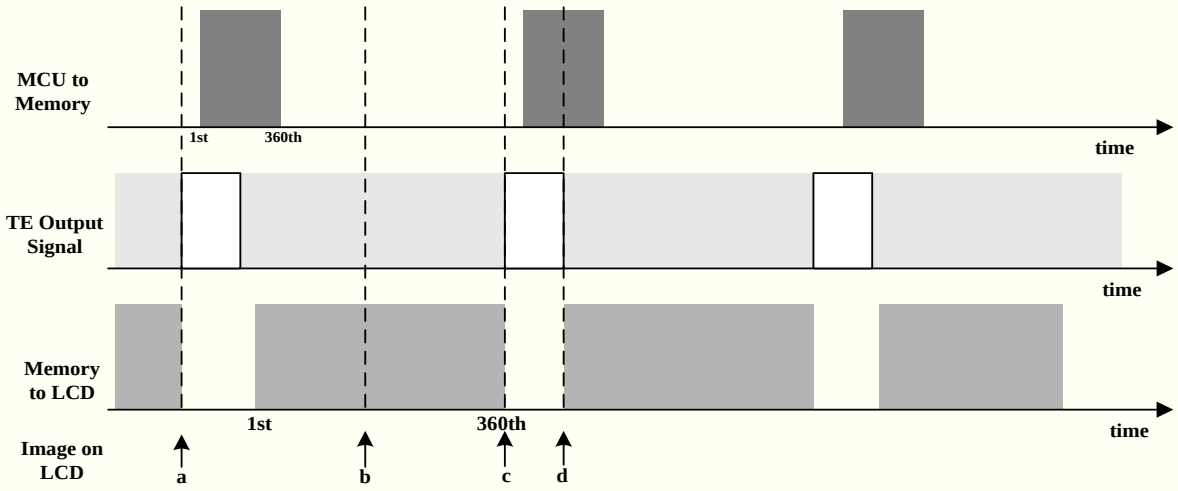
TEOFF(34h) TEON(35h) TELOM	STESL(44h) N[15:0]	TE Output
34h	X	TE off(output low)
35h with TELOM=0	N[15:0]=0	TE high in V-porch region（VS output1）
35h with TELOM=0	N[15:0]≠0	TE high at N-th line after Vsync（VS output2）
35h with TELOM =1	X	TE high in all V-porch and H-porch region（HS output）



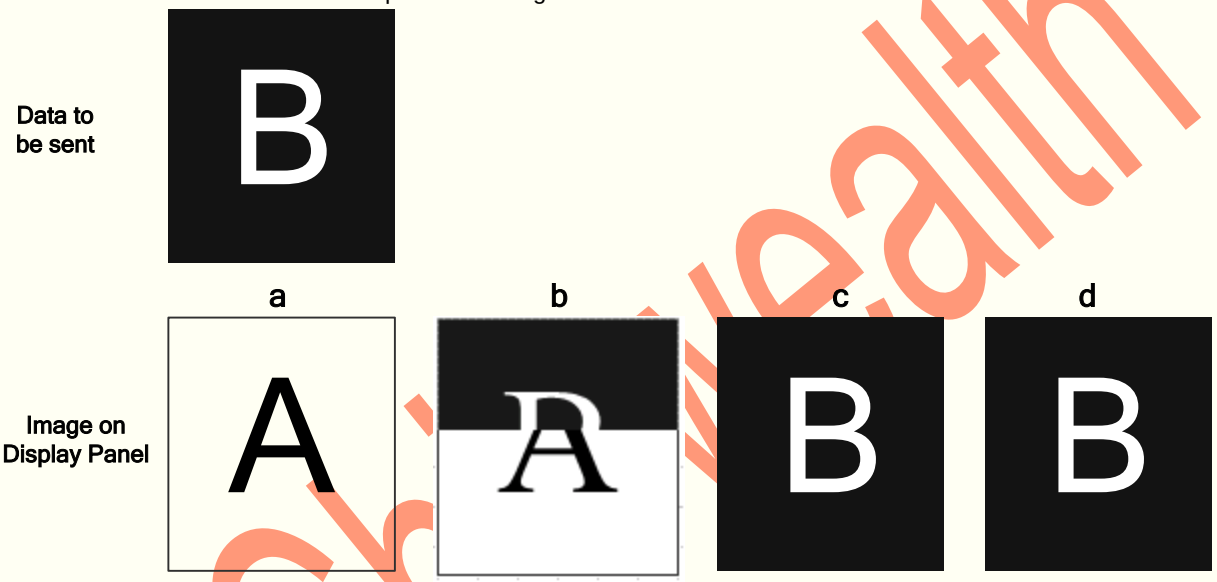
Notes:

1. During Sleep In Mode, the Tearing Output Pin is active Low.
2. N≦Displayed line + Porch line.
   Tvdh = width of porch line when N≦Displayed line
   tvdh = width of (Displayed line + Porch line-N) when N>Displayed line (falling edge of TE fixed at next Vsync)
3. Porch line = VBP+VFP.

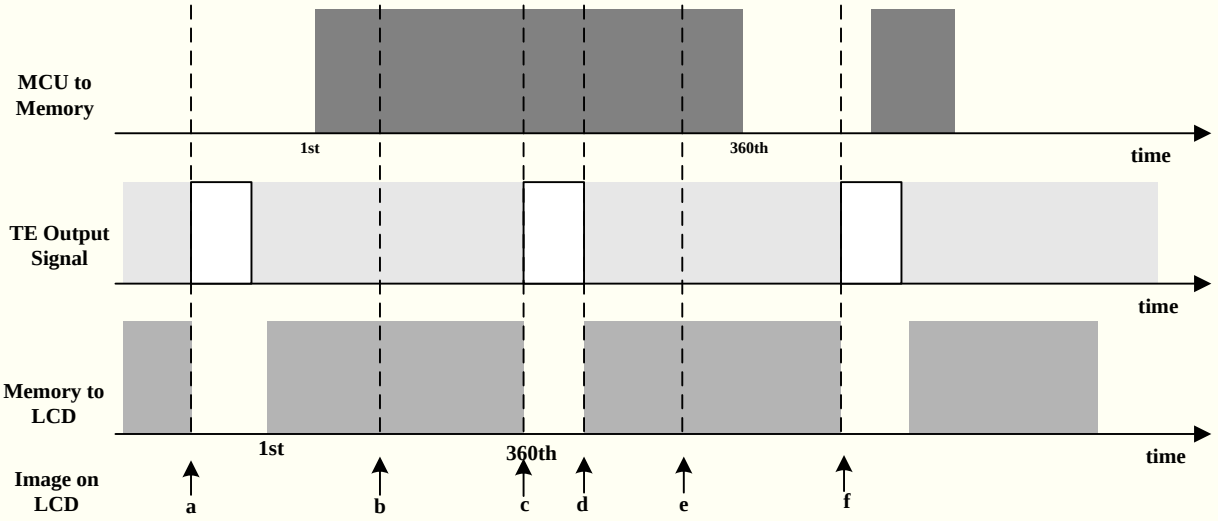
7.8.3 MPU Write is Faster Than Panel Read.



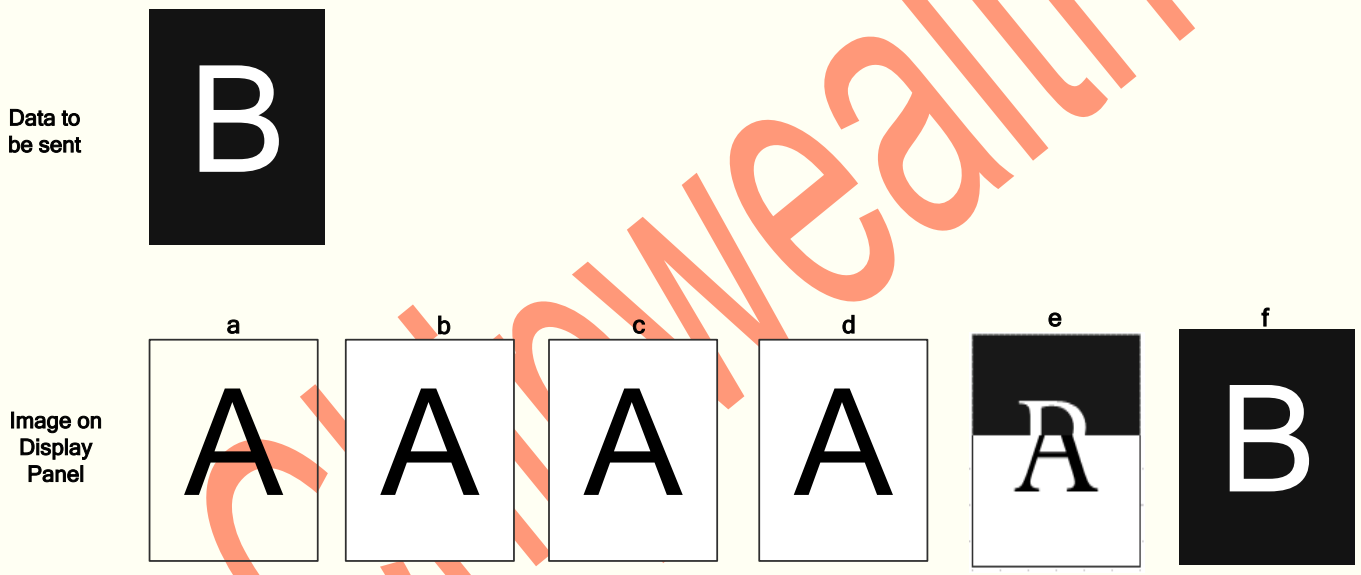
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



7.8.4 MPU Write is Slower Than Panel Read



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.



8 Electrical Specification

8.1 Absolute maximum ratings

Item	Symbol	Rating	unit
Supply voltage	VDDA,VDDB	-0.3 ~ +5.5	V
Supply voltage	VDDIO,VDDR	-0.3 ~ +5.5	V
Supply voltage (MV)	AVDD-VSS	-0.3 ~ +6.6	V
	AVEE-VSS	+0.3 ~ -5.5	V
Supply voltage (HV)	VGH-VSS	-0.3 ~ +15	V
	VGL-VSS	+0.3 ~ -15	V
	VGH-VGL (VGHO-VGLO)	-0.3 ~+32	V
Logic Input voltage range	VIN	-0.3 ~ VDDIO+0.3	V
Logic Output voltage range	VO	-0.3 ~ VDDIO+0.3	V
Differential Input Voltage	CLKP/N, D0P/N, D1P/N	-0.3 ~ +1.45	V
Operating temperature range	TOPR	-40 ~ +85	℃
Storage Temperature range	TSTG	-55 ~ +125	℃

NOTE:
1. VSS means VSSR, VSSG, VSSAM, VSSIO, AVSS and VSSB.
2. If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

8.2 DC characteristics

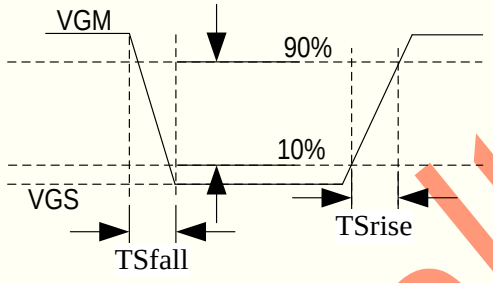
Basic characteristics

parameter	symbol	conditions	specification			Unit	Related Pins
			Min.	Typ.	Max.		
Power & Operation voltage							
Analog operating voltage	VDDA	Operating voltage	2.7	2.8	3.6	V	Note 1,2
Analog operating voltage	VDDB	Operating voltage	2.7	2.8	3.6	V	Note 1,2
Interface operating voltage	VDDIO	I/O supply voltage	1.65	1.8	3.6	V	Note 1,2
Logic operating voltage	VDDR	Logic supply voltage	1.65	1.8	3.6	V	Note 1,2
Input / Output							
Logic High Level Input Voltage	VIH	VDDIO=1.65~3.6	0.7VDDIO	-	VDDIO	V	Note 1,2,3
Logic Low Level Input Voltage	VIL	VDDIO=1.65~3.6	VSS	-	0.3VDDIO	V	Note 1,2,3
Logic High Level Output Voltage	VOH	VDDIO=1.65~3.6 IOH= -1.0 mA	0.8VDDIO	-	VDDIO	V	Note 1,2,5
Logic Low Level Output Voltage	VOL	VDDIO=1.65~3.6 IOL= +1.0 mA	VSS	-	0.2VDDIO	V	Note 1,2,5
Logic High level leakage (Except MIPI)	ILIH	Vin=0~VDDIO	-	-	1	μA	Note 1,2,3
Logic Low level leakage (Except MIPI)	ILIL	Vin=0~VDDIO	-1	-	-	μA	Note 1,2,3
Logic High level leakage (MIPI)	ILIH	Vin=0~DVDD	-	-	1	μA	Note 2,8
Logic Low level leakage (MIPI)	ILIL	Vin=0~DVDD	-1	-	-	μA	Note 2,8
DC/DC Converter Operation							
AVDD booster voltage	AVDD	-	4.5	5.6	6.5	V	Note 2,7
AVEE booster voltage	AVEE	-	-5.5	-5.5	-1*VDDB	V	Note 2,7
VREFP reference voltage	VREFP	-	0.5	1.5	5.0	V	Note 2,7
VREFN reference voltage	VREFN	-	-5.0	-3	-0.2	V	Note 2,7
VGHO reference voltage	VGHO	-	3.0	6.5	10.0	V	Note 2,7
VGLO reference voltage	VGLO	-	-10.0	-8	-3.0	V	Note 2,7
ELVDD reference voltage	VEP	-	0.5	4.6	5.0	V	Note 2,7
ELVDD output current capability	I_{VEP}	VEP=4.6V/drop 50mV (AVDD=2*VDDB)	-	-	4.5	mA	Note 2,7
		VEP=4.6V/drop 50mV (AVDD=3*VDDB)	-	-	3.7	mA	Note 2,7
ELVSS reference voltage	VEN	-	-5.0	-2.4	-0.2,0	V	Note 2,7
ELVSS output current capability	I_{VEN}	VEN=-4.5V/drop 50mV (AVEE=-2*VDDB)	-	-	4	mA	Note 2,7
		VEN=-2.5V/drop 50mV (AVEE=-VDDB)	-	-	3.5	mA	Note 2,7
VGH booster voltage	VGH	-	AVDD	8.4	2*AVDD	V	Note 2,6
VGL booster voltage	VGL	-	AVEE	-11.1	AVEE-AVDD	V	Note 2,6

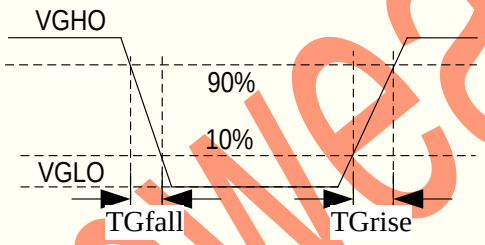
parameter	symbol	conditions	specification			Unit	Related Pins
			Min.	Typ.	Max.		
Voltage difference between VGH and VGL	VGHL	$\lvert VGH - VGL \rvert$	-	-	30	V	Note 2
Oscillator tolerance	ΔOSC	-40 ℃~ +85℃	-8	-	8	%	
Source Driver							
Gamma reference voltage	VGM	-	2.0	5.4	6.3	V	-
	VGS	-	0,0.2	2.15	4.5	V	

Output offset voltage	V_{OFFSET}	-	-	-	15	mV	Note 4
Output deviation voltage	Vdev	2.0V<Sout<5.0V	-	5	-	mV	Note 4
Output rising/falling Time	Tsr/Tsf	-	-	TBD	-	μs	Note 9
GOA Driver							
GOA rising/falling time	TGr/TGf	-	-	TBD	-	μs	Note10

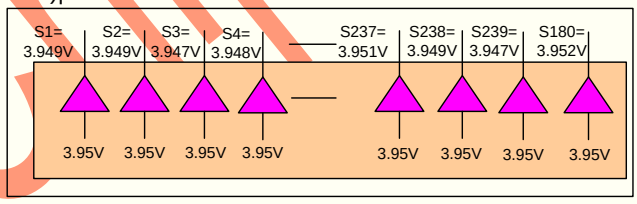
Note 1) VDDIO/ VDDR =1.65 to 3.6V, VDDA/VDDB=2.7 to 3.6V, VSS means VSSIO=DVSS=VSSG=VSSAM=VSSR=VSSB=0V, Ta=-40 ℃~ +85℃.
Note 2) when the measurements are performed with module. Measurement Points for all characteristics.
Note 3) RSTB, CSB, SCL, SDI, DSWAP, PSWAP, IM[1:0].
Note 4) Channel loading=18.5p, R=1.1k / channel, Ta=25 ºC after chop function.
Note 5) SDO, TE.
Note 6) VDDA/VDDB =2.8V, Ta=25 ºC, no load on panel and Iload=TBD mA, |Output Voltage – Target Voltage| < 100mV.
Note 7) VDDA/VDDB =2.8V, Ta=25 ºC, no load on panel and Iload=TBD mA, power pad serial resistor is smaller than maximum value.
Note 8) Vin = 0 to 1.2V, VDDA/VDDB =2.7 to 3.6V, VDDIO /VDDR=1.65 to 3.6V, VSSIO=DVSS=VSSG=VSSAM=VSSR =VSSB=0V, Ta=-40 ℃~ +85℃.
Note 9) VGM=6.2V, VGS=1.2V, Ta=25 ºC, Channel loading=18.5p, R=1.1k / channel, Trise <TBD, Tfall <TBD;



Note 10) VGHO=7V,VGLO=-7V, Ta=25 ºC,C=77p, R=20.20.1k / channel , Trise <TBD, Tfall <TBD;



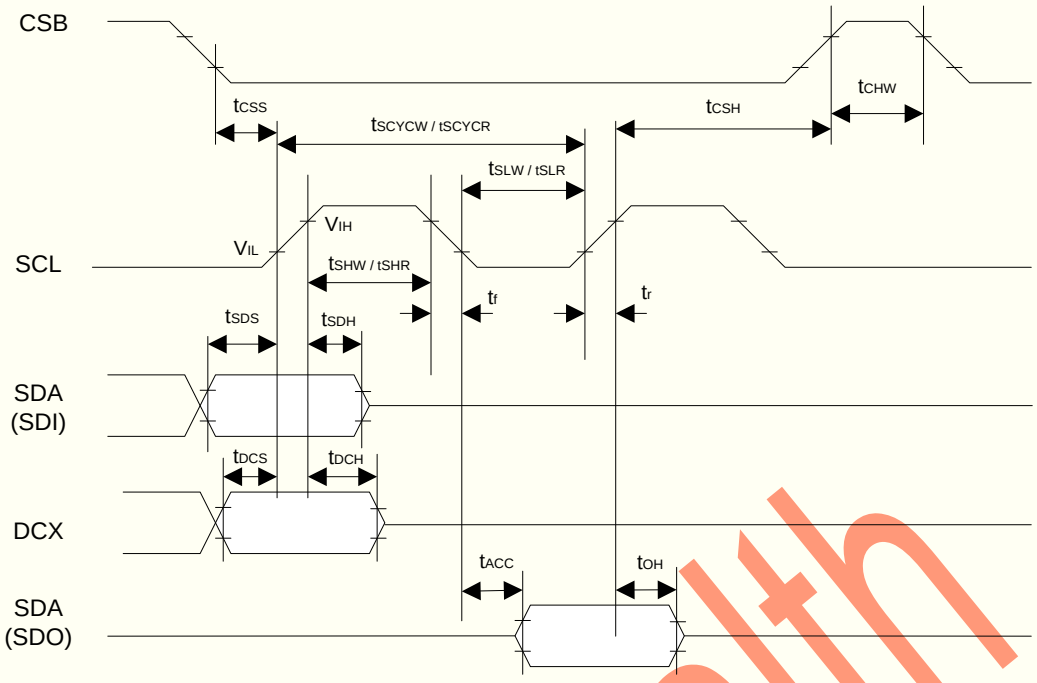
Measurement Points for all characteristics.
- When 2.0V <=Sout <= 5.0V
|(S1, S2, S3 …. , S240) – Average (S1, S2, S3, …. , S240)| <= 5mV
- Sout=V0~V255
$|S_{Target} - Average (S1, S2, S3, … , S240)| <= 15mV$



Source output deviation

8.3 AC Characteristics

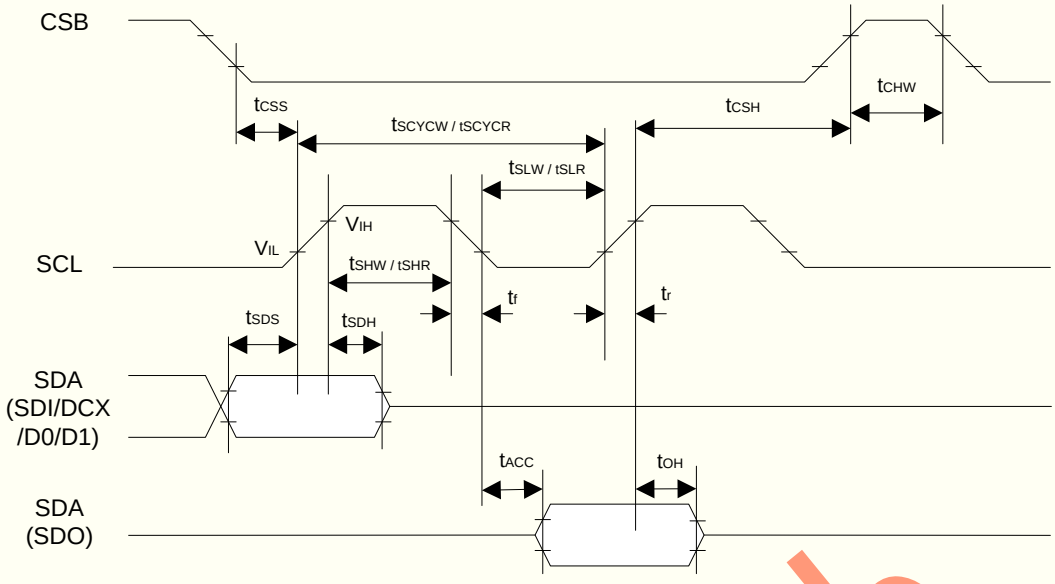
8bit/9bit SPI Connect with Host Characteristics



Signal	Symbol	Parameter	Min.	Max.	Unit	Description
SCL	t_{SCYCW}	Serial clock cycle (Write)	20	-	ns	
	t_{SHW}	SCL “H” pulse width (Write)	9	-	ns	
	t_{SLW}	SCL “L” pulse width (Write)	9	-	ns	
	t_{SCYCR}	Serial clock cycle (Read register)	300	-	ns	
	t_{SHR}	SCL “H” pulse width (Read register)	140	-	ns	
	t_{SLR}	SCL “L” pulse width (Read register)	140	-	ns	
SDI (SDO) DCX	t_{SDS}/t_{DCS}	Data setup time	5	-	ns	
	t_{SDH}/t_{DCH}	Data hold time	5	-	ns	
	t_{ACC}	Access time	-	120	ns	
	t_{OH}	Output disable time	5	-	ns	
CSB	t_{CHW}	Chip select “H” pulse width	45	-	ns	
	t_{CSS}	Chip select setup time	10	-	ns	
	t_{CSH}	Chip select hold time	10	-	ns	

Note 1: VDDIO/VDDR =1.65 to 3.6V, VDDA/VDDB =2.7 to 3.6V, VSSIO=DVSS=VSSG=VSSAM=VSSR =VSSB=0V, Ta=-40 to +85 ºC.

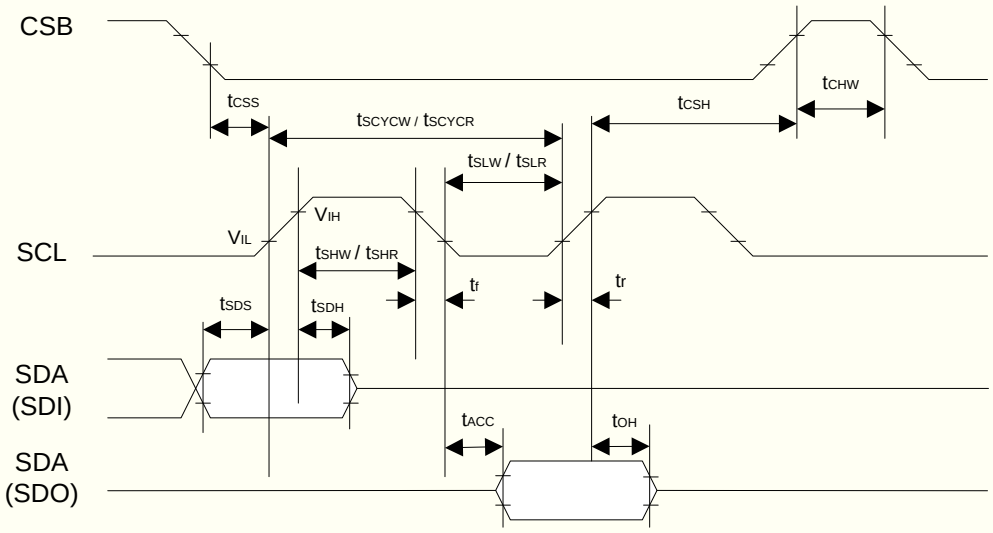
Quad SPI Connect with Host Characteristics



Signal	Symbol	Parameter	Min.	Max.	Unit	Description
SCL	t_{SCYCW}	Serial clock cycle (Write)	20	-	ns	
	t_{SHW}	SCL “H” pulse width (Write)	9	-	ns	
	t_{SLW}	SCL “L” pulse width (Write)	9	-	ns	
	t_{SCYCR}	Serial clock cycle (Read register)	100	-	ns	
	t_{SHR}	SCL “H” pulse width (Read register)	46	-	ns	
	t_{SLR}	SCL “L” pulse width (Read register)	46	-	ns	
SDI (SDO) DCX	t_{SDS}/t_{DCS}	Data setup time	5	-	ns	
	t_{SDH}/t_{DCH}	Data hold time	5	-	ns	
	t_{ACC}	Access time	-	40	ns	
	t_{OH}	Output disable time	5	-	ns	
CSB	t_{CHW}	Chip select “H” pulse width	45	-	ns	
	t_{CSS}	Chip select setup time	10	-	ns	
	t_{CSH}	Chip select hold time	10	-	ns	

Note 1: VDDIO/VDDR =1.65 to 3.6V, VDDA/VDDB =2.7 to 3.6V, VSSIO=DVSS=VSSG=VSSAM=VSSR =VSSB=0V, Ta=-40 to +85 ºC.

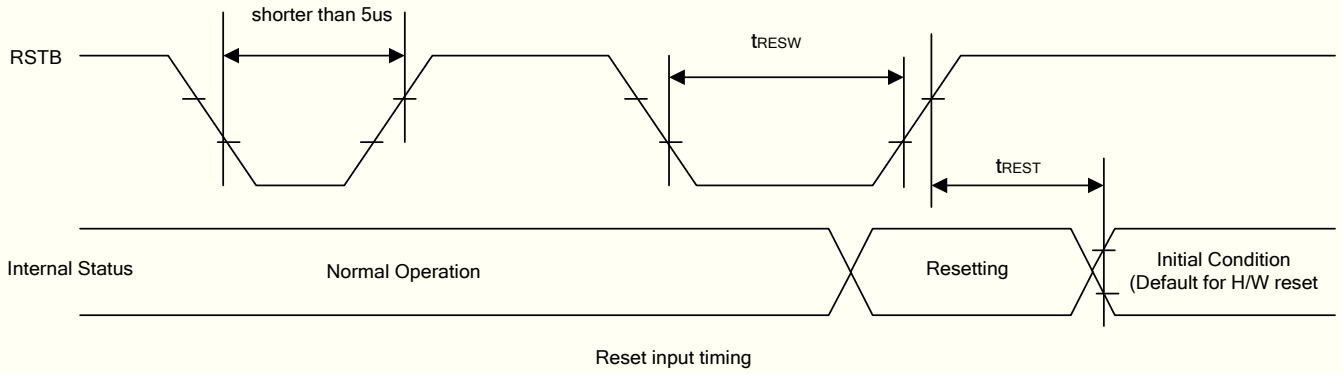
16-bit SPI characteristics



Signal	Symbol	Parameter	Min.	Max.	Unit	Description
SCL	t_{SCYCW}	Serial clock cycle (Write)	100	-	ns	
	t_{SHW}	SCL “H” pulse width (Write)	40	-	ns	
	t_{SLW}	SCL “L” pulse width (Write)	40	-	ns	
	t_{SCYCR}	Serial clock cycle (Read register)	300	-	ns	
	t_{SHR}	SCL “H” pulse width (Read register)	140	-	ns	
	t_{SLR}	SCL “L” pulse width (Read register)	140	-	ns	
SDI (SDO)	t_{SDS}	Data setup time	20	-	ns	
	t_{SDH}	Data hold time	20	-	ns	
	t_{ACC}	Access time	-	120	ns	
	t_{OH}	Output disable time	5	-	ns	
CSB	t_{CHW}	Chip select “H” pulse width	45	-	ns	
	t_{CSS}	Chip select setup time	20	-	ns	
	t_{CSH}	Chip select hold time	50	-	ns	

Note 1: VDDIO/ VDDR =1.65 to 3.6V, VDDA/VDDB =2.7 to 3.6V, VSSIO=DVSS=VSSG=VSSAM=VSSR =VSSB=0V, Ta=-40 to +85 ºC

Reset Input Timing



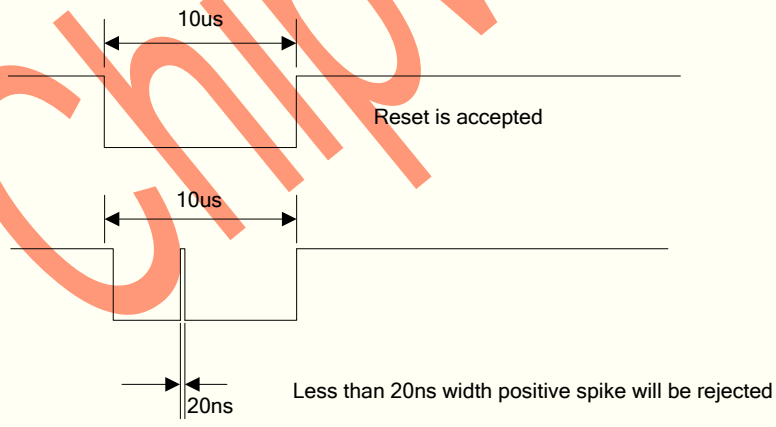
Reset input timing

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
RSTB	tRESW	Reset "L" pulse width (Note 1)	10	-	-	μs	-
	tREST	Reset complete time (Note 2)	-	-	10	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode

Note 1: Spike due to an electrostatic discharge on RSTB line does not cause irregular system Reset according to the table below.

RSTB Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 10μs	Reset
Between 5μs and 10μs	Reset Start

Note 2: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In–mode) and then return to Default condition for H/W Reset.
Note 3: During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W Reset complete time (t_{REST}) within 5ms after a rising edge of RSTB.
Note 4: Spike Rejection also applies during a valid Reset pulse as shown below:



Note 5: It is necessary to wait 5msec after releasing RSTB before sending commands. Also Sleep Out command cannot be sent for 120msec.

8.4 ESD Protection level

Model	Test Condition	Protection Level	Unit
Human Body Model	C = 100 pF, R = 1.5 kΩ	> 2500	V
Machine Model	C = 200 pF, R = 0.0 Ω	> 250	V

8.5 Latch-up protection level

The device will not latch up at trigger current levels less than ±200 mA.

8.6 Current consumption

Parameter	Symbol	Conditions	Specification			Unit
			Min.	Typ.	Max.	
Sleep out & display on mode	I total (I_{VDDA}+ I_{VDDB} + I_{VDDIO} + I_{VDDR})	VDDIO=VDDR=1.8V,VDDA/VDDB=2.8V, ta = 25ºC,white picture	-	TBD	-	mW
Sleep in mode (Note 1)	I total (I_{VDDA}+ I_{VDDB} + I_{VDDIO} + I_{VDDR})	VDDIO=VDDR=1.8V,VDDA/VDDB=2.8V, ta = 25ºC,white picture	-	TBD	-	μW
Deep standby mode (Note 2)	I total (I_{VDDA}+ I_{VDDB} + I_{VDDIO} + I_{VDDR})	VDDIO=VDDR=1.8V,VDDA/VDDB=2.8V, ta = 25ºC,white picture	-	TBD	-	μW

Note 1: For sleep in mode, MIPI in stop state (LP11). SPI Interface also included in it.
Note 2: All Interfaces included.

9 Data Sheet History

Version	Contents	Date
V0.00	Original	2023-08-02