

Crystalfontz America, Inc.

CUSTOMER : _____

MODULE NO.: **CFAL12864L-Y-B2**

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY
ISSUED DATE:			

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1.Module Classification Information

CFA L 12864 Z – Y – B2

Brand : CRYSTALFONTZ AMERICA, INCORPORATED	
Display Type : H→Character Type, G→Graphic Type , L→ OLED	
Display's Logical Dimensions : 128 columns by 64 rows.	
Model Variant: Z	
Color :	Y→Yellow
Special Code	B2→PCB

2.Precautions in use of OLED Modules

- (1) Avoid applying excessive shocks to the module or making any alterations or modifications to it.
- (2) Don't make extra holes on the printed circuit board, modify its shape or change the components of OLED module.
- (3) Don't disassemble the OLED.
- (4) Don't operate it above the absolute maximum rating.
- (5) Don't drop, bend or twist OLED.
- (6) Soldering: only to the I/O terminals.
- (7) Storage: please storage in anti-static electricity container and clean environment.

3.General Specification

Item	Dimension	Unit
Number of Characters	128 columns x 64 Rows	—
Module dimension	74 x 53.5 x 6.0	mm
View area	63.4 x 32.7	mm
Active area	61.41 x 30.69	mm
Dot size	0.45 x 0.45	mm
Dot pitch	0.48 x 0.48	mm
LCD type	OLED , Yellow	
Duty	1/64	

4.Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T _{OP}	-20	—	+70	°C
Storage Temperature	T _{ST}	-30	—	+80	°C
Input Voltage	V _I	0	—	V _{DD}	V
Supply Voltage	V _{DD}	2.4	3.0	3.5	V

5. Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	$V_{DD}-V_{SS}$	—	2.4	3.0	3.5	V
Input High Volt.	V_{IH}	—	2.4	—	3.5	V
Input Low Volt.	V_{IL}	—	0	—	$0.2 V_{DD}$	V
Total Power	P_T	$V_{DD}=3.0V$	—	—	250	mW

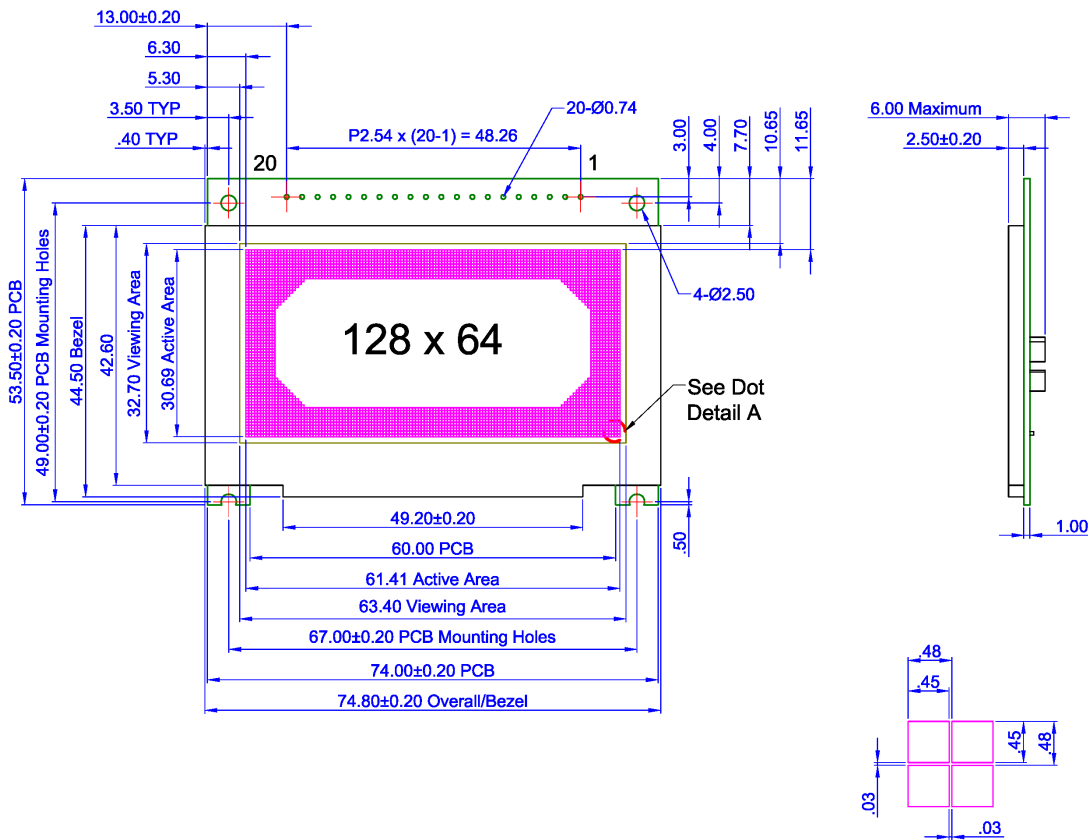
6. Optical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
View Angle	(V) θ			160		deg
	(H) ϕ			160		deg
Contrast Ratio (Dark Room)	CR	80cd/m^2	—	100:1	—	—
Brightness		With polarizer		80		cd/m^2

7.Interface Pin Function


PIN NAME	PIN NO	DESCRIPTION			
GND	1	Ground			
VDD	2	Logic Voltage +3V			
NC	3	No Connect			
D/C#	4	Data/Command Select. This is the Data/Command control pin. When it is pulled HIGH, the input at D7-D0 is treated as display data. When it is pulled LOW, the input at D7-D0 is transferred to the command registers. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.			
R/W#	5	This is a MCU interface input pin. When 6800-series Parallel Interface mode is selected, this pin is used as Read/Write (R/W) selection input. Pull this pin to HIGH for read mode and pull it to LOW for write mode. When 8080-series Parallel Interface mode is selected, this pin is used as Write (WR#) selection input. Pull this pin to LOW for write mode. Data write operation is initiated when this pin is pulled LOW and the CS# is pulled LOW.			
E(RD#)	6	This is a MCU interface input pin. When 6800-series Parallel Interface is selected, this pin is used as Enable (E) signal. Read/Write operation is initiated when this pin is pulled HIGH and the CS# pin is pulled LOW. When 8080-series Parallel Interface is selected, this pin is used to receive the Read Data (RD#)signal. Data read operation is initiated when this pin is pulled LOW and CS# pin is pulled LOW.			
D0-D7	7-14	These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial interface mode is selected, D1 will be the serial data input, SDIN, and D0 will be the serial clock input, SCLK.			
CS#	15	Chip Select,active low			
RES#	16	Reset,active low			
M80/68#	17	These are MCU interface input selection pins. See the following table for selecting different interfaces:			
MS	18	Table	6800-paralle interface	8080-parallel interface	Serial interface
		M80/68#	0	1	0
		MS	1	1	0
NC	19	No Connect			
FG	20	Frame Ground			

8. Contour Drawing & Block Diagram

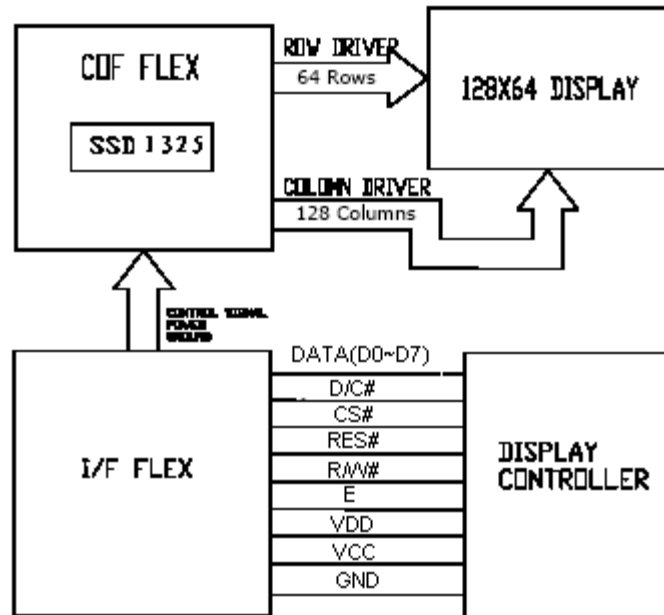


Note: Tolerance is ±0.3 mm unless specified.

Dot Detail A

 Crystalfontz America, Inc. <small>copyright © 2008 by www.crystalfontz.com/products/</small>	Part No.(s): CFAL12864Z-Y-B2 CFAL12864Z-G-B2	Scale: Not to scale	Drawing Number: CFAL12864Z-B2_master	Hardware Rev.: v2.2
		Units: Millimeters	Date: 2008/12/15	Sheet: 1 of 1

CFAL12864Z OLED Module



NOTE: Some pins omitted

9. Graphic Display DDRAM Map

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x80x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. (Refer to Table 3-7 for GDDRAM address map description)

Table 4 – GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, ... , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs Column Address (HEX)
		00		01			3E		3F		
COM0	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	
COM1	01	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
COM78	4E	D4992[3:0]	D4992[7:4]	D4993[3:0]	D4993[7:4]		D5054[3:0]	D5054[7:4]	D5055[3:0]	D5055[7:4]	
COM79	4F	D5056[3:0]	D5056[7:4]	D5057[3:0]	D5057[7:4]		D5118[3:0]	D5118[7:4]	D5119[3:0]	D5119[7:4]	

COM Outputs Row Address (HEX)
(Display Startline=0)

Table 5 – GDDRAM address map showing Horizontal Address Increment A[2]=1, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, ... , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs Column Address (HEX)
		00		01			3E		3F		
COM0	00	D0[3:0]	D0[7:4]	D80[3:0]	D80[7:4]		D4960[3:0]	D4960[7:4]	D5040[3:0]	D5040[7:4]	
COM1	01	D1[3:0]	D1[7:4]	D81[3:0]	D81[7:4]		D4961[3:0]	D4961[7:4]	D5041[3:0]	D5041[7:4]	
COM78	4E	D78[3:0]	D78[7:4]	D158[3:0]	D158[7:4]		D5038[3:0]	D5038[7:4]	D5118[3:0]	D5118[7:4]	
COM79	4F	D79[3:0]	D79[7:4]	D159[3:0]	D159[7:4]		D5039[3:0]	D5039[7:4]	D5119[3:0]	D5119[7:4]	

COM Outputs Row Address (HEX)
(Display Startline=0)

Table 6 – GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=1, Nibble Re-map A[1]=1, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, ... , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs Column Address (HEX)
		3F		3E			01		00		
COM0	00	D63[7:4]	D63[3:0]	D62[7:4]	D62[3:0]		D1[7:4]	D1[3:0]	D0[7:4]	D0[3:0]	
COM1	01	D127[7:4]	D127[3:0]	D126[7:4]	D126[3:0]		D65[7:4]	D65[3:0]	D64[7:4]	D64[3:0]	
COM78	4E	D5055[7:4]	D5055[3:0]	D5054[7:4]	D5054[3:0]		D4993[7:4]	D4993[3:0]	D4992[7:4]	D4992[3:0]	
COM79	4F	D5119[7:4]	D5119[3:0]	D5118[7:4]	D5118[3:0]		D5057[7:4]	D5057[3:0]	D5056[7:4]	D5056[3:0]	
COM Outputs	Row Address (HEX)										

(Display Startline=0)

Table 7 – GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=1, and Display Start Line=16H (Data byte sequence: D0, D1, ... , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs Column Address (HEX)
		00		01			3E		3F		
COM15	0F	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	
COM14	0E	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
COM17	11	D4992[3:0]	D4992[7:4]	D4993[3:0]	D4993[7:4]		D5054[3:0]	D5054[7:4]	D5055[3:0]	D5055[7:4]	
COM16	10	D5056[3:0]	D5056[7:4]	D5057[3:0]	D5057[7:4]		D5118[3:0]	D5118[7:4]	D5119[3:0]	D5119[7:4]	
COM Outputs	Row Address (HEX)										

(Display Startline=10H)

Table 8 – GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, Display Start Line=00H (Data byte sequence: D0, D1, ... , D4834, D4835), Column Start Address=01H, Column End Address=3EH, Row Start Address=01H and Row End Address=4EH

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs Column Address (HEX)
		00		01			3E		3F		
COM0	00										
COM1	01			D0[3:0]	D0[7:4]		D61[3:0]	D61[7:4]			
COM78	4E			D4774[3:0]	D4774[7:4]		D4835[3:0]	D4835[7:4]			
COM79	4F										
COM Outputs	Row Address (HEX)										

(Display Startline=0)

10. Instruction Table

Command table (D/C =0, R/W (WR#)=0, E (RD#)=1)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0 0	15 A[5:0] B[5:0]	0 * *	0 * *	0 A5 B5	1 A4 B4	0 A3 B3	1 A2 B2	0 A1 B1	1 A0 B0	Set Column Address	Second command A[5:0] sets the column start address from 0-63, POR = 00H. Third command B[5:0] sets the column end address from 0-63, POR = 3FH.
0 0 0	75 A[6:0] B[6:0]	0 * *	1 A6 B6	1 A5 B5	1 A4 B4	0 A3 B3	1 A2 B2	0 A1 B1	1 A0 B0	Set Row address	Second command A[6:0]sets the row start address from 0-79, POR = 00H. Third command B[6:0] sets the row end address from 0-79, POR = 4FH.
0 0	81 A[6:0]	1 *	0 A6	0 A5	0 A4	0 A3	0 A2	0 A1	1 A0	Set Contrast Control Register	Double byte command to select 1 out of 128 contrast steps. Contrast increases as level increase. The level is set to 40H after POR
0	84~86	1	0	0	0	0	1	X1	X0	Set Current Range	84H = Quarter Current Range (POR) 85H = Half Current Range 86H = Full Current Range
0 0	A0 A[6:0]	1 *	0 A6	1 A5	0 A4	0 A3	0 A2	0 A1	0 A0	Set Re-map	A[0]=0, Disable Column Address Re-map (POR) A[0]=1, Enable Column Address Re-map A[1]=0, Disable Nibble Re-map (POR) A[1]=1, Enable Nibble Re-map A[2]=0, Horizontal Address Increment (POR) A[2]=1, Vertical Address Increment A[4]=0, Disable COM Re-map disable (POR) A[4]=1, Enable COM Re-map A[5]=0, Reserved (POR) A[5]=1, Reserved A[6]=0, Disable COM Split Odd Even (POR) A[6]=1, Enable COM Split Odd Even
0 0	A1 A[6:0]	1 *	0 A6	1 A5	0 A4	0 A3	0 A2	0 A1	1 A0	Set Display Start Line	Set display RAM display start line register from 079. Display start line register is reset to 00H after POR.
0 0	A2 A[6:0]	1 *	0 A6	1 A5	0 A4	0 A3	0 A2	1 A1	0 A0	Set Display Offset	Set vertical scroll by COM from 0-79. The value is reset to 00H after POR.
0	A4~A7	1	0	1	0	0	X2	X1	X0	Set Display Mode	A4H = Normal Display (POR) A5H = Entire Display On, all pixels turns on in GS level 15 A6H = Entire Display Off, all pixels turns off A7H = Inverse Display
0 0	A8 A[6:0]	1 *	0 A6	1 A5	0 A4	1 A3	0 A2	0 A1	0 A0	Set Multiplex Ratio	The next command determines multiplex ratio N from 16MUX-80MUX, POR=4FH(80MUX)

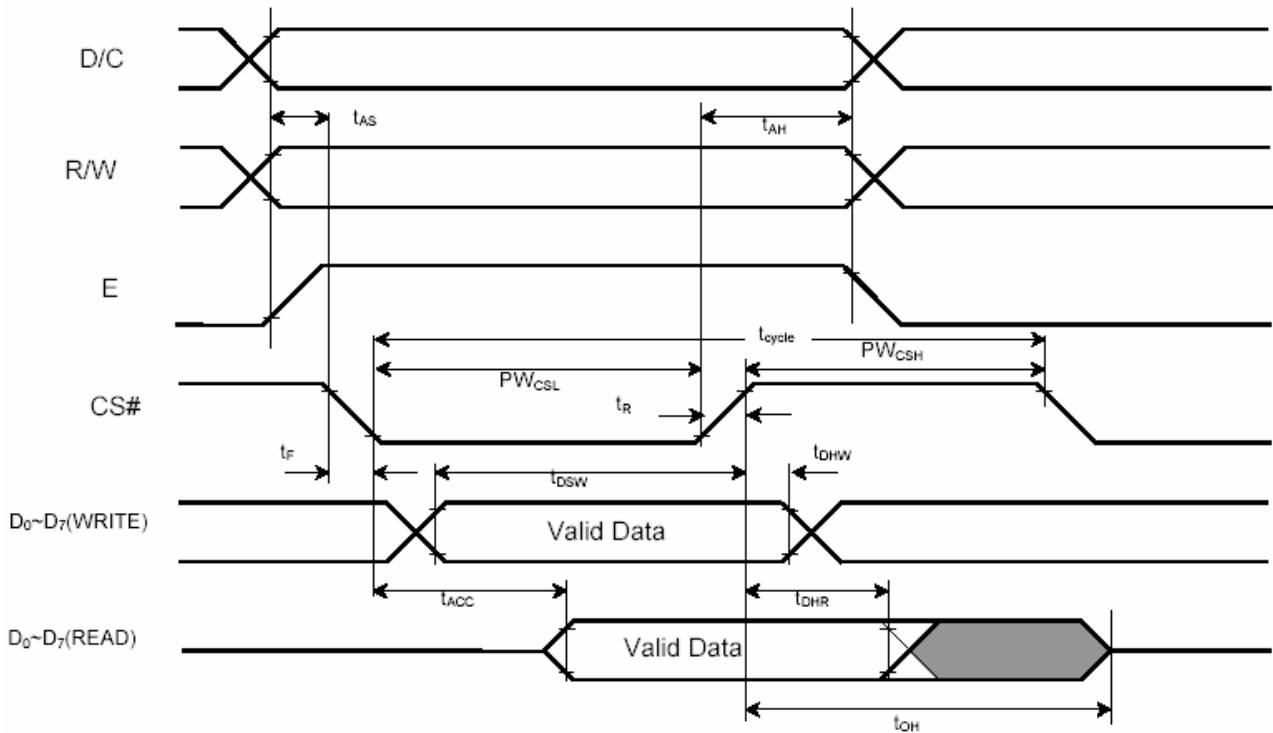
0	AD	1	0	1	0	1	1	0	1	Set Master Configuration	A[0] = 0, Disable DC-DC converter
0	A[1:0]	*	*	*	*	*	*	A1	A0		A[0] = 1, Enable DC-DC converter (POR)
											A[1] = 0, Disable internal VCOMH
											A[1] = 1, Enable internal VCOMH (POR)
0	AE~AF	1	0	1	0	X3	1	1	1	Set Display On/Off	AEH = Display Off (Sleep mode) (POR) AFH = Display On
0	BE	1	0	1	1	1	1	1	0	Set VCOMH Voltage	Second command A[5:0] sets the VCOMH voltage
0	A[5:0]	*	*	A5	A4	A3	A2	A1	A0		level 000000-011111
											A[5:0] = 1xxxxx = 1.0*VREF
											A[5:0] = 010001(POR)
0	BC	1	0	1	1	1	1	0	0	Set Precharge Voltage	Second command A[7:0] sets the precharge voltage level 00000000-00011111
0	A[7:0]	A7	A6	A5	A4	A3	A2	A1	A0		A[7:0] = 1xxxxxxx connects to VCOMH
											A[7:0] = 001xxxxx equals 1.0*VREF
											A[7:0] = 00011000(POR)
0	B1	1	0	1	1	0	0	0	1	Set Phase Length	A[3:0] = P1, phase 1 period of 1-15 DCLK clocks,
0	A[3:0]	*	*	*	*	A3	A2	A1	A0		POR = 3DLKS = 3H
0	A[7:4]	A7	A6	A5	A4	*	*	*	*		A[7:4] = P2, phase 2 period of 1-15 DCLK clocks, POR = 5DLKS = 5H
0	B2	1	0	1	1	0	0	1	0	Set Row Period	The next command sets the number of DCLKs, K, per row between 2-158DLKS, POR = 37DLKS = 25H
0	A[7:0]	A7	A6	A5	A4	A3	A2	A1	A0		The K value should be set as
											K = P1+P2+GS15 pulse width (POR: 3+5+29DLKS)
0	B3	1	0	1	1	0	0	1	1	Set Display Clock Divide Ratio/Oscillator Frequency	The lower nibble of the next command sets the divide ratio of the display clocks: Divide ratio = 1-16, POR = 2
0	A[3:0]	*	*	*	*	A3	A2	A1	A0		The higher nibble of the next command sets the Oscillator Frequency. Oscillator Frequency increases with the value of
0	A[7:4]	A7	A6	A5	A4	*	*	*	*		A[7:4] and vice versa. POR=0
0	B8	1	0	1	1	1	0	0	0	Set Gray Scale Table	The next eight bytes of command set the gray scale
0	A[2:0]	*	*	*	*	*	A2	A1	A0		level of GS1-15 as below:
0	B[2:0]	*	*	*	*	*	B2	B1	B0		A[2:0] = L1, POR=1
0	B[6:4]	*	B6	B5	B4	*	*	*	*		B[2:0] = L2, POR=1
0	C[2:0]	*	*	*	*	*	C2	C1	C0		B[6:4] = L3, POR=1
0	C[6:4]	*	C6	C5	C4	*	*	*	*		C[2:0] = L4 POR=1
0	D[2:0]	*	*	*	*	*	D2	D1	D0		C[6:4] = L5, POR=1
0	D[6:4]	*	D6	D5	D4	*	*	*	*		D[2:0] = L6, POR=1
0	E[2:0]	*	*	*	*	*	E2	E1	E0		D[6:4] = L7, POR=1
0	E[6:4]	*	E6	E5	E4	*	*	*	*		E[2:0] = L8, POR=1
0	F[2:0]	*	*	*	*	*	F2	F1	F0		E[6:4] = L9, POR=1
0	F[6:4]	*	F6	F5	F4	*	*	*	*		F[2:0] = L10, POR=1

0	G[2:0]	*	*	*	*	*	G2	G1	G0		F[6:4] = L11, POR=1
0	G[6:4]	*	G6	G5	G4	*	*	*	*		G[2:0] = L12, POR=1
0	H[2:0]	*	*	*	*	*	H2	H1	H0		G[6:4] = L13, POR=1
0	H[6:4]	*	H6	H5	H4	*	*	*	*		H[2:0] = L14, POR=1
											H[6:4] = L15, POR=1
0	CF	1	1	0	0	1	1	1	1	Set Biasing Current for	F0H = High (POR)
0	A[7:6]	A7	A6	*	*	*	*	*	*	DC-DC converter	70H = Low
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No Operation

11. Timing Characteristics

6800-Series MPU Parallel Interface Timing Characteristics (VDD - VSS = 2.4 to 3.5V, TA = 25°C)

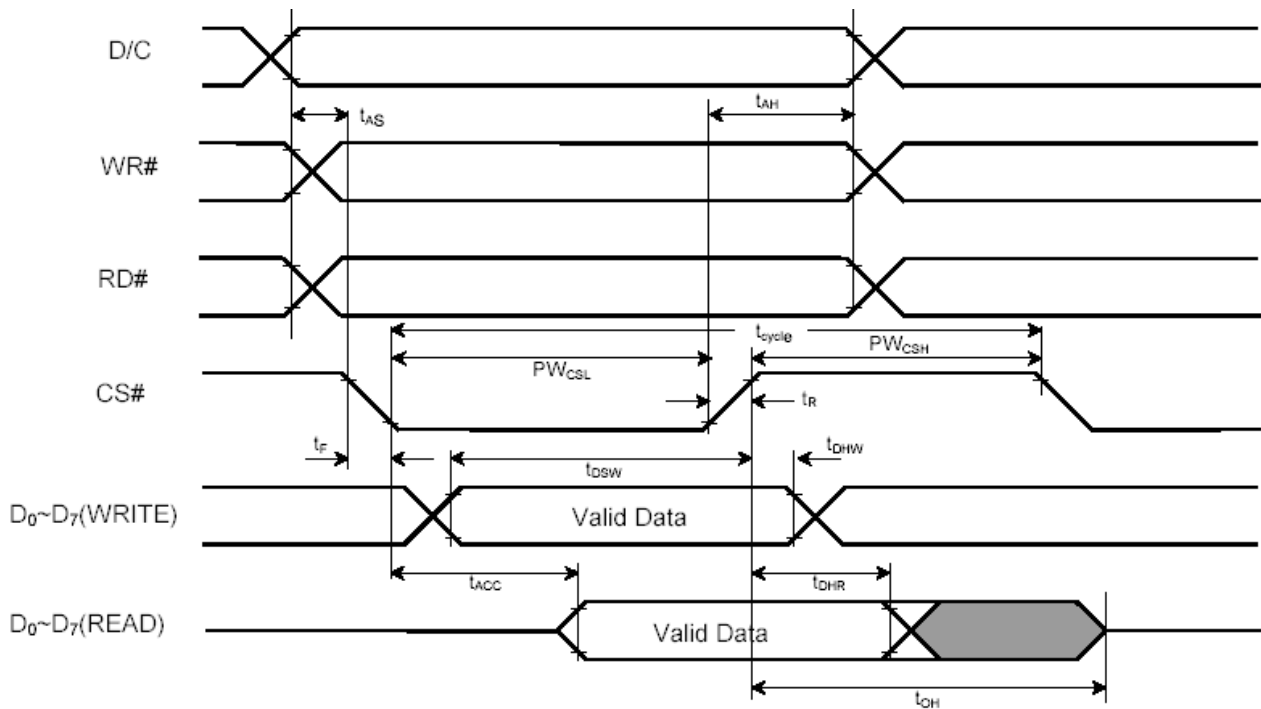
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



6800-series MPU parallel interface characteristics

8080-Series MPU Parallel Interface Timing Characteristics (VDD - VSS = 2.4 to 3.5V, TA =25°C)

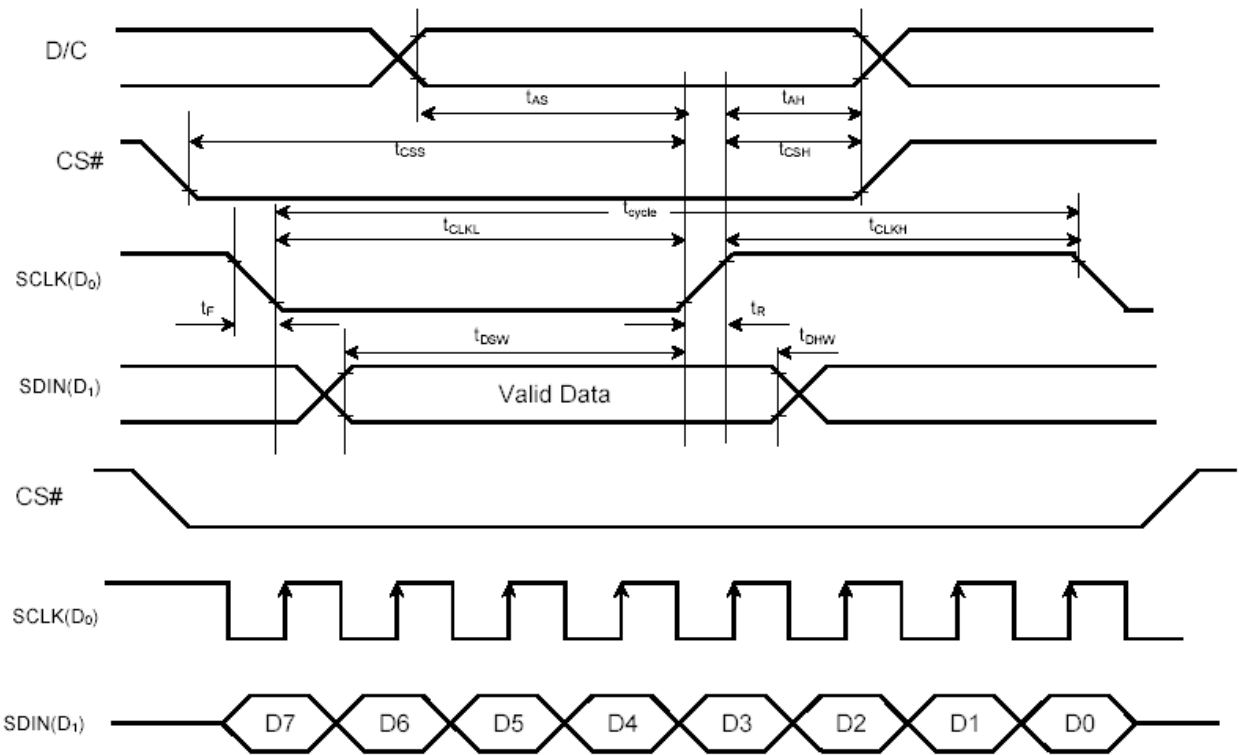
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



8080-series MPU parallel interface characteristics

Serial Interface Timing Characteristics (VDD - VSS = 2.4 to 3.5V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns </td
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



Serial interface characteristics

12. OLED Lifetime

Conditions :

Temperature : 25°C

Brightness decay to 50% of original value

Panel lifetime is a function of the brightness as follows :

Average Brightness (cd/m²)	Lifetime (Hours)
80	10,000
40	20,000