



CrystalFontz America, Incorporated

GRAPHIC OLED MODULE SPECIFICATIONS



Shown actual size.

CrystalFontz Model Number	CFAL12864N-A-B1
Hardware Version	Revision A
Data Sheet Version	Revision 1.1 March 2009
Product Pages	www.crystalfontz.com/product/CFAL12864N-A-B1.html

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REVISION HISTORY

HARDWARE
Current hardware version: vA

DATA SHEET	
2009/03/05	<p>Current Data Sheet version: v1.1 Changes since last Data Sheet (v1.0):</p> <ul style="list-style-type: none">● Corrected error in Circuit Example – Externally Supplied VPANEL (Pg. 11). Drawing incorrectly showed a direct connection between GND and V_{LOGIC}. Part Change Notification has been issued, PCN #10013.● Added illustration to explain Power Up and Power Down Sequencing (Pg. 13).● Added a photo with pins labeled. See Quick Reference for Pin Functions (Front Photo) (Pg. 17).● Added APPENDIX C: OLED MODULE TERMS AND SYMBOLS (Pg. 30).● Minor changes to tables and text to improve readability.
2009/01/15	<p>Data Sheet version: v1.0 New Data Sheet.</p>

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MAIN FEATURES

COMPARISON TO LCD (LIQUID CRYSTAL DISPLAY) MODULE

The CFAL12864N-A-B1 is a two-color 128 x 64 dot matrix Organic Light-Emitting Diode (OLED) display module. The light weight, small size, and ultrathin form factor allows you to use this OLED module in applications where it would be difficult or impossible to fit a traditional STN LCD. The low power requirements make it possible for the CFAL12864N-A-B1 to be used in battery powered portable devices such as remote controls and scientific meters (for example, temperature, sound, and gas detection).

Compared to most LCD modules, this OLED module has a quicker response time and an extremely wide viewing angle. At the low end of an STN LCD's temperature range, an LCD module's contrast will typically be poor and the response time will be very slow. The contrast and response time of the CFAL12864N-A-B1 OLED module will remain essentially constant through the operating range, allowing it to operate in cold environments without the need for a heater.

FEATURES

- ☐ 128 x 64 OLED COG (Chip on Glass) with a FPC tail (Flexible Printed Circuit).
 - OLED panel is 26.7 (W) x 19.26 (H) x 2.15 (D) millimeters (1.05" (W) x .76" (H) x .085" (D)).
 - Overall height (OLED panel + FPC) is 29.06 millimeters (1.14").
- ☐ 8-bit parallel (8080 or 6800) interface or SPI Interface.
- ☐ Built-in Sino Wealth [SH1101A](#) Controller.
- ☐ Emissive display with two distinct color areas: 128 x 16 yellow dots on top and 128 x 48 blue dots on bottom. (Displays yellow or blue dots on a dark area or dark dots on a yellow or blue area).
- ☐ Viewing Angle is >160°.
- ☐ Wide temperature operation: -20°C to +70°C.
- ☐ FPC has .62 mm maximum bend radius.
- ☐ RoHS compliant.

MODULE CLASSIFICATION INFORMATION

CFA L 128 64 N - A - B1 *
① ② ③ ④ ⑤ ⑥ ⑦ ⑧

①	Brand	CrystalFontz America, Inc.
②	Display Type	L – OLED
③	Number of Dots (Width)	128 dots
④	Number of Dots (Height)	64 dots
⑤	Model Identifier	N
⑥	Display Color	A – Area colors
⑦	Special Codes 1	B1 – Manufacturer's codes
⑧	Special Codes 2	* – May have additional manufacturer's codes at this location



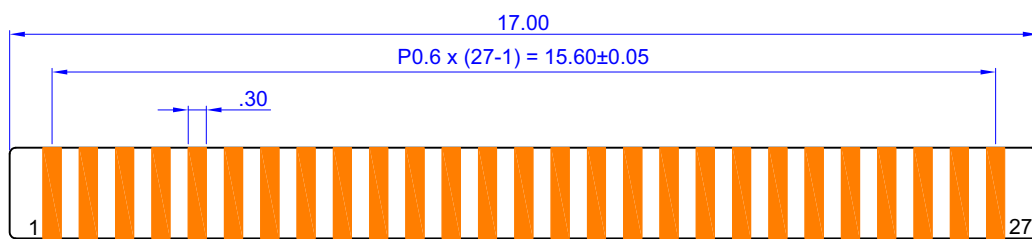
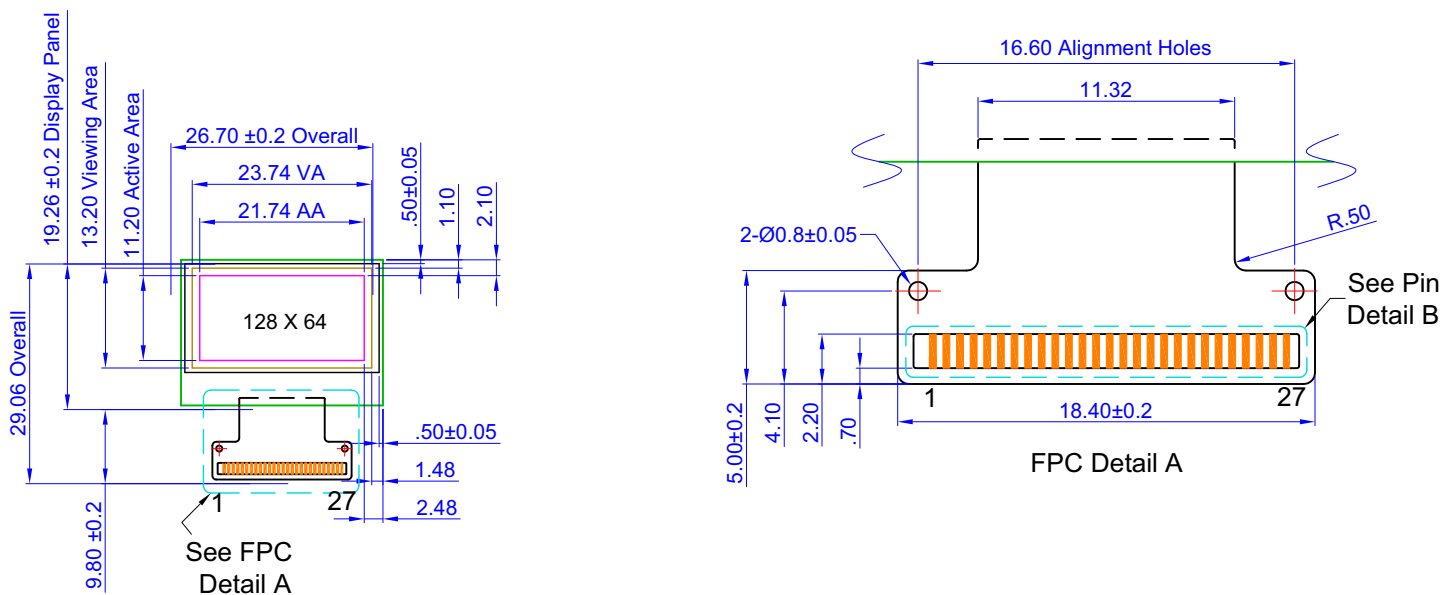
MECHANICAL SPECIFICATIONS

PHYSICAL CHARACTERISTICS

ITEM	SIZE
Number of Dots	128 x 64 dots
Panel Dimensions (excludes FPC Tail)	26.70 (W) x 19.26 (H) x 2.15 (D) mm
Overall Height Dimension (Panel + FPC Tail)	29.06 (H) mm
Polarizer	25.70 (W) x 14.40 (H) mm
Viewing Area	23.74 (W) x 13.20 (H) mm
Active Area	21.74 (W) x 11.20 (H) mm
Dot Size	0.15 (W) x 0.15 (H) mm
Dot Pitch	0.17 (W) x 0.17 (H) mm
Aperture Rate*	77.9%
Weight	2 grams (typical)
<i>*Aperture rate is defined by dividing an effective display area with unit dot area.</i>	



Figure 1. Module Outline Drawings (next 4 pages)



NC	GND	SW	V _{D02}	FB	SENSE	V _{BREF}	V _{LOGIC}	IS1	IS2	CS	RST	D/C	WR ₉₀₈₀ (R/W ₆₈₀₀)	RD ₈₀₈₀ (E ₆₈₀₀)	V _{CONH}	V _{PANEL}	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	I _{REF}	NC
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27

Pin Detail B

Note: Tolerance is ± 0.3 mm unless specified.



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Part No.(s): CFAL12864N-A-B1

Scale:
Not to scale

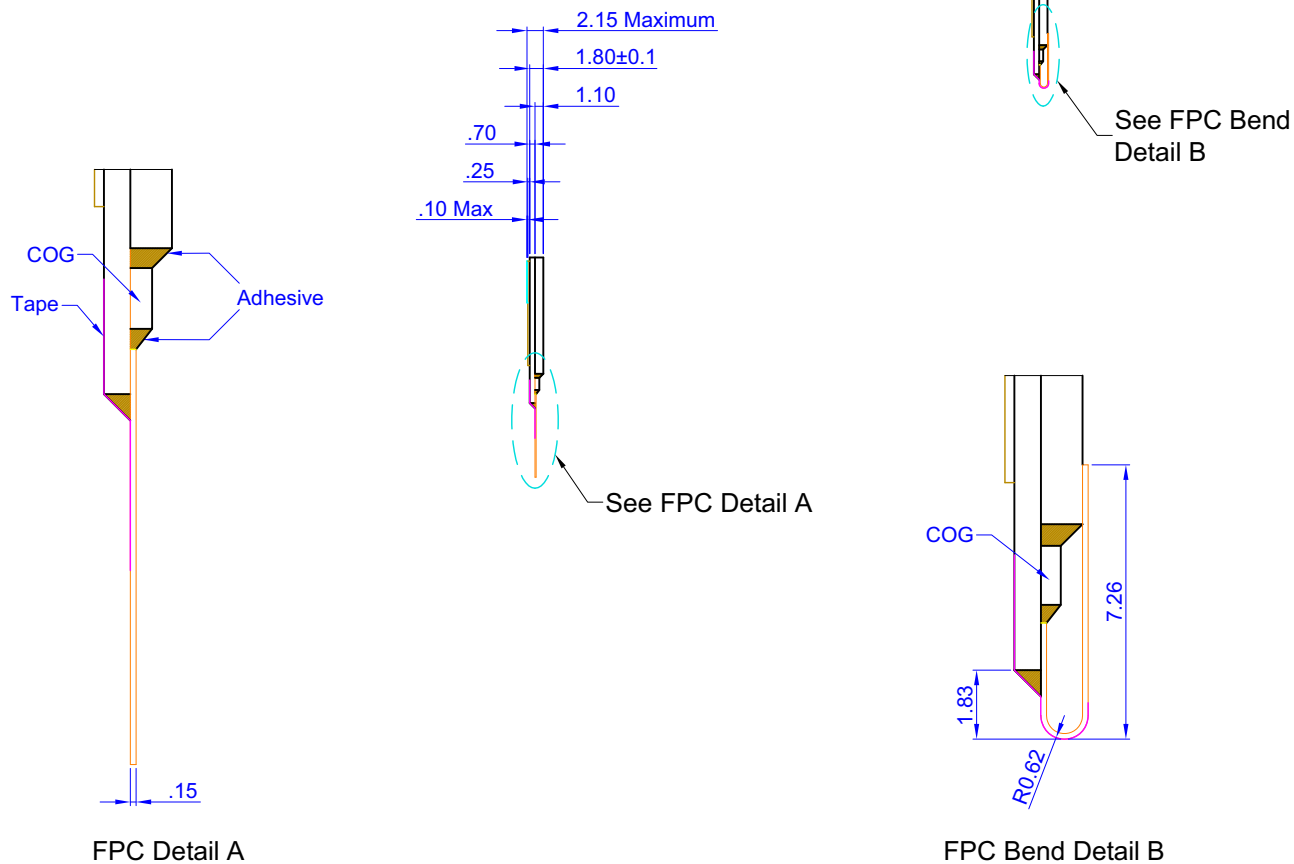
Units:
Millimeters

Drawing Number:
CFAL12864N master

Date:	2009/02/28
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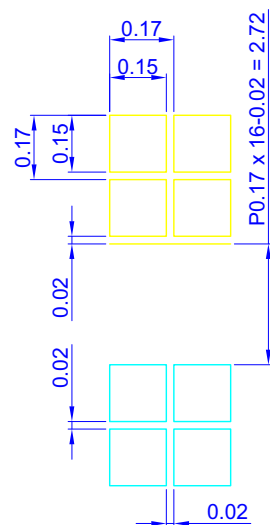
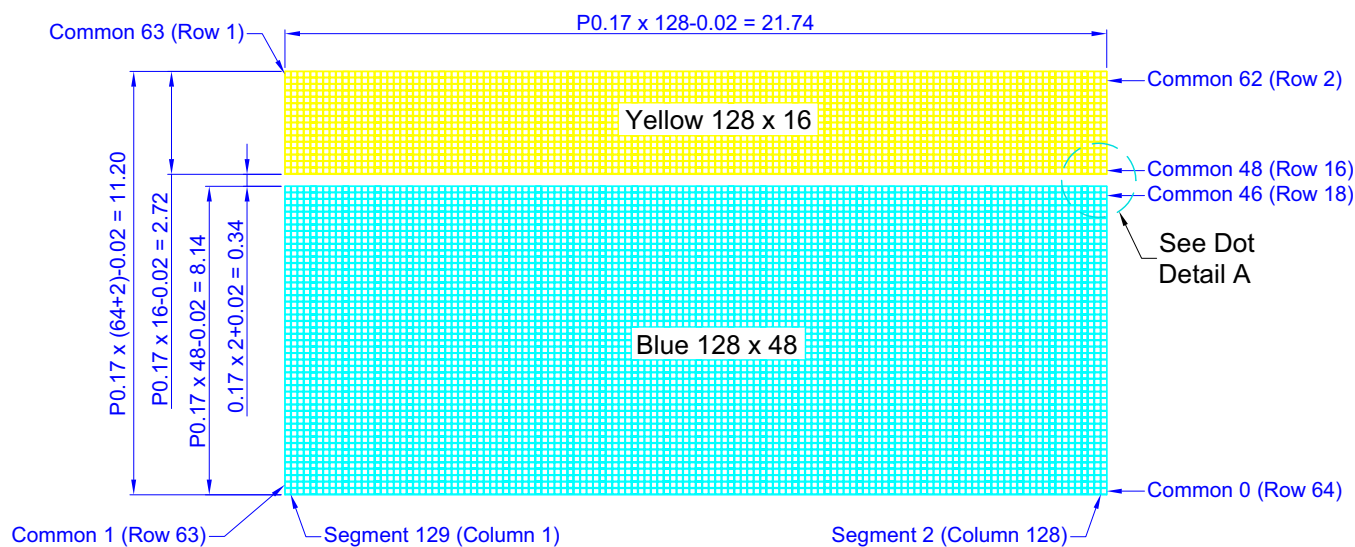
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Sheet: 1 of 4



Note: Tolerance is ± 0.3 mm unless specified.





Note: Tolerance is ± 0.3 mm unless specified.



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Units:
Millimeters

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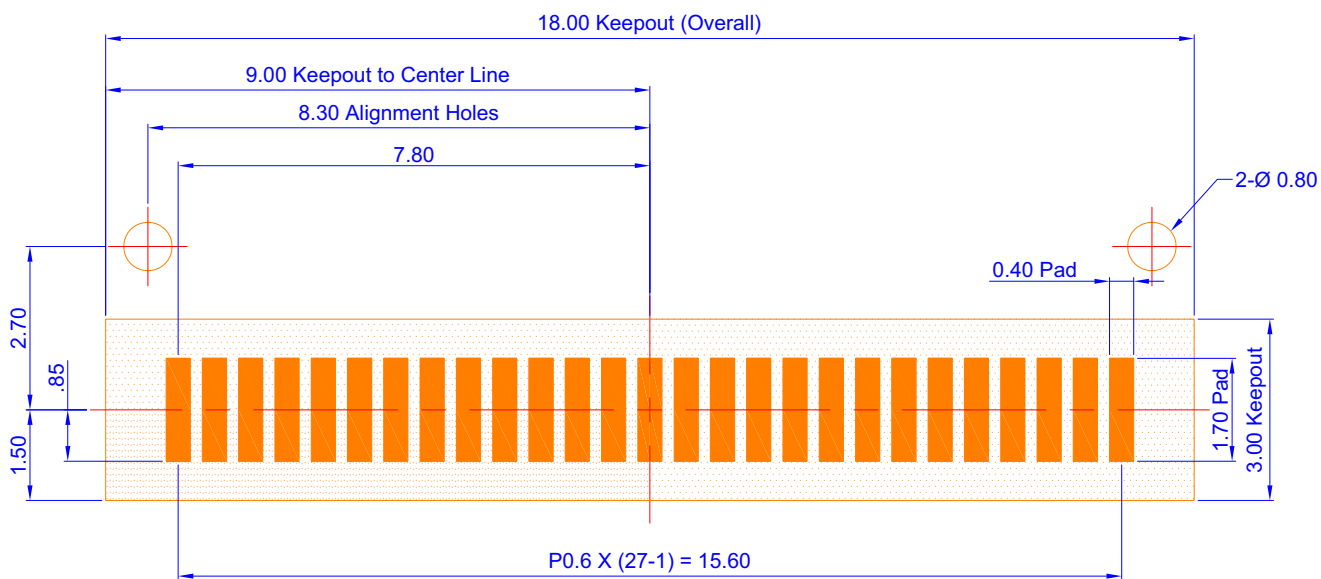
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3 of 4



PCB Footprint / Land Pattern



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Part No.(s): CFAL12864N-A-B1

Scale:
Not to scale

Units:
Millimeters

Drawing Number:
CFAL12864N_master

Date:
2009/02/28

Hardware Rev.:
vA

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4 of 4



ELECTRICAL SPECIFICATIONS

SYSTEM BLOCK DIAGRAM

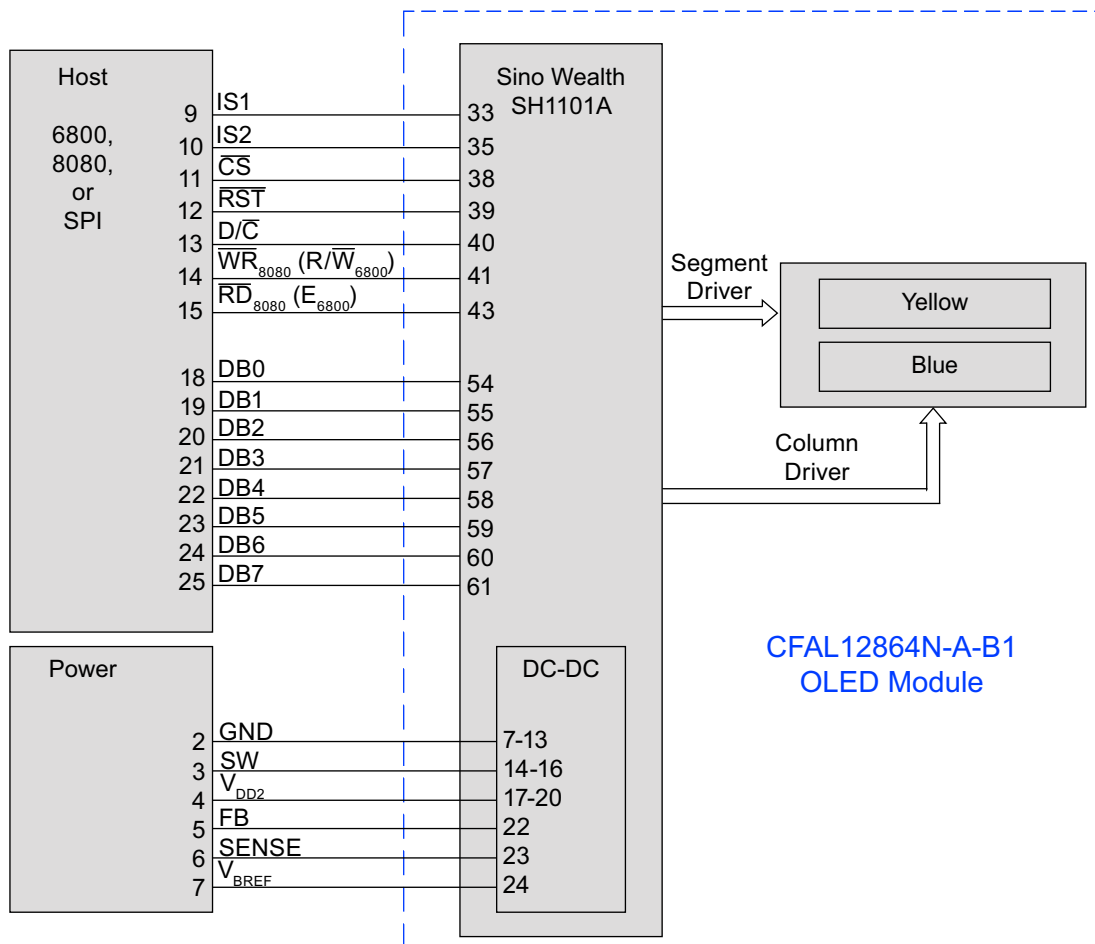


Figure 2. System Block Diagram



CIRCUIT EXAMPLE – EXTERNALLY SUPPLIED V_{PANEL}

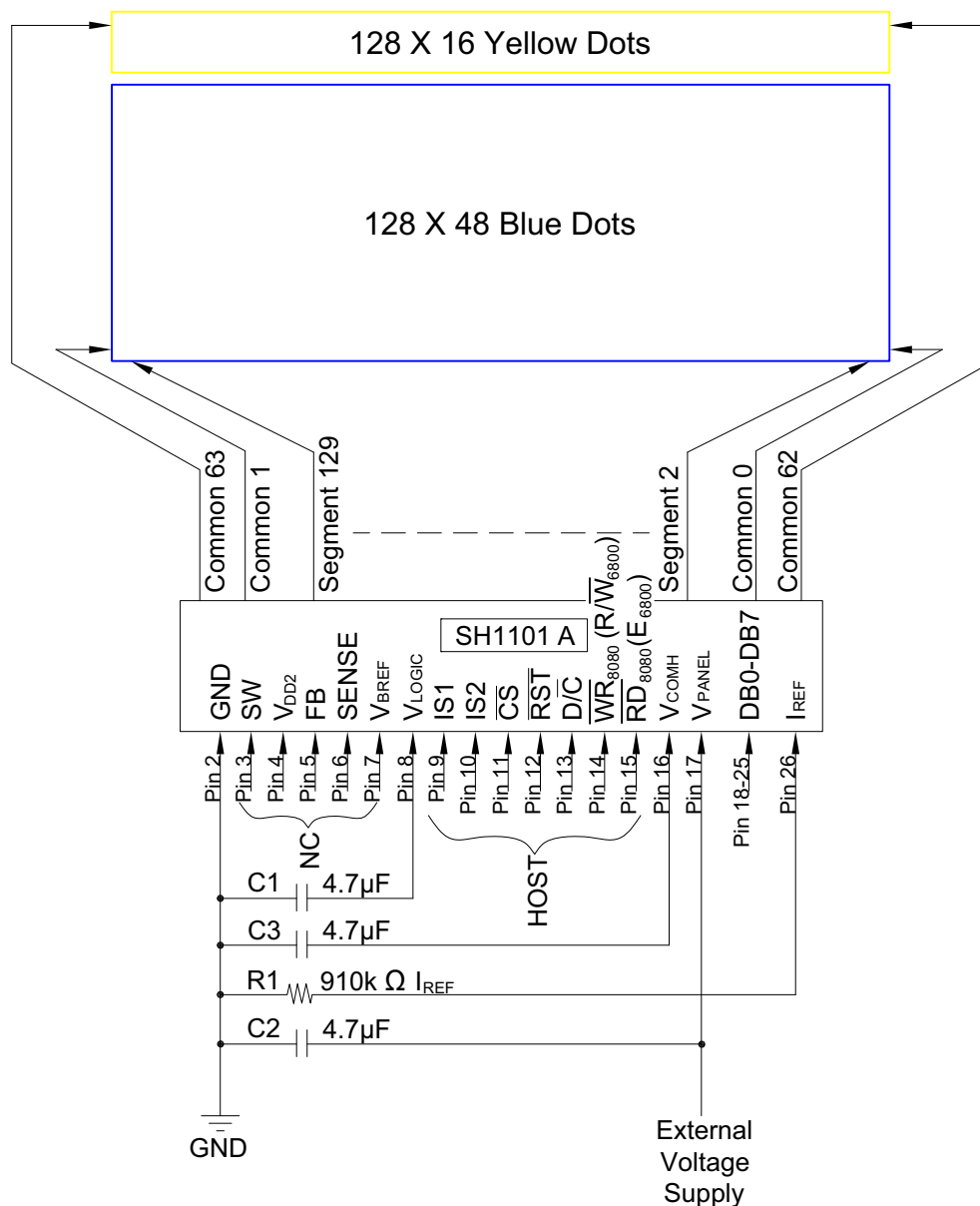


Figure 3. Externally Supplied V_{PANEL} Circuit Example

Circuit Example Notes:

- Host Interface Selection: IS1 and IS2
- Pin connected to Host interface: DB0~DB7, $\overline{\text{RD}}_{8080}$ (E_{6800}), $\overline{\text{WR}}_{8080}$ ($\text{R}/\overline{\text{W}}_{6800}$), $\overline{\text{D/C}}$, $\overline{\text{RST}}$, $\overline{\text{CS}}$
- When using external DC-DC converter: V_{BREF} , SENSE, FB, V_{DD2} , and SW should be left floating. Please observe V_{PANEL} sequencing as described in [Details of Interface Pin Functions \(Pg. 15\)](#)
- $910\text{k}\Omega = (\text{Voltage at } I_{\text{REF}} - \text{GND}) / I_{\text{REF}}$



CIRCUIT EXAMPLE – DC-DC CONVERTER

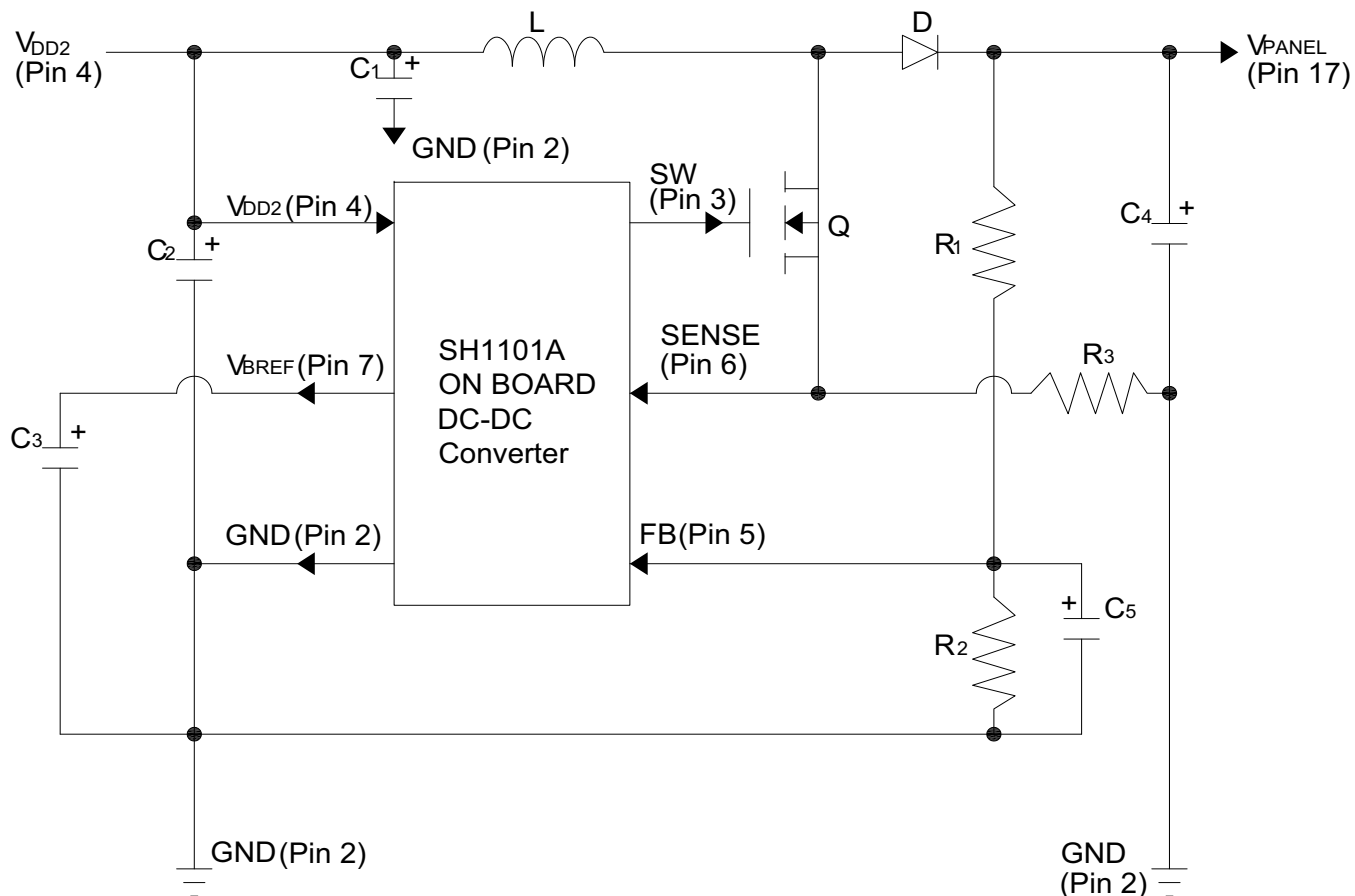


Figure 4. DC-DC Converter Circuit Example

Note: In this circuit, input voltage 3v V_{DD2} generates V_{PANEL} at about 12v@10 mA-25 mA



Signal	Part	Typical Value
L	Inductor LQH3C100K24	10 μ H
D	Schottky Diode, 20v@0.5A, MBR0520	
Q	MOSFET, N-FET with low $R_{DS(ON)}$ and low V_{TH} , MGSF1N02LT1	
R ₁	Resistor, 1%, 1/8W	930k Ω
R ₂	Resistor, 1%, 1/8W	110k Ω
R ₃	Resistor, 1%, 1/2W	0.12 Ω
C ₁	Capacitor, Low ESR, 6.3v	1 - 10 μ F
C ₂	Capacitor, Ceramic, 16v	0.1 - 1 μ F
C ₃	Capacitor, Ceramic, 16v	1 μ F
C ₄	Capacitor, Low ESR, 6.3v	6.8 μ F
C ₅	Capacitor, Ceramic, 16v	1000pF

POWER UP AND POWER DOWN SEQUENCING

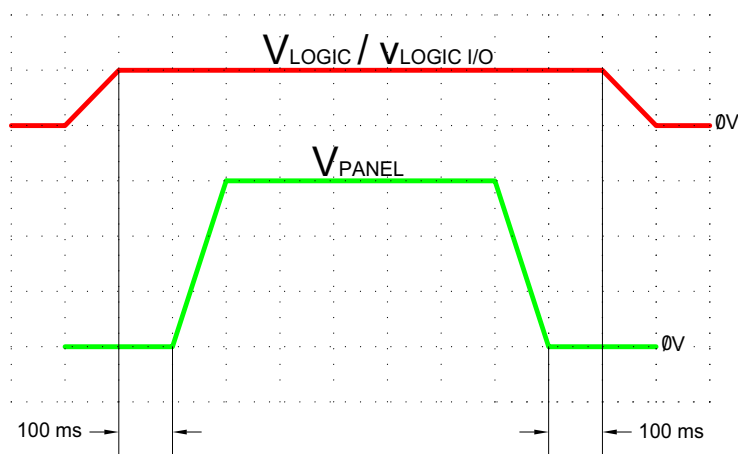


Figure 5. Power Up and Power Down Sequencing



ABSOLUTE MAXIMUM RATINGS

ABSOLUTE MAXIMUM RATINGS	SYMBOL	MINIMUM	MAXIMUM
Operating Temperature*	T _{OP}	-20°C	+70°C
Storage Temperature*	T _{ST}	-30°C	+80°C
Logic Supply Voltage	V _{LOGIC}	-0.3v	+3.5v
Driver Supply Voltage	V _{PANEL}	-0.3v	+15v
*Prolonged exposure at temperatures outside of this range may cause permanent damage to the module.			

DC CHARACTERISTICS (3.3V OPERATION)

ITEM	SYMBOL	TEST CONDITION	MINIMUM	TYPICAL	MAXIMUM
Logic Supply Voltage	V _{LOGIC}	T _{OP} = -30°C to +70°C	2.6v	3.3v	3.5v ¹
DC-DC Supply Voltage	V _{DD2}	T _{OP} = -30°C to +70°C	2.6v		3.5v
OLED Driver Supply Voltage²	V _{PANEL}	T _{OP} = -30°C to +70°C	8v	9v	10v
High Level Input Voltage	V _{IH}	I _{OUT} =0.5 mA 3.3MHz	0.8 V _{LOGIC}		V _{LOGIC}
Low Level Input Voltage	V _{IL}	I _{OUT} =0.5 mA 3.3MHz	0v		0.2 V _{LOGIC}
High Level Output Voltage	V _{OH}	I _{OUT} =0.5 mA 3.3MHz	0.8 V _{LOGIC}		V _{LOGIC}
High Level Output Voltage	V _{OL}	I _{OUT} =0.5 mA 3.3MHz	0v		0.2 V _{LOGIC}
Duty	1/32				
¹ Do not exceed 3.5v absolute maximum. ² The V_{PANEL} input must be a stable value with no ripple or noise. This is a summary of the module's major operating parameters. For detailed information see APPENDIX D: SINO WEALTH SH1101A CONTROLLER SPECIFICATION SHEET (Pg. 34) .					



DETAILS OF INTERFACE PIN FUNCTIONS

PIN	SIGNAL	LEVEL	DIRECTION	DESCRIPTION															
1	NC			No connection															
2	GND	0v		Ground. Must be connected to an external ground															
3	SW		O	Switch output drives gate of the external NMOS of the booster circuit															
4	V _{DD2}	+2.6v to +3.5v		Power supply for internal buffer of the DC-DC voltage converter.															
5	FB	variable	I	Feedback resistor input for the booster circuit. Use to adjust booster output voltage level, V _{PANEL} .															
6	SENSE			Source current for external NMOS of booster circuit															
7	V _{BREF}			Internal voltage reference for booster circuit. A stabilization capacitor, typically 1μF, should be connected to GND.															
8	V _{LOGIC}	+2.6v to +3.5v		Power supply input. Must be connected to an external source.															
9	IS1	H/L	I	<table><tr><th>IS1</th><th>IS2</th><th>Interface Mode</th></tr><tr><td>0</td><td>0</td><td>Serial</td></tr><tr><td>0</td><td>1</td><td>6800 Parallel</td></tr><tr><td>1</td><td>0</td><td>Not Allowed</td></tr><tr><td>1</td><td>1</td><td>8080 Parallel</td></tr></table>	IS1	IS2	Interface Mode	0	0	Serial	0	1	6800 Parallel	1	0	Not Allowed	1	1	8080 Parallel
IS1	IS2	Interface Mode																	
0	0	Serial																	
0	1	6800 Parallel																	
1	0	Not Allowed																	
1	1	8080 Parallel																	
10	IS2	H/L	I																
11	$\overline{\text{CS}}$	H/L	I	Chip select input. <i>Low:</i> Controller chip is selected. Communications with the host MPU is possible. <i>High:</i> Controller chip is not selected. MPU interface signals are ignored by the controller.															
12	$\overline{\text{RST}}$	H/L	I	Reset signal input. <i>Low:</i> Display controller is reset. The $\overline{\text{RST}}$ pin should be pulsed low shortly after power is applied. <i>High:</i> The $\overline{\text{RST}}$ pin should be brought high for normal operation.															
13	D/ $\overline{\text{C}}$	H/L	I	Data/Command control. Determines whether data bits are data or command. <i>1 – High:</i> DB0 to DB7 inputs are display data. <i>2 – Low:</i> DB0 to DB7 inputs transferred to command registers.															



PIN	SIGNAL	LEVEL	DIRECTION	DESCRIPTION
14	\overline{WR}_{8080} (R/\overline{W}_{6800})	H/L	I	Host interface input. <i>8080 Host:</i> Active low. Signal on the data bus is latched at the rising edge of \overline{WR} signal. <i>6800 Host:</i> read/write control signal output $R/\overline{W} = \text{High}$: Read (Host \leftarrow Module) $R/\overline{W} = \text{Low}$: Write (Host \rightarrow Module)
15	\overline{RD}_{8080} (E_{6800})	H/L	I	Host interface input. Read data is output on data bus when \overline{RD} is low. <i>8080 Host:</i> Active low. Signal on the data bus is latched at the rising edge of \overline{WR} signal. <i>6800 Host:</i> Enable control signal input active high. $E = \text{High}$: Read or Write Active $E = \text{Low}$: No Read or Write Active
16	V_{COMH}		O	High level voltage output for common signals. A low ESR capacitor should be connected between this pin and GND. Do not connect external power supply directly to this pin.
17	V_{PANEL}	+8v to +10v	I	Only high voltage input on chip. Power must be supplied externally or the internal DC-DC converter must be configured. <i>Note: You must observe power sequencing for this pin.</i> <i>Power Up</i> – Display must be powered up and initialized before power is applied to the pin. <i>Power Down</i> – Power must be removed from this pin before the display is powered off.
18	DB0	H/L	I/O	Bidirectional data bus connects to 8-bit or 16-bit standard host data bus. <i>In serial mode ($IS1=0$, $IS2=0$):</i> DB0 serves as the serial clock input signal (SCL) and DB1 serves as the serial data input pin (SI). DB2-DB7 are high impedance. <i>In serial mode</i> , data can be written to the display but not read. Pin 14 (\overline{WR}_{8080} (R/\overline{W}_{6800})) and pin15 (\overline{RD}_{8080} (E_{6800})) are unused and should be tied low. <i>In 6800 Parallel mode:</i> Pin 14 is used as R/\overline{W}_{6800} . Pin 15 is used as E_{6800} . Data is input or output on DB0-DB7. <i>In 8080 Parallel mode:</i> Pin 14 is used as \overline{WR}_{8080} . Pin 15 is used as \overline{RD}_{8080} . Data is input or output on DB0-DB7.
19	DB1	H/L	I/O	
20	DB2	H/L	I/O	
21	DB3	H/L	I/O	
22	DB4	H/L	I/O	
23	DB5	H/L	I/O	
24	DB6	H/L	I/O	
25	DB7	H/L	I/O	
26	I_{REF}			Segment output current reference for brightness adjustment. A resistor should be connected between this pin and GND. Set the current at 10 μ A.
27	NC			No connection



QUICK REFERENCE FOR PIN FUNCTIONS (FRONT PHOTO)

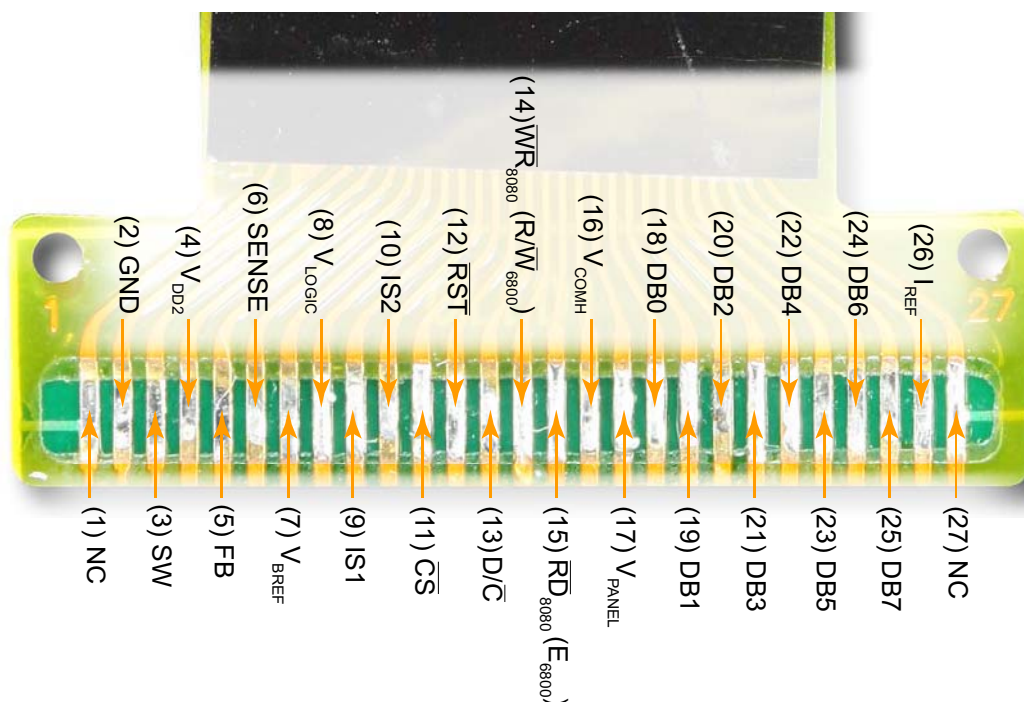


Figure 6. Front View of FPC (Labeled)

ESD (ELECTRO-STATIC DISCHARGE) SPECIFICATIONS

This circuitry is industry standard CMOS logic and is susceptible to ESD damage. Please use industry standard antistatic precautions as you would for any other PCB such as expansion cards or motherboards. For more information, see [CARE AND HANDLING PRECAUTIONS \(Pg. 20\)](#).



OPTICAL SPECIFICATIONS

OPTICAL CHARACTERISTICS

ITEM	SYMBOL	TEST CONDITION	MINIMUM	TYPICAL	MAXIMUM
Viewing Angle				>160°	
Dark Room Contrast Ratio ¹	CR			>100:1	
Response Time ²				<1 ms	
Normal Mode Power Consumption		all dots on V _{LOGIC} = 3.3v V _{PANEL} = 9v Frame Rate = 100 Hz Contrast Setting = 0x64		70.2 mW	87.3 mW
Luminous Intensity (IV)	L _{BR}	with polarizer		35 cd/m ²	60 cd/m ²
Blue Chromaticity	x	CIE (1931)	0.12	0.16	0.20
	y		0.22	0.26	0.30
Yellow Chromaticity	x		0.43	0.47	0.51
	y		0.40	0.50	0.54

¹Contrast Ratio = (brightness with dots light)/(brightness with dots dark).

²Response Time: The amount of time it takes a dot to change from active to inactive or back again.



Definition of Viewing Angle

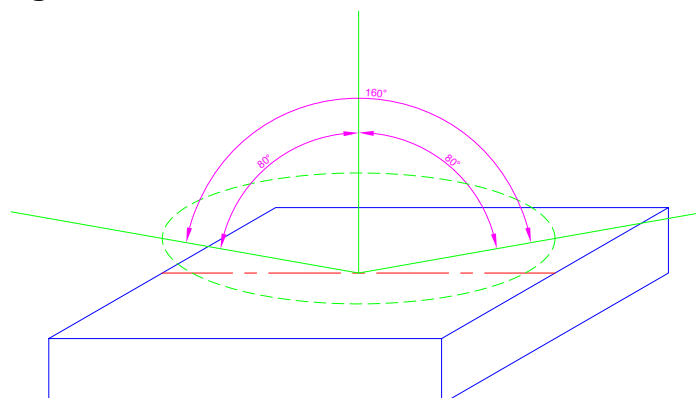


Figure 7. CFAL12864N-A-B1 has a 160° Viewing Angle

OLED CONTROLLER INTERFACE

This module uses a Sino Wealth SH1101A controller. For your reference, we added [APPENDIX D: SINO WEALTH SH1101A CONTROLLER SPECIFICATION SHEET \(Pg. 34\)](#) to this Data Sheet.

MODULE RELIABILITY AND LONGEVITY

MODULE RELIABILITY

ITEM	SPECIFICATION
CFAL12864N-A-B1	10,000 hours >50% of Initial Brightness (New Module)

OLED displays are an emissive technology. Each dot is susceptible to dimming based on its individual use (burn-in). Frequently used dots will dim more quickly than dots that are not used as often. Please avoid using a bright, static, high-contrast image for a long time. If you want to leave the display powered on, please use scrolling text or alternating images to "wear level" the dots. To conserve power and display lifetime, turn off or dim the display when it is not in use.

MODULE LONGEVITY (EOL / REPLACEMENT POLICY)

Crystalfontz is committed to making all of our modules available for as long as possible. For each module we introduce, we intend to offer it indefinitely. We do not preplan a module's obsolescence. The majority of modules we have introduced are still available.

We recognize that discontinuing a module may cause problems for some customers. However, rapidly changing technologies, component availability, or low customer order levels may force us to discontinue ("End of Life", EOL) a module. For example, we must occasionally discontinue a module when a supplier discontinues a component or a manufacturing process becomes obsolete. When we discontinue a module, we will do our best to find an acceptable replacement module with the same fit, form, and function.



In most situations, you will not notice a difference when comparing a "fit, form, and function" replacement module to the discontinued module. However, sometimes a change in component or process for the replacement module results in a slight variation, perhaps an improvement, over the previous design.

Although the replacement module is still within the stated Data Sheet specifications and tolerances of the discontinued module, changes may require modification to your circuit and/or firmware. Possible changes include:

- *Controller.* A new controller may require minor changes in your code.
- *Component tolerances.* Module components have manufacturing tolerances. In extreme cases, the tolerance stack can change the visual or operating characteristics.

Please understand that we avoid changing a module whenever possible; we only discontinue a module if we have no other option. We will post Part Change Notices on the product's webpage as soon as possible. If interested, you can subscribe to future part change notifications.

CARE AND HANDLING PRECAUTIONS

For optimum operation of the module and to prolong its life, please follow the precautions below.

ESD (ELECTRO-STATIC DISCHARGE)

The circuitry is industry standard CMOS logic and susceptible to ESD damage. Please use industry standard antistatic precautions as you would for any other PCB such as expansion cards or motherboards. Ground your body, work surfaces, and equipment.

DESIGN AND MOUNTING

- The exposed surface of the "glass" is actually a polarizer laminated on top of the glass. To protect the soft plastic polarizer from damage, the module ships with a protective film over the polarizer. Please peel off the protective film slowly. Peeling off the protective film abruptly may generate static electricity.
- The polarizer is made out of soft plastic and is easily scratched or damaged. When handling the module, avoid touching the polarizer. Finger oils are difficult to remove.
- To protect the soft plastic polarizer from damage, place a transparent plate (for example, acrylic, polycarbonate, or glass) in front of the module, leaving a small gap between the plate and the display surface. We use GE HP-92 Lexan, which is readily available and works well.
- Do not disassemble or modify the module.
- Do not modify the tab of the metal holder or make connections to it.
- For prototype work, hand soldering may be acceptable. Preset soldering iron to <260°C. Do not apply heat for more than 3 to 4 seconds.
- For production soldering, please use a commercial hot bar solder station, along with the appropriate fixture.
- Solder only to the exposed terminals of the FPC connector. Please note that the FPC is quite fragile; use extreme care when soldering by hand. The use of Kapton® tape to help locate and secure the FPC may be useful.
- Do not reverse polarity to the power supply connections. Reversing polarity will immediately ruin the module.
- Use care to keep the exposed terminals clean. Contamination, including fingerprints may make the soldering difficult, and the reliability of the soldered connection poor.



AVOID SHOCK, IMPACT, TORQUE, AND TENSION

- Do not expose the module to strong mechanical shock, impact, torque, or tension.
- Do not drop, toss, bend, or twist the module.
- Do not place weight or pressure on the module.

CLEANING

The polarizer (laminated to the glass) is soft plastic. The soft plastic is easily scratched or damaged. Be very careful when you clean the polarizer.

- Do not clean the polarizer with liquids. Do not wipe the polarizer with any type of cloth or swab (for example, Q-tips).
- Use the removable protective film to remove smudges (for example, fingerprints) and any foreign matter. If you no longer have the protective film, use standard transparent office tape (for example, Scotch® brand "Crystal Clear Tape"). If the polarizer is dusty, you may carefully blow it off with clean, dry, oil-free compressed air.

OPERATION

- We do not recommend connecting this module to a PC's parallel port as an "end product." This module is not "user friendly" and connecting it to a PC's parallel port is often difficult, frustrating, and can result in a "dead" display due to mishandling. For more information, see our forum thread at <http://www.crystalfontz.com/forum/showthread.php?s=&threadid=3257>.
- Your circuit should be designed to protect the module from ESD and power supply transients.
- Observe the operating temperature limitations: from -20°C minimum to +70°C maximum with minimal fluctuations. Operation outside of these limits may shorten the life and/or harm the display.
 - At lower temperatures of this range, response time is delayed.
 - At higher temperatures of this range, display becomes dark. (You may need to adjust the contrast.)
- Operate away from dust, moisture, and direct sunlight.

STORAGE AND RECYCLING



- Store in an ESD-approved container away from dust, moisture, and direct sunlight, fluorescent lamps, or any ultraviolet ray.
- Observe the storage temperature limitations: from -30°C minimum to +80°C maximum with minimal fluctuations. Rapid temperature changes can cause moisture to form, resulting in permanent damage.
- Do not allow weight to be placed on the modules while they are in storage.
- Please recycle your outdated CrystalFontz modules at an approved facility.



APPENDIX A: QUALITY ASSURANCE STANDARDS

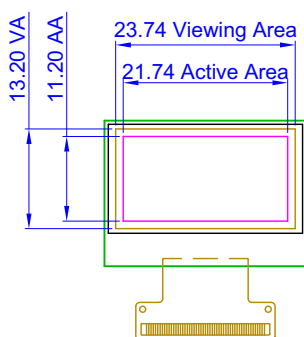
INSPECTION CONDITIONS

- Environment
 - Temperature: $25 \pm 5^{\circ}\text{C}$
 - Humidity: 30~85% RH (noncondensing)
- For visual inspection of active display area
 - Source lighting: two 20-Watt or one 40-Watt fluorescent light
 - Display adjusted for best contrast
 - Viewing distance: 30 ± 5 cm (about 12 inches)
 - Viewing angle: inspect at 45° angle of vertical line right and left, top and bottom

COLOR DEFINITIONS

We try to describe the appearance of our modules as accurately as possible. For the photos, we adjust or optimal appearance. Actual display appearance may vary due to (1) different operating conditions, (2) small variations of component tolerances, (3) inaccuracies of our camera, (4) color interpretation of the photos on your monitor, and/or (5) personal differences in the perception of color.

DEFINITION OF ACTIVE AREA AND VIEWING AREA



ACCEPTANCE SAMPLING

DEFECT TYPE	AQL*
Major	$\leq .65\%$
Minor	$< 1.0\%$
* Acceptable Quality Level: maximum allowable error rate or variation from standard	

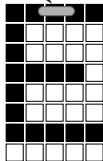
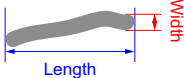


DEFECTS CLASSIFICATION

Defects are defined as:

- Major Defect: results in failure or substantially reduces usability of unit for its intended purpose
- Minor Defect: deviates from standards but is not likely to reduce usability for its intended purpose

ACCEPTANCE STANDARDS

#	DEFECT TYPE	CRITERIA			MAJOR / MINOR	
1	Electrical defects	1. No display, display malfunctions, or shorted segments. 2. Current consumption exceeds specifications.			Major	
2	Viewing area defect	Viewing area does not meet specifications.			Major	
3	Blemishes or foreign matter on display segments	<div>Blemish</div> 	Defect Size	Acceptable Qty	Minor	
			≤0.30 mm	3		
			≤2 defects within 10 mm of each other			
4	Dark lines or scratches in display area		Defect Width	Defect Length	Acceptable Qty	Minor
			≤0.03 mm	≤3.0 mm	3	
			0.03 to 0.05	≤2.0 mm	2	
			0.05 to 0.08	≤2.0 mm	1	
			0.08 to 0.10	≤3.0 mm	0	
			≥0.10	>3.0 mm	0	
5	Bubbles between polarizer film and glass		Defect Size	Acceptable Qty	Minor	
			≤0.20 mm	Ignore		
			0.20 to 0.40 mm	3		
			0.40 to 0.60 mm	2		
			≥0.60 mm	0		



#	DEFECT TYPE	CRITERIA	MAJOR / MINOR	
6	Display pattern defect		<div>Minor</div>	
		<div>Dot Size</div> <div>Acceptable Qty</div>		
		<div>$((A+B)/2) \leq 0.20 \text{ mm}$</div>		<div>$\leq 3 \text{ total defects}$</div> <div>$\leq 2 \text{ pinholes per digit}$</div>
		<div>$C > 0 \text{ mm}$</div>		
		<div>$((D+E)/2) \leq 0.25 \text{ mm}$</div>		
		<div>$((F+G)/2) \leq 0.25 \text{ mm}$</div>		
7	PCB defects	<div>1. Oxidation or contamination on connectors.*</div> <div>2. Wrong parts, missing parts, or parts not in specification.*</div> <div>3. Jumpers set incorrectly.</div> <div>4. Solder (if any) on bezel, LED pad, zebra pad, or screw hole pad is not smooth.</div> <div>*Minor if display functions correctly. Major if the display fails.</div>	Minor	
8	Soldering defects	<div>1. Unmelted solder paste.</div> <div>2. Cold solder joints, missing solder connections, or oxidation.*</div> <div>3. Solder bridges causing short circuits.*</div> <div>4. Residue or solder balls.</div> <div>5. Solder flux is black or brown.</div> <div>*Minor if display functions correctly. Major if the display fails.</div>	Minor	



APPENDIX B: SAMPLE CODE

Graphic driver libraries may save you a lot of time and help you develop a more professional product. One library sources is [RAMTEX](#).

This code will initialize the display and then cycle through between two images. You can download the complete source from this link: <http://www.crystalfontz.com/product/CFAL12864NAB1.html#docs>.

Note: Please observe V_{PANEL} sequencing as described in [Details of Interface Pin Functions \(Pg. 15\)](#).

```
#include <avr/io.h>
#include <util/delay.h>

// all on PORTC
#define OLED_CD PC7
#define OLED_RW PC6 // WR in 8080 mode
#define OLED_E PC5 // RD in 8080 mode
#define OLED_WR PC6 // WR in 8080 mode
#define OLED_RD PC5 // RD in 8080 mode
#define OLED_CS PC3
#define OLED_RES PC2

#define CLR_CD PORTC &= ~(1<<OLED_CD);
#define SET_CD PORTC |= (1<<OLED_CD);

#define CLR_CS PORTC &= ~(1<<OLED_CS);
#define SET_CS PORTC |= (1<<OLED_CS);

#define CLR_RESET PORTC &= ~(1<<OLED_RES);
#define SET_RESET PORTC |= (1<<OLED_RES);

// 6800 mode pin functions
#define CLR_RW PORTC &= ~(1 << OLED_RW); // 6800 mode
#define SET_RW PORTC |= (1 << OLED_RW); // 6800 mode
#define CLR_E PORTC &= ~(1 << OLED_E); // 6800 mode
#define SET_E PORTC |= (1 << OLED_E); // 6800 mode

// 8080 mode pin functions
#define CLR_WR PORTC &= ~(1 << OLED_WR); // 8080 mode
#define SET_WR PORTC |= (1 << OLED_WR); // 8080 mode
#define CLR_RD PORTC &= ~(1 << OLED_RD); // 8080 mode
#define SET_RD PORTC |= (1 << OLED_RD); // 8080 mode

#define MODE6800 0

// for bmp function
typedef uint8_t bitmap_t[8][132];
/*-----*/
void delay(uint32_t twait)
{
    while (twait--)
        asm volatile ("nop");
}
```



```
}
/*-----*/
uint8_t boot_logo[8][132] =
    { /* Binary data for image, deleted for clarity. Please
      download full zip from the link above. */ };

uint8_t bitmap[8][132] =
    { /* Binary data for image, deleted for clarity. Please
      download full zip from the link above. */ };

uint8_t bitmap2[8][132] =
    { /* Binary data for image, deleted for clarity. Please
      download full zip from the link above. */ };
/*-----*/
void oled_cmd(uint8_t cmd)
{
    PORTA = cmd; // set up data on bus
    CLR_CS; // chip selected
    CLR_CD; // command mode

#ifdef MODE6800

    CLR_RW;

    // clock E
    SET_E;
    CLR_E;

#else

    SET_RD;

    // clock WR
    CLR_WR;
    SET_WR;

#endif

    SET_CS; // unselect chip
}
/*-----*/
void oled_data(uint8_t dat)
{
    PORTA = dat; // set up data on bus
    SET_CD; // data mode
    CLR_CS; // chip selected

#ifdef MODE6800

    CLR_RW;

    // clock E
    SET_E;
    CLR_E;
```



```
#else          // 8080 mode

SET_RD;

// clock WR
CLR_WR;
SET_WR;

#endif

SET_CS;    // unselect chip
}
/*-----*/
void OLED_clr(uint8_t color)
{
    int i,p;

    oled_cmd(0x40);

    for (p=0;p<8;p++) // pages
    {
        oled_cmd(0xB0 + p); // set page address
        oled_cmd(0x10);    // set high column address
        oled_cmd(0x00);    // set low column address
        for (i=0;i<132;i++)
        {
            oled_data(color);
        }
    }
}
/*-----*/
void bmp(bitmap_t b)
{
    unsigned char j=0;
    unsigned char page=0;

    for(page=0;page<8;page++)
    {
        oled_cmd(0xB0+page); // set page address
        oled_cmd(0x00);    // set high column address
        oled_cmd(0x10);    // set low column address

        for(j=0;j<132;j++)
        {
            oled_data(b[page][j]);
        }
    }
}
/*-----*/
void init_OLED()
{
    PORTD = 0;    // all off
    DDRD |= (1<<3); // VPANEL output
```



```
DDRA = 0xFF; // set PORTA for output
```

```
#ifdef MODE6800
```

```
    PORTC = 0b11011110;
```

```
#else
```

```
    PORTC = 0b11111110;
```

```
#endif
```

```
    DDRC = 0xFE;
```

```
    DDRD |= 0x06; // oled pins output
```

```
    delay(20000L);
```

```
    // reset the display
```

```
    CLR_RESET;
```

```
    delay(10000);
```

```
    SET_RESET;
```

```
    delay(20000);
```

```
    // enable VPANEL
```

```
    PORTD |= (1<<3);
```

```
    delay(200000L);
```

```
    oled_cmd(0xAE); // display OFF/ON 0xAE = display off, 0xAF = display on
```

```
    oled_cmd(0xAD); // DC-DC voltage converter OFF/ON
```

```
    oled_cmd(0x8A); // 0x8A = OFF, 0x8B = ON
```

```
    oled_cmd(0xA8); // Set multiplex ratio
```

```
    oled_cmd(0x3F); // set for 64
```

```
    oled_cmd(0xD3); // Set display offset
```

```
    oled_cmd(0x00); // no offset (0-63 are acceptable values)
```

```
    oled_cmd(0x40); // Set display start line (0x40 = start at line 0)
```

```
    oled_cmd(0xA1); // Segment mapping (0xA0 normal, 0xA1 reversed)
```

```
    oled_cmd(0xC8); // Common output scan direction (0xC0 = (0 - COM[N-1]), 0xC8 = (COM[N-1] - 0)
```

```
    oled_cmd(0xA6); // Set normal / reverse display (0xA6 = normal, 0xA7 = inverted/reverse)
```

```
    oled_cmd(0xA4); // Set entire display off / on (0xA4 = off, 0xA5 = on)
```

```
    oled_cmd(0x81); // Contrast control mode set
```

```
    oled_cmd(0x88); // (0x00 - 0xFF valid)
```

```
    oled_cmd(0xD5); // Set Display clock divide ratio/oscillator frequency
```

```
    oled_cmd(0x60); // Set for -5%
```



```
oled_cmd(0x00); // Set lower column address (0x00 - 0x0F valid)

oled_cmd(0xD9); // Set discharge/precharge period
oled_cmd(0x84); // (A3 - A0 pre charge, A7 - A4 dis charge) period adjustment

oled_cmd(0xAF); // Display on

delay(5000L);

OLED_clr(0x00); // clear display
}
/*****/
int main()
{
    init_OLED();

    delay(20000L);

    while (1)
    {
        bmp(boot_logo);
        delay(5000000L);
        bmp(bitmap);
        delay(5000000L);
        bmp(bitmap2);
        delay(5000000L);
    }

    return 0;
}
/*****/
```



APPENDIX C: OLED MODULE TERMS AND SYMBOLS

CrystalFontz Symbol	Equivalent	Equivalent	Equivalent	Description
C				Capacitor
cd/m ²	nit			Candela meter squared is the standard unit of measurement for luminous intensity (photometric brightness).
CIE				A color model based on human perception developed by the CIE (Commission Internationale de l'Eclairage) committee.
CLS				Clock select pin.
COF	COT			Chip On Flex. (Chip on Tab.)
COM				Common driver. Common signal output for OLED display.
CR				Contrast Ratio = (brightness with dots)/(brightness with dots dark).
$\overline{\text{CS}}$	CS#			Chip select input. <i>Low</i> : Controller chip is selected. Communications with host MPU is possible. <i>High</i> : Controller chip is not selected. Host MPU interface signals are ignored by the controller.
D				Diode
DB0 ~ DB _n	D0 ~ D _n			Bidirectional data bus connects to 8-bit or 16-bit standard host data bus. When serial interface is selected, DB0 serves as the serial clock input signal (SCL) and DB1 serves as the serial data input signal (SI). DB2 to DB _n are set to high impedance.
D/ $\overline{\text{C}}$	RS	A0	CD or D/C#	Data/Command control. Determines whether data bits are data or command. <i>1 – High</i> : Addresses the data register. <i>0 – Low</i> : Addresses the command register.
FB				Feedback resistor input for the booster circuit. Use to adjust booster output voltage level, V _{PANEL} .
GDR				Gate Drive. Output signal drives the gate of the external NMOS of the booster circuit.
GND	V _{SS}			Ground. Must be connected to an external ground.
I _{LOGIC}	I _{DD}			Operating current for V _{LOGIC} .

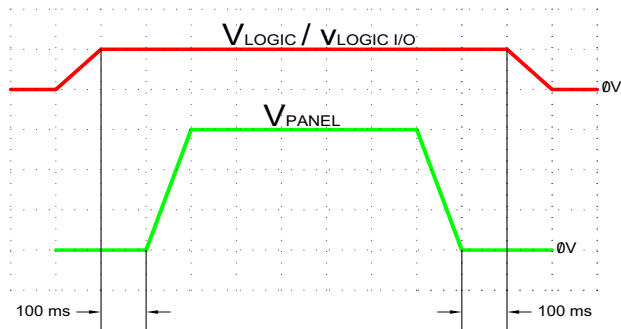


Crystalfontz Symbol	Equivalent	Equivalent	Equivalent	Description															
I _{LOGIC, SLEEP}	I _{DD, SLEEP}			Sleep mode current for V _{LOGIC} .															
I _{PANEL}	I _{CC}			Supply current for V _{PANEL} .															
I _{PANEL, SLEEP}	I _{CC, SLEEP}			Sleep mode current for V _{PANEL} .															
I _{REF}				Segment output current reference for brightness adjustment. A resistor should be connected between this pin and GND. Used to set the current.															
IS1	BS1	C86	M80	<table><tr><th>IS1</th><th>IS2</th><th>Interface Mode</th></tr><tr><td>0</td><td>0</td><td>Serial</td></tr><tr><td>0</td><td>1</td><td>6800 Parallel</td></tr><tr><td>1</td><td>0</td><td>Not Allowed</td></tr><tr><td>1</td><td>1</td><td>8080 Parallel</td></tr></table>	IS1	IS2	Interface Mode	0	0	Serial	0	1	6800 Parallel	1	0	Not Allowed	1	1	8080 Parallel
IS1	IS2	Interface Mode																	
0	0	Serial																	
0	1	6800 Parallel																	
1	0	Not Allowed																	
1	1	8080 Parallel																	
IS2	BS2	P/S	MS, MS ⁻ or M/S#																
L _{BR}	IV			Luminous Intensity Brightness.															
NC	nc			No Connection.															
Q				Transistor, including FET and MOSFET.															
R				Resistor															
RD ₈₀₈₀ (E ₆₈₀₀)	RD (E)	E (RD)	E	Host interface input. Read data is output on data bus when RD is low. 8080 Host: Active low. Signal on the data bus is latched at the rising edge of WR signal. 6800 Host: Enable control signal input active high. E = High: Read or Write Active E = Low: No Read or Write Active															
RST	RES	RST#	RES#	Reset signal Low: Display controller is reset. The RST pin should be pulsed low shortly after power is applied. High: The RST pin should be brought high for normal operation.															
SCL				Serial Clock signal.															
SEG				Segment driver. Segment signal output for OLED display.															
SENSE				Source current for external NMOS of booster circuit.															
SI	SDA	MOSI		Serial data Input signal.															



CrystalFontz Symbol	Equivalent	Equivalent	Equivalent	Description
SW				Switch output drives the gate of the external NMOS of the booster circuit.
T _{OP}	T _a			Operating temperature.
T _{ST}	T _{STG}			Storage temperature.
V _{BREF}				Internal voltage reference for booster circuit. A decoupling capacitor, typically 1μF, should be connected to GND.
V _{COMH}				High level voltage output for common signals. A low ESR capacitor should be connected between this pin and GND. Do not connect external power supply directly to this pin.
V _{DD2}	V _{DDB}			Power supply for internal buffer of the DC-DC voltage converter.
V _{IH}	V _{ICH}			High level input voltage.
V _{IL}	V _{LCH}			Low level input voltage.
V _{LOGIC}	V _{DD}	V _{DD1}		Power supply input. Must be connected to an external source.
V _{LOGIC I/O}	V _{DD I/O}	V _{I/O}		Supply voltage for I/O signals.
V _{OH}	V _{OHC}			High level output voltage.
V _{OL}	V _{OLC}			Low level output voltage.



Crystalfontz Symbol	Equivalent	Equivalent	Equivalent	Description
V_{PANEL}	V_{PP}	V_{CC}		<p>Driver supply voltage. Only high voltage input on chip. Power must be supplied externally or the internal DC-DC converter must be configured.</p> <p>Note: You must observe power sequencing for this signal.</p> <p>Power Up – Display must be powered up and initialized before power is applied to the signal.</p> <p>Power Down – Power must be removed from this signal before the display is powered off.</p> 
V_{REF}				Voltage reference pin for pre-charge voltage in driving OLED device. Voltage should be set to match with the OLED driving voltage in current drive phase. It can either be supplied externally or by connecting to V_{PANEL} .
V_{SL}				Segment voltage reference pin. This pin should be left open.
V_{SSB}				Ground pin for the internal buffer of the DC-DC voltage converter. It must be connected to GND.
$\overline{\text{WR}}_{8080} (\text{R}/\overline{\text{W}}_{6800})$	$\text{R}/\overline{\text{W}} (\overline{\text{WR}})$	$\overline{\text{WR}} (\text{R}/\overline{\text{W}})$	$\text{R}/\text{W}\#$	<p>Host interface input.</p> <p>8080 microprocessor host: Active LOW. Signal on the data bus is latched at the rising edge of $\overline{\text{WR}}$ signal.</p> <p>6800 microprocessor host: Read/Write control signal output.</p> <p>$\text{R}/\overline{\text{W}}$ = High: Read (Host←Module)</p> <p>$\text{R}/\overline{\text{W}}$ = Low: Write (Host→Module)</p>



APPENDIX D: SINO WEALTH SH1101A CONTROLLER SPECIFICATION SHEET

The complete *Sino Wealth 132 x 64 Dot Matrix OLED/PLED Segment/Common Driver with Controller* Data Sheet (59 pages) follows.



SINO WEALTH



SH1101A

132 X 64 Dot Matrix OLED/PLED Segment/Common Driver with Controller

Features

- Support maximum 132 X 64 dot matrix panel
- Embedded 132 X 64 bits SRAM
- Operating voltage: (Normal mode)
 - Logic voltage supply: $V_{DD1} = 2.4V - 3.5V$
 - DC-DC voltage supply: $V_{DD2} = 2.4V - 3.5V$
 - OLED Operating voltage supply: $V_{PP} = 7.0V - 16.0V$
- Operating voltage: (Low voltage mode)
 - Logic voltage supply: $V_{DD1} = 1.65V - 3.5V$
 - DC-DC voltage supply: $V_{DD2} = 2.4V - 3.5V$
 - OLED Operating voltage supply: $V_{PP} = 7.0V - 9.0V$
- Maximum segment output current: 320 μ A
- Maximum common sink current: 45mA
- 8-bit 6800-series parallel interface, 8-bit 8080-series parallel interface, serial peripheral interface
- Programmable frame frequency and multiplexing ratio
- Row re-mapping and column re-mapping (ADC)
- Vertical scrolling
- On-chip oscillator
- Available internal DC-DC converter
- 256-step contrast control on monochrome passive OLED panel
- Low power consumption
 - Sleep mode: <5 μ A
- Wide range of operating temperatures: -40 to +85°C
- Available in COG and TCP form

General Description

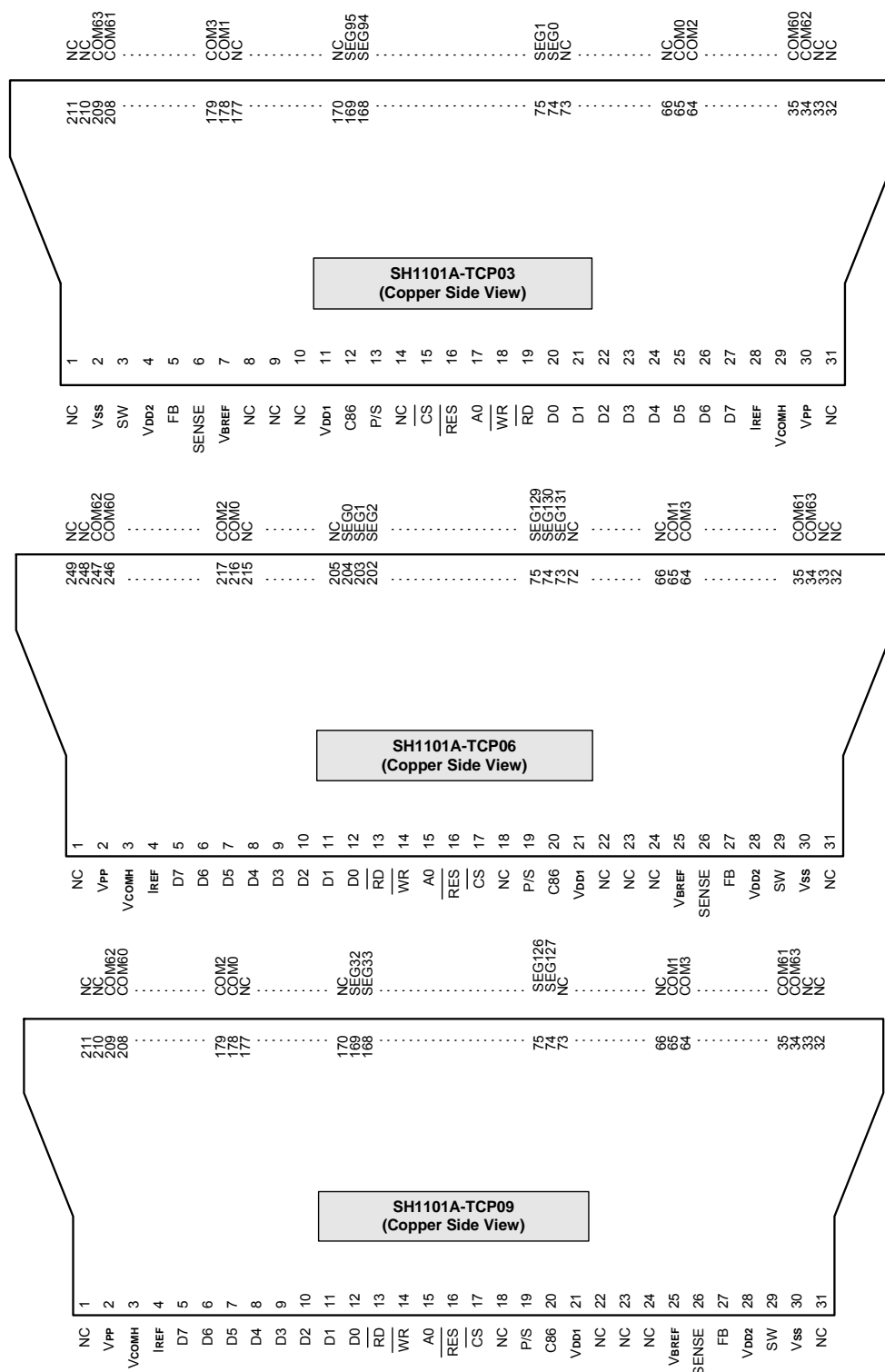
SH1101A is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. SH1101A consists of 132 segments, 64 commons that can support a maximum display resolution of 132 X 64. It is designed for Common Cathode type OLED panel.

SH1101A also support low voltage mode: $V_{DD1} = 1.65 - 3.5V$ and $V_{PP} = 7.0V - 9.0V$.

SH1101A embeds with contrast control, display RAM oscillator and efficient DC-DC converter, which reduces the number of external components and power consumption. SH1101A is suitable for a wide range of compact portable applications, such as sub-display of mobile phone, calculator and MP3 player, etc.



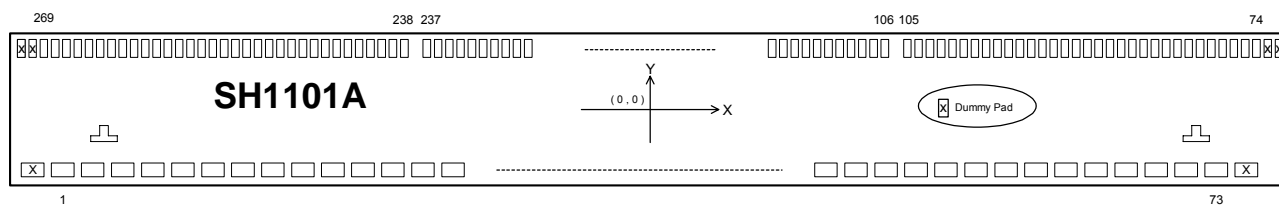
Pin Configuration

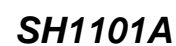




SH1101A

Pad Configuration





The diagram illustrates the internal architecture of the 6400 Series TFT-LCD Controller. It shows the following components and their interconnections:

- Power Supply and DC-DC Section:**
 - Power supply circuit:** Receives V_{DD1} , V_{DD2} , V_{SS} , V_{COMH} , V_{CL} , V_{SL} , I_{REF} , and V_{REF} . It provides power to the Segment driver and Common driver.
 - DC-DC:** Receives V_{PP} , SW , $SENSE$, and FB . It provides V_{BREF} to the Output status selector circuit.
- Display Data Path:**
 - 132 X 64-dots Display Data RAM:** Receives data from the Display data latch and outputs to the Segment driver via the I/O buffer circuit.
 - Display data latch:** Receives data from the Shift register and outputs to the Display Data RAM.
 - Shift register:** Receives data from the Initial display line register and outputs to the Display data latch.
 - Line counter:** Receives data from the Initial display line register and outputs to the Line address decoder.
 - Initial display line register:** Receives data from the Display Timing Generator Circuit and outputs to the Line counter and Shift register.
 - Line address decoder:** Receives data from the Line counter and outputs to the I/O buffer circuit.
 - Column address decoder:** Receives data from the 8-bit column address counter and outputs to the I/O buffer circuit.
 - 8-bit column address counter:** Receives data from the 8-bit column address counter and outputs to the Column address decoder.
 - 8-bit column address counter:** Receives data from the Display Timing Generator Circuit and outputs to the 8-bit column address counter.
- Control and Timing Section:**
 - Page Address Register:** Receives data from the Microprocessor Interface and outputs to the I/O buffer circuit.
 - Output status selector circuit:** Receives data from the DC-DC and outputs to the I/O buffer circuit.
 - Display Timing Generator Circuit:** Receives data from the Oscillator and outputs to the Line counter, Initial display line register, and 8-bit column address counter.
 - Oscillator:** Receives data from the CLS pin and outputs to the Display Timing Generator Circuit.
 - Bus Holder:** Receives data from the Microprocessor Interface and outputs to the I/O buffer circuit.
 - Command Decoder:** Receives data from the Microprocessor Interface and outputs to the I/O buffer circuit.
- Microprocessor Interface and I/O Buffer:**
 - Microprocessor Interface:** Receives control signals (\overline{CS} , $A0$, \overline{RD} , \overline{WR} , P/S , $C86$, \overline{RES}) and outputs data to the I/O Buffer.
 - I/O Buffer:** Receives data from the Microprocessor Interface and outputs data to the I/O buffer circuit. It also receives data from the I/O buffer circuit and outputs data to the I/O pins ($D7, D6, D5, D4, D3, D2, D1, D0$).
- Output Pins:**
 - SEG0, SEG131, COM0, COM63:** Output pins for the Segment driver and Common driver.
 - CL, CLS:** Clock and Clock Source pins for the Display Timing Generator Circuit.



Pad Description

Power Supply

Pad No.	Symbol	I/O	Description
28 - 31	VDD1	Supply	Power supply input: Normal mode: 2.4 - 3.5V Low voltage mode: 1.65 - 3.5V
34, 44, 62	VDD1	Supply	Power supply output for pad option: Normal mode: 2.4 - 3.5V Low voltage mode: 1.65 - 3.5V
17 - 20	VDD2	Supply	2.4 - 3.5V power supply pad for the internal buffer of the DC-DC voltage converter.
7 - 13	VSS	Supply	Ground.
21, 32, 36, 42, 64	VSS	Supply	Ground output for pad option.
49 - 53, 71 - 73	VPP	Supply	This is the most positive voltage supply pad of the chip. It should be supplied externally.
66	VPP	Supply	This is the most positive voltage output for pad option, which cannot be used as the most positive voltage input.
4 - 6	VSL	Supply	This is a segment voltage reference pad. This pad should be connected to VSS externally.
1 - 3	VCL	Supply	This is a common voltage reference pad. This pad should be connected to VSS externally.

OLED Driver Supplies

Pad No.	Symbol	I/O	Description
70	VREF	I	This is a voltage reference pad for pre-charge voltage in driving OLED device. Voltage should be set to match with the OLED driving voltage in current drive phase. It can either be supplied externally or by connecting to VPP.
65	IREF	O	This is a segment current reference pad. A resistor should be connected between this pad and VSS. Set the current at 10μA.
45 - 48, 67 - 69	VCOMH	O	This is a pad for the voltage output high level for common signals. A capacitor should be connected between this pad and VSS.
14 - 16	SW	O	This is an output pad driving the gate of the external NMOS of the booster circuit.
22	FB	I	This is a feedback resistor input pad for the booster circuit. It is used to adjust the booster output voltage level, VPP.
23	SENSE	I	This is a source current pad of the external NMOS of the booster circuit.
24	VBREF	O	This is an internal voltage reference pad for booster circuit. A stabilization capacitor, typical 1μF, should be connected to VSS.



System Bus Connection Pads

Pad No.	Symbol	I/O	Description												
37	CL	I/O	This pad is the system clock input. When internal clock is enabled, this pad should be Left open. The internal clock is output from this pad. When internal oscillator is disabled, this pad receives display clock signal from external clock source.												
63	CLS	I	This is the internal clock enable pad. CLS = "H": Internal oscillator circuit is enabled. CLS = "L": Internal oscillator circuit is disabled (requires external input). When CLS = "L", an external clock source must be connected to the CL pad for normal operation.												
33	C86	I	This is the MPU interface switch pad. C86 = "H": 8080 series MPU interface. C86 = "L": 6800 series MPU interface.												
35	P/S	I	This is the parallel data input/serial data input switch pad. P/S = "H": Parallel data input. P/S = "L": Serial data input. When P/S = "L", D2 to D7 are HZ. D2 to D7 may be "H", "L" or Open. \overline{RD} (E) and \overline{WR} (R/W) are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported. These are MPU interface input selection pads. See the following table for selecting different interfaces: <table border="1"> <thead> <tr> <th></th><th>6800-Parallel Interface</th><th>8080-Parallel Interface</th><th>Serial Interface</th></tr> </thead> <tbody> <tr> <td>C86</td><td>0</td><td>1</td><td>0</td></tr> <tr> <td>P/S</td><td>1</td><td>1</td><td>0</td></tr> </tbody> </table>		6800-Parallel Interface	8080-Parallel Interface	Serial Interface	C86	0	1	0	P/S	1	1	0
	6800-Parallel Interface	8080-Parallel Interface	Serial Interface												
C86	0	1	0												
P/S	1	1	0												
38	\overline{CS}	I	This pad is the chip select input. When \overline{CS} = "L", then the chip select becomes active, and data/command I/O is enabled.												
39	\overline{RES}	I	This is a reset signal input pad. When \overline{RES} is set to "L", the settings are initialized. The reset operation is performed by the \overline{RES} signal level.												
40	A0	I	This is the Data/Command control pad which determines whether the data bits are data or a command. A0 = "H": the inputs at D0 to D7 are treated as display data. A0 = "L": the inputs at D0 to D7 are transferred to the command registers.												
41	\overline{WR} (R/W)	I	This is a MPU interface input pad. When connected to an 8080 MPU, this is active LOW. This pad connects to the 8080 MPU \overline{WR} signal. The signals on the data bus are latched at the rising edge of the \overline{WR} signal. When connected to a 6800 Series MPU: This is the read/write control signal input terminal. When R/W = "H": Read. When R/W = "L": Write.												
43	\overline{RD} (E)	I	This is a MPU interface input pad. When connected to an 8080 series MPU, it is active LOW. This pad is connected to the \overline{RD} signal of the 8080 series MPU, and the SH1101A data bus is in an output status when this signal is "L". When connected to a 6800 series MPU, this is active HIGH. This is used as an enable clock input of the 6800 series MPU.												
54 - 61 54 55	D0 - D7 (SCL) (SI)	I/O I I	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected, then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SI). At this time, D2 to D7 are set to high impedance. When the chip select is inactive, D0 to D7 are set to high impedance.												

**OLED Drive Pads**

Pad No.	Symbol	I/O	Description
105 - 74, 238 - 269	COM0 - 63	O	These pads are Common signal output for OLED display.
106 - 237	SEG0 - 131	O	These pads are Segment signal output for OLED display.

Test Pads

Pad No.	Symbol	I/O	Description
25	TEST1	I	Test pads, internal pull low, no connection for user.
27	TEST2	O	Test pads, no connection for user.
26	TEST3	I	Test pads, no connection for user.
-	NC	-	NC pads, no connection for user.



Functional Description

Microprocessor Interface Selection

The 8080-Parallel Interface, 6800-Parallel Interface or Serial Interface (SPI) can be selected by different selections of C86, P/S as shown in Table 1.

Table. 1

	6800-Parallel Interface	8080-Parallel Interface	Serial Interface
C86	0	1	0
P/S	1	1	0

6800-series Parallel Interface

The parallel interface consists of 8 bi-directional data pads (D7-D0), \overline{WR} (R/ \overline{W}), \overline{RD} (E), A0 and \overline{CS} . When \overline{WR} (R/ \overline{W}) = "H", read operation from the display RAM or the status register occurs. When \overline{WR} (R/ \overline{W}) = "L", Write operation to display data RAM or internal command registers occurs, depending on the status of A0 input. The \overline{RD} (E) input serves as data latch signal (clock) when it is "H", provided that \overline{CS} = "L" as shown in Table. 2.

Table. 2

P/S	C86	Type	\overline{CS}	A0	\overline{RD}	\overline{WR}	D0 to D7
1	0	6800 microprocessor bus	\overline{CS}	A0	E	R/ \overline{W}	D0 to D7

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processings are internally performed, which require the insertion of a dummy read before the first actual display data read. This is shown in Figure. 1 below.

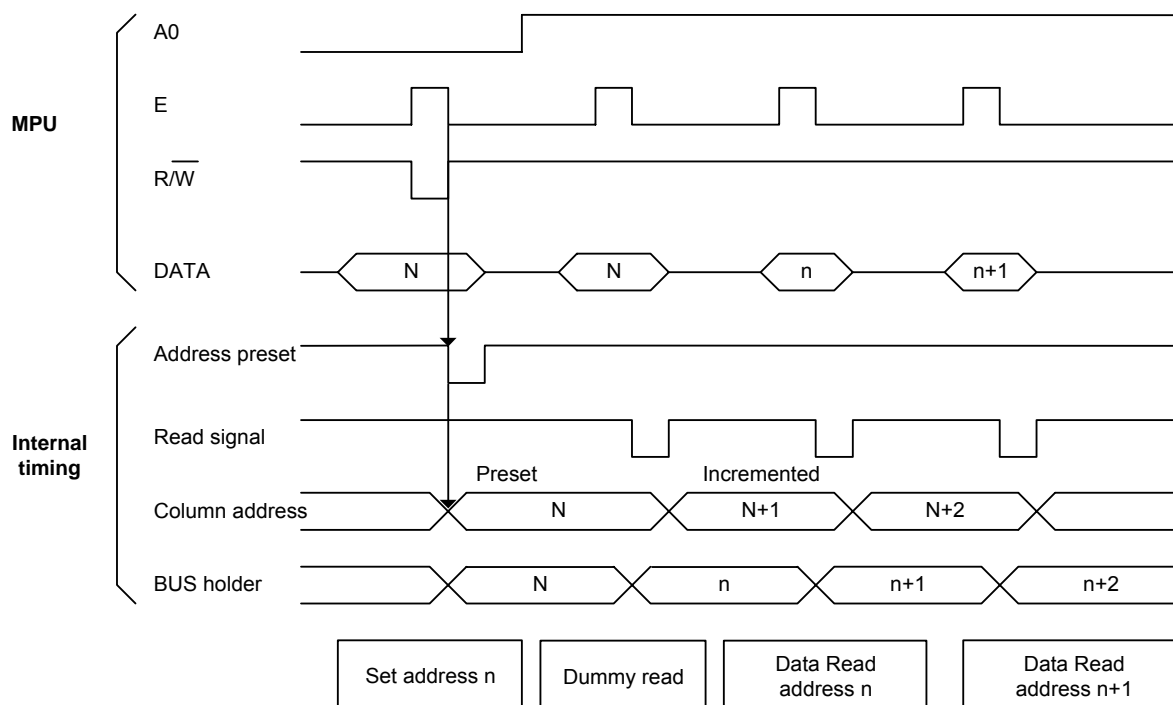


Figure. 1



8080-series Parallel Interface

The parallel interface consists of 8 bi-directional data pads (D7-D0), \overline{WR} (R/ \overline{W}), \overline{RD} (E), A0 and \overline{CS} . The \overline{RD} (E) input serves as data read latch signal (clock) when it is "L" provided that \overline{CS} = "L". Display data or status register read is controlled by A0 signal. The \overline{WR} (R/ \overline{W}) input serves as data write latch signal (clock) when it is "L" and provided that \overline{CS} = "L". Display data or command register write is controlled by A0 as shown in Table. 3.

Table. 3

P/S	C86	Type	\overline{CS}	A0	\overline{RD}	\overline{WR}	D0 to D7
1	1	8080 microprocessor bus	\overline{CS}	A0	\overline{RD}	\overline{WR}	D0 to D7

Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

Data Bus Signals

The SH1101A identifies the data bus signal according to A0, \overline{RD} (E) and \overline{WR} (R/ \overline{W}) signals.

Table. 4

Common	6800 processor	8080 processor		Function
A0	(R / \overline{W})	\overline{RD}	\overline{WR}	
1	1	0	1	Reads display data.
1	0	1	0	Writes display data.
0	1	0	1	Reads status.
0	0	1	0	Writes control data in internal register. (Command)



Serial Interface (SPI)

The serial interface consists of serial clock SCL, serial data SI, A0 and \overline{CS} . SI is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... and D0. A0 is sampled on every eighth clock and the data byte in the shift register is written to the display data RAM or command register in the same clock. See Figure. 2.

Table. 5

P/S	C86	Type	\overline{CS}	A0	\overline{RD}	\overline{WR}	D0	D1	D2 to D7
0	0	Serial Interface (SPI)	\overline{CS}	A0	-	-	SCL	SI	(HZ)

Note: “-” Must always be HIGH or LOW.

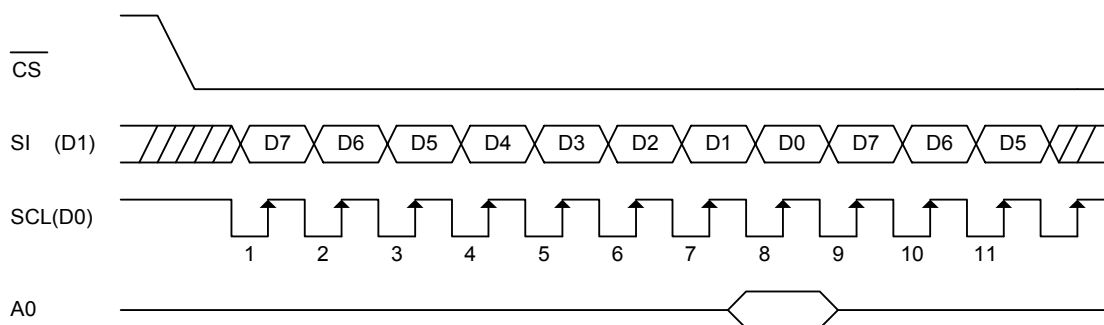


Figure. 2

- When the chip is not active, the shift registers and the counter are reset to their initial statuses.
- Read is not possible while in serial interface mode.
- Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

Access to Display Data RAM and Internal Registers

This module determines whether the input data is interpreted as data or command. When A0 = “H”, the inputs at D7 - D0 are interpreted as data and be written to display RAM. When A0 = “L”, the inputs at D7 - D0 are interpreted as command, they will be decoded and be written to the corresponding command registers.

Display Data RAM

The Display Data RAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 132 X 64 bits. For mechanical flexibility, re-mapping on both segment and common outputs can be selected by software. For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.



The Page Address Circuit

As shown in Figure. 3, page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access.

The Column Address

As shown in Figure. 3, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/ write command. This allows the MPU display data to be accessed continuously. Because the column address is independent of the page address, when moving, for example, from page0 column 83H to page 1 column 00H, it is necessary to re-specify both the page address and the column address.

Furthermore, as shown in Table. 6, the Column re-mapping (ADC) command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the OLED module is assembled can be minimized.

Table. 6

Segment Output	SEG0	SEG131
ADC "0"	0 (H) →	Column Address → 83 (H)
ADC "1"	83 (H) ←	Column Address ← 0 (H)

The Line Address Circuit

The line address circuit, as shown in Figure. 3, specifies the line address relating to the common output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified (this is the COM0 output when the common output mode is normal, and the COM63 output for SH1101A, when the common output mode is reversed. The display area is a 64-line area for the SH1101A from the display start line address.

If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, etc. that can be performed relationship between display data RAM and address (if initial display line is 1DH).

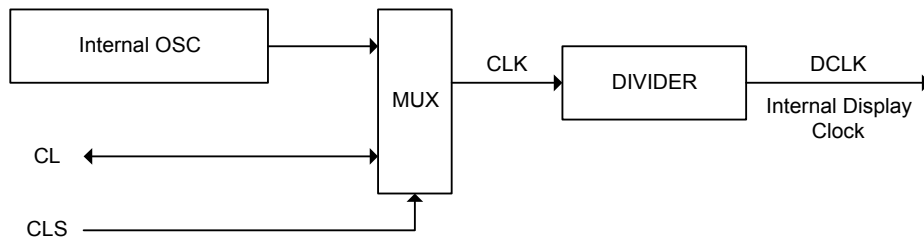


SH1101A

Page Address				Data				Line Address				OUTPUT			
D3 D2 D1 D0 0 0 0 0				D0	PAGE 0						00H	COM0			
				D1							01H	COM1			
				D2							02H	COM2			
				D3							03H	COM3			
				D4							04H	COM4			
				D5							05H	COM5			
				D6							06H	COM6			
				D7							07H	COM7			
D3 D2 D1 D0 0 0 0 1				D0	PAGE1						08H	COM8			
				D1							09H	COM9			
				D2							0AH	COM10			
				D3							0BH	COM11			
				D4							0CH	COM12			
				D5							0DH	COM13			
				D6							0EH	COM14			
				D7							0FH	COM15			
D3 D2 D1 D0 0 0 1 0				D0	PAGE2						10H	COM16			
				D1							11H	COM17			
				D2							12H	COM18			
				D3							13H	COM19			
				D4							14H	COM20			
				D5							15H	COM21			
				D6							16H	COM22			
				D7							17H	COM23			
D3 D2 D1 D0 0 0 1 1				D0	PAGE3						18H	COM24			
				D1							19H	COM25			
				D2							1AH	COM26			
				D3							1BH	COM27			
				D4							1CH	COM28			
				D5							1DH	COM29			
				D6							1EH	COM30			
				D7							1FH	COM31			
D3 D2 D1 D0 0 1 0 0				D0	PAGE4						20H	COM32			
				D1							21H	COM33			
				D2							22H	COM34			
				D3							23H	COM35			
				D4							24H	COM36			
				D5							25H	COM37			
				D6							26H	COM38			
				D7							27H	COM39			
D3 D2 D1 D0 0 1 0 1				D0	PAGE5						28H	COM40			
				D1							29H	COM41			
				D2							2AH	COM42			
				D3							2BH	COM43			
				D4							2CH	COM44			
				D5							2DH	COM45			
				D6							2EH	COM46			
				D7							2FH	COM47			
D3 D2 D1 D0 0 1 1 0				D0	PAGE6						30H	COM48			
				D1							31H	COM49			
				D2							32H	COM50			
				D3							33H	COM51			
				D4							34H	COM52			
				D5							35H	COM53			
				D6							36H	COM54			
				D7							37H	COM55			
D3 D2 D1 D0 0 1 1 1				D0	PAGE7						38H	COM56			
				D1							39H	COM57			
				D2							3AH	COM58			
				D3							3BH	COM59			
				D4							3CH	COM60			
				D5							3DH	COM61			
				D6							3EH	COM62			
				D7							3FH	COM63			
Column Address				ADC											
				D0="1"											
				D0="0"											
				D0="1"											
LCD OUT				SEG0											
				SEG1											
				SEG2											

**The Oscillator Circuit**

This is a RC type oscillator (Figure. 4) that produces the display clock. The oscillator circuit is only enabled when CLS = "H". When CLS = "L", the oscillation stops and the display clock is inputted through the CL terminal.

**Figure. 4**



DC-DC Voltage Converter

It is a switching voltage generator circuit, designed for hand held applications. In SH1101A, built-in DC-DC voltage converter accompanied with an external application circuit (shown in Figure. 5) can generate a high voltage supply V_{PP} from a low voltage supply input V_{DD2} . V_{PP} is the voltage supply to the OLED driver block.

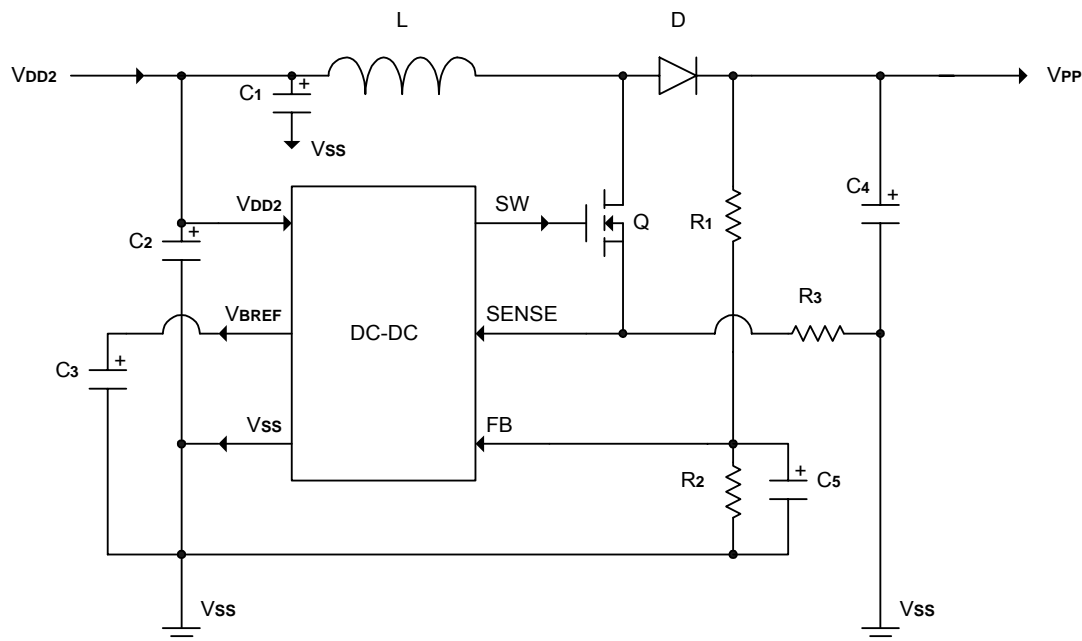


Figure. 5

$$V_{PP} = \left(1 + \frac{R_1}{R_2}\right) \times V_{BREF}, (R_2: 80 - 120k\Omega)$$

Current Control and Voltage Control

This block is used to derive the incoming power sources into different levels of internal use voltage and current. V_{PP} and V_{DD2} are external power supplies. V_{REF} , a reference voltage, which is used to derive the driving voltage for segments and commons. I_{REF} is a reference current source for segment current drivers.

Common Drivers/Segment Drivers

Segment drivers deliver 132 current sources to drive OLED panel. The driving current can be adjusted up to 320 μ A with 256 steps. Common drivers generate voltage scanning pulses.

Reset Circuit

When the \overline{RES} input falls to "L", these reenter their default state. The default settings are shown below:

1. Display is OFF. Common and segment are in high impedance state.
2. 132 X 64 Display mode.
3. Normal segment and display data column address and row address mapping (SEG0 is mapped to column address 00H and COM0 mapped to row address 00H).
4. Shift register data clear in serial interface.
5. Display start line is set at display RAM line address 00H.
6. Column address counter is set at 0.
7. Normal scanning direction of the common outputs.
8. Contrast control register is set at 80H.
9. Internal DC-DC is selected.



Commands

The SH1101A uses a combination of A0, \overline{RD} (E) and \overline{WR} (R/\overline{W}) signals to identify data bus signals. As the chip analyzes and executes each command using internal timing clock only regardless of external clock, its processing speed is very high and its busy check is usually not required. The 8080 series microprocessor interface enters a read status when a low pulse is input to the \overline{RD} pad and a write status when a low pulse is input to the \overline{WR} pad. The 6800 series microprocessor interface enters a read status when a high pulse is input to the R/\overline{W} pad and a write status when a low pulse is input to this pad. When a high pulse is input to the E pad, the command is activated. (For timing, see AC Characteristics.). Accordingly, in the command explanation and command table, \overline{RD} (E) becomes 1(HIGH) when the 6800 series microprocessor interface reads status of display data. This is an only different point from the 8080 series microprocessor interface.

Taking the 8080 series, microprocessor interface as an example command will explain below.

When the serial interface is selected, input data starting from D7 in sequence.

Command Set

1. Set Lower Column Address: (00H - 0FH)
2. Set Higher Column Address: (10H - 1FH)

Specifies column address of display RAM. Divide the column address into 4 higher bits and 4 lower bits. Set each of them into successions. When the microprocessor repeats to access to the display RAM, the column address counter is incremented during each access until address 132 is accessed. The page address is not changed during this time.

	A0	$\frac{E}{\overline{RD}}$	$\frac{R/\overline{W}}{\overline{WR}}$	D7	D6	D5	D4	D3	D2	D1	D0
Higher bits	0	1	0	0	0	0	1	A7	A6	A5	A4
Lower bits	0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
			:					:
1	0	0	0	0	0	1	1	131

Note: Don't use any commands not mentioned above.

3 - 5. Reserved Command

These three commands are reserved for user.

6. Set Display Start Line: (40H - 7FH)

Specifies line address (refer to Figure. 3) to determine the initial display line or COM0. The RAM display data becomes the top line of OLED screen. It is followed by the higher number of lines in ascending order, corresponding to the duty cycle. When this command changes the line address, the smooth scrolling or page change takes place.

A0	$\frac{E}{\overline{RD}}$	$\frac{R/\overline{W}}{\overline{WR}}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	A5	A4	A3	A2	A1	A0

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
		:				:
1	1	1	1	1	0	62
1	1	1	1	1	1	63



7. Set Contrast Control Register: (Double Bytes Command)

This command is to set contrast setting of the display. The chip has 256 contrast steps from 00 to FF. The segment output current increases as the contrast step value increases.

Segment output current setting: $I_{SEG} = \alpha / 256 \times I_{REF} \times \text{scale factor}$

Where: α is contrast step; I_{REF} is reference current equals 10 μ A; Scale factor = 32.

■ The Contrast Control Mode Set: (81H)

When this command is input, the contrast data register set command becomes enabled. Once the contrast control mode has been set, no other command except for the contrast data register command can be used. Once the contrast data set command has been used to set data into the register, then the contrast control mode is released.

A0	$\frac{E}{RD}$	$\frac{R/\overline{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

■ Contrast Data Register Set: (00H - FFH)

By using this command to set eight bits of data to the contrast data register; the OLED segment output assumes one of the 256 current levels.

When this command is input, the contrast control mode is released after the contrast data register has been set.

A0	$\frac{E}{RD}$	$\frac{R/\overline{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	I _{SEG}
0	1	0	0	0	0	0	0	0	0	0	Small
0	1	0	0	0	0	0	0	0	1	0	
0	1	0	0	0	0	0	0	0	1	1	
0	1	0					:				
0	1	0	1	0	0	0	0	0	0	0	POR
0	1	0					:				
0	1	0	1	1	1	1	1	1	1	0	
0	1	0	1	1	1	1	1	1	1	1	Large

When the contrast control function is not used, set the D7 - D0 to 1000,0000.

8. Set Segment Re-map: (A0H - A1H)

Change the relationship between RAM column address and segment driver. The order of segment driver output pads can be reversed by software. This allows flexible IC layout during OLED module assembly. For details, refer to the column address section of Figure. 3. When display data is written or read, the column address is incremented by 1 as shown in Figure. 1.

A0	$\frac{E}{RD}$	$\frac{R/\overline{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	ADC

When ADC = "L", the right rotates (normal direction). (POR)

When ADC = "H", the left rotates (reverse direction).

9. Set Entire Display OFF/ON: (A4H - A5H)

Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held.

This command has priority over the normal/reverse display command.

A0	$\frac{E}{RD}$	$\frac{R/\overline{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When D = "L", the normal display status is provided. (POR)

When D = "H", the entire display ON status is provided.



10. Set Normal/Reverse Display: (A6H -A7H)

Reverses the display ON/OFF status without rewriting the contents of the display data RAM.

A0	$\frac{E}{RD}$	$\frac{R/\overline{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

When D = "L", the RAM data is high, being OLED ON potential (normal display). (POR)

When D = "H", the RAM data is low, being OLED ON potential (reverse display)

11. Set Multiplex Ratio: (Double Bytes Command)

This command switches default 64 multiplex modes to any multiplex ratio from 1 to 64. The output pads COM0-COM63 will be switched to corresponding common signal.

■ Multiplex Ratio Mode Set: (A8H)

A0	$\frac{E}{RD}$	$\frac{R/\overline{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	0	0

■ Multiplex Ratio Data Set: (00H - 3FH)

A0	$\frac{E}{RD}$	$\frac{R/\overline{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Multiplex Ratio
0	1	0	*	*	0	0	0	0	0	0	1
0	1	0	*	*	0	0	0	0	1	0	2
0	1	0	*	*	0	0	0	0	1	1	3
0	1	0					:				:
0	1	0	*	*	1	1	1	1	1	0	63
0	1	0	*	*	1	1	1	1	1	1	64 (POR)

12. Set DC-DC OFF/ON: (Double Bytes Command)

This command is to control the DC-DC voltage converter. The converter will be turned on by issuing this command then display ON command. The panel display must be off while issuing this command.

■ DC-DC Control Mode Set: (ADH)

A0	$\frac{E}{RD}$	$\frac{R/\overline{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	0	1

■ DC-DC ON/OFF Mode Set: (8AH - 8BH)

A0	$\frac{E}{RD}$	$\frac{R/\overline{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	1	0	1	D

When D = "L", DC-DC is disable.

When D = "H", DC-DC will be turned on when display on. (POR)

Table. 7

DC-DC STATUS	DISPLAY ON/OFF STATUS	Description
0	0	Sleep mode
0	1	External VPP must be used.
1	0	Sleep mode
1	1	Built-in DC-DC is used, Normal Display



13. Display OFF/ON: (AEH - AFH)

Alternatively turns the display on and off.

A0	\overline{E} RD	R / \overline{W} \overline{WR}	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

When D = "L", Display OFF OLED. (POR)

When D = "H", Display ON OLED.

When the display OFF command is executed, power saver mode will be entered.

Sleep mode:

This mode stops every operation of the OLED display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:

- (1) Stops the oscillator circuit and DC-DC circuit.
- (2) Stops the OLED drive and outputs HZ as the segment/common driver output.
- (3) Holds the display data and operation mode provided before the start of the sleep mode.
- (4) The MPU can access to the built-in display RAM.

14. Set Page Address: (B0H - B7H)

Specifies page address to load display RAM data to page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed.

A0	\overline{E} RD	R / \overline{W} \overline{WR}	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	A ₃	A ₂	A ₁	A ₀

A ₃	A ₂	A ₁	A ₀	Page address
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7

Note: Don't use any commands not mentioned above for user.



15. Set Common Output Scan Direction: (C0H - C8H)

This command sets the scan direction of the common output allowing layout flexibility in OLED module design. In addition, the display will have immediate effect once this command is issued. That is, if this command is sent during normal display, the graphic display will be vertically flipped.

A0	\overline{E} RD	$\overline{R/W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	D	*	*	*

When D = "L", Scan from COM0 to COM [N -1]. (POR)

When D = "H", Scan from COM [N -1] to COM0.

16. Set Display Offset: (Double Bytes Command)

This is a double byte command. The next command specifies the mapping of display start line to one of COM0-63 (it is assumed that COM0 is the display start line, that equals to 0). For example, to move the COM16 towards the COM0 direction for 16 lines, the 6-bit data in the second byte should be given by 010000. To move in the opposite direction by 16 lines, the 6-bit data should be given by (64-16), so the second byte should be 100000.

■ Display Offset Mode Set: (D3H)

A0	\overline{E} RD	$\overline{R/W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0	0	1	1

■ Display Offset Data Set: (00H~3FH)

A0	\overline{E} RD	$\overline{R/W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0	COMx
0	1	0	*	*	0	0	0	0	0	0	0 (POR)
0	1	0	*	*	0	0	0	0	1	0	1
0	1	0	*	*	0	0	0	0	1	1	2
0	1	0					:				:
0	1	0	*	*	1	1	1	1	1	0	62
0	1	0	*	*	1	1	1	1	1	1	63

Note: "*" stands for "Don't care"



17. Set Display Clock Divide Ratio/Oscillator Frequency: (Double Bytes Command)

This command is used to set the frequency of the internal display clocks (DCLKs). It is defined as the divide ratio (Value from 1 to 16) used to divide the oscillator frequency. POR is 1. Frame frequency is determined by divide ratio, number of display clocks per row, MUX ratio and oscillator frequency.

■ Divide Ratio/Oscillator Frequency Mode Set: (D5H)

A0	$\frac{E}{RD}$	$\frac{R/\overline{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0	1	0	1

■ Divide Ratio/Oscillator Frequency Data Set: (00H - 3FH)

A0	$\frac{E}{RD}$	$\frac{R/\overline{W}}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A7	A6	A5	A4	A3	A2	A1	A0

A3 - A0 defines the divide ration of the display clocks (DCLK). Divide Ratio = A[3:0]+1.

A3	A2	A1	A0	Divide Ratio
0	0	0	0	1 (POR)
		:		:
1	1	1	1	16

A7 - A4 sets the oscillator frequency. Oscillator frequency increase with the value of A[7:4] and vice versa.

A7	A6	A5	A4	Oscillator Frequency of f_{osc}
0	0	0	0	-25%
0	0	0	1	-20%
0	0	1	0	-15%
0	0	1	1	-10%
0	1	0	0	-5%
0	1	0	1	f_{osc} (POR)
0	1	1	0	+5%
0	1	1	1	+10%
1	0	0	0	+15%
1	0	0	1	+20%
1	0	1	0	+25%
1	0	1	1	+30%
1	1	0	0	+35%
1	1	0	1	+40%
1	1	1	0	+45%
1	1	1	1	+50%



18. Set Dis-charge/Pre-charge Period: (Double Bytes Command)

This command is used to set the duration of the pre-charge period. The interval is counted in number of DCLK. POR is 2 DCLKs.

■ Pre-charge Period Mode Set: (D9H)

A0	\overline{E} RD	$\overline{R/\overline{W}}$ WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	0	1

■ Dis-charge/Pre-charge Period Data Set: (00H - FFH)

A0	\overline{E} RD	$\overline{R/\overline{W}}$ WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A7	A6	A5	A4	A3	A2	A1	A0

Pre-charge Period Adjust: (A3 - A0)

A3	A2	A1	A0	Pre-charge Period
0	0	0	0	INVALID
0	0	0	1	1 DCLKs
0	0	1	0	2 DCLKs (POR)
		:		:
1	1	1	0	14 DCLKs
1	1	1	1	15 DCLKs

Dis-charge Period Adjust: (A7 - A4)

A7	A6	A5	A4	Dis-charge Period
0	0	0	0	INVALID
0	0	0	1	1 DCLKs
0	0	1	0	2 DCLKs (POR)
		:		:
1	1	1	0	14 DCLKs
1	1	1	1	15 DCLKs

19. Set Common pads hardware configuration: (Double Bytes Command)

This command is to set the common signals pad configuration (sequential or alternative) to match the OLED panel hardware layout

■ Common Pads Hardware Configuration Mode Set: (DAH)

A0	\overline{E} RD	$\overline{R/\overline{W}}$ WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	1	0

■ Sequential/Alternative Mode Set: (02H - 12H)

A0	\overline{E} RD	$\overline{R/\overline{W}}$ WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	D	0	0	1	0

When D = "L", Sequential.

COM31, 30 - 1, 0	SEG0, 1 - 130, 131	COM32, 33 - 62, 63
------------------	--------------------	--------------------

When D = "H", Alternative. (POR)

COM62, 60 - 2, 0	SEG0, 1 - 130, 131	COM1, 3 - 61, 63
------------------	--------------------	------------------



20. Set VCOM Deselect Level: (Double Bytes Command)

This command is to set the common pad output voltage level at deselect stage.

■ VCOM Deselect Level Mode Set: (DBH)

A0	\overline{E} RD	$\overline{R/W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	1	1

■ VCOM Deselect Level Data Set: (00H - FFH)

A0	\overline{E} RD	$\overline{R/W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A7	A6	A5	A4	A3	A2	A1	A0

$$V_{COM} = \beta \times V_{REF} = (0.430 + A[7:0] \times 0.006415) \times V_{REF}$$

A[7:0]	β	A[7:0]	β
00H	0.430	20H	0.770 (POR)
01H		21H	
02H		22H	
03H		23H	
04H		24H	
05H		25H	
06H		26H	
07H		27H	
08H		28H	
09H		29H	
0AH		2AH	
0BH		2BH	
0CH		2CH	
0DH		2DH	
0EH		2EH	
0FH		2FH	
10H		30H	
11H		31H	
12H		32H	
13H		33H	
14H		34H	
15H		35H	
16H		36H	
17H		37H	
18H		38H	
19H		39H	
1AH		3AH	
1BH		3BH	
1CH		3CH	
1DH		3DH	
1EH		3EH	
1FH		3FH	
40H - FFH	1		



21. Read-Modify-Write: (E0H)

A pair of Read-Modify-Write and End commands must always be used. Once read-modify-write is issued, column address is not incremental by read display data command but incremental by write display data command only. It continues until End command is issued. When the End is issued, column address returns to the address when read-modify-write is issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or others.

A0	\overline{E} RD	$\overline{R/W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Cursor display sequence:

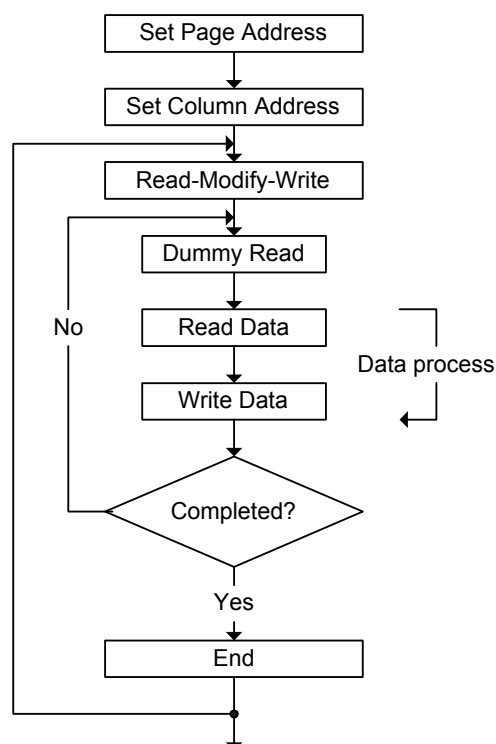


Figure. 6

22. End: (EEH)

Cancels Read-Modify-Write mode and returns column address to the original address (when Read-Modify-Write is issued.)

A0	\overline{E} RD	$\overline{R/W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

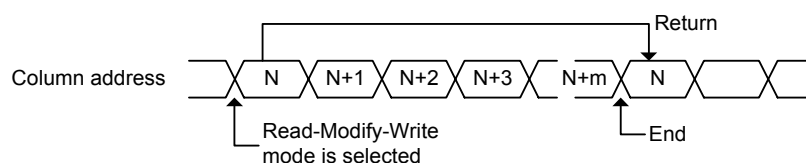


Figure. 7

**23. NOP: (E3H)**

Non-Operation Command.

A0	\overline{E} RD	$\overline{R/W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

24. Write Display Data

Write 8-bit data in display RAM. As the column address is incremental by 1 automatically after each write, the microprocessor can continue to write data of multiple words.

A0	\overline{E} RD	$\overline{R/W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write RAM data							

25. Read Status

A0	\overline{E} RD	$\overline{R/W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ON/OFF	*	*	*	0	0	0

BUSY: When high, the SH1101A is busy due to internal operation or reset. Any command is rejected until BUSY goes low. The busy check is not required if enough time is provided for each cycle.

ON/OFF: Indicates whether the display is on or off. When goes low the display turns on. When goes high, the display turns off. This is the opposite of Display ON/OFF command.

26. Read Display Data

Reads 8-bit data from display RAM area specified by column address and page address. As the column address is increment by 1 automatically after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after column address being setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

A0	\overline{E} RD	$\overline{R/W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read RAM data							



Command Table

Command	Code											Function
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	
1. Set Column Address 4 lower bits	0	1	0	0	0	0	0	Lower column address				Sets 4 lower bits of column address of display RAM in register. (POR = 00H)
2. Set Column Address 4 higher bits	0	1	0	0	0	0	1	Higher column address				Sets 4 higher bits of column address of display RAM in register. (POR = 10H)
3. Reserved Command	0	1	0	0	0	1	0	0	1	0	0	Reserved
4. Reserved Command	0	1	0	0	0	1	0	0	1	1	0	Reserved
5. Reserved Command	0	1	0	0	0	1	0	1	1	1	D	Reserved
6. Set Display Start Line	0	1	0	0	1	Line address						Specifies RAM display line for COM0. (POR = 40H)
7. The Contrast Control Mode Set Contrast Data Register Set	0	1	0	1	0	0	0	0	0	0	1	This command is to set Contrast Setting of the display. The chip has 256 contrast steps from 00 to FF. (POR = 80H)
	0	1	0	Contrast Data								
8. Set Segment Re-map (ADC)	0	1	0	1	0	1	0	0	0	0	ADC	The right (0) or left (1) rotation. (POR = A0H)
9. Set Entire Display OFF/ON	0	1	0	1	0	1	0	0	1	0	D	Selects normal display (0) or Entire Display ON (1). (POR = A4H)
10. Set Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	D	Normal indication (0) when low, but reverse indication (1) when high. (POR = A6H)
11. Multiplex Ration Mode Set Multiplex Ration Data Set	0	1	0	1	0	1	0	1	0	0	0	This command switches default 63 multiplex mode to any multiplex ratio from 1 to 64. (POR = 3FH)
	0	1	0	*	*	Multiplex Ratio						
12. DC-DC Control Mode Set DC-DC ON/OFF Mode Set	0	1	0	1	0	1	0	1	1	0	1	This command is to control the DC-DC voltage DC-DC will be turned on when display on converter (1) or DC-DC OFF (0). (POR = 8BH)
	0	1	0	1	0	0	0	1	0	1	D	



Command Table (Continued)

Command	Code											Function
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	
13. Display OFF/ON	0	1	0	1	0	1	0	1	1	1	D	Turns on OLED panel (1) or turns off (0). (POR = AEH)
14. Set Page Address	0	1	0	1	0	1	1	Page Address				Specifies page address to load display RAM data to page address register. (POR = B0H)
15. Set Common Output Scan Direction	0	1	0	1	1	0	0	D	*	*	*	Scan from COM0 to COM [N - 1] (0) or Scan from COM [N -1] to COM0 (1). (POR = C0H)
16. Display Offset Mode Set	0	1	0	1	1	0	1	0	0	1	1	This is a double byte command which specifies the mapping of display start line to one of COM0-63. (POR = 00H)
Display Offset Data Set	0	1	0	*	*	COMx						
17. Set Display Divide Ratio/Oscillator Frequency Mode Set	0	1	0	1	1	0	1	0	1	0	1	This command is used to set the frequency of the internal display clocks. (POR = 50H)
Divide Ratio/Oscillator Frequency Data Set	0	1	0	Oscillator Frequency				Divide Ratio				
18. Dis-charge / Pre-charge Period Mode Set	0	1	0	1	1	0	1	1	0	0	1	This command is used to set the duration of the dis-charge and pre-charge period. (POR = 22H)
Dis-charge /Pre-charge Period Data Set	0	1	0	Dis-charge Period				Pre-charge Period				
19. Common Pads Hardware Configuration Mode Set	0	1	0	1	1	0	1	1	0	1	0	This command is to set the common signals pad configuration. (POR = 12H)
Sequential/Alternative Mode Set	0	1	0	0	0	0	D	0	0	1	0	
20. VCOM Deselect Level Mode Set	0	1	0	1	1	0	1	1	0	1	1	This command is to set the common pad output voltage level at deselect stage. (POR = 35H)
VCOM Deselect Level Data Set	0	1	0	VCOM (β X VREF)								
21. Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-Modify-Write start.
22. End	0	1	0	1	1	1	0	1	1	1	0	Read-Modify-Write end.
23. NOP	0	1	0	1	1	1	0	0	0	1	1	Non-Operation Command
24. Write Display Data	1	1	0	Write RAM data								
25. Read Status	0	0	1	BUSY	ON/OFF	*	*	*	0	0	0	
26. Read Display Data	1	0	1	Read RAM data								

Note: Do not use any other command, or the system malfunction may result.

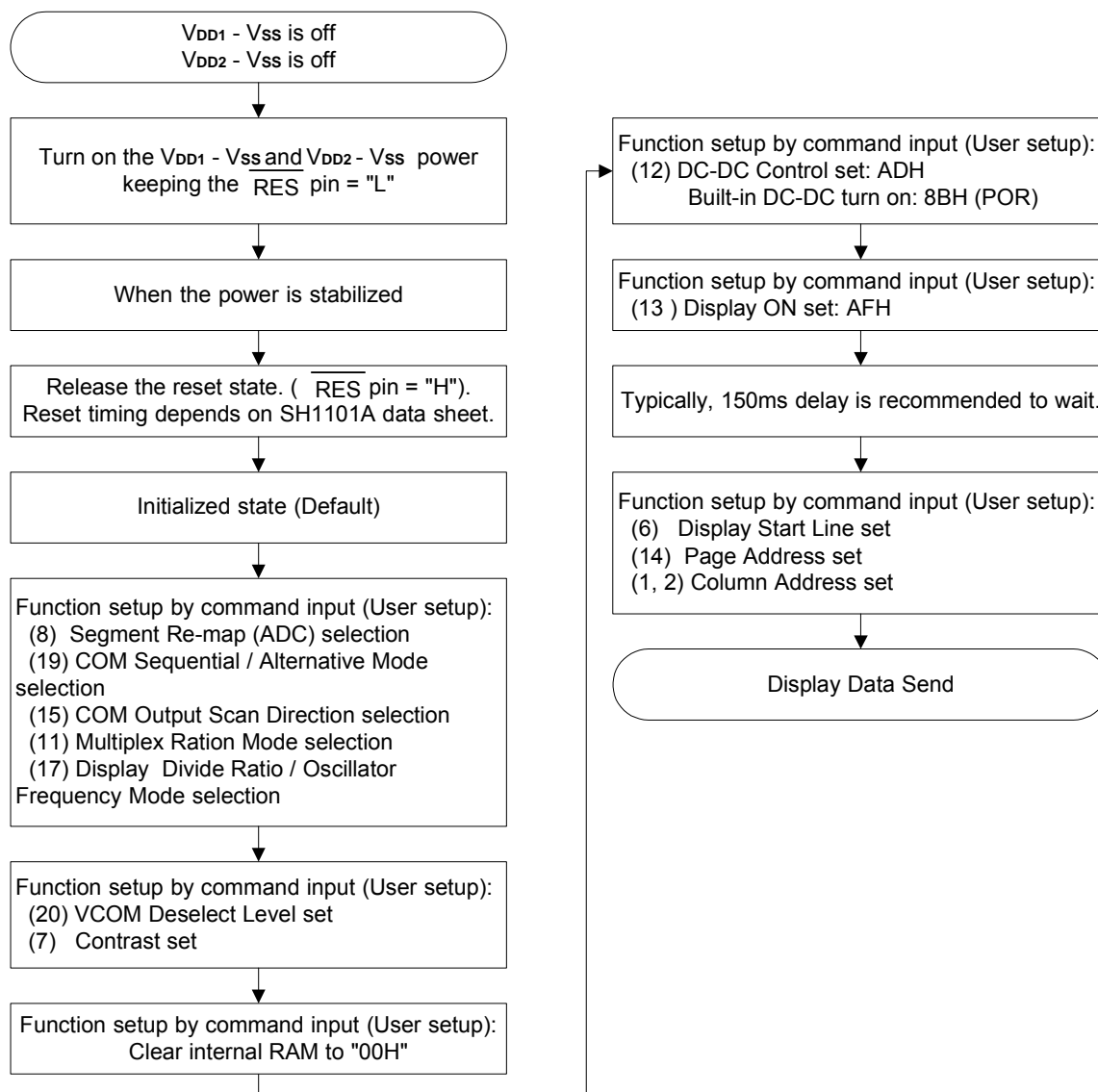


Command Description

Instruction Setup: Reference

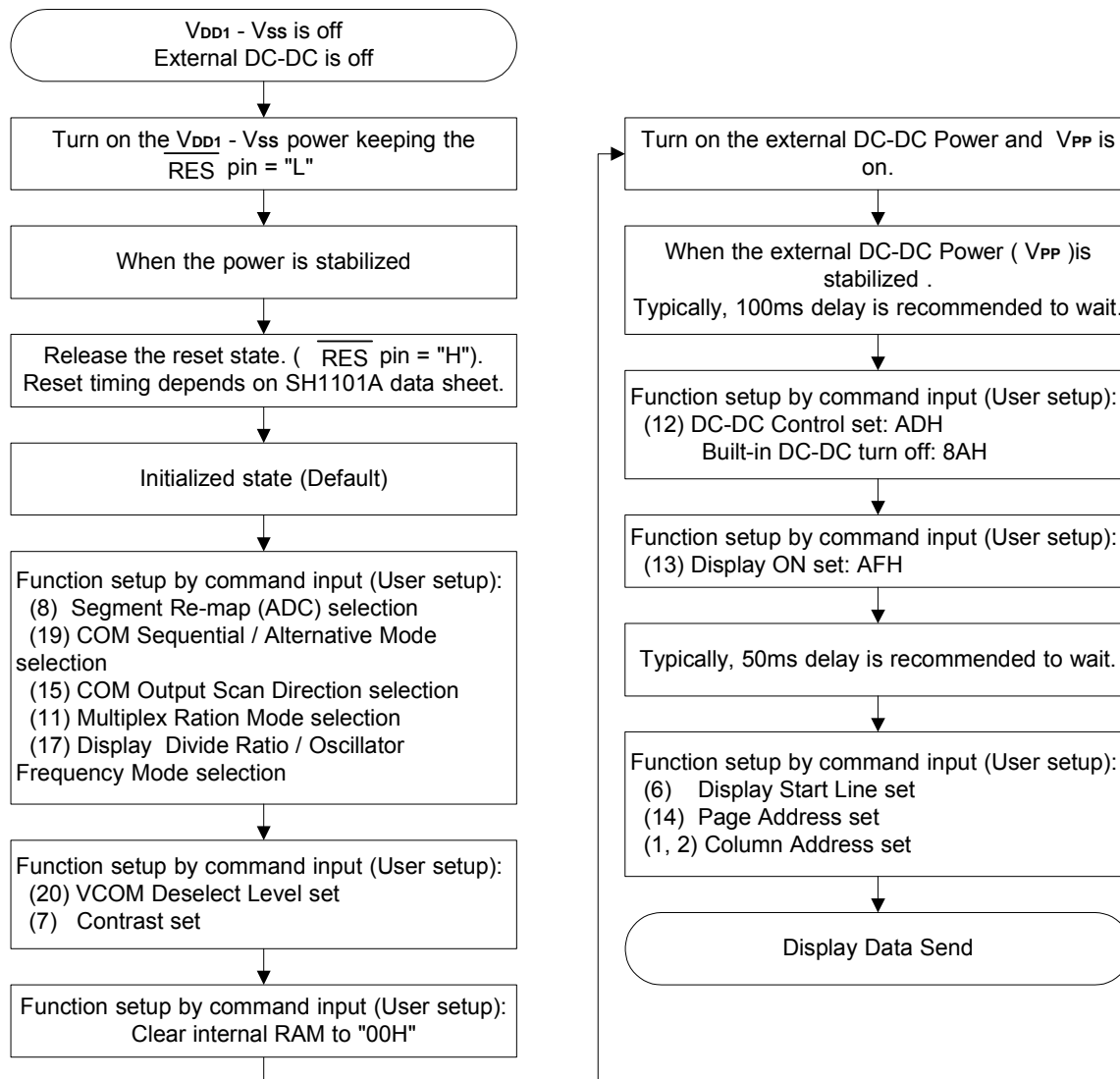
1. Power On and Initialization

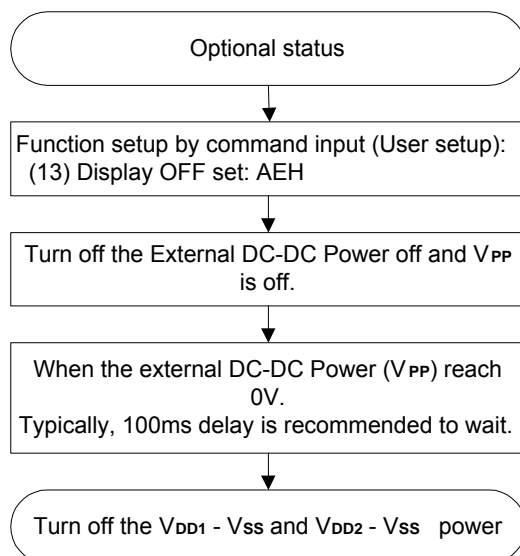
1.1. When the built-in DC-DC pump power is being used immediately after turning on the power:





1.2. When the external DC-DC pump power is being used immediately after turning on the power:



**2. Power Off**



Absolute Maximum Rating*

DC Supply Voltage (VDD1, VDD2)	-0.3V to +3.6V
DC Supply Voltage (VPP)	-0.3V to +18V
Input Voltage	-0.3V to VDD1 + 0.3V
Operating Ambient Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

DC Characteristics (Vss = 0V, VDD1 = 2.4 - 3.5V TA = +25°C, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
VDD1	Operating voltage	2.4	-	3.5	V	Normal mode
		1.65	-	3.5		Low voltage mode
VDD2	Operating voltage	2.4	-	3.5	V	
VPP	OLED Operating voltage	7.0	-	16.0	V	Normal mode
		7.0	-	9.0		Low voltage mode
VBREF	Internal voltage reference	-5%	1.26*	+5%	V	With one 1μF capacitor, 1.26V is the reference value.
IDD1	Dynamic current consumption 1	-	110	160	μA	VDD1 = 3V, VDD2 = 3V, IREF = 10μA, Contrast α = 256, Bulid-in DC-DC OFF, Display ON, display data = All ON, No panel attached.
IDD2	Dynamic current consumption 2	-	190	285	μA	VDD1 = 3V, VDD2 = 3V, VPP = 12V, IREF = -10μA, Contrast α = 256, Bulid-in DC-DC ON, Display ON, Display data = All ON, No panel attached.
IPP	OLED dynamic current consumption	-	550	825	μA	VDD1 = 3V, VDD2 = 3V, VPP = 12V, IREF = -10μA, Contrast α = 256, Display ON, All ON, No panel attached.
ISP	Sleep mode current consumption in VDD1 & VDD2	-	0.01	5	μA	During sleep, TA = +25°C, VDD1 = 3V, VDD2 = 3V.
	Sleep mode current consumption in VPP	-	0.01	5	μA	During sleep, TA = +25°C, VPP = 12V.
ISEG	Segment output current	-308	-320	-342	μA	VDD1 = 3V, VPP = 12V, IREF = -10μA, RLOAD = 20kΩ, Display ON. Contrast α = 256.
		-	-220	-	μA	VDD1 = 3V, VPP = 12V, IREF = -10μA, RLOAD = 20kΩ, Display ON. Contrast α = 176.
		-	-120	-	μA	VDD1 = 3V, VPP = 12V, IREF = -10μA, RLOAD = 20kΩ, Display ON. Contrast α = 96.
		-	-20	-	μA	VDD1 = 3V, VPP = 12V, IREF = -10μA, RLOAD = 20kΩ, Display ON. Contrast α = 16.
ΔISEG1	Segment output current uniformity	-	-	±3	%	ΔISEG1 = (ISEG - IMID)/IMID X 100% IMID = (IMAX + IMIN)/2 ISEG [0:131] at contrast α = 256.
ΔISEG2	Adjacent segment output current uniformity	-	-	±2	%	ΔISEG2 = (ISEG [N] - ISEG [N+1])/ (ISEG [N] + ISEG [N+1]) X 100% ISEG [0:131] at contrast α = 256.



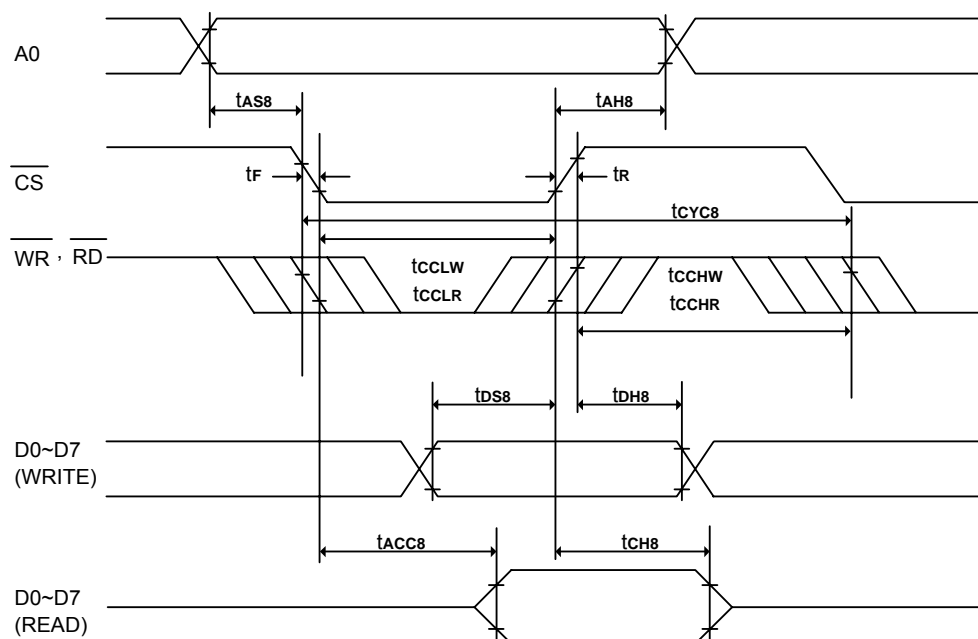
DC Characteristics (Continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V _{IHC}	High-level input voltage	0.8 X V _{DD1}	-	V _{DD1}	V	A0, D0 - D7, \overline{RD} (E), \overline{WR} (R/ \overline{W}), \overline{CS} , CLS, CL, C86, P/S and \overline{RES} .
V _{ILC}	Low-level input voltage	V _{SS}	-	0.2 X V _{DD1}	V	
V _{OHC}	High-level output voltage	0.8 X V _{DD1}	-	V _{DD1}	V	I _{OH} = -0.5mA (D0 - D7, and CL).
V _{OLC}	Low -level output voltage	V _{SS}	-	0.2 X V _{DD1}	V	I _{OL} = 0.5mA (D0 - D7, and CL).
I _{LI}	Input leakage current	-1.0	-	1.0	μA	V _{IN} = V _{DD1} or V _{SS} (A0, \overline{RD} (E), \overline{WR} (R/ \overline{W}), \overline{CS} , CLS, C86, P/S and \overline{RES}).
I _{HZ}	HZ leakage current	-1.0	-	1.0	μA	When the D0 - D7, and CL are in high impedance.
f _{osc}	Oscillation frequency	315	360	420	kHz	T _A = +25°C.
f _{FRM}	Frame frequency for 64 Commons	-	104	-	Hz	When f _{osc} = 360kHz, Divide ratio = 1, common width = 54 DCLKs.



AC Characteristics

(1) System buses Read/Write characteristics 1 (For the 8080 Series Interface MPU)



(VDD1 = 2.4 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tCYC8	System cycle time	300	-	-	ns	
tAS8	Address setup time	0	-	-	ns	
tAH8	Address hold time	0	-	-	ns	
tDS8	Data setup time	40	-	-	ns	
tDH8	Data hold time	15	-	-	ns	
tCH8	Output disable time	10	-	70	ns	CL = 100pF
tACC8	\overline{RD} access time	-	-	140	ns	CL = 100pF
tCCLW	Control L pulse width (WR)	100	-	-	ns	
tCCLR	Control L pulse width (RD)	120	-	-	ns	
tCCHW	Control H pulse width (WR)	100	-	-	ns	
tCCHR	Control H pulse width (RD)	100	-	-	ns	
tR	Rise time	-	-	15	ns	
tF	Fall time	-	-	15	ns	



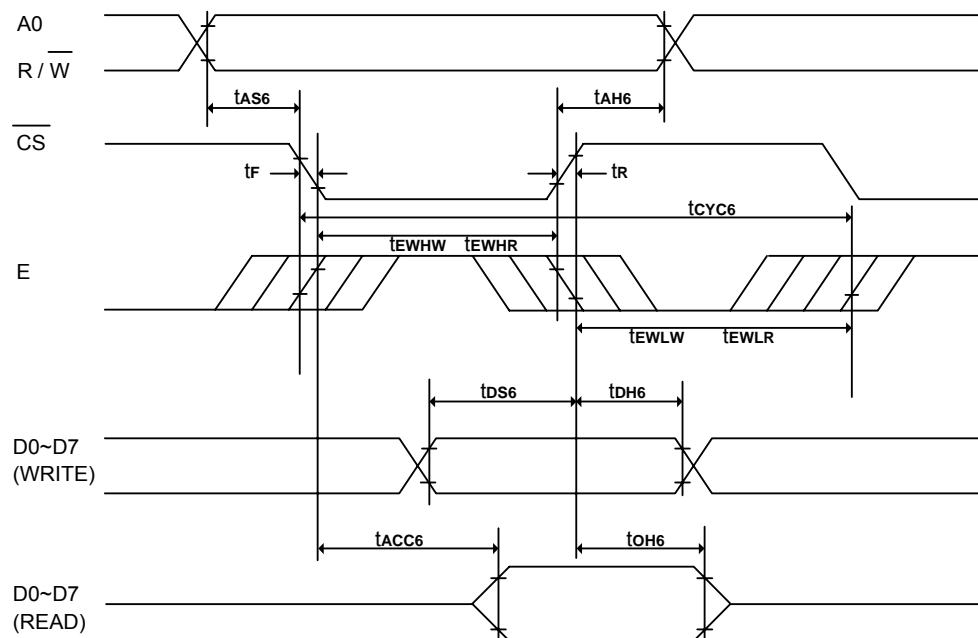
SH1101A

(VDD1 = 1.65 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tCYC8	System cycle time	600	-	-	ns	
tAS8	Address setup time	0	-	-	ns	
tAH8	Address hold time	0	-	-	ns	
tDS8	Data setup time	80	-	-	ns	
tDH8	Data hold time	30	-	-	ns	
tCH8	Output disable time	20	-	140	ns	CL = 100pF
tACC8	\overline{RD} access time	-	-	280	ns	CL = 100pF
tcCLW	Control L pulse width (WR)	200	-	-	ns	
tcCLR	Control L pulse width (RD)	240	-	-	ns	
tcCHW	Control H pulse width (WR)	200	-	-	ns	
tcCHR	Control H pulse width (RD)	200	-	-	ns	
tR	Rise time	-	-	30	ns	
tF	Fall time	-	-	30	ns	



(2) System buses Read/Write Characteristics 2 (For the 6800 Series Interface MPU)



(V_{DD1} = 2.4 - 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t _{CYC6}	System cycle time	300	-	-	ns	
t _{AS6}	Address setup time	0	-	-	ns	
t _{AH6}	Address hold time	0	-	-	ns	
t _{DS6}	Data setup time	40	-	-	ns	
t _{DH6}	Data hold time	15	-	-	ns	
t _{OH6}	Output disable time	10	-	70	ns	C _L = 100pF
t _{ACC6}	Access time	-	-	140	ns	C _L = 100pF
t _{EWHW}	Enable H pulse width (Write)	100	-	-	ns	
t _{EWHR}	Enable H pulse width (Read)	120	-	-	ns	
t _{EWLW}	Enable L pulse width (Write)	100	-	-	ns	
t _{EWLR}	Enable L pulse width (Read)	100	-	-	ns	
t _R	Rise time	-	-	15	ns	
t _F	Fall time	-	-	15	ns	



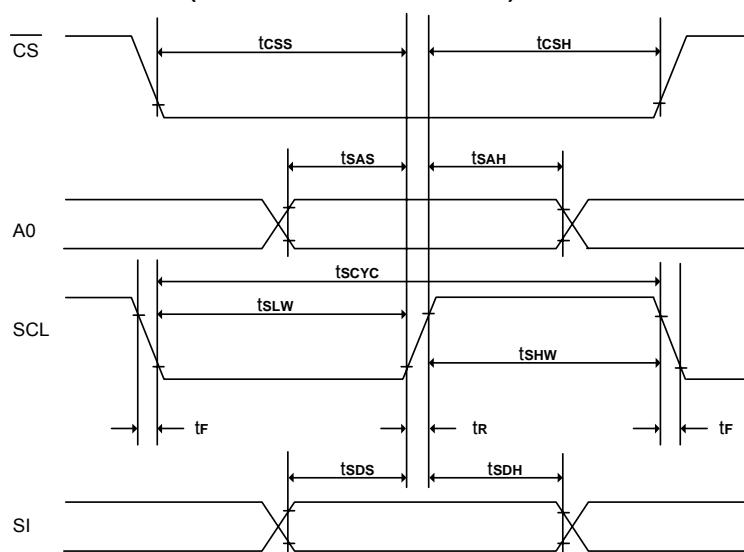
SH1101A

(V_{DD1} = 1.65 - 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t _{CYC6}	System cycle time	600	-	-	ns	
t _{AS6}	Address setup time	0	-	-	ns	
t _{AH6}	Address hold time	0	-	-	ns	
t _{DS6}	Data setup time	80	-	-	ns	
t _{DH6}	Data hold time	30	-	-	ns	
t _{OH6}	Output disable time	20	-	140	ns	C _L = 100pF
t _{ACC6}	Access time	-	-	280	ns	C _L = 100pF
t _{EWHW}	Enable H pulse width (Write)	200	-	-	ns	
t _{EWHR}	Enable H pulse width (Read)	240	-	-	ns	
t _{EWLW}	Enable L pulse width (Write)	200	-	-	ns	
t _{EWLR}	Enable L pulse width (Read)	200	-	-	ns	
t _R	Rise time	-	-	30	ns	
t _F	Fall time	-	-	30	ns	



(3) System buses Write characteristics 3(For the Serial Interface MPU)



(VDD1 = 2.4 - 3.5V, TA = +25°C)

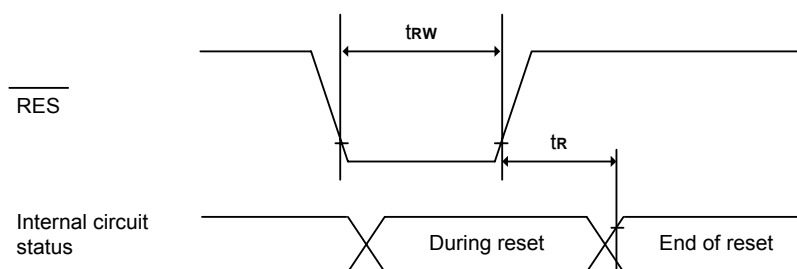
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	250	-	-	ns	
tSAS	Address setup time	150	-	-	ns	
tSAH	Address hold time	150	-	-	ns	
tSDS	Data setup time	100	-	-	ns	
tSDH	Data hold time	100	-	-	ns	
tCSS	\overline{CS} setup time	120	-	-	ns	
tCSH	\overline{CS} hold time time	60	-	-	ns	
tSHW	Serial clock H pulse width	100	-	-	ns	
tSLW	Serial clock L pulse width	100	-	-	ns	
tR	Rise time	-	-	15	ns	
tF	Fall time	-	-	15	ns	

. (VDD1 = 1.65 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	500	-	-	ns	
tSAS	Address setup time	300	-	-	ns	
tSAH	Address hold time	300	-	-	ns	
tSDS	Data setup time	200	-	-	ns	
tSDH	Data hold time	200	-	-	ns	
tCSS	\overline{CS} setup time	240	-	-	ns	
tCSH	\overline{CS} hold time time	120	-	-	ns	
tSHW	Serial clock H pulse width	200	-	-	ns	
tSLW	Serial clock L pulse width	200	-	-	ns	
tR	Rise time	-	-	30	ns	
tF	Fall time	-	-	30	ns	



(4) Reset Timing



($V_{DD1} = 2.4 - 3.5V$, $T_A = +25^{\circ}C$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_R	Reset time	-	-	1.0	μs	
t_{RW}	Reset low pulse width	5.0	-	-	μs	

($V_{DD1} = 1.65 - 3.5V$, $T_A = +25^{\circ}C$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_R	Reset time	-	-	2.0	μs	
t_{RW}	Reset low pulse width	10.0	-	-	μs	



Application Circuit (for reference only)

Reference Connection to MPU:

1. 8080 series interface: (Internal oscillator, External Vpp)

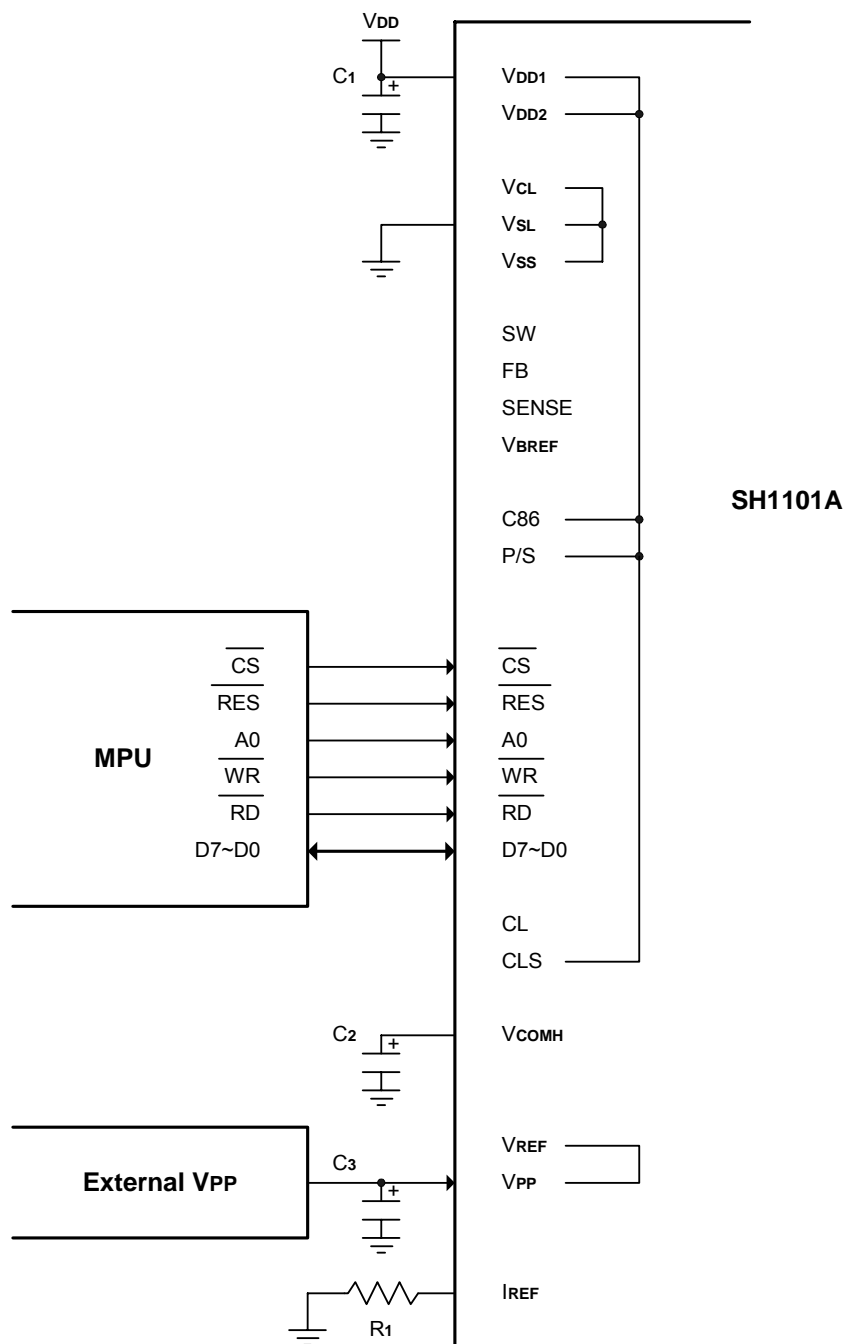


Figure. 8

Note:

C1 - C3: 4.7μF.

R1: about 910kΩ, $R1 = (\text{Voltage at IREF} - V_{SS})/I_{REF}$





2. 6800 Series Interface: (Internal oscillator, Built-in DC-DC)

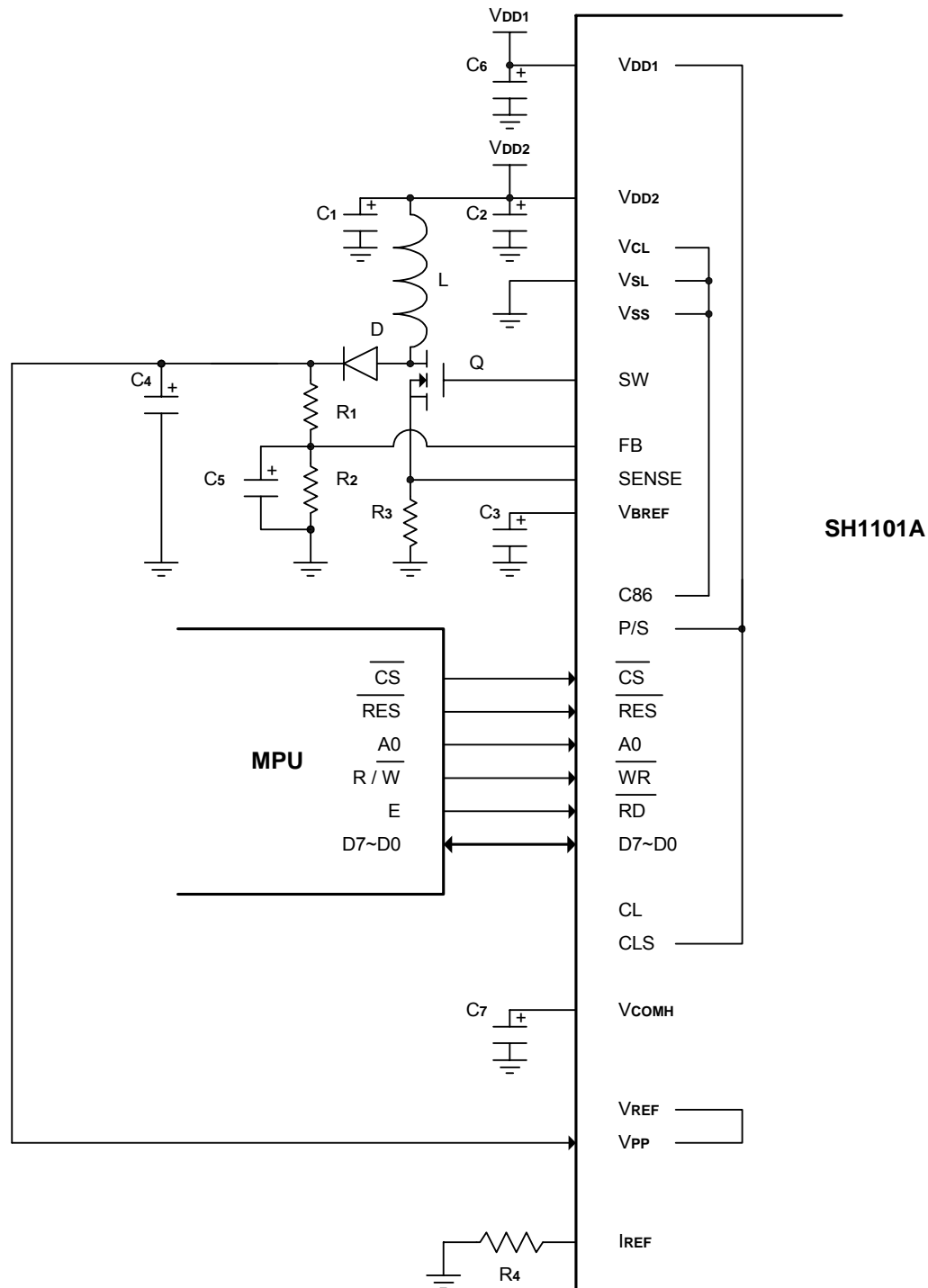


Figure. 9

Note:

L, D, Q, R1, R2, R3, C1 - C6: Please refer to following description of DC-DC module.

C6, C7: 4.7μF

R3: about 910kΩ, R4 = (Voltage at IREF - VSS)/IREF





3. Serial Interface: (External oscillator, External VPP)

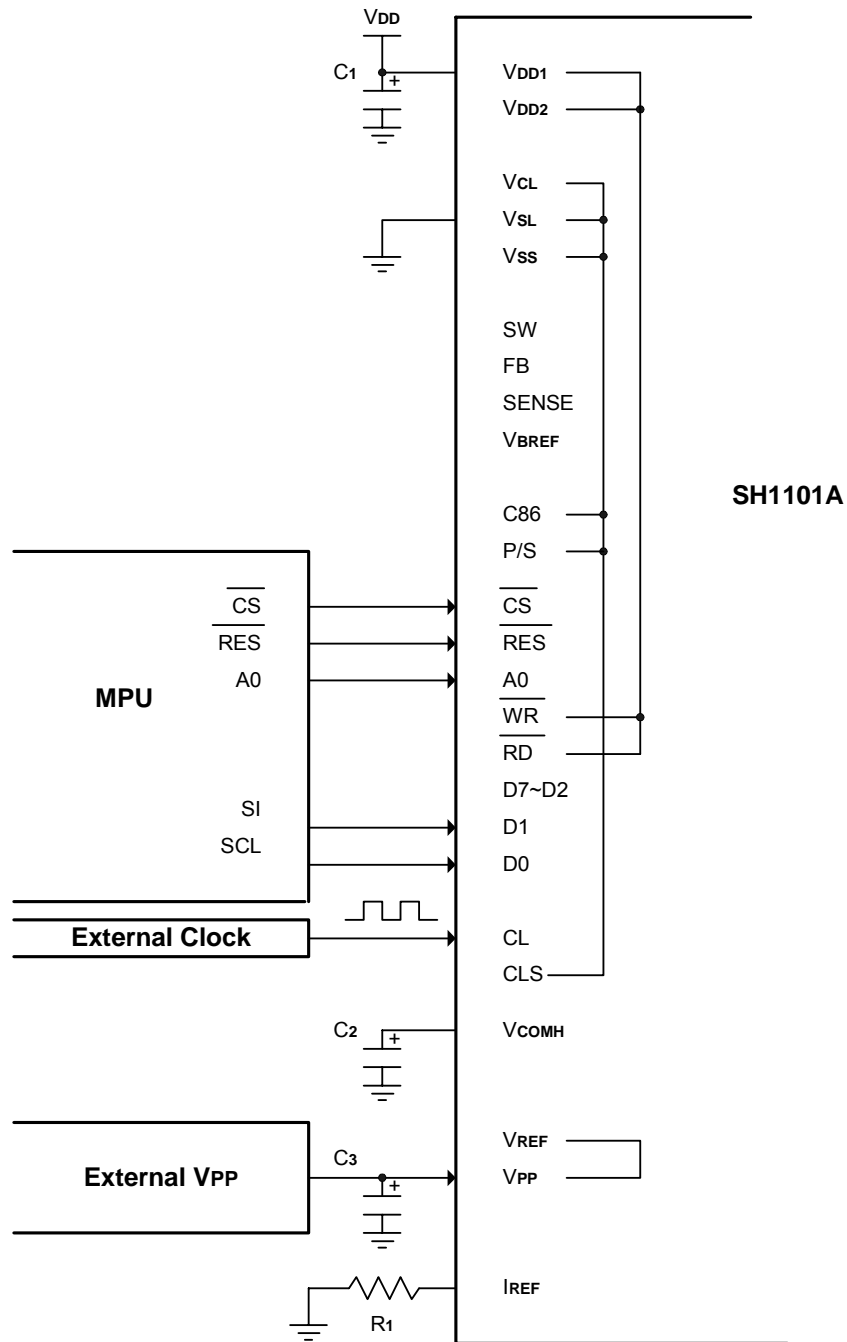


Figure. 10

Note:

$C1 - C3$: $4.7\mu F$

$R1$: about $910k\Omega$, $R1 = (Voltage\ at\ I_{REF} - V_{SS})/I_{REF}$



DC-DC:

Below application circuit is an example for the input voltage of 3V V_{DD2} to generate V_{PP} of about 12V@10mA-25mA application.

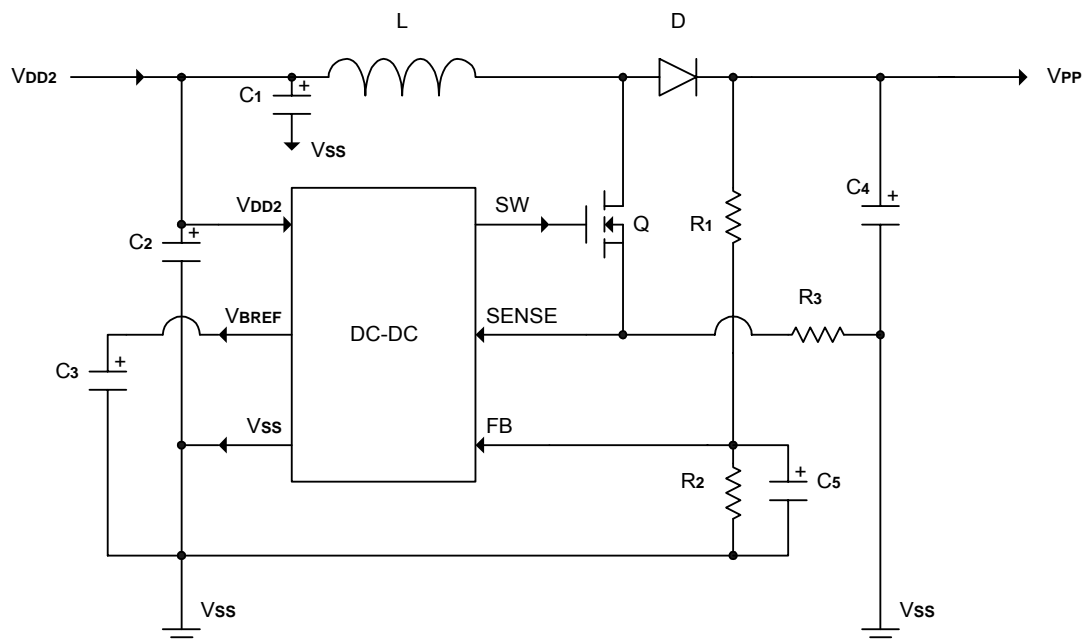


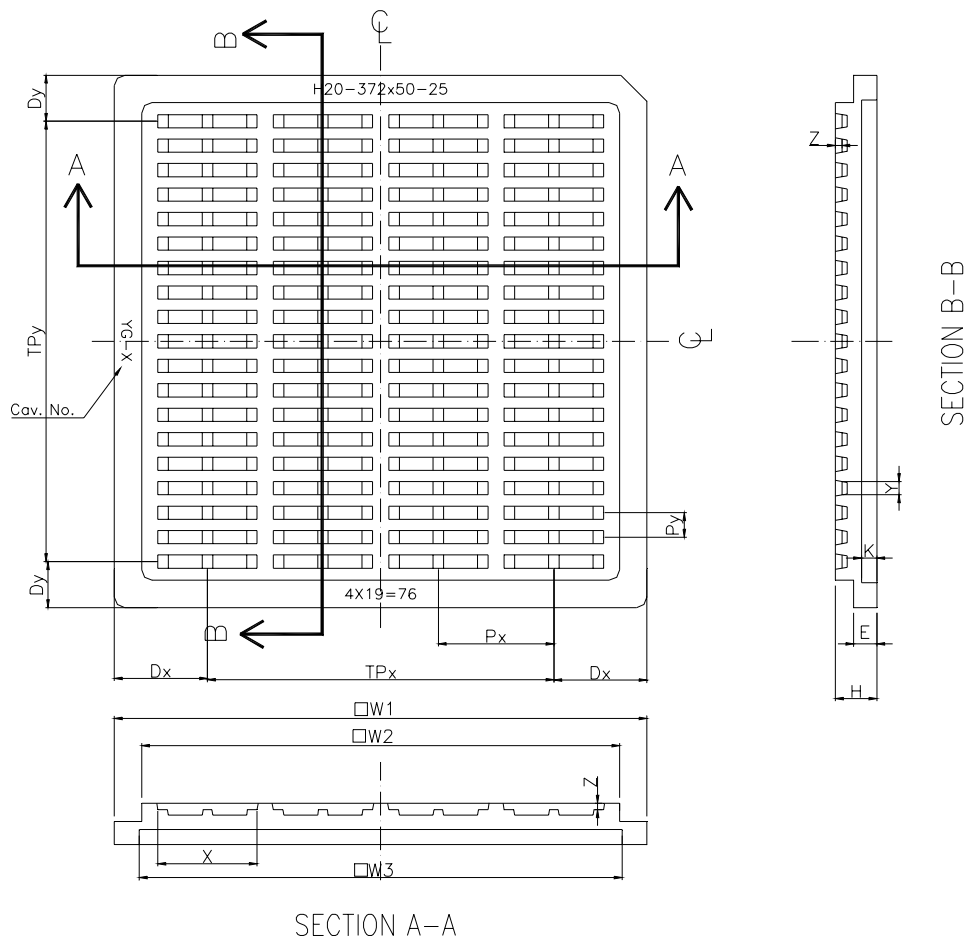
Figure. 11

Symbol	Value	Recommendation
L	10 μ H	LQH3C100K24
D	SCHOTTKY DIODE	20V@0.5A, MBR0520
Q	MOSFET	N-FET with low $R_{DS(on)}$ and low V_{TH} , MGSF1N02LT1
R1	930k Ω	1%, 1/8W
R2	110k Ω	1%, 1/8W
R3	0.12 Ω	1%, 1/2W
C1	1 - 10 μ F	Low ESR/6.3V
C2	0.1 - 1 μ F	Ceramic/16V
C3	1 μ F	Ceramic/16V
C4	6.8 μ F	Low ESR/16V
C5	1000pF	Ceramic/16V



SH1101A

Tray Information



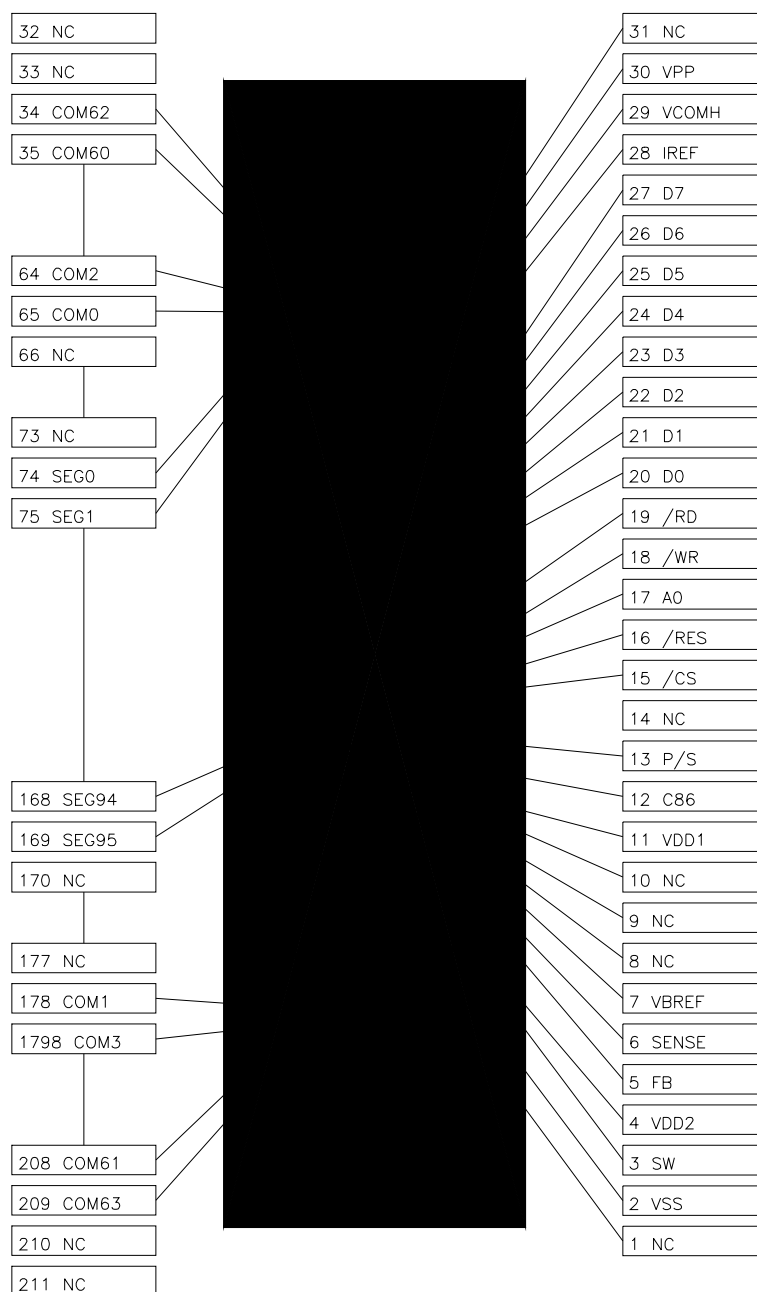
SECTION A-A

	Spec
	mm (mil)
W1	50.70±0.05 (1996)
W2	45.50±0.10 (1791)
W3	45.95±0.10 (1809)
H	3.95±0.05 (156)
E	2.20±0.05 (87)
K	1.45±0.10 (57)
Dx	8.87±0.05 (349)
TPx	32.97±0.10 (1298)
Dy	4.38±0.05 (172)
TPy	41.94±0.10 (1651)
Px	10.99±0.05 (433)
Py	2.33±0.05 (92)
X	9.45±0.05 (372)
Y	1.26±0.05 (50)
Z	0.63±0.05 (25)
N	76(pocket number)





SH1101A-TCP03 TCP Pin Layout



(Copper Side View)



SH1101A-TCP03 TCP Pin Assignment (Total: 211 pins)

Pin No.	Designation	Pin No.	Designation	Pin No.	Designation	Pin No.	Designation
1	NC	41	COM48	81	SEG7	121	SEG47
2	Vss	42	COM46	82	SEG8	122	SEG48
3	SW	43	COM44	83	SEG9	123	SEG49
4	VDD2	44	COM42	84	SEG10	124	SEG50
5	FB	45	COM40	85	SEG11	125	SEG51
6	SENSE	46	COM38	86	SEG12	126	SEG52
7	VBREF	47	COM36	87	SEG13	127	SEG53
8	NC	48	COM34	88	SEG14	128	SEG54
9	NC	49	COM32	89	SEG15	129	SEG55
10	NC	50	COM30	90	SEG16	130	SEG56
11	VDD1	51	COM28	91	SEG17	131	SEG57
12	C86	52	COM26	92	SEG18	132	SEG58
13	P/S	53	COM24	93	SEG19	133	SEG59
14	NC	54	COM22	94	SEG20	134	SEG60
15	CS	55	COM20	95	SEG21	135	SEG61
16	RES	56	COM18	96	SEG22	136	SEG62
17	A0	57	COM16	97	SEG23	137	SEG63
18	WR	58	COM14	98	SEG24	139	SEG64
19	RD	59	COM12	99	SEG25	139	SEG65
20	D0	60	COM10	100	SEG26	140	SEG66
21	D1	61	COM8	101	SEG27	141	SEG67
22	D2	62	COM6	102	SEG28	142	SEG68
23	D3	63	COM4	103	SEG29	143	SEG69
24	D4	64	COM2	104	SEG30	144	SEG70
25	D5	65	COM0	105	SEG31	145	SEG71
26	D6	66	NC	106	SEG32	146	SEG72
27	D7	67	NC	107	SEG33	147	SEG73
28	IREF	68	NC	108	SEG34	148	SEG74
29	VCOMH	69	NC	109	SEG35	149	SEG75
30	VPP	70	NC	110	SEG36	150	SEG76
31	NC	71	NC	111	SEG37	151	SEG77
32	NC	72	NC	112	SEG38	152	SEG78
33	NC	73	NC	113	SEG39	153	SEG79
34	COM62	74	SEG0	114	SEG40	154	SEG80
35	COM60	75	SEG1	115	SEG41	155	SEG81
36	COM58	76	SEG2	116	SEG42	156	SEG82
37	COM56	77	SEG3	117	SEG43	157	SEG83
38	COM54	78	SEG4	118	SEG44	158	SEG84
39	COM52	79	SEG5	119	SEG45	159	SEG85
40	COM50	80	SEG6	120	SEG46	160	SEG86



SH1101A-TCP03 TCP Pin Assignment (continued)

Pin No.	Designation	Pin No.	Designation	Pin No.	Designation	Pin No.	Designation
161	SEG87	176	NC	191	COM27	206	COM57
162	SEG88	177	NC	192	COM29	207	COM59
163	SEG89	178	COM1	193	COM31	208	COM61
164	SEG90	179	COM3	194	COM33	209	COM63
165	SEG91	180	COM5	195	COM35	210	NC
166	SEG92	181	COM7	196	COM37	211	NC
167	SEG93	182	COM9	197	COM39		
168	SEG94	183	COM11	198	COM41		
169	SEG95	184	COM13	199	COM43		
170	NC	185	COM15	200	COM45		
171	NC	186	COM17	201	COM47		
172	NC	187	COM19	202	COM49		
173	NC	188	COM21	203	COM51		
174	NC	189	COM23	204	COM53		
175	NC	190	COM25	205	COM55		

Note:

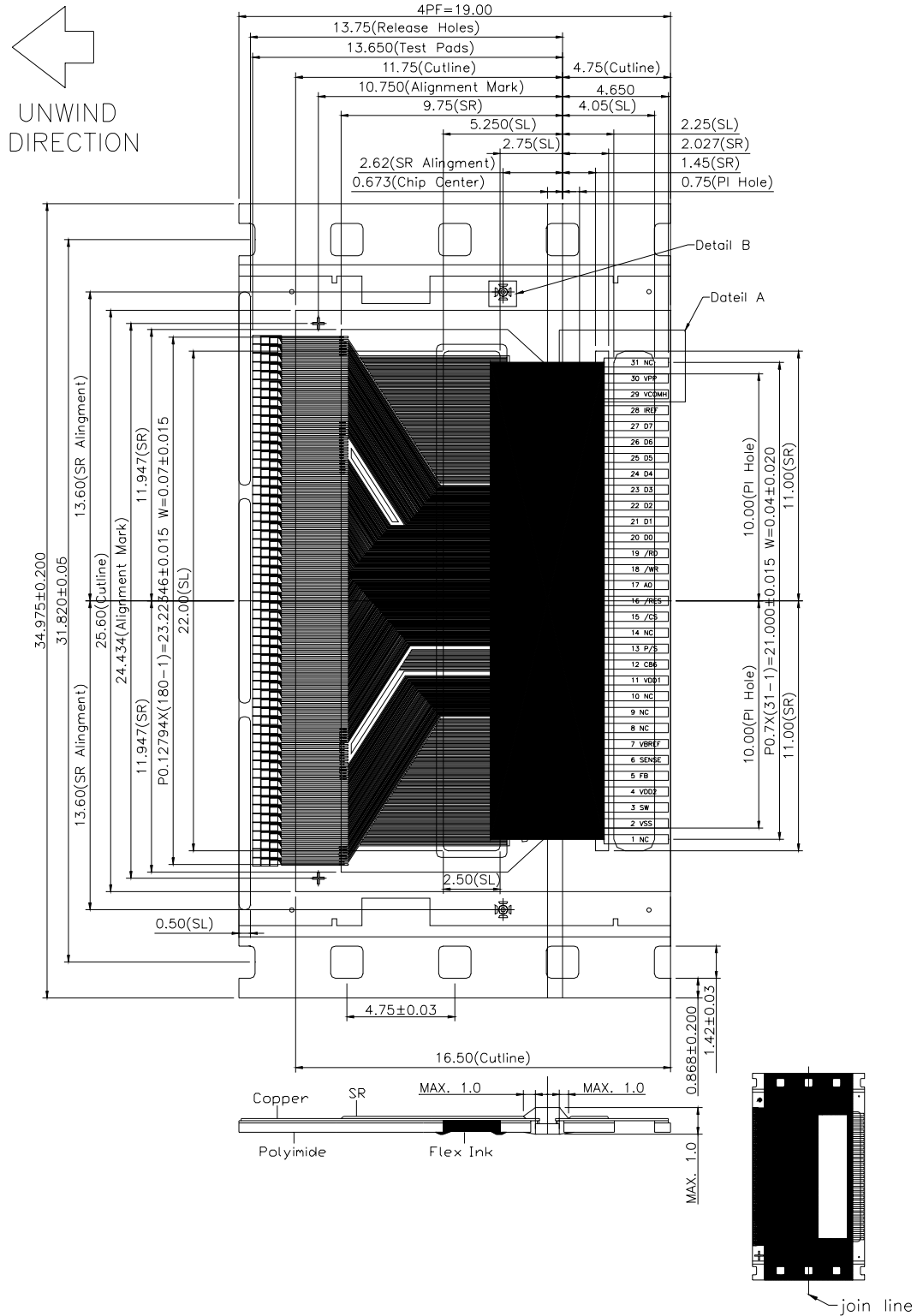
Following is the details of pad connection in SH1101A-TCP03 (TCP Form).

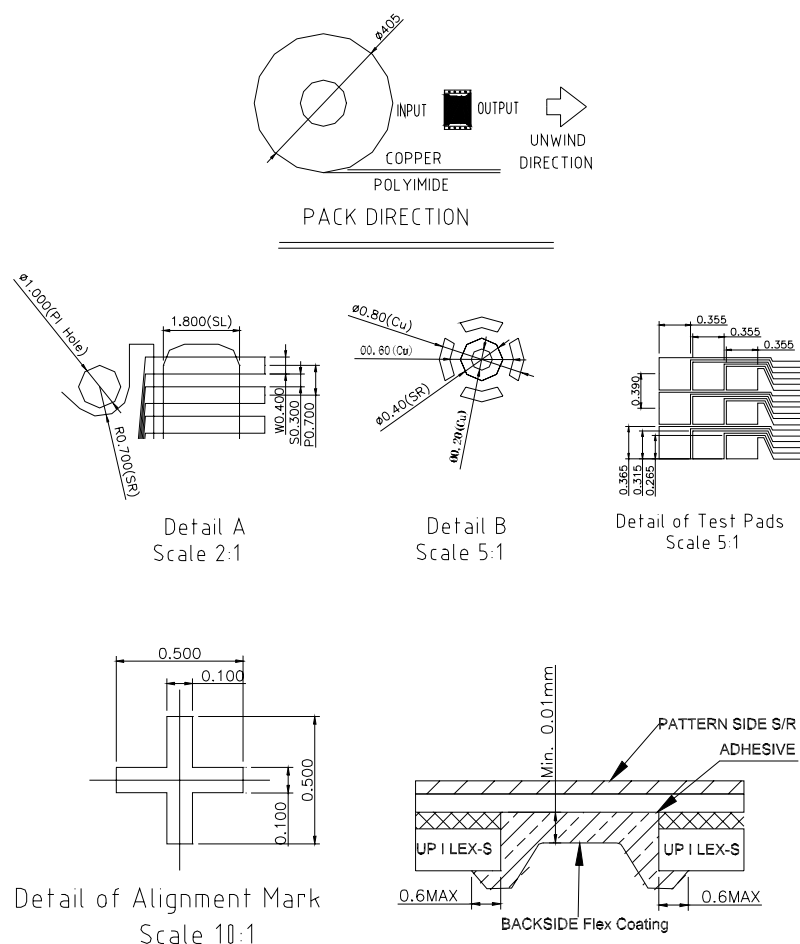
- “CLS” pad connects to “VDD1” pad, Internal oscillator circuit is enabled.
- “VREF” pad connects to “VPP” pad.
- “VCL” & “VSL” pad connects to “VSS” pad.
- “C86” & “P/S” pad options can be selected by user. So SH1101A-TCP03 (TCP Form) supports 8-bit 6800-series parallel interface, 8-bit 8080-series parallel interface or serial peripheral interface.
- SH1101A-TCP03 (TCP Form) supports internal DC-DC converter function.



SH1101A

External View of SH1101A-TCP03 TCP Pins





NOTES:

1. All SR Dimension Tolerance $\pm 0.200\text{mm}$ if not specified
2. All SL Dimension Tolerance $\pm 0.05\text{mm}$ if not specified
3. Corner radii unless otherwise specified is 0.20mm
4. PKG Reel Size : $\phi 4.05\text{mm}$
5. Input IL total pitch from left 2nd to right 2nd
6. Output IL total pitch from left 2nd to right 2nd
7. IL Pitch=45um ; Min Pitch=45um/IL/Trace

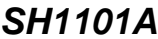
Cautions Concerning Storage:

1. When storing the product, it is recommended that it be left in its shipping package.
After the seal of the packing bag has been broken, store the products in a nitrogen atmosphere.
2. Storage conditions:

Storage state	Storage conditions
unopened (less than 90 days)	Temperature: 5 to 30 ; humidity: 80%RH or less.
After seal of broken (less than 30 days)	Room temperature, dry nitrogen atmosphere

3. Don't store in a location exposed to corrosive gas or excessive dust.
4. Don't store in a location exposed to direct sunlight or subject to sharp changes in temperature.
5. Don't store the product such that it is subjected to an excessive load weight, such as by stacking.
6. Deterioration of the plating may occur after long-term storage, so special care is required.
It is recommended that the products be inspected before use.





Appendix



SH1101A

SH1101A-TCP06 TAB Pin Assignment (Total: 249 pads)

Pin No.	Designation	Pin No.	Designation	Pin No.	Designation	Pin No.	Designation
1	NC	41	COM49	81	SEG123	121	SEG83
2	VPP	42	COM47	82	SEG122	122	SEG82
3	VCOMH	43	COM45	83	SEG121	123	SEG81
4	IREF	44	COM43	84	SEG120	124	SEG80
5	D7	45	COM41	85	SEG119	125	SEG79
6	D6	46	COM39	86	SEG118	126	SEG78
7	D5	47	COM37	87	SEG117	127	SEG77
8	D4	48	COM35	88	SEG116	128	SEG76
9	D3	49	COM33	89	SEG115	129	SEG75
10	D2	50	COM31	90	SEG114	130	SEG74
11	D1	51	COM29	91	SEG113	131	SEG73
12	D0	52	COM27	92	SEG112	132	SEG72
13	RD	53	COM25	93	SEG111	133	SEG71
14	WR	54	COM23	94	SEG110	134	SEG70
15	A0	55	COM21	95	SEG109	135	SEG69
16	RES	56	COM19	96	SEG108	136	SEG68
17	CS	57	COM17	97	SEG107	137	SEG67
18	NC	58	COM15	98	SEG106	139	SEG66
19	P/S	59	COM13	99	SEG105	139	SEG65
20	C86	60	COM11	100	SEG104	140	SEG64
21	VDD1	61	COM9	101	SEG103	141	SEG63
22	NC	62	COM7	102	SEG102	142	SEG62
23	NC	63	COM5	103	SEG101	143	SEG61
24	NC	64	COM3	104	SEG100	144	SEG60
25	VBREF	65	COM1	105	SEG99	145	SEG59
26	SENSE	66	NC	106	SEG98	146	SEG58
27	FB	67	NC	107	SEG97	147	SEG57
28	VDD2	68	NC	108	SEG96	148	SEG56
29	SW	69	NC	109	SEG95	149	SEG55
30	VSS	70	NC	110	SEG94	150	SEG54
31	NC	71	NC	111	SEG93	151	SEG53
32	NC	72	NC	112	SEG92	152	SEG52
33	NC	73	SEG131	113	SEG91	153	SEG51
34	COM63	74	SEG130	114	SEG90	154	SEG50
35	COM61	75	SEG129	115	SEG89	155	SEG49
36	COM59	76	SEG128	116	SEG88	156	SEG48
37	COM57	77	SEG127	117	SEG87	157	SEG47
38	COM55	78	SEG126	118	SEG86	158	SEG46
39	COM53	79	SEG125	119	SEG85	159	SEG45
40	COM51	80	SEG124	120	SEG84	160	SEG44

**TAB Pin Assignment (continued)**

Pin No.	Designation	Pin No.	Designation	Pin No.	Designation	Pin No.	Designation
161	SEG43	184	SEG20	207	NC	230	COM28
162	SEG42	185	SEG19	208	NC	231	COM30
163	SEG41	186	SEG18	209	NC	232	COM32
164	SEG40	187	SEG17	210	NC	233	COM34
165	SEG39	188	SEG16	211	NC	234	COM36
166	SEG38	189	SEG15	212	NC	235	COM38
167	SEG37	190	SEG14	213	NC	236	COM40
168	SEG36	191	SEG13	214	NC	237	COM42
169	SEG35	192	SEG12	215	NC	238	COM44
170	SEG34	193	SEG11	216	COM0	239	COM46
171	SEG33	194	SEG10	217	COM2	240	COM48
172	SEG32	195	SEG9	218	COM4	241	COM50
173	SEG31	196	SEG8	219	COM6	242	COM52
174	SEG30	197	SEG7	220	COM8	243	COM54
175	SEG29	198	SEG6	221	COM10	244	COM56
176	SEG28	199	SEG5	222	COM12	245	COM58
177	SEG27	200	SEG4	223	COM14	246	COM60
178	SEG26	201	SEG3	224	COM16	247	COM62
179	SEG25	202	SEG2	225	COM18	248	NC
180	SEG24	203	SEG1	226	COM20	249	NC
181	SEG23	204	SEG0	227	COM22		
182	SEG22	205	NC	228	COM24		
183	SEG21	206	NC	229	COM26		

Note:

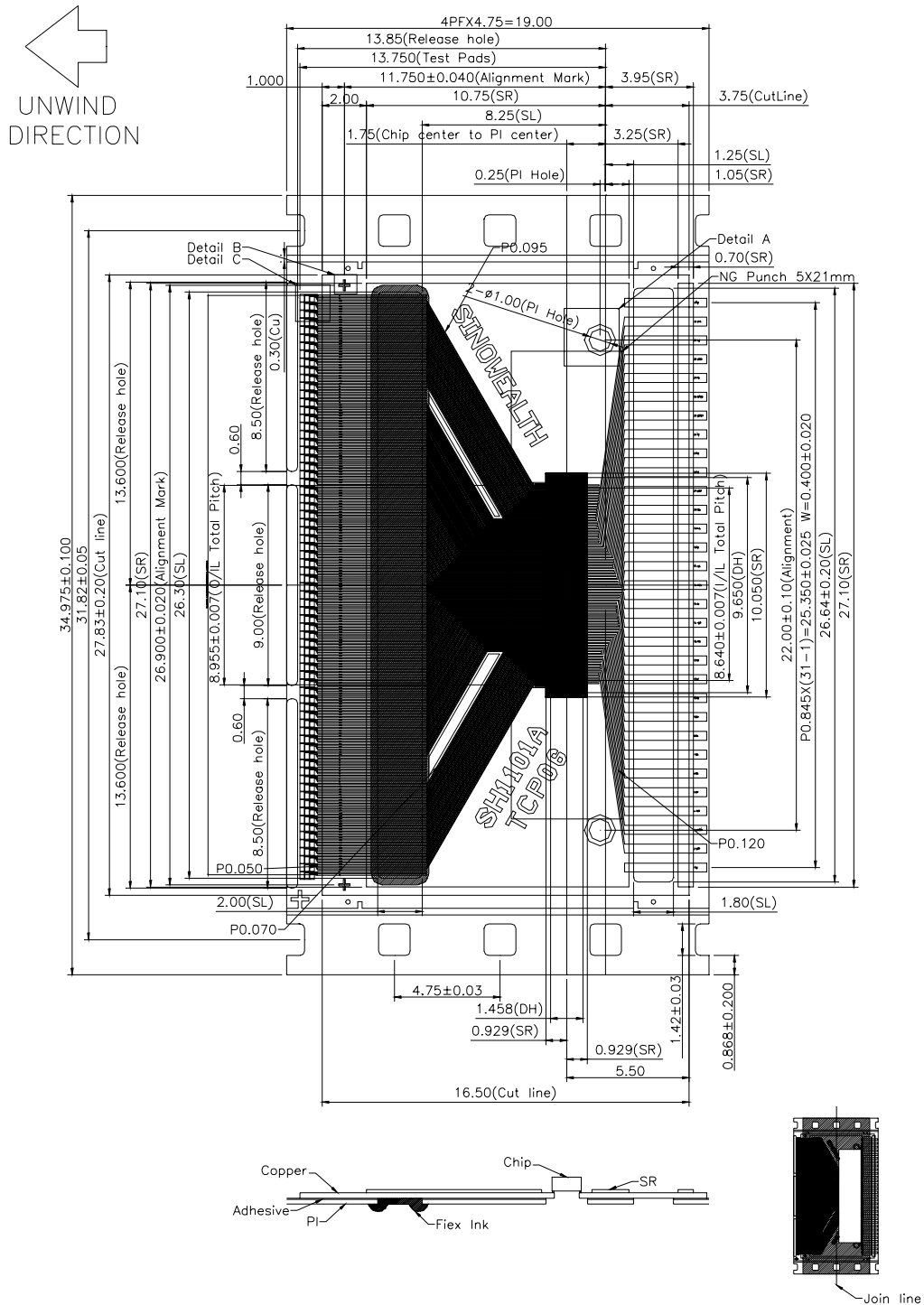
Following is the details of pad connection in SH1101A-TCP06 (TCP Form).

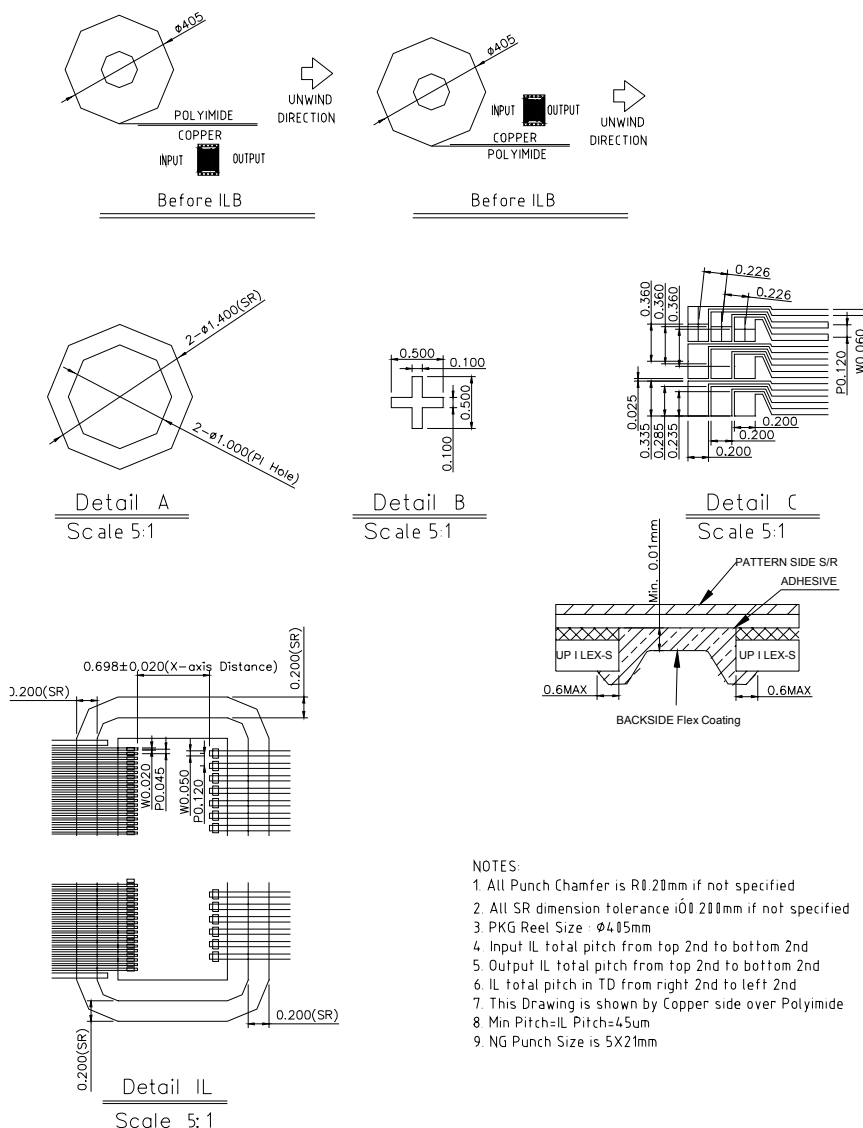
- “CLS” pad connects to “VDD1” pad, Internal oscillator circuit is enabled.
- “VREF” pad connects to “VPP” pad.
- “VCL” & “VSL” pad connects to “VSS” pad.
- “C86” & “P/S” pad options can be selected by user. So SH1101A-TCP06 (TCP Form) supports 8-bit 6800-series parallel interface, 8-bit 8080-series parallel interface or serial peripheral interface.
- SH1101A-TCP06 (TCP Form) supports internal DC-DC converter function.



SH1101A

External View of SH1101A-TCP06 TAB Pins





Cautions Concerning Storage:

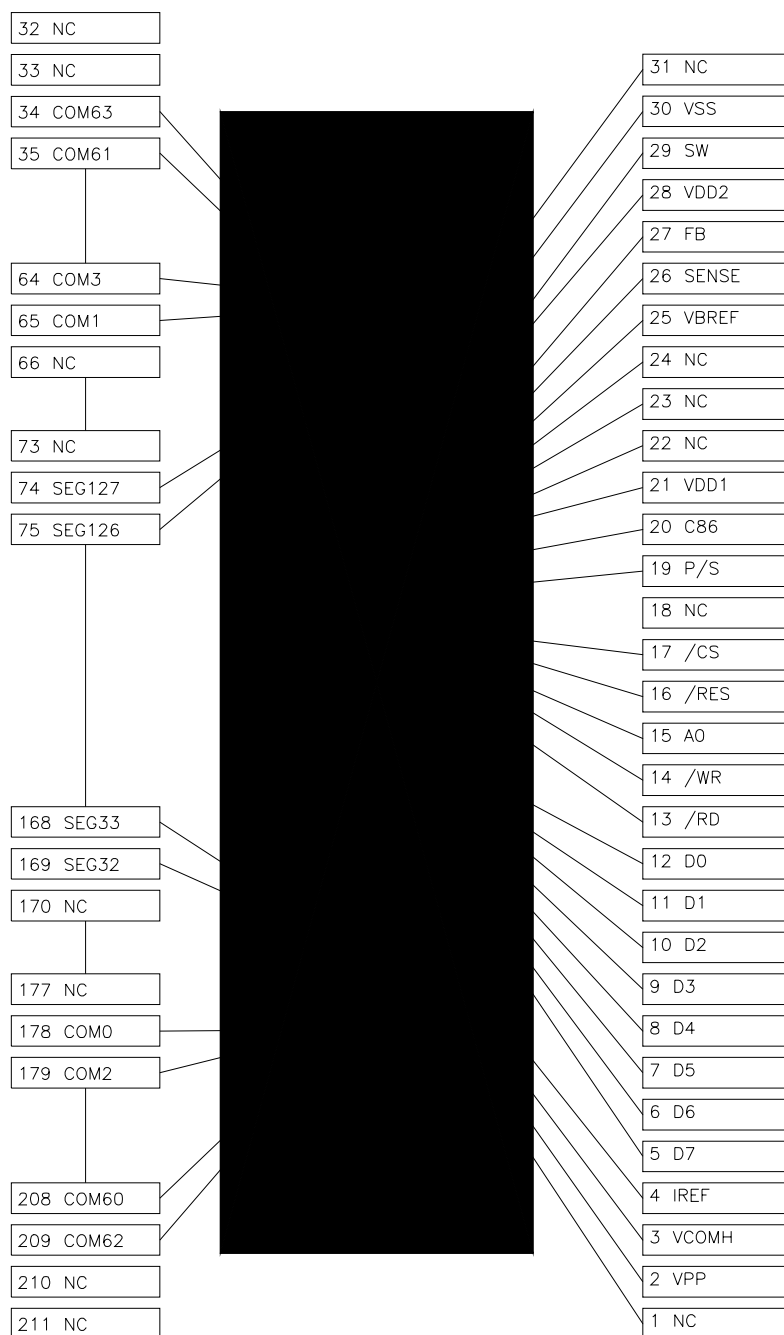
1. When storing the product, it is recommended that it be left in its shipping package.
After the seal of the packing bag has been broken, store the products in a nitrogen atmosphere.
2. Storage conditions:

Storage state	Storage conditions
unopened (less than 90 days)	Temperature: 5 to 30 ; humidity: 80%RH or less.
After seal of broken (less than 30 days)	Room temperature, dry nitrogen atmosphere

3. Don't store in a location exposed to corrosive gas or excessive dust.
4. Don't store in a location exposed to direct sunlight or subject to sharp changes in temperature.
5. Don't store the product such that it subjected to an excessive load weight, such as by stacking.
6. Deterioration of the plating may occur after long-term storage, so special care is required.
It is recommended that the products be inspected before use.



SH1101A-TCP09 TCP Pin Layout



(Copper Side View)



SH1101A

SH1101A-TCP09 TCP Pin Assignment (Total: 211 pads)

Pin No.	Designation	Pin No.	Designation	Pin No.	Designation	Pin No.	Designation
1	NC	41	COM49	81	SEG120	121	SEG80
2	V _{PP}	42	COM47	82	SEG119	122	SEG79
3	V _{COMH}	43	COM45	83	SEG118	123	SEG78
4	I _{REF}	44	COM43	84	SEG117	124	SEG77
5	D7	45	COM41	85	SEG116	125	SEG76
6	D6	46	COM39	86	SEG115	126	SEG75
7	D5	47	COM37	87	SEG114	127	SEG74
8	D4	48	COM35	88	SEG113	128	SEG73
9	D3	49	COM33	89	SEG112	129	SEG72
10	D2	50	COM31	90	SEG111	130	SEG71
11	D1	51	COM29	91	SEG110	131	SEG70
12	D0	52	COM27	92	SEG109	132	SEG69
13	$\overline{\text{RD}}$	53	COM25	93	SEG108	133	SEG68
14	$\overline{\text{WR}}$	54	COM23	94	SEG107	134	SEG67
15	A0	55	COM21	95	SEG106	135	SEG66
16	$\overline{\text{RES}}$	56	COM19	96	SEG105	136	SEG65
17	$\overline{\text{CS}}$	57	COM17	97	SEG104	137	SEG64
18	NC	58	COM15	98	SEG103	139	SEG63
19	P/S	59	COM13	99	SEG102	139	SEG62
20	C86	60	COM11	100	SEG101	140	SEG61
21	V _{DD1}	61	COM9	101	SEG100	141	SEG80
22	NC	62	COM7	102	SEG99	142	SEG79
23	NC	63	COM5	103	SEG98	143	SEG78
24	NC	64	COM3	104	SEG97	144	SEG77
25	V _{BREF}	65	COM1	105	SEG96	145	SEG76
26	SENSE	66	NC	106	SEG95	146	SEG75
27	FB	67	NC	107	SEG94	147	SEG74
28	V _{DD2}	68	NC	108	SEG93	148	SEG73
29	SW	69	NC	109	SEG92	149	SEG72
30	V _{SS}	70	NC	110	SEG91	150	SEG71
31	NC	71	NC	111	SEG90	151	SEG70
32	NC	72	NC	112	SEG89	152	SEG69
33	NC	73	NC	113	SEG88	153	SEG68
34	COM63	74	SEG127	114	SEG87	154	SEG67
35	COM61	75	SEG126	115	SEG86	155	SEG66
36	COM59	76	SEG125	116	SEG85	156	SEG65
37	COM57	77	SEG124	117	SEG84	157	SEG64
38	COM55	78	SEG123	118	SEG83	158	SEG63
39	COM53	79	SEG122	119	SEG82	159	SEG62
40	COM51	80	SEG121	120	SEG81	160	SEG61



SH1101A-TCP09 TCP Pin Assignment (continued)

Pin No.	Designation	Pin No.	Designation	Pin No.	Designation	Pin No.	Designation
161	SEG60	176	NC	191	COM26	206	COM56
162	SEG59	177	NC	192	COM28	207	COM58
163	SEG58	178	COM0	193	COM30	208	COM60
164	SEG57	179	COM2	194	COM32	209	COM62
165	SEG56	180	COM4	195	COM34	210	NC
166	SEG55	181	COM6	196	COM36	211	NC
167	SEG54	182	COM8	197	COM38		
168	SEG53	183	COM10	198	COM40		
169	SEG52	184	COM12	199	COM42		
170	SEG51	185	COM14	200	COM44		
171	SEG50	186	COM16	201	COM46		
172	SEG49	187	COM18	202	COM48		
173	SEG48	188	COM20	203	COM50		
174	SEG47	189	COM22	204	COM52		
175	SEG46	190	COM24	205	COM54		

Note:

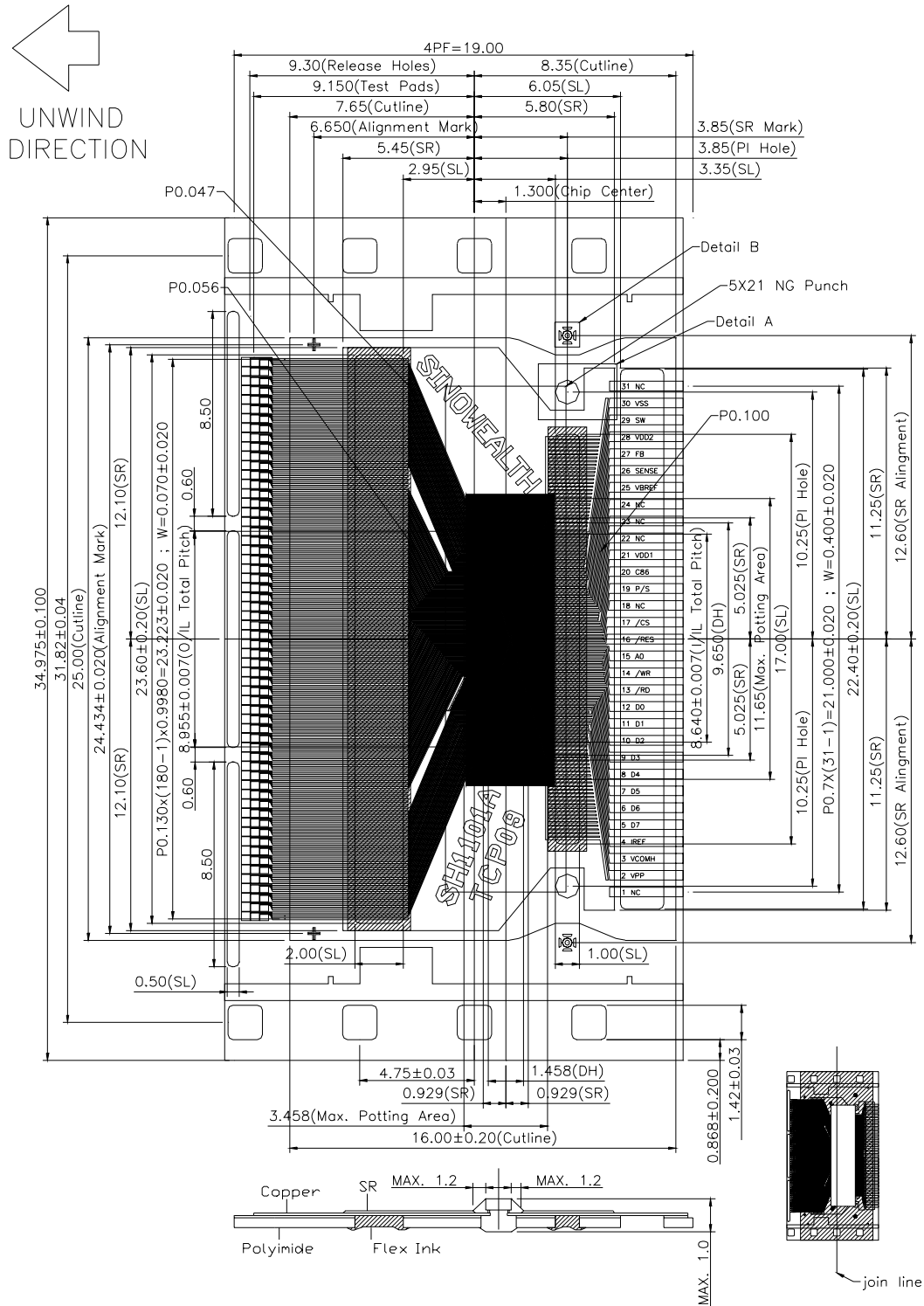
Following is the details of pad connection in SH1101A-TCP09 (TCP Form).

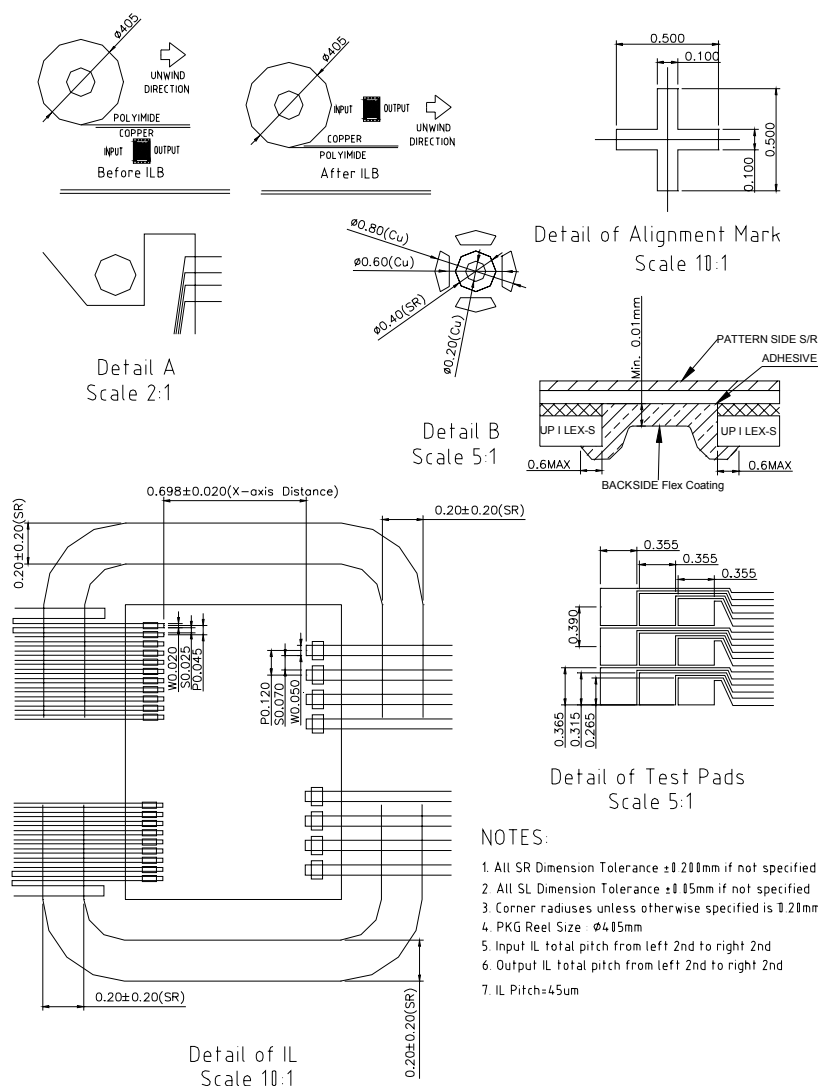
- “CLS” pad connects to “VDD1” pad, Internal oscillator circuit is enabled.
 - “VREF” pad connects to “VPP” pad.
 - “VCL” & “VSL” pad connects to “VSS” pad.
 - “C86” & “P/S” pad options can be selected by user. So SH1101A-TCP09 (TCP Form) supports 8-bit 6800-series parallel interface, 8-bit 8080-series parallel interface or serial peripheral interface.
- SH1101A-TCP09 (TCP Form) supports internal DC-DC converter function.



SH1101A

External View of SH1101A-TCP09 TCP Pins





Cautions Concerning Storage:

1. When storing the product, it is recommended that it be left in its shipping package.
After the seal of the packing bag has been broken, store the products in a nitrogen atmosphere.
2. Storage conditions:

Storage State	Storage Conditions
unopened (less than 90 days)	Temperature: 5 to 30 ; humidity: 80%RH or less.
After seal of broken (less than 30 days)	Room temperature, dry nitrogen atmosphere

3. Don't store in a location exposed to corrosive gas or excessive dust.
4. Don't store in a location exposed to direct sunlight or subject to sharp changes in temperature.
5. Don't store the product such that it subjected to an excessive load weight, such as by stacking.
6. Deterioration of the plating may occur after long-term storage, so special care is required.
It is recommended that the products be inspected before use.



SH1101A

Ordering Information

Part No.	Package
SH1101A-COG01	Gold bump on chip tray
SH1101A-TCP03	TCP Form
SH1101A-TCP06	TCP Form
SH1101A-TCP09	TCP Form

**Data Sheet Revision History**

Version	Content	Date
2.2	1. Change operating voltage from 1.8~3.5V to 1.65~3.5V in low voltage mode	Nov. 2006
2.1	2. Add low voltage mode 3. Add DC/AC Characteristics in low voltage mode	Aug. 2006
2.0	1. Add TCP09 Form information 2. DC Characteristics change V_{BREF} condition	Apr. 2006
1.0	Original	Nov. 2005