# *Crystalfontz America, Inc.*

**CUSTOMER :** ______________________

**MODULE NO.:** **CFAP1602A-Y-JCS**

| SALES BY | APPROVED BY | CHECKED BY | PREPARED BY |
|---|---|---|---|
| | | | |
| **ISSUED DATE:** | | | |


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# Contents

# 1.Module Classification Information

CFA P 1 6 0 2 A - Y - JCS

① ② ③ ④ ⑤ ⑥

| | | | |
|---|---|---|---|
| ① | Brand：**CRYSTALFONTZ AMERICA, INCORPORATED** | | |
| ② | Display Type：H→ Character Type, G→ Graphic Type , **P➡ PLED** | | |
| ③ | Display's Logical Dimensions：**16** columns by **2** lines.. | | |
| ④ | Model serials no. | | |
| ⑤ | Backlight Type： | **Y➡ Yellow Green** | |
| ⑥ | Special Code | **JCS: English and Japanese standard font** | |

# 2.Precautions in use of PLED Modules

(1)Avoid applying excessive shocks to the module or making any alterations or modifications to it.

(2)Don't make extra holes on the printed circuit board, modify its shape or change the components of PLED module.

(3)Don't disassemble the PLEDM.

(4)Don't operate it above the absolute maximum rating.

(5)Don't drop, bend or twist PLEDM.

(6)Soldering: only to the I/O terminals.

(7)Storage: please storage in anti-static electricity container and clean environment.

# 3.General Specification

| Item | Dimension | Unit |
|---|---|---|
| Number of Characters | 16 characters x 2 Lines | - |
| Module dimension | 84.0 x 44.0 x 9.5(MAX) | mm |
| View area | 66.0 x 16.0 | mm |
| Active area | 50.67 x 10.36 | mm |
| Dot size | 0.51 x 0.60 | mm |
| Dot pitch | 0.54 x 0.63 | mm |
| Character size | 2.67 x 5.01 | mm |
| Character pitch | 3.20 x 5.35 | mm |
| LCD type | PLED , Green | |
| Duty | 1/16 | |

# 4.Absolute Maximum Ratings

| Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Operating Temperature | $T_{OP}$ | -20 | 25 | +50 | ℃ |
| Storage Temperature | $T_{ST}$ | -30 | - | +70 | ℃ |
| Input Voltage | $V_I$ | -0.3 | - | $V_{DD}$ | V |
| Supply Voltage For Logic | $V_{DD}-V_{SS}$ | -0.3 | - | 7 | V |
| Supply Voltage For LCD | $V_{BT-}$ $V_{SS}$ | -0.3 | - | 5.0 | V |

# 5. Electrical Characteristics

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage For Logic | $V_{DD}$-$V_{SS}$ | - | 4.5 | 5.0 | 5.5 | V |
| Supply Voltage For LCD | $V_{BT}$ | Ta=25℃ | 2.0 | 2.5 | 5.0 | V |
| Input High Volt. | $V_{IH}$ | - | 0.7 $V_{DD}$ | - | $V_{DD}$ | V |
| Input Low Volt. | $V_{IL}$ | - | -0.3 | - | 0.55 | V |
| Output High Volt. | $V_{OH}$ | - | 2.4 | - | - | V |
| Output Low Volt. | $V_{OL}$ | - | - | - | 0.4 | V |
| Supply Current | $I_{DD}$ | $V_{DD}$=5V | - | 0.35 | 0.6 | mA |

# 6. Optical Characteristics

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| View Angle | (V)θ | | | 80 | | deg |
| | (H)φ | | | 80 | | deg |
| Contrast Ratio | CR | 100 lux | - | 100 | - | - |
| Response Time | T rise | - | | 10 | | us |
| | T fall | - | | 10 | | us |
| Brightness | | With polarizer | | 40 | | nits |

# 7.Interface Pin Function

| Pin No. | Symbol | Level | Description |
|---|---|---|---|
| 1 | $V_{SS}$ | 0V | Ground |
| 2 | $V_{DD}$ | 5.0V | Supply Voltage for logic |
| 3 | □$V_{BT}$ | (Variable) | Operating voltage for PLED Brightness adjhstment |
| 4 | RS | H/L | H: DATA, L: Instruction code |
| 5 | R/W | H/L | H: Read(MPU→Module) L: Write(MPU→Module) |
| 6 | E | H,H→L | Chip enable signal |
| 7 | DB0 | H/L | Data bit 0 |
| 8 | DB1 | H/L | Data bit 1 |
| 9 | DB2 | H/L | Data bit 2 |
| 10 | DB3 | H/L | Data bit 3 |
| 11 | DB4 | H/L | Data bit 4 |
| 12 | DB5 | H/L | Data bit 5 |
| 13 | DB6 | H/L | Data bit 6 |
| 14 | DB7 | H/L | Data bit 7 |
| 15 | NC | - | |
| 16 | NC | - | |

# Brightness Control

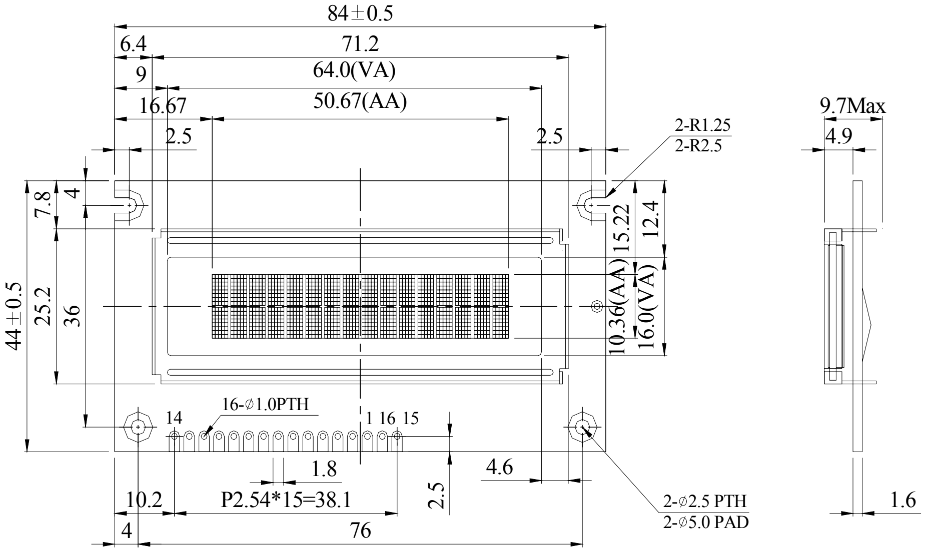
| VBT | Brightness(nits) | Power consumption(measured with random texts) |
|---|---|---|
| 2.5V | 20(typical) | 50mW |
| 3.0V | 45(typical) | 63mW |

Note:1.When random texts pattern is running averagely,at any instance, about 1/4 of pixels will be on.

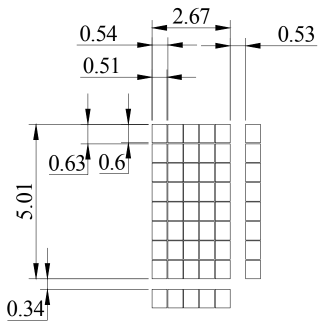
2.If VBT is not operated within 2V and 3V,non-uniformity display may occur.

**3.You have to use the saving mode by VBT 2.5V in order to make long life.**

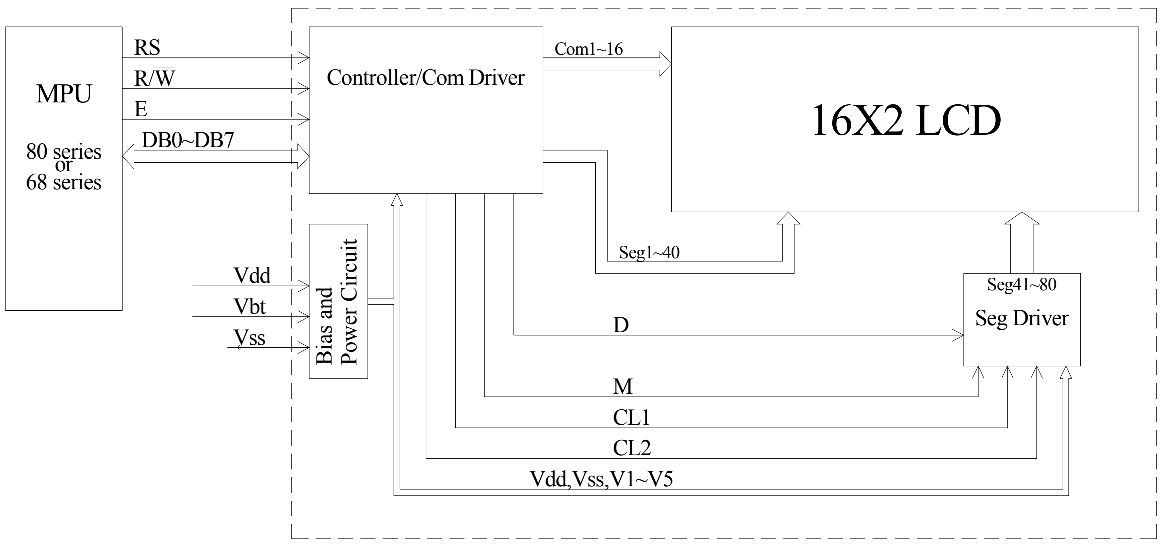
# 8.Counter Drawing &Block Diagram




| PIN NO. | SYMBOL |
|---|---|
| 1 | Vss |
| 2 | Vdd |
| 3 | Vo |
| 4 | RS |
| 5 | R/$\overline{W}$ |
| 6 | E |
| 7 | DB0 |
| 8 | DB1 |
| 9 | DB2 |
| 10 | DB3 |
| 11 | DB4 |
| 12 | DB5 |
| 13 | DB6 |
| 14 | DB7 |
| 15 | NC |
| 16 | NC |




DOT SIZES




| | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Character located | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
| DDRAM address | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F |
| DDRAM address | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | 4C | 4D | 4E | 4F |

# 9.Function Description

The LCD display Module is built in a LSI controller, the controller has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DDRAM) and character generator (CGRAM). The IR can only be written from the MPU. The DR temporarily stores data to be written or read from DDRAM or CGRAM. When address information is written into the IR, then data is stored into the DR from DDRAM or CGRAM. By the register selector (RS) signal, these two registers can be selected.

| RS | R/W | Operation |
|---|---|---|
| 0 | 0 | IR write as an internal operation (display clear, etc.) |
| 0 | 1 | Read busy flag (DB7) and address counter (DB0 to DB7) |
| 1 | 0 | Write data to DDRAM or CGRAM (DR to DDRAM or CGRAM) |
| 1 | 1 | Read data from DDRAM or CGRAM (DDRAM or CGRAM to DR) |

**Busy Flag (BF)**

When the busy flag is 1, the controller LSI is in the internal operation mode, and the next instruction will not be accepted. When RS=0 and R/W=1, the busy flag is output to DB7. The next instruction must be written after ensuring that the busy flag is 0.

**Address Counter (AC)**

The address counter (AC) assigns addresses to both DDRAM and CGRAM

**Display Data RAM (DDRAM)**

This DDRAM is used to store the display data represented in 8-bit character codes. Its extended capacity is 80×8 bits or 80 characters. Below figure is the relationships between DDRAM addresses and positions on the liquid crystal display.

| | High bits | | | Low bits | | | |
|---|---|---|---|---|---|---|---|
| AC (hexadecimal) | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Example: DDRAM addresses 4E

| | | | | | | |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 1 | 1 | 0 |

Display position DDRAM address

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F |
| 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | 4C | 4D | 4E | 4F |

2-Line by 16-Character Display

**Character Generator ROM (CGROM)**

The CGROM generate 5×8 dot or 5×10 dot character patterns from 8-bit character codes. See Table 2.

**Character Generator RAM (CGRAM)**

In CGRAM, the user can rewrite character by program. For 5×8 dots, eight character patterns can be written, and for 5×10 dots, four character patterns can be written.
Write into DDRAM the character code at the addresses shown as the left column of table 1. To show the character patterns stored in CGRAM.

**Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character patterns**

**Table 1.**

For 5 * 8 dot character patterns

| Character Codes (DDRAM data) 7 6 5 4 3 2 1 0 (High … Low) | CGRAM Address 5 4 3 (High) | CGRAM Address 2 1 0 (Low) | Character Patterns (CGRAM data) 7 6 5 (High) | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| | | 0 0 0 | * * * | ■ | ■ | ■ | ■ | 0 | Character pattern( 1 ) |
| | | 0 0 1 | * * * | ■ | 0 | 0 | 0 | ■ | |
| | | 0 1 0 | * * * | ■ | 0 | 0 | 0 | ■ | |
| | | 0 1 1 | * * * | ■ | ■ | ■ | ■ | 0 | |
| 0 0 0 0 * 0 0 0 | 0 0 0 | 1 0 0 | * * * | ■ | 0 | ■ | 0 | 0 | |
| | | 1 0 1 | * * * | ■ | 0 | 0 | ■ | 0 | |
| | | 1 1 0 | * * * | ■ | 0 | 0 | 0 | ■ | |
| | | 1 1 1 | * * * | 0 | 0 | 0 | 0 | 0 | Cursor pattern |
| | | 0 0 0 | * * * | ■ | 0 | 0 | 0 | ■ | Character pattern( 2 ) |
| | | 0 0 1 | * * * | 0 | ■ | 0 | ■ | 0 | |
| | | 0 1 0 | * * * | ■ | ■ | ■ | ■ | ■ | |
| | | 0 1 1 | * * * | 0 | 0 | ■ | 0 | 0 | |
| 0 0 0 0 * 0 0 1 | 0 0 1 | 1 0 0 | * * * | ■ | ■ | ■ | ■ | ■ | |
| | | 1 0 1 | * * * | 0 | 0 | ■ | 0 | 0 | |
| | | 1 1 0 | * * * | 0 | 0 | ■ | 0 | 0 | |
| | | 1 1 1 | * * * | 0 | 0 | 0 | 0 | 0 | Cursor pattern |
| | | 0 0 0 | * * * | | | | | | |
| | | 0 0 1 | | | | | | | |
| 0 0 0 0 * 1 1 1 | 1 1 1 | 1 0 0 | | | | | | | |
| | | 1 0 1 | | | | | | | |
| | | 1 1 0 | | | | | | | |
| | | 1 1 1 | * * * | | | | | | |

For 5 * 10 dot character patterns

| Character Codes (DDRAM data) 7 6 5 4 3 2 1 0 (High … Low) | CGRAM Address 5 4 (High) | CGRAM Address 3 2 1 0 (Low) | Character Patterns (CGRAM data) 7 6 5 (High) | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| | | 0 0 0 0 | * * * | 0 | 0 | 0 | 0 | 0 | |
| | | 0 0 0 1 | * * * | 0 | 0 | 0 | 0 | 0 | |
| | | 0 0 1 0 | * * * | ■ | 0 | ■ | ■ | 0 | |
| | | 0 0 1 1 | * * * | ■ | ■ | 0 | 0 | ■ | |
| | | 0 1 0 0 | * * * | ■ | 0 | 0 | 0 | ■ | |
| 0 0 0 0 * 0 0 0 | 0 0 | 0 1 0 1 | * * * | ■ | 0 | 0 | 0 | ■ | |
| | | 0 1 1 0 | * * * | ■ | ■ | ■ | ■ | 0 | Character pattern |
| | | 0 1 1 1 | * * * | ■ | 0 | 0 | 0 | 0 | |
| | | 1 0 0 0 | * * * | ■ | 0 | 0 | 0 | 0 | |
| | | 1 0 0 1 | * * * | ■ | 0 | 0 | 0 | 0 | |
| | | 1 0 1 0 | * * * | 0 | 0 | 0 | 0 | 0 | Cursor pattern |
| | | | | | | | | | |
| | | 1 1 1 1 | * * * | * | * | * | * | * | |

■ : " High "

# 10.Character Generator ROM Pattern

**Table.2**

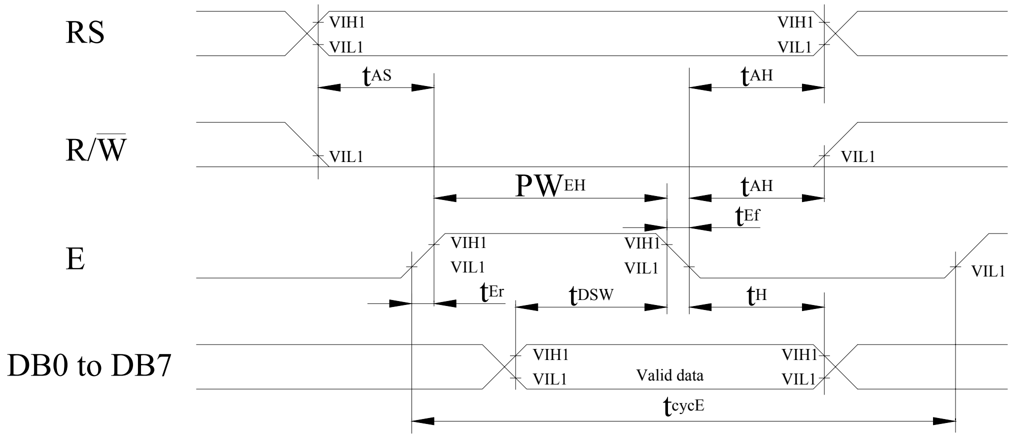
| Upper 4 bit / Lower 4 bit | LLLL | LLLH | LLHL | LLHH | LHLL | LHLH | LHHL | LHHH | HLLL | HLLH | HLHL | HLHH | HHLL | HHLH | HHHL | HHHH |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LLLL | CG RAM (1) | | | 0 | @ | P | ` | p | | | | ー | タ | ミ | α | p |
| LLLH | (2) | | ! | 1 | A | Q | a | q | | | 。 | ア | チ | ム | ä | q |
| LLHL | (3) | | " | 2 | B | R | b | r | | | 「 | イ | ツ | メ | β | θ |
| LLHH | (4) | | # | 3 | C | S | c | s | | | 」 | ウ | テ | モ | ε | ∞ |
| LHLL | (5) | | $ | 4 | D | T | d | t | | | 、 | エ | ト | ヤ | μ | Ω |
| LHLH | (6) | | % | 5 | E | U | e | u | | | ・ | オ | ナ | ユ | σ | ü |
| LHHL | (7) | | & | 6 | F | V | f | v | | | ヲ | カ | ニ | ヨ | ρ | Σ |
| LHHH | (8) | | ' | 7 | G | W | g | w | | | ァ | キ | ヌ | ラ | g | π |
| HLLL | (1) | | ( | 8 | H | X | h | x | | | ィ | ク | ネ | リ | √ | x̄ |
| HLLH | (2) | | ) | 9 | I | Y | i | y | | | ゥ | ケ | ノ | ル | $^{-1}$ | y |
| HLHL | (3) | | * | : | J | Z | j | z | | | ェ | コ | ハ | レ | j | 千 |
| HLHH | (4) | | + | ; | K | [ | k | { | | | ォ | サ | ヒ | ロ | ˣ | 万 |
| HHLL | (5) | | , | < | L | ¥ | l | \| | | | ャ | シ | フ | ワ | ¢ | 円 |
| HHLH | (6) | | - | = | M | ] | m | } | | | ュ | ス | ヘ | ン | £ | ÷ |
| HHHL | (7) | | . | > | N | ^ | n | → | | | ョ | セ | ホ | ゛ | ñ | |
| HHHH | (8) | | / | ? | O | _ | o | ← | | | ッ | ソ | マ | ゜ | ö | █ |

# 11.Instruction Table

| Instruction | Instruction Code | | | | | | | | | | Description | Execution time (fosc=270Khz) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | |
| Clear Display | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Write “00H” to DDRAM and set DDRAM address to “00H” from AC | 1.52ms |
| Return Home | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | - | Set DDRAM address to “00H” from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed. | 1.52ms |
| Entry Mode Set | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | SH | Assign cursor moving direction and enable the shift of entire display.<br>I/D=1:Increment；0: Decrement<br>SH=1:Display shift on | 37μ s |
| Display ON/OFF Control | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | Set display (D), cursor (C), and blinking of cursor (B) on/off control bit.<br>D=1:Display on<br>C=1:Cursor display on<br>B=1:Cursor blink on | 37μ s |
| Cursor or Display Shift | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | - | - | Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.<br>S/C=1:Shift display；0:Move cursor<br>R/L=1:Shift right；0:Shift leftf | 37μ s |
| Function Set | 0 | 0 | 0 | 0 | 1 | DL | N | F | - | - | Set interface data length (DL)<br>DL=1:8-bit；0:4-bit<br>Set numbers of display lines(N)<br>N=1:Dual line；0:Single line<br>Set display font type (F)<br>F=1:5x10 dots；0:5x8dots | 37μ s |
| Set CGRAM Address | 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set CGRAM address in address counter. | 37μ s |
| Set DDRAM Address | 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set DDRAM address in address counter. | 37μ s |
| Read Busy Flag and Address | 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.<br>BF=1:Internal operation<br>BF=0:Ready for instruction | 0μ s |
| Write Data to RAM | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Write data into internal RAM (DDRAM/CGRAM). | 37μ s |
| Read Data from RAM | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Read data from internal RAM (DDRAM/CGRAM). | 37μ s |

* ” - ”：don’t care

# 12.Timing Characteristics

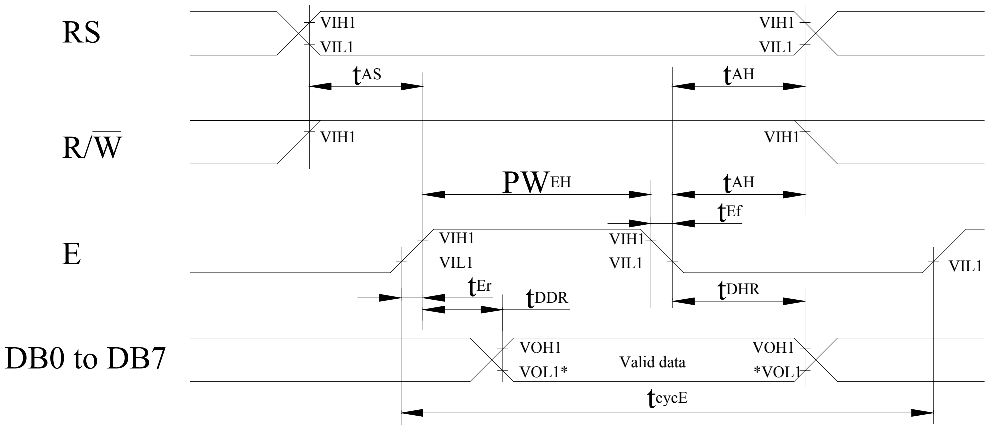



## 12.1 Write Operation

Ta=25℃, VDD=5.0± 0.5V

| Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Enable cycle time | $t_{cycE}$ | 500 | - | - | ns |
| Enable pulse width (high level) | $PW_{EH}$ | 230 | - | - | ns |
| Enable rise/fall time | $t_{Er}$,$t_{Ef}$ | - | - | 20 | ns |
| Address set-up time (RS, R/W to E) | $t_{AS}$ | 40 | - | - | ns |
| Address hold time | $t_{AH}$ | 10 | - | - | ns |
| Data set-up time | $t_{DSW}$ | 80 | - | - | ns |
| Data hold time | $t_H$ | 10 | - | - | ns |

## 12.2 Read Operation




NOTE: *VOL1 is assumed to be 0.8V at 2 MHZ operation.

Ta=25℃, VDD=5.0± 0.5V

| Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Enable cycle time | $t_{cycE}$ | 500 | - | - | ns |
| Enable pulse width (high level) | $PW_{EH}$ | 230 | - | - | ns |
| Enable rise/fall time | $t_{Er}$,$t_{Ef}$ | - | - | 20 | ns |
| Address set-up time (RS, R/W to E) | $t_{AS}$ | 40 | - | - | ns |
| Address hold time | $t_{AH}$ | 10 | - | - | ns |
| Data delay time | $t_{DDR}$ | - | - | 160 | ns |
| Data hold time | $t_{DHR}$ | 5 | - | - | ns |

# 13.Initializing of LCM

Power on

Wait for more than 15 ms after $V_{CC}$ rises to 4.5 V

BF can not be checked before this instruction.

| RS | $R/\overline{W}$ | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 | * | * | * | * |

Function set ( Interface is 8 bits long. )

Wait for more than 4.1 ms

BF can not be checked before this instruction.

| RS | $R/\overline{W}$ | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 | * | * | * | * |

Function set ( Interface is 8 bits long. )

Wait for more than 100 μs

BF can not be checked before this instruction.

| RS | $R/\overline{W}$ | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 | * | * | * | * |

Function set ( Interface is 8 bits long. )

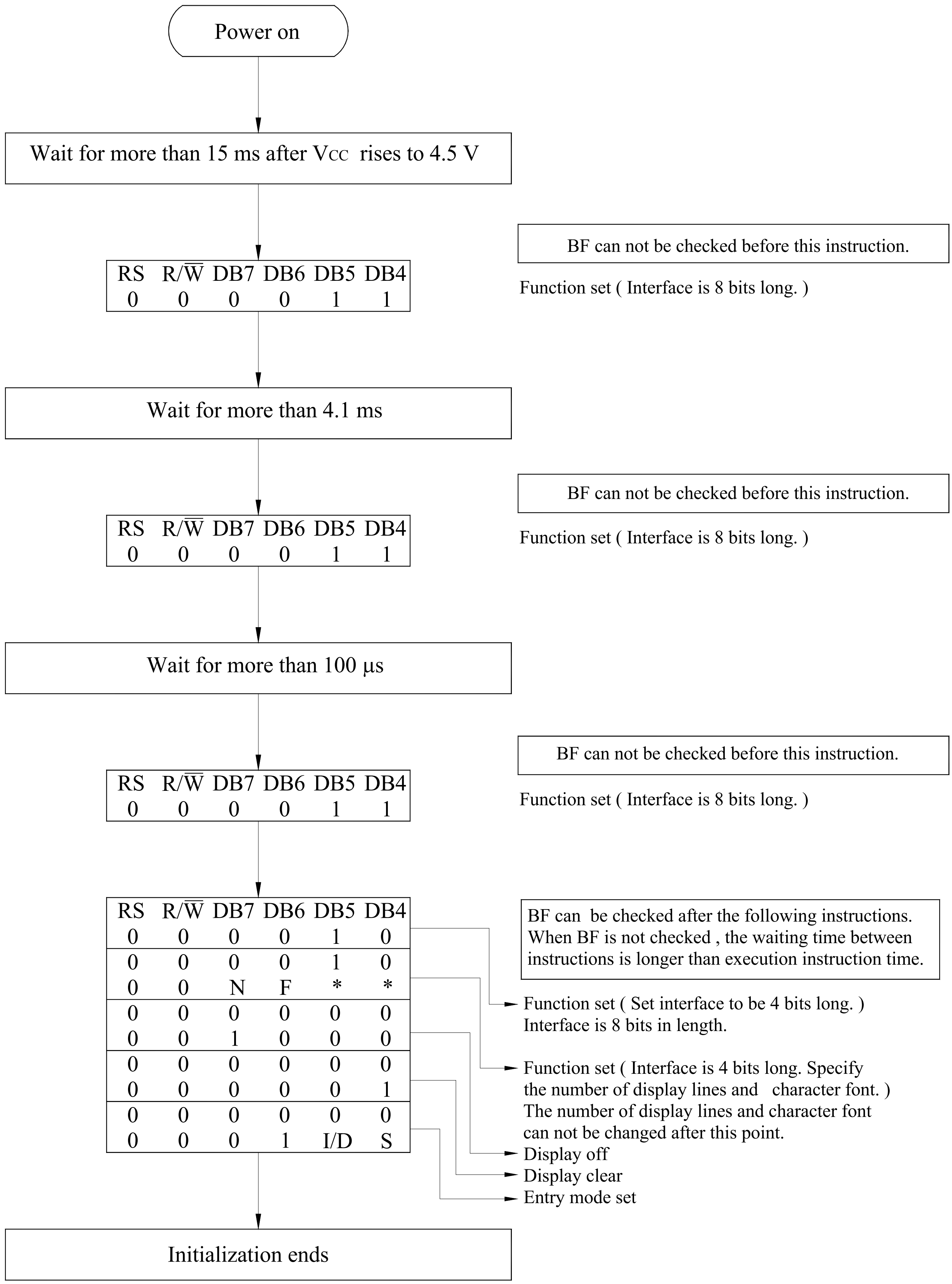
BF can be checked after the following instructions. When BF is not checked , the waiting time between instructions is longer than execution instruction time.

| RS | $R/\overline{W}$ | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 | N | F | * | * |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S |

Function set ( Interface is 8 bits long. Specify the number of display lines and font. )
The number of display lines and character font can not be changed after this point.
Display off
Display clear
Entry mode set

Initialization ends

8-Bit Ineterface




4-Bit Ineterface

# 14.Quality Assurance

**Screen Cosmetic Criteria**

| Item | Defect | Judgment Criterion | Partition |
|---|---|---|---|
| 1 | Spots | A)Clear<br>Size: d mm — Acceptable Qty in active area<br>d ≦ 0.1 — Disregard<br>0.1<d≦ 0.2 — 6<br>0.2<d≦ 0.3 — 2<br>0.3<d — 0<br>Note: Including pin holes and defective dots which must be within one pixel size.<br>B)Unclear<br>Size: d mm — Acceptable Qty in active area<br>d ≦ 0.2 — Disregard<br>0.2<d≦ 0.5 — 6<br>0.5<d≦ 0.7 — 2<br>0.7<d — 0 | Minor |
| 2 | Bubbles in Polarize | Size: d mm — Acceptable Qty in active area<br>d≦ 0.3 — Disregard<br>0.3<d≦ 1.0 — 3<br>1.0<d≦ 1.5 — 1<br>1.5<d — 0 | Minor |
| 3 | Scratch | In accordance with spots cosmetic criteria. When the light reflects on the panel surface, the scratches are not to be remarkable. | Minor |
| 4 | Allowable Density | Above defects should be separated more than 30mm each other. | Minor |
| 5 | Coloration | Not to be noticeable coloration in the viewing area of the LCD panels.<br>Back-light type should be judged with back-light on state only. | Minor |

# 15.PLED Lifetime

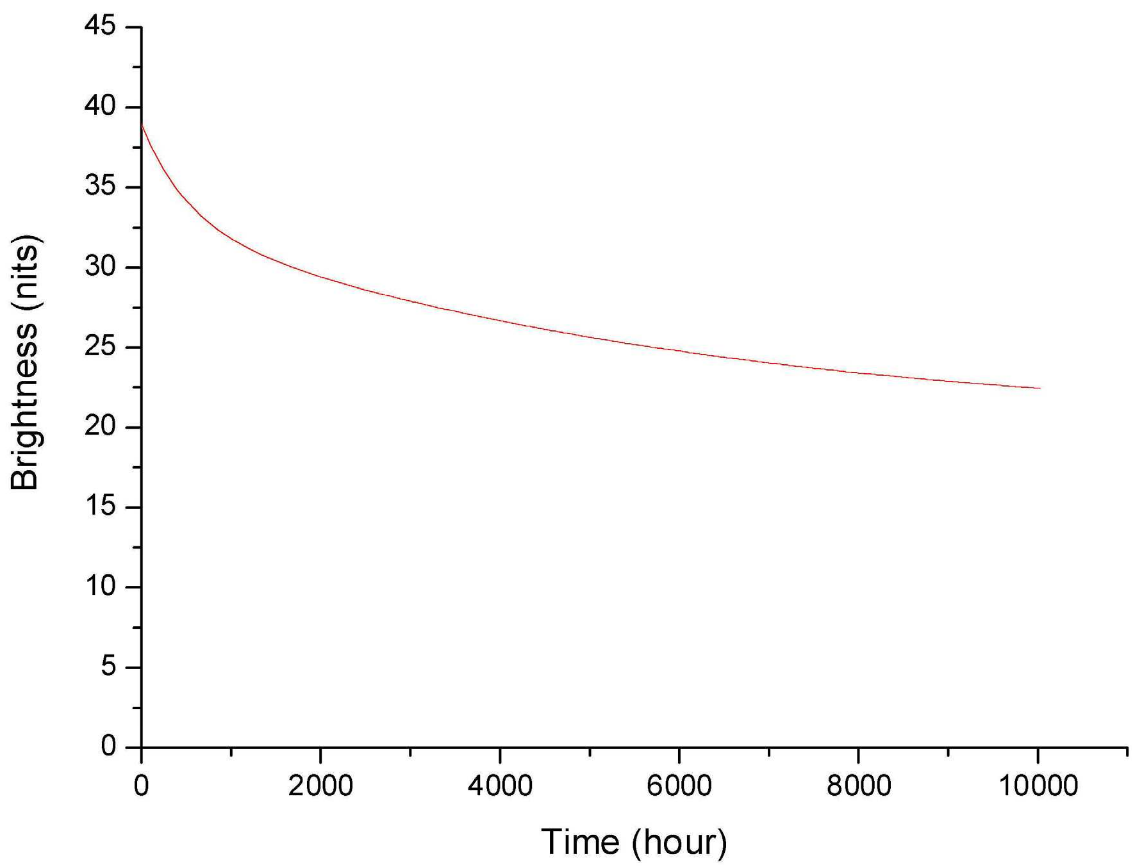
Conditions：

Temperature：25℃

Brightness decay to 50％ of original value

Panel lifetime is a function of the brightness as follows：

| **Average Brightness (nits)** | **Lifetime (Hours)** |
|---|---|
| 40 | 10,000 |
| 20 | 15,000 |
| 10 | 20,000 |



# 16.Reliability

**Content of Reliability Test**

| **Environmental Test** | | | |
|---|---|---|---|
| **Test Item** | **Content of Test** | **Test Condition** | **Applicable Standard** |
| High Temperature storage | Endurance test applying the high storage temperature for a long time. | 70℃<br>200hrs | —— |
| Low Temperature storage | Endurance test applying the high storage temperature for a long time. | -30℃<br>200hrs | —— |
| High Temperature Operation | Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time. | 50℃<br>200hrs | —— |
| Low Temperature Operation | Endurance test applying the electric stress under low temperature for a long time. | -20℃<br>200hrs | —— |
| High Temperature/ Humidity Storage | Endurance test applying the high temperature and high humidity storage for a long time. | 70℃,90%RH<br>96hrs | —— |
| High Temperature/ Humidity Operation | Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time. | 50℃,90%RH<br>96hrs | —— |
| Temperature Cycle | Endurance test applying the low and high temperature cycle.<br>-20℃ 25℃ 50℃<br>30min 5min 30min<br>1 cycle | -20℃/50℃<br>10 cycles | —— |
| Mechanical Test | | | |
| Vibration test | Endurance test applying the vibration during transportation and using. | 10~22Hz→ 1.5mmp-p<br>22~500Hz→ 1.5G<br>Total 0.5hrs | —— |
| Shock test | Constructional and mechanical endurance test applying the shock during transportation. | 50G Half sign wave 11 msedc<br>3 times of each direction | —— |
| Atmospheric pressure test | Endurance test applying the atmospheric pressure during transportation by air. | 115mbar<br>40hrs | —— |
| Others | | | |
| Static electricity test | Endurance test applying the electric stress to the terminal. | VS=800V,RS=1.5kΩ<br>CS=100pF<br>1 time | —— |

***Supply voltage for logic system=5V. Supply voltage for LCD system =Operating voltage at 25℃