Crystalfontz America, Inc.

CUSTOMER : _____

MODULE NO.: **CFAG12232D-NYG-VA** **(preliminary)**

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY
ISSUED DATE:			

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Contents

1.Module Classification Information

CFA G 1 2 2 3 2 D N Y G VA
① ② ③ ④ ⑤ ⑥ ⑦ ⑧

①	Brand：CRYSTALFONTZ AMERICA, INCORPORATED		
②	Display Type：H→Character Type, **G→Graphic Type**		
③	Display's logical dimensions: **122** pixels by **32** pixels		
④	PCB Variant: **D**		
⑤	Backlight Type	**N→Without backlight** B→EL, Blue green D→EL, Green W→EL, White F→CCFL, White Y→LED, Yellow Green	 A→LED, Amber R→LED, Red O→LED, Orange G→LED, Green
⑥	LCD Mode	B→TN Positive, Gray T→FSTN Negative N→TN Negative, G→STN Positive, Gray **Y→STN Positive, Yellow Green** M→STN Negative, Blue F→FSTN Positive	
⑦	LCD Polarize Type/ Temperature range/ View direction	A→Reflective, N.T, 6:00 D→Reflective, N.T, 12:00 **G→Reflective, W. T, 6:00** J→Reflective, W. T, 12:00 B→Transflective, N.T,6:00 E→Transflective, N.T.12:00	H→Transflective, W.T,6:00 K→Transflective, W.T,12:00 C→Transmissive, N.T,6:00 F→Transmissive, N.T,12:00 I→Transmissive, W. T, 6:00 L→Transmissive, W.T,12:00
⑧	Special Code	**V→negative voltage generator on board; A→Avant IC**	

2.Precautions in use of LCD Modules

(1)Avoid applying excessive shocks to the module or making any alterations or modifications to it.

(2)Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD module.

(3)Don't disassemble the LCM.

(4)Don't operate it above the absolute maximum rating.

(5)Don't drop, bend or twist LCM.

(6)Soldering: only to the I/O terminals.

(7)Storage: please storage in anti-static electricity container and clean environment.

3.General Specification

Item	Dimension	Unit
Number of Characters	122 x 32	
Module dimension	59.0 x 29.3 x 5.5(MAX)	mm
View area	52.0 x 15.0	mm
Active area	45.72 x 11.97	mm
Dot size	0.345 x 0.345	mm
Dot pitch	0.375 x 0.375	mm
LCD type	STN, Positive, Transflective , Yellow Green	
Duty	1/32	
View direction	6 o'clock	
Backlight Type	None	

4.Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T_{OP}	-20		+70	°C
Storage Temperature	T_{ST}	-30		+80	°C
Input Voltage	V_I	0		V_{DD}	V
Supply Voltage For Logic	V_{DD}	0		6.7	V
Supply Voltage For LCD	V_{DD}-V_{LCD}	0		-10	V
Supply Voltage For LCD	VEE	0		-10	V

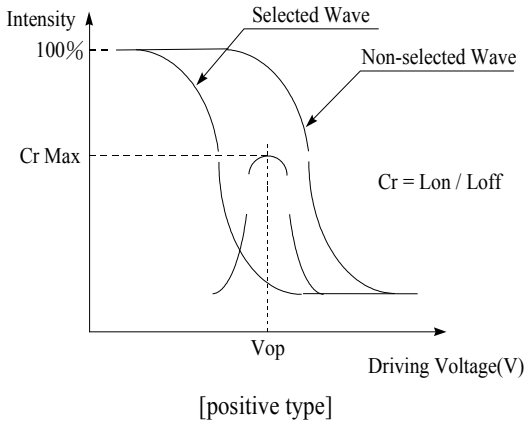
5.Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	V_{DD}-V_{SS}		4.75	5.0	5.25	V
Supply Voltage For LCD	V_{DD}-V_O	Ta=-20°C Ta=25°C Ta=+70°C	 3.9	 4.7	5.8	V V V
Input High Volt.	V_{IH}		2.0		V_{DD}	V
Input Low Volt.	V_{IL}		0		0.8	V
Output High Volt.	V_{OH}		2.7		V_{DD}	V
Output Low Volt.	V_{OL}		0		0.4	V
Supply Current	I_{DD}		0.6	0.8	1.2	mA

6.Optical Characteristics

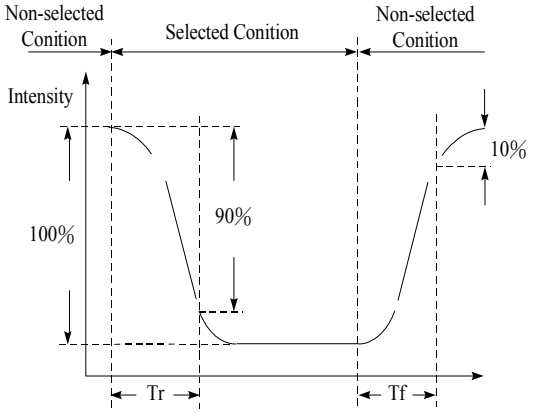
Item	Symbol	Condition	Min	Typ	Max	Unit
View Angle	(V)θ	CR≥2	20	-	40	deg
	(H)φ	CR≥2	-30	-	30	deg
Contrast Ratio	CR	-		3	-	-
Response Time	T rise	-	-	100	150	ms
	T fall	-	-	100	150	ms

Definition of Operation Voltage (Vop)



[positive type]

Definition of Response Time (Tr , Tf)



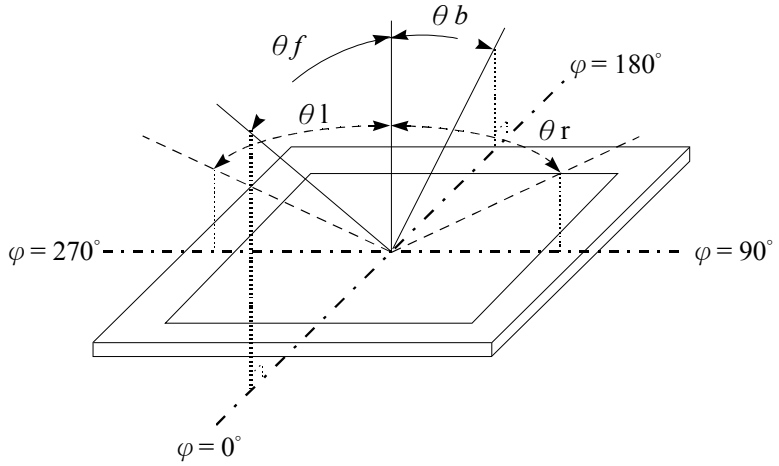
[positive type]

Conditions :

Operating Voltage : Vop　　Viewing Angle(θ，φ) : 0°， 0°

Frame Frequency : 64 HZ　　Driving Waveform : 1/N duty , 1/a bias

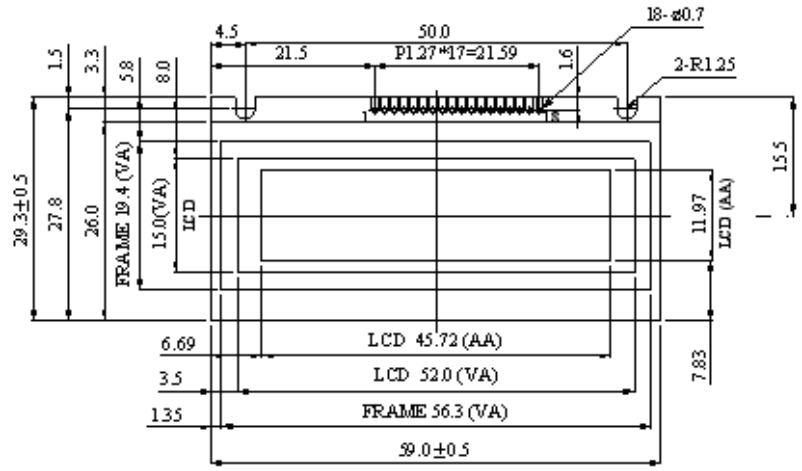
Definition of viewing angle(CR≥2)

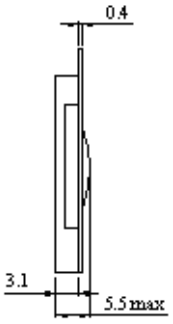


7.Interface Description

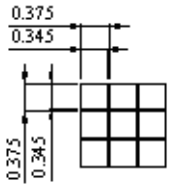
Pin No.	Symbol	Level	Description
1	/VLED	0V	NC
2	V_{ss}	0V	Ground
3	V_{dd}	5V	Power supply for logic
4	Vo	(Variable)	Operating voltage for LCD
5	A0	H/L	H : Data L : Instruction
6	E1	H/L	Chip select signal for IC1 (left 61*32 dots) active “H”
7	E2	H/L	Chip select signal for IC2 (right 61*32 dots) active “H”
8	DB0	H/L	Data bus line
9	DB1	H/L	Data bus line
10	DB2	H/L	Data bus line
11	DB3	H/L	Data bus line
12	DB4	H/L	Data bus line
13	DB5	H/L	Data bus line
14	DB6	H/L	Data bus line
15	DB7	H/L	Data bus line
16	R/W	H/L	H : Read ; L : Write
17	VEE		Negative Voltage output
18	NC		NC

8.Contour Drawing & Block Diagram



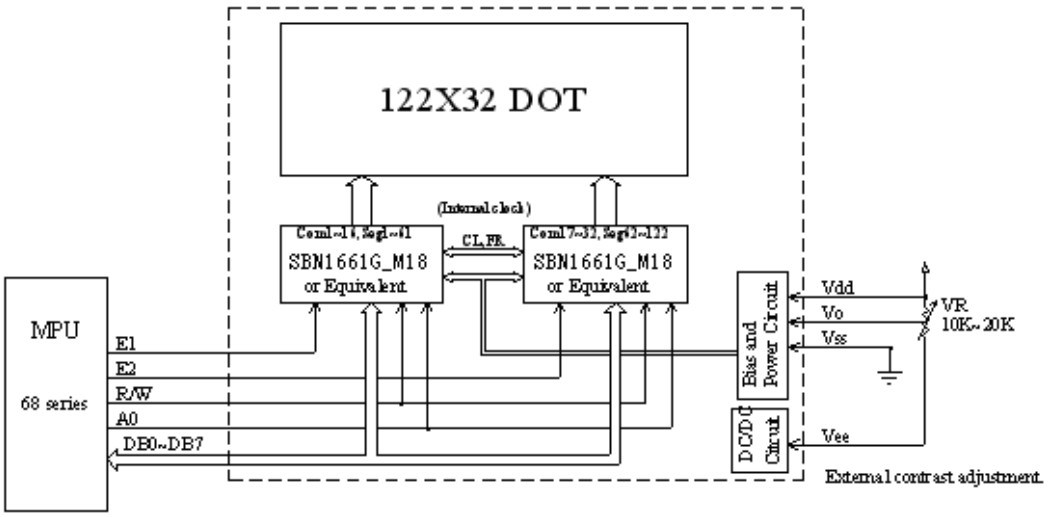


PIN NO.	SYMBOL
1	NC
2	VSS
3	VDD
4	VO
5	AO
6	E1
7	E2
8	DB0
9	DB1
10	DB2
11	DB3
12	DB4
13	DB5
14	DB6
15	DB7
16	R/W
17	VEE
18	NC



DOT SIZE
SCALE 15/1

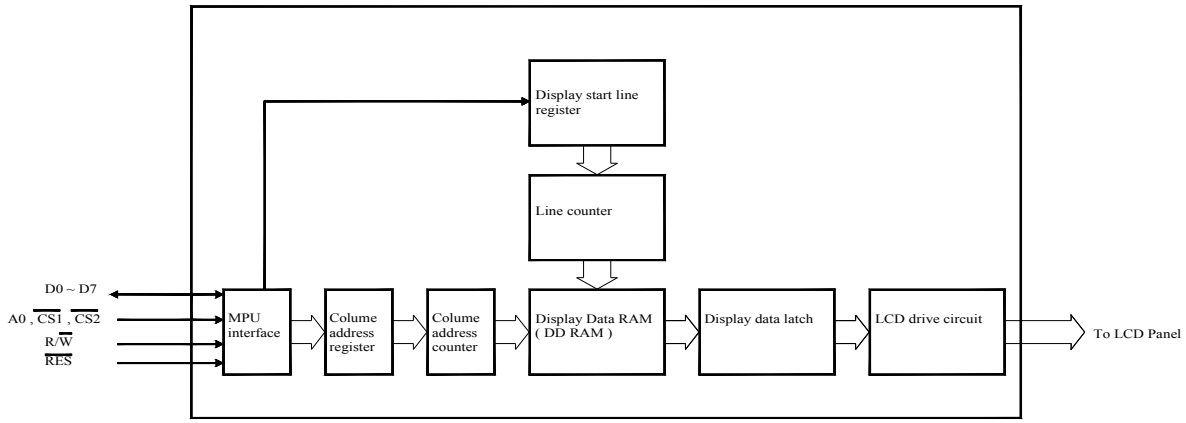
The non-specified tolerance of dimension is ? .3 mm .



9.Function Description

Block Diagram

This 122×32 dots LCD Module built in two SBN1661G_M18-D LSI controller.



MPU interface

The SBN1661G_M18-D controller transfers data via 8-bit bidirecional data buses (Do to D7), it can fit any MPU if it corresponds to SBN1661G_M18-D Read and Write Timing Characteristics.

Data transfer

The SBN1661G_M18-D driver uses the A0, E and R/W signals to transfer data between the system MPU and internal registers, The combinations used are given in the table below.

A0	R/W	Function
1	1	Read display data
1	0	Write display data
0	1	Read status
0	0	Write to internal register (command)

Busy flag

When the Busy flag is logical 1, the SBN1661G_M18-D series is executing its internal operations. Any command other than Status Read is rejected during this time. The Busy flag is output at pin D7 by the Status Read command. If an appropriate cycle time (t_{CYC}) is given, this flag needs not be checked at the beginning of each command and, therefore, the MPU processing capacity can greatly be enhanced.

Display Start Line and Line Count Registers

The contents of this register form a pointer to a line of data in display data RAM corresponding to the first line of the display (COM0), and are set by the Display Start Line command.

Column Address Counter

The column address counter is a 7-bit presentable counter that supplies the column address for MPU access to the display data RAM. See Figure 1. The counter is incremented by one every time the driver receives a Read or Write Display Data command. Addresses above 50H are invalid, and the counter will not increment past this value. The contents of the column address counter are set with the Set Column Address command.

Display Data RAM

The display data RAM stores the LCD display data, on a 1-bit per pixel basis. The relation-ship between display data, display address and the display is shown in Figure 1

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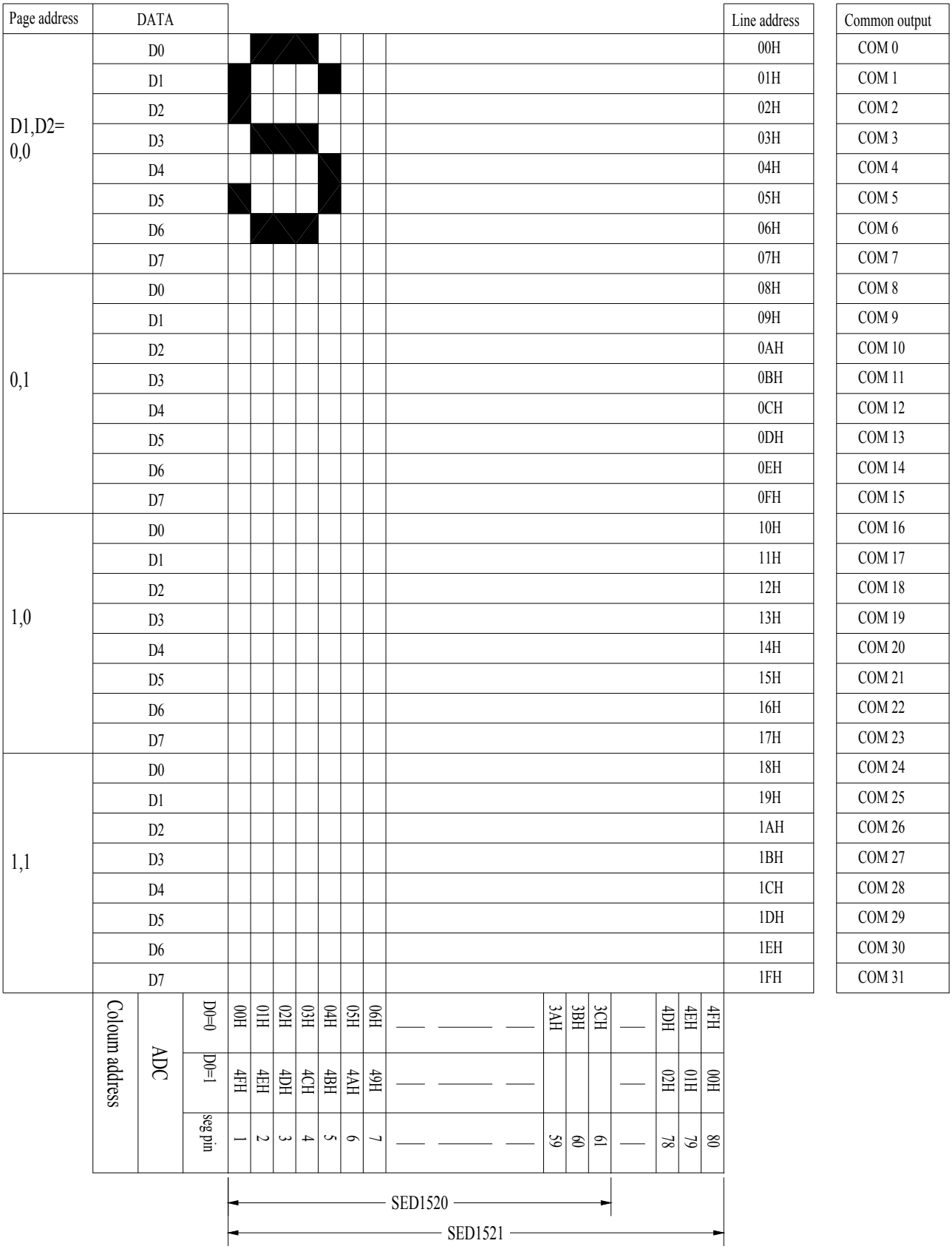
Page Register

The page register is a 2-bit register that supplies the page address for MPU access to the display data RAM. See Figure 1. The contents of the page register are set by the Set Page Register command.

Figure 1.

Display Data RAM Address



Page address	DATA	Line address	Common output
D1,D2= 0,0	D0	00H	COM 0
	D1	01H	COM 1
	D2	02H	COM 2
	D3	03H	COM 3
	D4	04H	COM 4
	D5	05H	COM 5
	D6	06H	COM 6
	D7	07H	COM 7
0,1	D0	08H	COM 8
	D1	09H	COM 9
	D2	0AH	COM 10
	D3	0BH	COM 11
	D4	0CH	COM 12
	D5	0DH	COM 13
	D6	0EH	COM 14
	D7	0FH	COM 15
1,0	D0	10H	COM 16
	D1	11H	COM 17
	D2	12H	COM 18
	D3	13H	COM 19
	D4	14H	COM 20
	D5	15H	COM 21
	D6	16H	COM 22
	D7	17H	COM 23
1,1	D0	18H	COM 24
	D1	19H	COM 25
	D2	1AH	COM 26
	D3	1BH	COM 27
	D4	1CH	COM 28
	D5	1DH	COM 29
	D6	1EH	COM 30
	D7	1FH	COM 31

Coloum address	ADC																								
		D0=0	00H	01H	02H	03H	04H	05H	06H				3AH	3BH	3CH			4DH	4EH	4FH					
		D0=1	4FH	4EH	4DH	4CH	4BH	4AH	49H									02H	01H	00H					
		seg pin	1	2	3	4	5	6	7				59	60	61			78	79	80					

SED1520

SED1521

The 122*32 dots display area is consisted 2 61*32,The inyerface pin CS1 enable the left 61*32 ,CS2 enable the right 61*32 dots.

10.Commands Descriptions

The host microcontroller can issue commands to the SBN1661G_X. Table 27 lists all the commands. When issuing a command, the host microcontroller should put the command code on the data bus. The host microcontroller should also give the control bus C/D, E(RD), and R/W(WR) proper value and timing.

Commands

COMMAND	COMMAND CODE								FUNCTION
	D7	D6	D5	D4	D3	D2	D1	D0	
Write Display Data	Data to be written into the Display Data Memory.								Write a byte of data to the Display Data Memory.
Read Display Data	Data read from the Display Data Memory.								Read a byte of data from the Display Data Memory.
Read-Modify-Write	1	1	1	0	0	0	0	0	Start Read-Modify-Write operation.
END	1	1	1	0	1	1	1	0	Stop Read-Modify-Write operation.
Software Reset	1	1	1	0	0	0	1	0	Software Reset.

Write Display Data

The Write Display Data command writes a byte (8 bits) of data to the Display Data Memory. Data is put on the data bus by the host microcontroller. The location which accepts this byte of data is pointed to by the Page Address Register and the Column Address Register. At the end of the command operation, the content of the Column Address Register is automatically incremented by 1.

The setting of the control bus for issuing Write Display Data command

$\overline{C}$/D	E/($\overline{RD}$)	R/$\overline{W}$($\overline{WR}$)
1	1	0

Read Display Data

The Read Display Data command starts a 3-step operation.

1. First, the current data of the internal 8-bit output latch of the Display Data Memory is read by the microcontroller, via the 8-bit data bus DB0~DB7.
2. Then, a byte of data of the Display Data Memory is transferred to the 8-bit output latch from a location specified by the Page Address Register and the Column Address Register,
3. Finally, the content of the Column Address Register is automatically incremented by one. Fig. 16 shows the internal 8-bit ouptut latch located between the 8-bit I/O data bus and the Display Data Memory cell array. Because of this internal 8-bit output latch, a dummy read is needed to obtain correct data from the Display Data Memory. For Display Data Write operation, a dummy write **is not** needed, because data can be directly written from the data bus to internal memory cells.

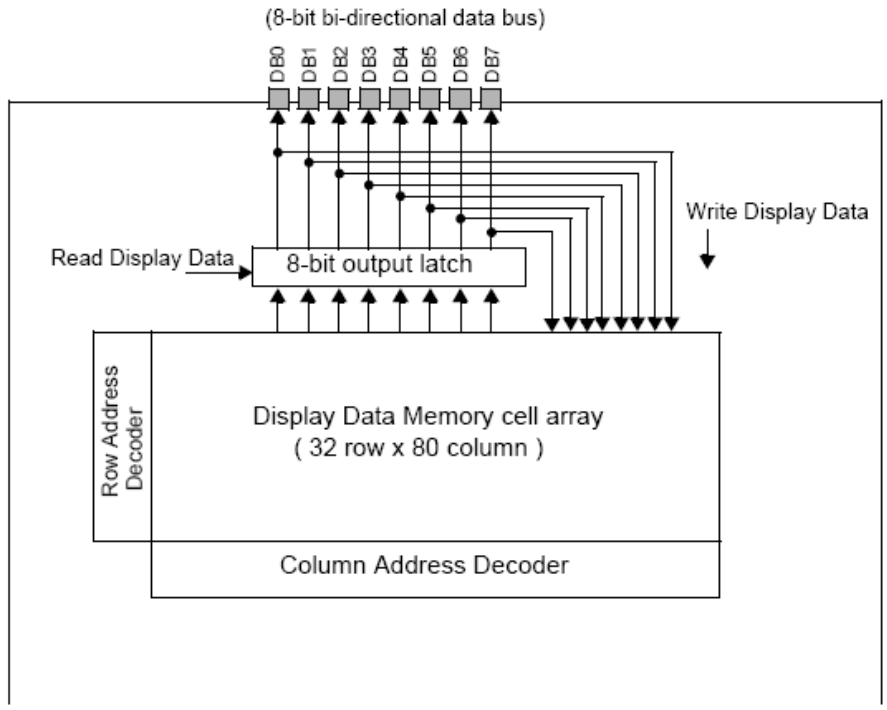


Fig.16 Read Display Data Memory

The setting of the control bus for issuing Read Display Data command

$\overline{C}$/D	E/($\overline{RD}$)	R/$\overline{W}$($\overline{WR}$)
1	0	1

Read-Modify-Write

When the Read-Modify-Write command is issued, the SBN1661G_X enters into Read-Modify-Write mode. In normal operation, when a Read Display Data command or a Write Display Data command is issued, the content of the Column Address Register is automatically incremented by one after the command operation is finished. However, during Read-Modify-Write mode, the content of the Column Address Register is not incremented by one after a Read Display Data command is finished; only the Write Display Data command can make the content of the Column Address Register automatically incremented by one after the command operation is finished. During Read-Modify-Write mode, any other registers, except the Column Address Register, can be modified. This command is useful when a block of the Display Data Memory needs to be repeatedly read and updated.

Fig. 17 gives the change sequence of the Column Address Register during Read-Modify-Write mode. Figure 18 gives the flow chart for Read-Modify-Write command.

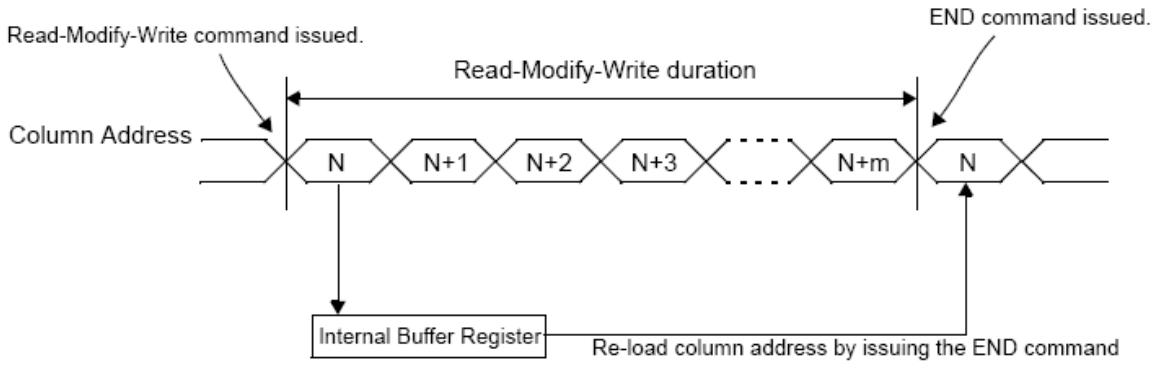


Fig.17 Column address change during Read-Modify-Write

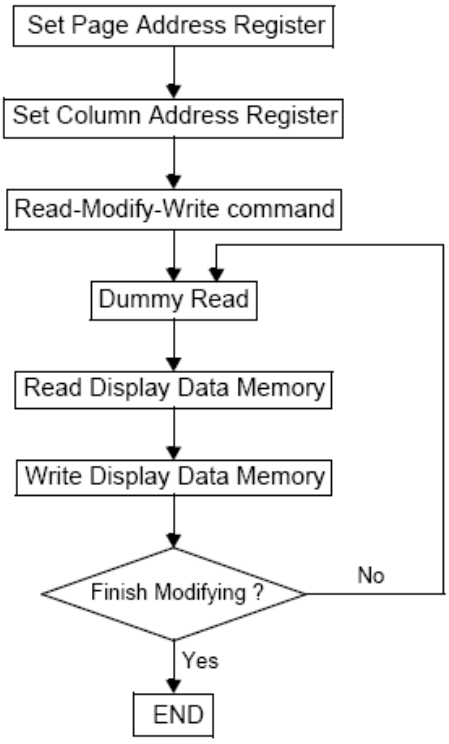


Fig.18 The flowchart for Read-Modify-Write

The setting of the control bus for the Read-Modify-Write command

$\overline{C}$/D	E/($\overline{RD}$)	R/$\overline{W}$($\overline{WR}$)
0	1	0

The setting of the data bus for the Read-Modify-Write command

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
1	1	1	0	0	0	0	0

The END command

The END command releases the Read-Modify-Write mode and re-loads the Column Address Register with the value previously stored in the internal buffer (refer to Fig. 17) when the Read-Modify-Write command was issued.

The setting of the control bus for the END command

$\overline{C}$/D	E/($\overline{RD}$)	R/$\overline{W}$($\overline{WR}$)
0	1	0

The setting of the data bus for the END command

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
1	1	1	0	1	1	1	0

The command code is EE Hex.

Software RESET command

The Software Reset command is different from the hardware reset and can not be used to replace hardware reset.

When Software Reset is issued by the host microcontroller,

• the content of the Display Start Line Register is cleared to zero(A4~A0=00000),

• the Page Address Register is set to 3 (A1 A0 = 11),

• the content of the Display Data Memory remains unchanged.

• the content of all other registers remains unchanged.

The setting of the control bus for Software RESET

$\overline{C}$/D	E/($\overline{RD}$)	R/$\overline{W}$($\overline{WR}$)
0	1	0

The setting of the data bus for Software RESET

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
1	1	1	0	0	0	1	0

The command code is E2 Hex.

11.Timing Characteristics

CL and FR timing

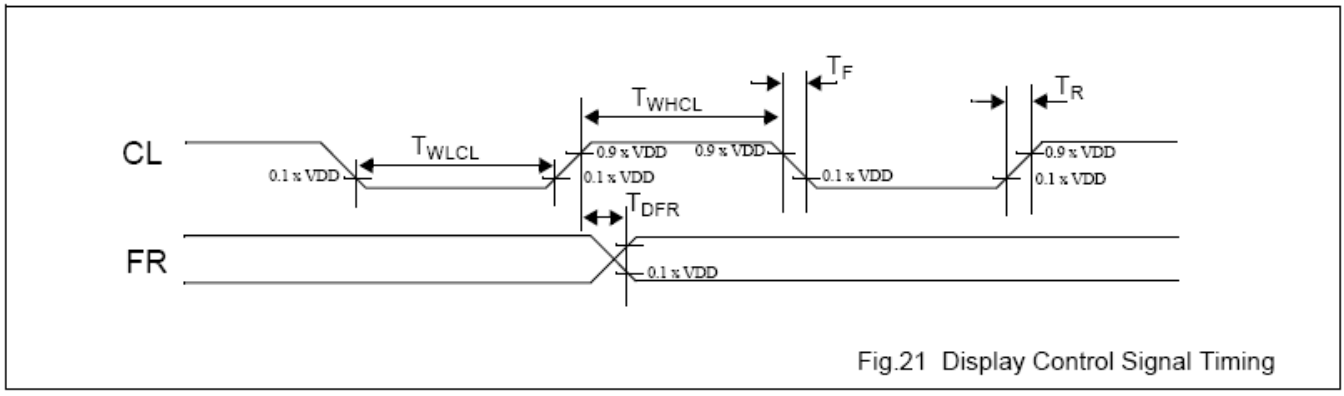


Fig.21 Display Control Signal Timing

CL and FR timing characteristics at VDD=5 volts

VDD = 5 V ±10%; VSS = 0 V; all voltages with respect to VSS unless otherwise specified; Tamb = −20 to +75 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNI
T_{WHCL}	CL clock high pulse width		33			µs
T_{WLCL}	CL cock low pulse width		33			µs
T_R	CL clock rise time			28	120	ns
T_F	CL clock fall time			28	120	ns
$T_{DFR(input)}$	FR delay time (input)	When used as input in Slave Mode application	-2.0	0.2	1.6	µS
$T_{DFR(output)}$	FR delay time (output)	When used as output in Master Mode application, with CL= 100 pF.		0.2	0.36	µS

CL and FR timing characteristics at VDD=3 volts

VDD = 3 V ±10%; VSS = 0 V; all voltages with respect to VSS unless otherwise specified; Tamb = −20 to +75 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{WHCL}	CL clock high pulse width		65			µs
T_{WLCL}	CL cock low pulse width		65			µs
T_R	CL clock rise time			50	220	ns
T_F	CL clock fall time			50	220	ns
$T_{DFR(input)}$	FR delay time (input)	When used as input in Slave Mode application	-3.6	0.36	3.6	µS
$T_{DFR(output)}$	FR delay time (output)	When used as output in Master Mode application, with CL= 100 pF.		0.32	0.6	µS

AC timing for interface with an 80-type microcontroller

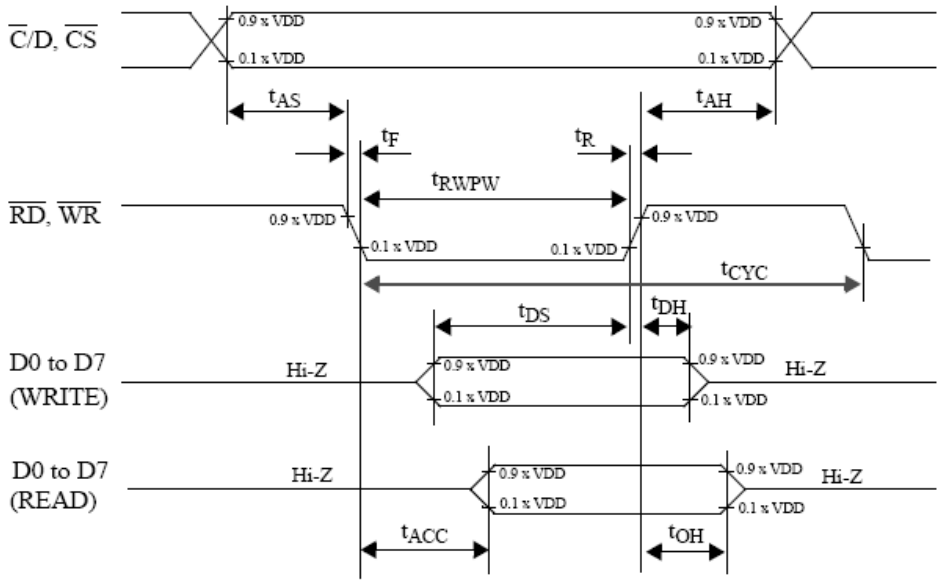


Fig.22 AC timing for interface with a 80-type microcontroller

AC timing for interface with a 80-type microcontorller at VDD=5 volts VDD = 5 V ±10%; VSS = 0 V; Tamb = -20 °C to +75°C.

symbol	parameter	min.	max.	test conditons	unit
t_{AS}	Address set-up time	20			ns
t_{AH}	Address hold time	10			ns
t_F, t_R	Read/Write pulse falling/rising time		15		ns
t_{RWPW}	Read/Write pulse width	200			ns
t_{CYC}	System cycle time	1000			ns
t_{DS}	Data setup time	80			ns
t_{DH}	Data hold time	10			ns
t_{ACC}	Data READ access time		90	CL= 100 pF.	ns
t_{OH}	Data READ output hold time	10	60	Refer to Fig. 23.	ns

AC timing for interface with an 80-type microcontorller at VDD=3 volts VDD = 3 V ±10%; VSS = 0 V; Tamb = -20 °C to +75°C.

symbol	parameter	min.	max.	test conditons	unit
t_{AS}	Address set-up time	40			ns
t_{AH}	Address hold time	20			ns
t_F, t_R	Read/Write pulse falling/rising time		15		ns
t_{RWPW}	Read/Write pulse width	400			ns
t_{CYC}	System cycle time	2000			ns
t_{DS}	Data setup time	160			ns

symbol	parameter	min.	max.	test conditons	unit
t_{DH}	Data hold time	20			ns
t_{ACC}	Data READ access time		180	CL= 100 pF,	ns
t_{OH}	Data READ output hold time	20	120	Refer to 23.	ns

Note:

The measurement is with the load circuit connected. The load circuit is shown in Fig. 23.

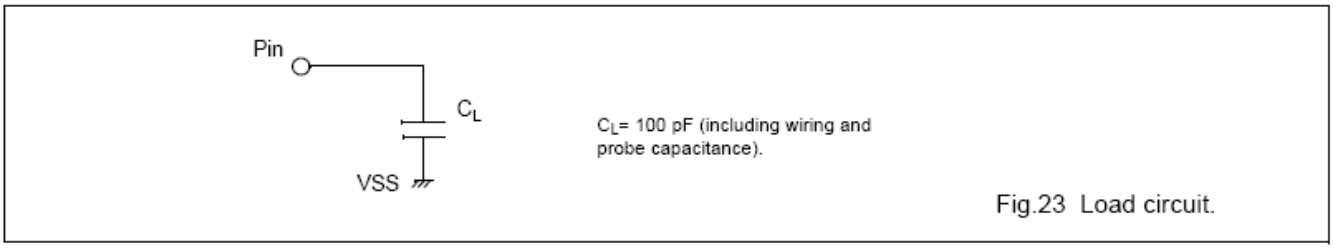


Fig.23 Load circuit.

AC timing for interface with a 68-type microcontroller

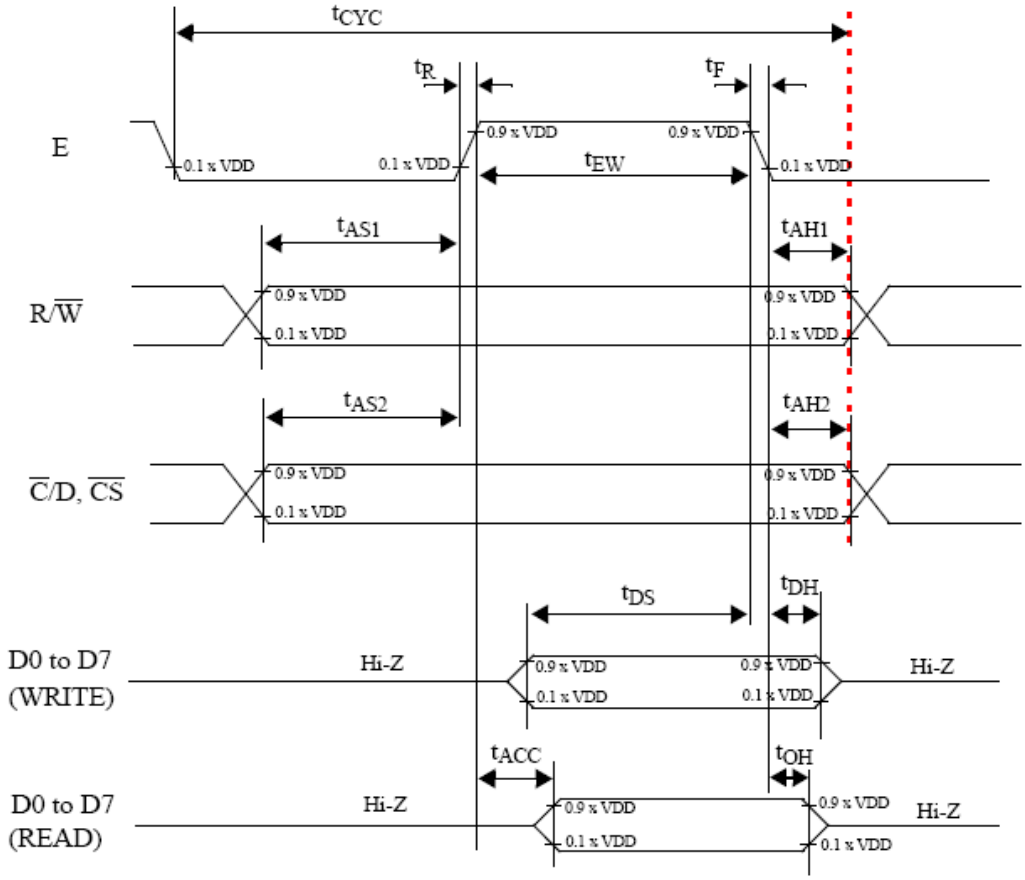


Fig.24 AC timing for interface with a 68-type microcontroller

AC timing for interface with a 68-type microcontroller at VDD=5 volts VDD = 5 V ±10%; VSS = 0 V; Tamb = -20 °C to +75°C.

symbol	parameter	min.	max.	test conditons	unit
t_{AS1}	Address set-up time with respect to R/$\overline{W}$	20			ns
t_{AS2}	Address set-up time with respect to $\overline{C}$/D, $\overline{CS}$	20			ns
t_{AH1}	Address hold time with respect to R/$\overline{W}$	10			ns
t_{AH2}	Address hold time respect with to $\overline{C}$/D, $\overline{CS}$	10			ns
t_F, t_R	Enable (E) pulse falling/rising time		15		ns
t_{CYC}	System cycle time	1000		Note 1	ns
t_{EWR}	Enable pulse width for READ	100			ns
t_{EWW}	Enable pulse width for WRITE	80			ns
t_{DS}	Data setup time	80			ns
t_{DH}	Data hold time	10			ns
t_{ACC}	Data access time		90	CL= 100 pF.	ns
t_{OH}	Data output hold time	10	60	Refer to Fig. 23.	ns

AC timing for interface with a 68-type microcontroller at VDD=3 volts VDD = 3 V ±10%; VSS = 0 V; Tamb = -20 °C to +75°C.

symbol	parameter	min.	max.	test conditons	unit
t_{AS1}	Address set-up time with respect to R/$\overline{W}$	40			ns
t_{AS2}	Address set-up time with respect to $\overline{C}$/D, $\overline{CS}$	40			ns
t_{AH1}	Address hold time with respect to R/$\overline{W}$	20			ns
t_{AH2}	Address hold time respect with to $\overline{C}$/D, $\overline{CS}$	20			ns
t_F, t_R	Enable (E) pulse falling/rising time		15		ns
t_{CYC}	System cycle time	2000		Note 1	ns
t_{EWR}	Enable pulse width for READ	200			ns
t_{EWW}	Enable pulse width for WRITE	160			ns
t_{DS}	Data setup time	160			ns
t_{DH}	Data hold time	20			ns
t_{ACC}	Data access time		180	CL= 100 pF.	ns
t_{OH}	Data output hold time	20	120	Refer to Fig. 23.	ns

Note:

1. The system cycle time(tCYC) is the time duration from the time when Chip Enable is enabled to the time when Chip Select is released.

12.Quality Assurance

Screen Cosmetic Criteria

No.	Defect	Judgment Criterion	Partition
1	Spots	A)Clear Size: d mm — Acceptable Qty in active area d ≤0.1 — Disregard 0.1<d≤0.2 — 6 0.2<d≤0.3 — 2 0.3<d — 0 Note: Including pin holes and defective dots which must be within one pixel size. B)Unclear Size: d mm — Acceptable Qty in active area d ≤0.2 — Disregard 0.2<d≤0.5 — 6 0.5<d≤0.7 — 2 0.7<d — 0	Minor
2	Bubbles in Polarize	Size: d mm — Acceptable Qty in active area d≤0.3 — Disregard 0.3<d≤1.0 — 3 1.0<d≤1.5 — 1 1.5<d — 0	Minor
3	Scratch	In accordance with spots cosmetic criteria. When the light reflects on the panel surface, the scratches are not to be remarkable.	Minor
4	Allowable Density	Above defects should be separated more than 30mm each other.	Minor
5	Coloration	Not to be noticeable coloration in the viewing area of the LCD panels. Back-light type should be judged with back-light on state only.	Minor

13.Reliability

Content of Reliability Test

Environmental Test			
Test Item	**Content of Test**	**Test Condition**	**Applicable Standard**
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80°C 200hrs	——
Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-30°C 200hrs	——
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70°C 200hrs	——
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20°C 200hrs	——
High Temperature/ Humidity Storage	Endurance test applying the high temperature and high humidity storage for a long time.	80°C,90%RH 96hrs	——
High Temperature/ Humidity Operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	70°C,90%RH 96hrs	——
Temperature Cycle	Endurance test applying the low and high temperature cycle. -30°C 25°C 80°C 30min 5min 30min 1 cycle	-30°C/ 80°C 10 cycles	——
Mechanical Test			
Vibration test	Endurance test applying the vibration during transportation and using.	10~55Hz→1.5mmp-p x, y, z Total 1.5hrs	——
Others			
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V,RS=1.5kΩ CS=100pF 1 time	——

***Supply voltage for logic system=5V. Supply voltage for LCD system =Operating voltage at 25°C