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Specification

For

LCD Module

CFAF240400D-030T

MODULE:	**CFAF240400D-030T**
CUSTOMER:	

REV	DESCRIPTION	DATE
1.1	SECOND ISSUE	2010-08-05

TZD	INITIAL	DATE
APREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

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Revision History

Data Rev.	No.	Page	Summary
2009-5-6	1.0	16	First issue.
2010-08-05	1.1	16	Corrected pin names 9, 10, and 33 in section "3.1 Input Signal & Power". Also replaced module drawing.
2011/08/09	2.0		No changes except the part number. Previous part number was CFAF176220M-T. Part number now includes diagonal dimension. For more information, see Technical Bulletin #10335 published 2011/03/29. Improved Module Outline Drawings. Controller Data Sheet added as an appendix.

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Contents

General Description

* Description

This is a color active matrix TFT (Thin Film Transistor) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching devices. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit ,back-light unit. The resolution of a 3.0" TFT-LCD contains 240 x 400 pixels, and can display up to 262K colors.

* Features

-Low Input Voltage : VCC : 2.8V
-Display Colors of TFT LCD : 262K colors
-CPU Interface : 8080 parallel 8 bit/16bit/18bit
-Internal Power Supply Circuit.

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	38.88(H) *64.80(V) (3.0 inch)	mm -	
Driver element	a-Si TFT active matrix	-	-
Display colors	262K	colors -	
Number of pixels	240(RGB) *400	dots -	
Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.162(H) *0.162 (V)	mm -	
Viewing angle	12	o'clock	-
Drive IC	SPFD5420A	- -	
Display mode	Transmissive/ Normally White	- -	
Operating temperature	-20～+70℃	- -	
Storage temperature	-30～+80℃	- -	

- **Mechanical Information**

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H) -		45.04	-	mm	-
	Vertical(V)	-	77.00	-	mm -	
	Depth(D) -		2.6	-	mm -	
Weight		- TBD -			g	-

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1. Optical Characteristics

The following items are measured under stable conditions. The optical characteristics should be measured in a dark room or equivalent state with the methods shown in Note (1).
Measuring equipment: LCD-7200, BM-5A, BM-7, PR-650, EZ-Contrast

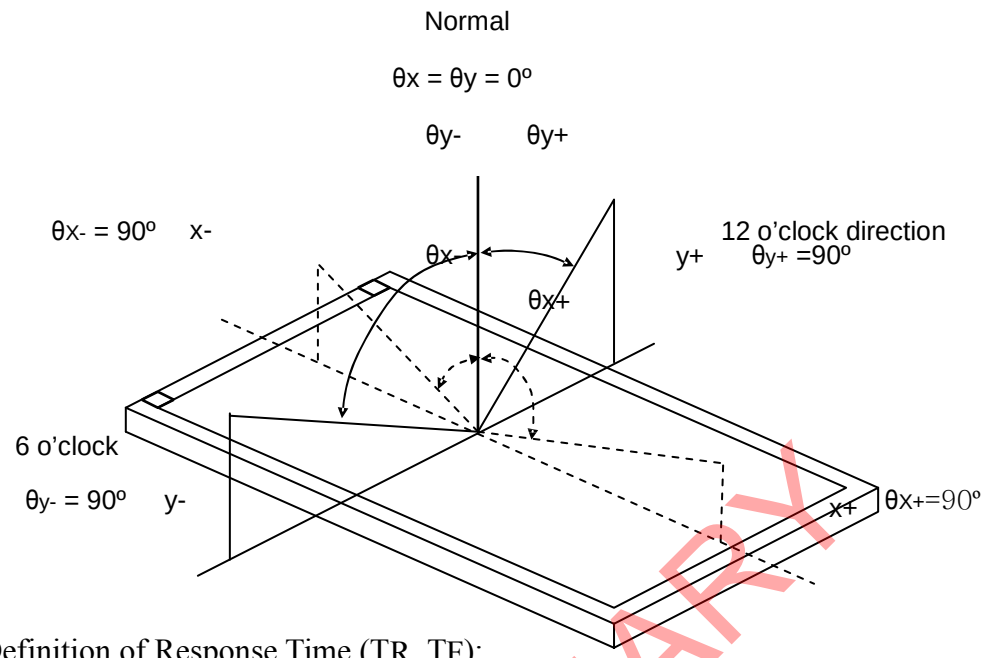
ITEM		SYMBOL	CONDITION	Min.	TYP.	Max.
Color Filter Chromacicity (Note.1)	White	x	θ = ϕ = 0°	(0.283)	(0.303)	(0.323)
		y		(0.322)	(0.342)	(0.362)
		Y		(27.7)	(31.7)	(35.7)
	Red	x	θ = ϕ = 0°	(0.633)	(0.653)	(0.673)
		y		(0.311)	(0.331)	(0.351)
		Y		(14.9)	(17.9)	(20.9)
	Green	x	θ = ϕ = 0°	(0.290)	(0.310)	(0.330)
		y		(0.554)	(0.574)	(0.594)
		Y		(57.3)	(61.3)	(65.3)
	Blue	x	θ = ϕ = 0°	(0.115)	(0.135)	(0.155)
		y		(0.115)	(0.135)	(0.155)
		Y		(12.8)	(15.8)	(18.8)

Measuring equipment : BM-7
Note (1) If product is exposed to high temperatures for extended time, there is a possibility of the polarizer film damage which could degrade the optical characteristics.

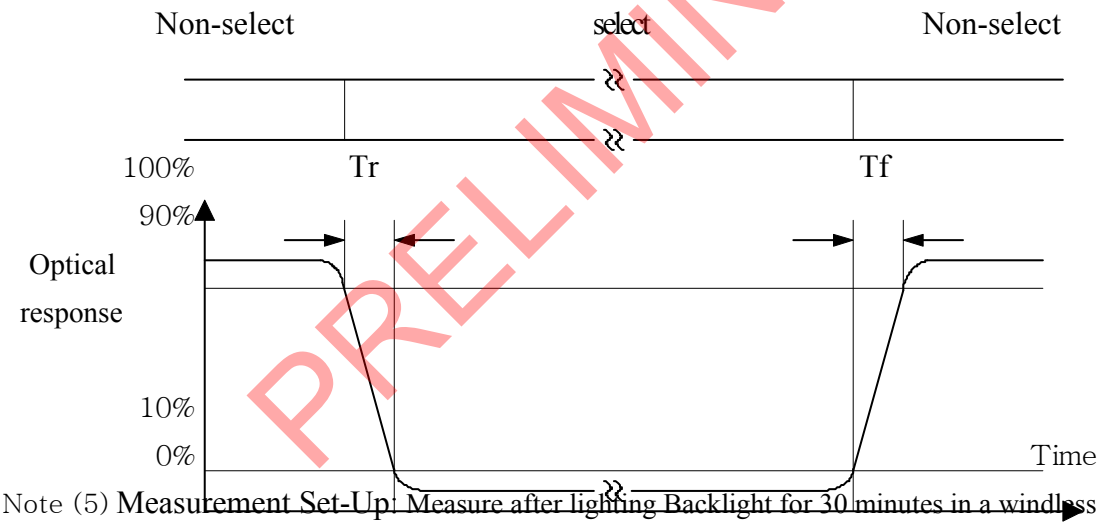
Note (2) Definition of Contrast Ratio (CR):

$$CR = \frac{\text{Luminance (brightness) all pixels "White"}}{\text{Luminance (brightness) all pixels "dark"}}$$

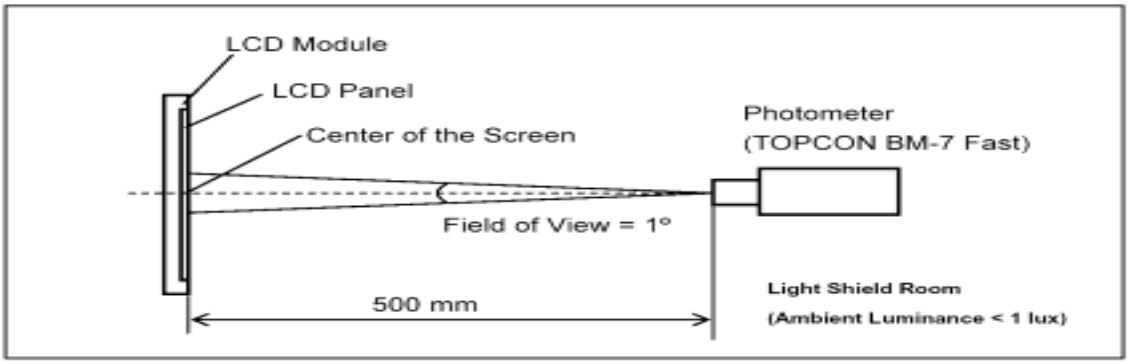
Note (3). Definition of Viewing Angle (θx, θy):



Note (4) Definition of Response Time (TR, TF):



Note (5) Measurement Set-Up: Measure after lighting Backlight for 30 minutes in a windless room.



2. Electrical Characteristics

2.1 ABSOLUTE MAXIMUM RATING(Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage for Logic	V_{CC}	2.7 2.8		+ 3.3 V		-
Logic signal input voltage	V_{IN}	-0.3 -		V_{DDI}+ 0.3	V	-
Operating temperature	T_{OP}	-20	-	+70	℃	1,2
Storage temperature	T_{ST}	-30	-	+80	℃ 1,2	

Note1: Background color changes slightly depending on ambient temperature. This phenomenonis reversible. Ta70℃: 75%RH max

Ta>70℃: absolute humidity must be lower than the humidity of 75%RH at 70℃

Note2: Ta at -30℃will be <48hrs, at 80℃ will be <120hrs

2.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage for Logic	V_{CC}	2.7 2.8		3.3 V		-
Current consum ption	I_{CC}+ I_{CI}	- 8			mA	-
Level input voltage	V_{IH}	0.7V_{DDI}	-	V_{DDI} V		-
	V_{IL}	V_{SS} -		0.3V_{DDI}	V -	
Level output voltage	V_{OH}	V_{SS} -		V_{DDI}	V	-
	V_{OL}	V_{SS} -		0.2V_{DDI}	V	-

2.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 4chips White LED in parallel

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	- 60 -			mA	
Forward Voltage	V_F	- 3.2 -			V	-
Luminance	L_V	-- TBD		-	cd/m2	–
Uniformity	A_{Vg}	80 -		-	% -	

3. Input terminal Pin Assignment

3.1 Input signal & Power

Pin NO.	Symbol	Function
1	GND	System ground
2	NC	NC
3-6	LEDK4-LEDK1	LED Cathode K4-K1
7	LEDA	LED Anode
8	RESET	This signal will reset the device and it must be applied to properly
9	IM1	Connect to Host IM1
10	IM2	Connect to Host IM2
11-28	DB17-DB00	MCU parallel interface data busDB17-DB00.
29	RD	Read enable in 8080 MCU parallel interface.
30	WR	Write enable in 8080 MCU parallel interface.
31	RS	Display data/command selection pin in MCU interface. RS='1':display data or parameter. RS='0': command data.
32	CS	Chip selection pin ("Low" is enable) signal
33	ID / IM0	IM0
34	XL	NC
35	YD	NC
36	XR	NC
37	YU	NC
38	VDD	Power supply
39	GND	System ground

3.2 Input Signal, Basic Display Colors and Gray scale of Each Colors

COLOR	Display	RED						GREEN						BLUE						GRAY SCALE LEVEL
		R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	B4	B5	
BASIC COLOR	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	BLUE	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	-
	GREEN	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	-
	CYAN	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	-
	RED	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	-
	MAGENTA	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	-
	YELLOW	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	-
	WHITE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-
GRAY SCALE OF RED	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0
	DARK	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1
	↑	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	R3~R60
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	↓	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R61
	LIGHT	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R62
	RED	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R63
GRAY SCALE OF GRE EN	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G0
	DARK	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	G1
	↑	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	G2
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	G3~G60
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	↓	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0	G61
	LIGHT	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	G62
	GREEN	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	G63
GRAY SCALE OF BLUE	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	B0
	DARK	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	B1
	↑	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	B2
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	B3~B60
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	↓	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	B61
	LIGHT	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	B62
	BLUE	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	B63

Note) Defintion of Gray :

Rn: Red Gray, Gn : Green Gray, Bn: Blue Gray (n = Gray level)

Input Signal : 0 = Low level voltage , 1 = High level votage

4. Operating Principle & Methods

4.1 Please refer to SPFD5420A datasheet for more details.

80-System Interface Timing Characteristics

Table 13-4 Normal write operation (HWM=0), IOVCC=1.65V~3.60V

Item	Symbol		Unit	Min.	Typ.	Max.
Bus cycle time	Write	tCYCW	ns	150	-	-
	Read	tCYCR	ns	450	-	-
Write low-level pulse width		PWLW	ns	55	-	-
Read low-level pulse width		PWLR	ns	170	-	-
Write high-level pulse width		PWHW	ns	70	-	-
Read high-level pulse width		PWHR	ns	250	-	-
Write/Read rise/ fall time		tWRr, WRf	ns		-	10
Setup time	Write (RS to CS*,WR*)	tAS	ns	0	-	-
	Read (RS to CS*, RD*)		ns	10	-	-
Address Hold Time		tAH	ns	2	-	-
Write data setup time		tDSW	ns	25	-	-
Write data hold time		tH	ns	10	-	-
Read data delay time		tDDR	ns	-	-	150
Read data hold time		tDHR	ns	5	-	-

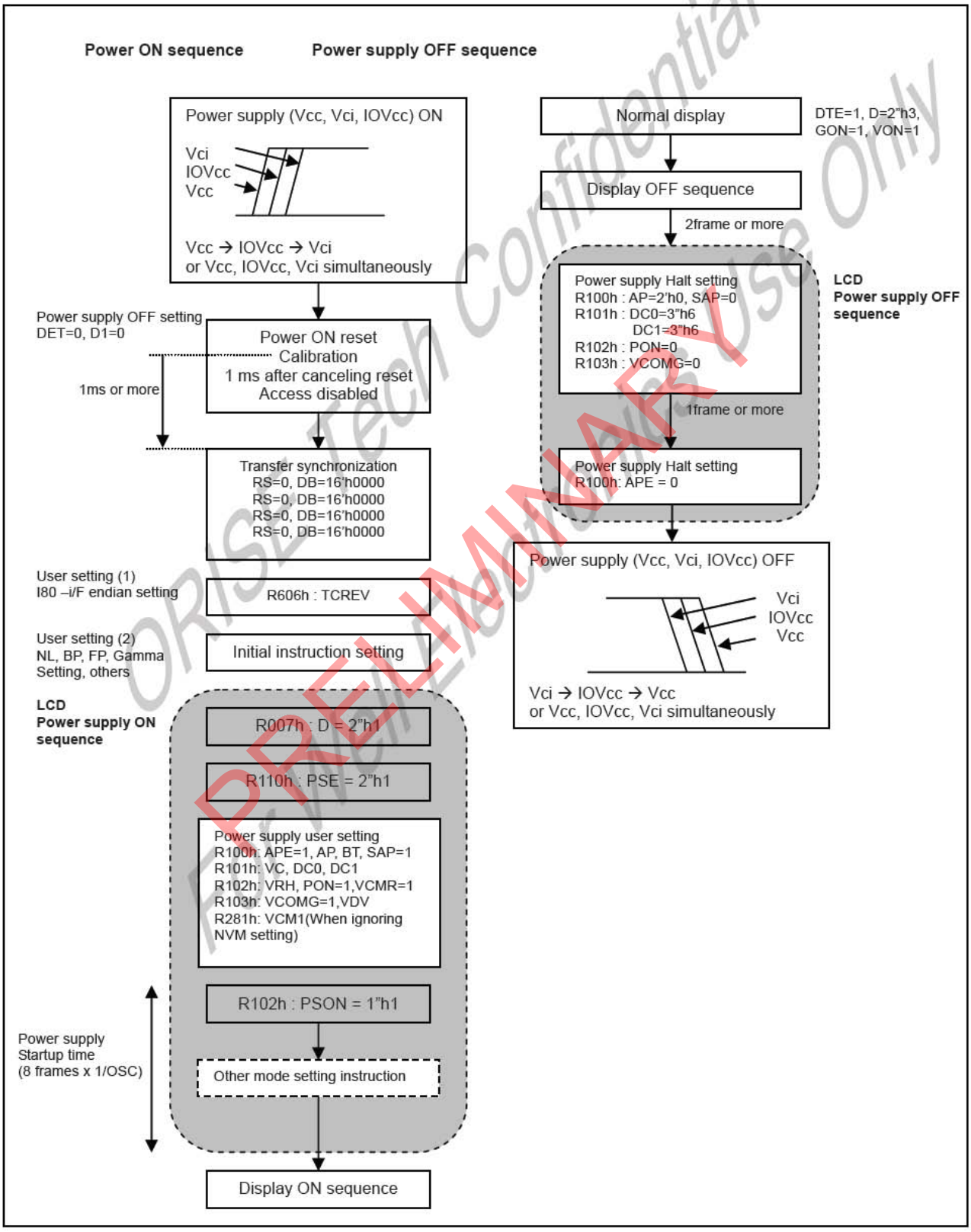
Figure 4.1 **80 SYSTEM BUS TIMING**

4.2 RESET TIMING

Item	Symbol	Unit	Min.	Typ.	Max.
Reset low-level width	tRES	ms	1	—	—
Reset rise time	trRES	µs	—	—	10

5. Operation Sequence:

5.1 Power On/Off Sequence



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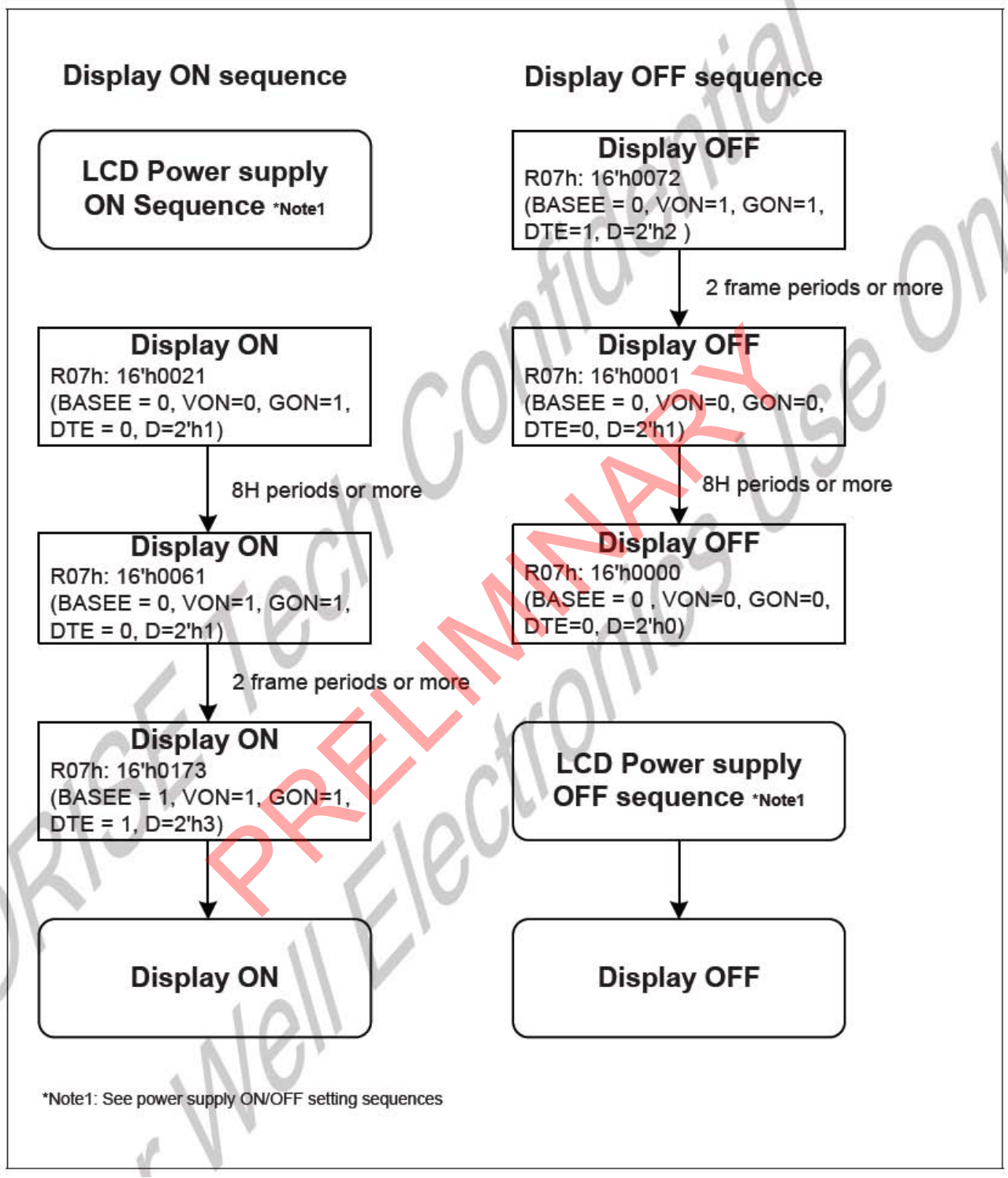
5.2 Display On/Off Sequence



6. Reliability Test Result

6.1 Condition

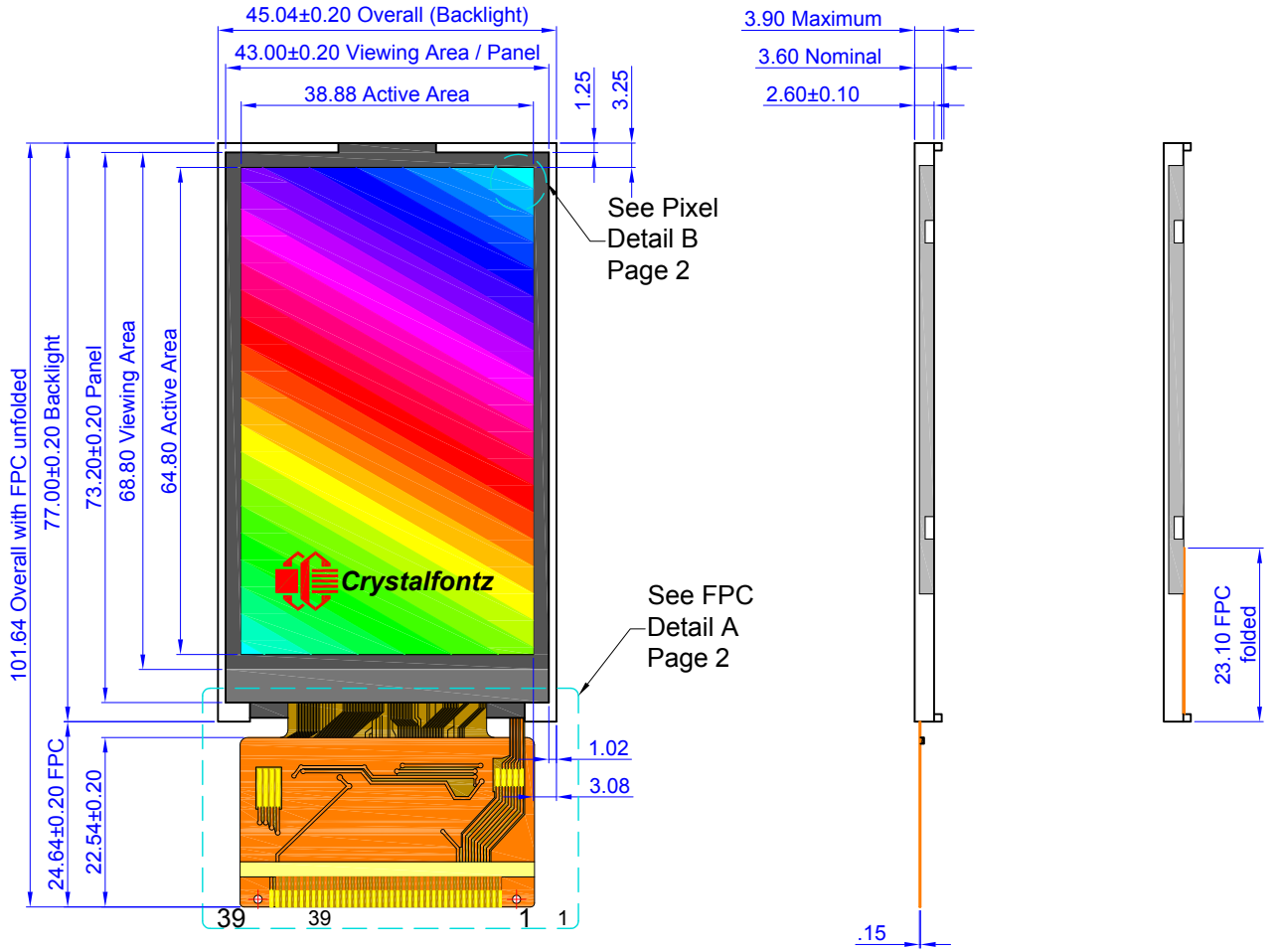
Item	Condition	Sample Size	Test Result	Note
Low Temperature Operating Life test	-20℃, 96HR	5ea TBD		-
Thermal Humidity Operating Life test	60℃, 90%RH, 96HR	10ea TBD		-
Temperature Cycle ON/OFF test	-20℃ ↔ 70 ℃, ON/OFF, 20CYC	5ea TBD		(1)
High Temperature Storage test	80℃, 96HR	5ea TBD		-
Low Temperature Storage test	－30℃, 96HR	5ea TBD		-
Thermal Shock test	(-20℃ ⇔ 70℃) 8CYC	5ea TBD		(2)
ESD CDM Contact +/-4kV,	5 times	5ea	TBD	
ESD CDM Air +/-8kV	, 5 times	5ea	TBD	
Box Vibration Test	Acceleration:1.5G, Vibration width : 3 mm Sweep range : 5-55 Hz Vibration direction : X, Y, Z axis 120 cyc	1box TBD		
Box Drop Test	1 Corner 3 Edges 6 faces, 66㎝(MEDIUM BOX)	1box TBD		-

Note (1) ON Time over 10 seconds, OFF Time under 10 seconds

(2)

STEP Order	Temperature	Humidity	Time	Test	Note
1	+ 25 ℃	65 %	3 Hr	Function Test	① Tem perature : within 3 ℃ below 1 ℃/min
2	－ 20 ℃	0 %	12 Hr	Auto Test	
3	+ 25℃	65 %	1 Hr	Function Test	
4	+ 70 ℃	90 %	12 Hr	Auto Test	
5	+ 25 ℃	65 %	1 Hr	Function Test	
6	－ 20 ℃	0 %	12 Hr	Auto Test	
7	+ 70 ℃	95 %	12 Hr	Auto Test	
8	+ 25 ℃	65 %	3 Hr	Final Test	

Module Outline Dimensions are on the following 2 pages.



Note: 1) Tolerance is ±0.3 mm unless specified.
2) FPC = Flexible Printed Circuit.
3) Diagonal = 2.98"

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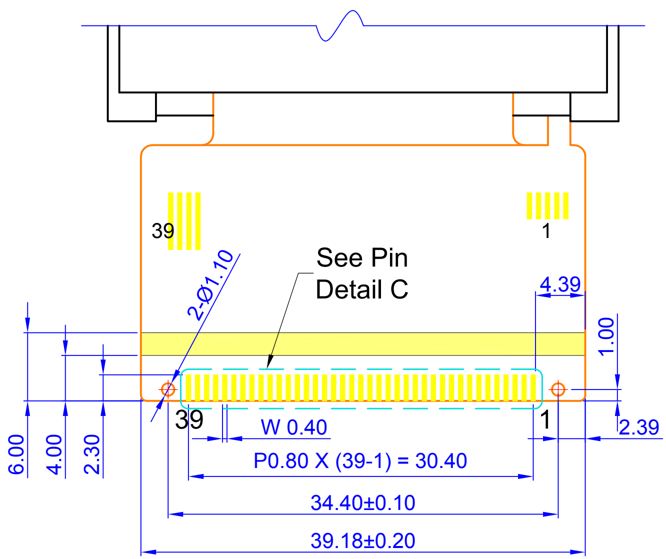
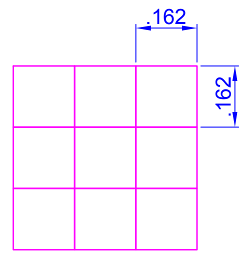
Part No.(s):	Scale:	Drawing Number:	Hardware Rev.:
CFAF240400D-030T Preliminary Drawing	Not to scale	CFAF240400D-030T	vA
	Units: Millimeters	Date: 2011/08/09	Sheet: 1 of 2

Pin	Signal
1	GND
2	NC
3	LEDK4
4	LEDK3
5	LEDK2
6	LEDK1
7	LEDA
8	RESET
9	IM1
10	IM2
11	DB-17
12	DB-16
13	DB-15
14	DB-14
15	DB-13
16	DB-12
17	DB-11
18	DB-10
19	DB-9
20	DB-8
21	DB-7
22	DB-6
23	DB-5
24	DB-4
25	DB-3
26	DB-2
27	DB-1
28	DB-0
29	RD
30	WR
31	RS
32	CS
33	ID/IM0
34	NC
35	NC
36	NC
37	NC
38	VDD
39	GND

Pin Detail C

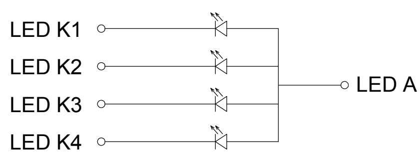


FPC Detail A



Pixel Detail B

LED Circuit Diagram:



Note: 1) Tolerance is ±0.3 mm unless specified.
2) FPC = Flexible Printed Circuit.
3) Diagonal = 2.98"

Part No.(s):	Scale:	Drawing Number:	Hardware Rev.:
CFAF240400D-030T Preliminary Drawing	Not to scale	CFAF240400D-030T	vA
	Units: Millimeters	Date: 2011/08/09	Sheet: 2 of 2

8. Packing

TBD

9. Cautions and Handling Precautions

9.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
(2) Protect the module from physical shock or any force. In addition to damage,
this may cause improper operation or damage to the module and back-light unit.
(3) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface.
(4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
(8) Protect the module from static, it may cause damage to the CMOS ICs.
(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
(10) Do not disassemble the module.
(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
(12) Pins of I/F connector shall not be touched directly with bare hands.
(13) Do not connect, disconnect the module in the “Power ON” condition.
(14) Power supply should always be turned on/off by the item 5.1 Power On Sequence &5.2 Power Off Sequence

9.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

Appendix

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ORISE TECH

DATA SHEET

SPFD5420A

720-channel 6-bit Source Driver with System-on-chip for Color Amorphous TFT-LCDs

Preliminary

JUL. 13, 2007

Version 0.2

Table of Contents

PAGE

720-CHANNEL DRIVER WITH SYSTEM-ON-CHIP (SOC) FOR COLOR AMORPHOUS TFT LCD

1. GENERAL DESCRIPTION

The SPFD5420A, a 262144-color System-on-Chip (SoC) driver LSI designed for small and medium sizes of TFT LCD display, is capable of supporting up to 240xRGBx432 in resolution which can be achieved by the designated RAM for graphic data. The 720-channel source driver has true 6-bit resolution, which generates 64 Gamma-corrected values by an internal D/A converter.

The SPFD5420A is able to operate with low IO interface power supply up to 1.65V and incorporate with several charge pumps to generate various voltage levels that form an on-chip power management system for gate driver and source driver.

The built-in timing controller in SPFD5420A can support several interfaces for the diverse request of medium or small size portable display. SPFD5420A provides system interfaces, which include 8-/9-/16-/18-bit parallel interfaces and serial interface (SPI), to configure system. Not only can the system interfaces be used to configure system, they can also access RAM at high speed for still picture display. In addition, the SPFD5420A incorporates 6, 16, and 18-bit RGB interfaces for picture movement display. The SPFD5420A also supports eight-color mode and standby mode for power saving consideration.

2. FEATURES

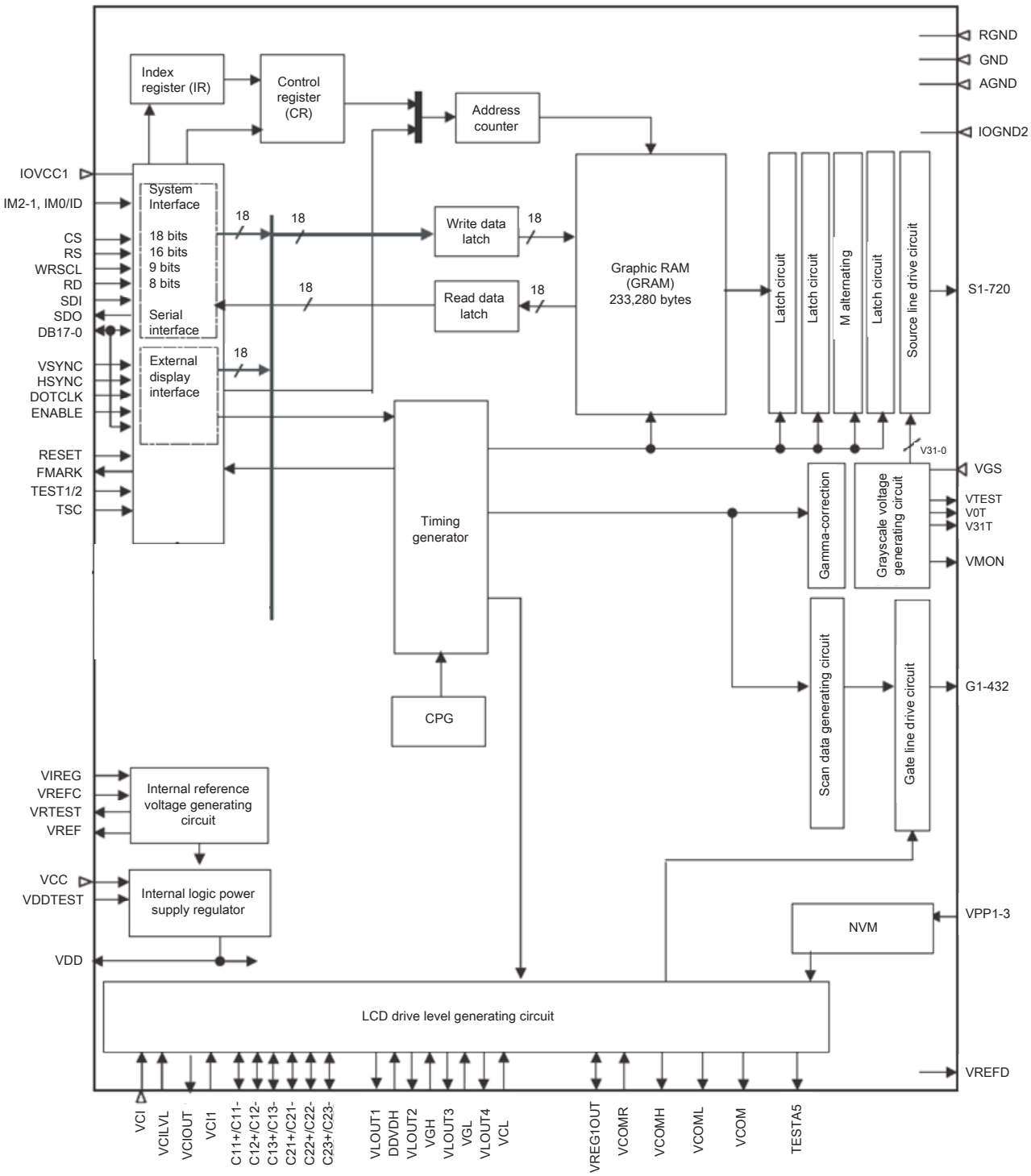
- One-chip solution for amorphous TFT-LCD.
- Supports resolution up to 240xRGBx432, incorporating a 720-channel source driver and a 432-channel gate driver
- Outputs 64 γ -corrected values using an internal true 6-bit resolution D/A converter to achieve 262K colors
- Built-in 233,280 bytes internal RAM
- Line Inversion AC drive / frame inversion AC drive
- System interfaces
  - High-speed interfaces to 8-, 9-, 16-, and 18-bit parallel ports
  - Serial Peripheral Interface (SPI)
- Interfaces for moving picture display
  - 6-, 16-, and 18-bit RGB interfaces
- Varies RAM accessing for functional display
  - Window address function to display at any area on the screen via a moving picture display interface
  - Window address function to limit the data rewriting area and reduce data transfer
  - Moving and still picture can display at the same time
  - Vertical scrolling function
  - Partial screen display
- Power supply
  - Logic power supply voltage (Vcc): 2.5 ~ 3.1 V
  - I/O interface supply voltage (IOVcc): 1.65 ~ 31 V
  - Analog power supply voltage (Vci): 2.5 ~ 3.1 V
- On-chip power management system
  - Power saving mode (standby / 8-color mode, etc)
  - Low power consumption structure for source driver.
- Built-in Charge Pump circuits
  - Source driver voltage level: DDVDH-GND=4.5V ~ 6V.
  - Gate driver voltage level (VGH, VGL)
    VGH = 10.0V ~15.0V
    VGL = -4.5V ~ -12.5V
    VGH – VGL $\leqq$ 28.0V
  - Built-in internal oscillator and hardware reset
- Built–in One-Time-Programmable (OTP) function for VCOM amplitude and VcomH voltage adjustment. User identification code,4 bits, VCOM level adjustment, 5 bits x 2 sets

3. ORDERING INFORMATION

Product Number	Package Type
SPFD5420A-C	Chip Form with Gold Bump

4. BLOCK DIAGRAM

4.1. Block Function



4.2. System Interface

4.2.1. The SPFD5420A supports three high-speed system interfaces:

1. 80-system high-speed interfaces with 8-, 9-, 16-, 18-bit parallel ports.
2. Serial Peripheral Interface (SPI).

The SPFD5420A has a 16-bit index register (IR) and two 18-bit data registers, a write-data register (WDR) and a read-data register (RDR). The IR register is used to store index information from control registers. The WDR register is used to temporarily store data to be written for register control and internal GRAM. The RDR register is used to temporarily store data read from the GRAM. When graphic data is written to the internal GRAM from MCU/graphic engine, the data is first written to the WDR and then automatically written to the internal GRAM in internal operation. When graphic data read operation is executed, graphic data is read via the RDR from the internal GRAM. Therefore, invalid data is first read out to the data bus when the SPFD5420A executes the 1st read operation. Thus, valid data can be read out after the SPFD5420A executes the 1st read operation.

4.2.2. External Display Interface

The SPFD5420A supports external RGB interface for picture movement display.

The SPFD5420A allows switching between one of the external display interfaces and the system interface via pin configuration so that the optimum interface is selected for still / moving picture displayed on the screen.

When the RGB interface is chosen, display operations are synchronized with external supplied signals, VSYNC, HSYNC, and DOTCLK. Moreover, valid display data (DB17-0) is written to GRAM, which synchronized with signal (DE) enabling.

4.2.3. Address Counter (AC)

SPFD5420A features an Address Counter (AC) giving an address to the internal GRAM. The address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

4.2.4. Graphics RAM (GRAM)

SPFD5420A features a 233,280-byte (240RGB x 432 x 18 / 8) Graphic RAM (GRAM).

4.2.5. Grayscale Voltage Generating Circuit

SPFD5420A has true 6-bit resolution D/A converter, which generates 64 Gamma-corrected values and cooperates with OP-AMP structure to enhance display quality. The grayscale voltage can be adjusted by grayscale data set in the γ-correction register.

4.2.6. Timing Controller

SPFD5420A has a timing controller, which can generate a timing signal for internal circuit operation such as gate output timing, RAM accessing timing, etc.

4.2.7. Oscillator (OSC)

The SPFD5420A also features an internal oscillator to generate RC oscillation with an internal resistor. In standby mode, RC oscillation is halted to reduce power consumption.

4.2.8. Source Driver Circuit

SPFD5420A consists of a 720-output source driver circuit (S1 ~ S720). Data in the GRAM are latched when the 720th bit data is input. The latched data controls the source driver and generates a drive waveform.

4.2.9. Gate Driver Circuit

SPFD5420A consists of a 432-output gate driver circuit (G1~G432). The gate driver circuit outputs gate driver signals at either VGH or VGL level.

4.2.10. LCD Driving Power Supply Circuit

The LCD driving power supply circuit generates the voltage levels DDVDH, VLOUT2, VLOUT3 and VCOM for driving an LCD. All this voltages can be adjusted by register setting.

5. SIGNAL DESCRIPTIONS

<table>
<tr><th>Signal</th><th>No. of pins</th><th>I/O</th><th>Connected with</th><th>Function</th></tr>
<tr><td colspan="5">System Configuration Input Signal</td></tr>
<tr><td>IM2~1, IM0/ID</td><td>3</td><td>I</td><td>GND/ IOVCC</td><td>Select a mode to interface to an MPU. In serial interface operation, the IM0 pin is used to set the ID bit of device code.
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0/ I D</th><th>Interface Mode</th><th>DB Pin</th><th>Colors</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>80-system 18-bit interface</td><td>DB17-0</td><td>262,144</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>80-system 9-bit interface</td><td>DB17-9</td><td>262,144</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>80-system 16-bit interface</td><td>DB17-10, DB8-1</td><td>262,144 see Note 1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>80-system 8-bit interface</td><td>DB17-10</td><td>262,144 see Note 2</td></tr>
<tr><td>1</td><td>0</td><td>*(ID)</td><td>Clock synchronous serial interface</td><td>-</td><td>65,536</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
</table>
Notes: 1. 65,536 colors in one transfer mode
2. 65,536 colors in two transfers mode</td></tr>
<tr><td>/RESET</td><td>1</td><td>I</td><td>MPU or external RC circuit</td><td>RESET pin. This is an active low signal.</td></tr>
<tr><td colspan="5">Interface input Signals</td></tr>
<tr><td>/CS</td><td>1</td><td>I</td><td>MPU</td><td>Chip select signal.
Low: the SPFD5420A is accessible
High: the SPFD5420A is not accessible
Must be connected to the GND or IOVCC level when not used.</td></tr>
<tr><td>RS</td><td>1</td><td>I</td><td>MPU</td><td>Register select signal.
Low: Index register or internal status is selected.
High: Control register is selected.
Must be connected to the GND or IOVCC level when not used.</td></tr>
<tr><td>(/WR) / (SCL)</td><td>1</td><td>I</td><td>MPU</td><td>(A) In 80-system interface mode, a write strobe signal can be input via this pin and initializes a write operation when the signal is low.
(B) In SPI mode, served as a synchronizing clock signal.</td></tr>
<tr><td>/RD</td><td>1</td><td>I</td><td>MPU</td><td>In 80-system interface mode, a read strobe signal can be input via this pin and initializes a read operation when the signal is low.
Must be connected to the GND or IOVCC level when not in use.</td></tr>
<tr><td>SDI</td><td>1</td><td>I</td><td>MPU</td><td>Serial Data is inputted on the rising edge of the SCL signal in SPI mode.
Must be connected to the GND or IOVCC level when not in use</td></tr>
<tr><td>SDO</td><td>1</td><td>O</td><td>MPU</td><td>Serial Data is outputted on the rising edge of the SCL signal in SPI mode.</td></tr>
<tr><td>DB0-DB17</td><td>1</td><td>I/O</td><td>MPU</td><td>Served as an 18-bit parallel bi-directional data bus. Data bus pin assignment corresponding to different modes are summarized in the table:
<table>
<tr><th>Mode</th><th>Pin Assignment</th></tr>
<tr><td>8-bit system interface</td><td>DB17-DB10</td></tr>
<tr><td>9-bit system interface</td><td>DB17-DB9</td></tr>
<tr><td>16-bit system interface</td><td>DB17-DB10, DB8-DB1</td></tr>
<tr><td>18-bit system interface</td><td>DB17-DB0</td></tr>
</table></td></tr>
</table>

Signal	No. of pins	I/O	Connected with	Function
				6-bit External (RGB) interface: DB17-DB12 16-bit External (RGB) interface: DB17-13, DB11-DB1 18-bit External (RGB) interface: DB17-DB0 Must be connected to the GND or IOVCC level when not in use.
VSYNC	1	I	MPU	In external interface mode, served as a vertical synchronize signal input Must be connected to the IOVCC or GND level when not in use.
HSYNC	1	I	MPU	In external interface mode, served as a horizontal synchronized signal input Must be connected to the IOVCC or GND level when not used.
ENABLE	1	I	MPU	In external interface mode, polarity of ENABLE signal is synchronized with valid graphic data input. Low: Valid data on DB17-DB0 High: Invalid data on DB17-DB0 Moreover, setting EPL bit can change the polarity of the ENABLE signal. Must be connected to the GND or IOVCC level when not in use.
DOTCLK	1	I	MPU	In external interface mode, served as a dot clock signal. When DPL = "0": Input data on the rising edge of DOTCLK When DPL = "1": Input data on the falling edge of DOTCLK It is fixed to the IOVCC level when not in use.
FMARK	1	O	MPU	Frame head pulse signal, which is used when writing data to the internal RAM. Keep this pin open when not used.
Charge Pump and Power Supply Signal				
C11P/N, C12P/N C13P/N C21P/N, C22P/N C23P/N	12	I/O	Step-up capacitor	Connect boost capacitors for the internal DC/DC converter circuit to these pins. Leave the pins open when DC/DC converter circuits are not used.
VCIOUT	1	O	Stabilizing capacitor, VCI1	Output voltage from the step-up circuit 1, generated from the reference voltage. VC bits set the output factor. Make sure to connect to stabilizing capacitor.
VCI1	1	I/O	VCIOUT	Reference voltage of step-up circuit 1. Make sure the output voltage levels from VLOUT1, VLOUT2, and VLOUT3 do not exceed the respective setting ranges.
VLOUT1	1	O	Stabilizing capacitor, DDVDH	Output voltage from the step-up circuit 1, generated from VCI1. The step-up factor is set by BT. Make sure to connect to stabilizing capacitor. VLOUT1 = 4.5V ~ 6.0V
DDVDH	1	I	VLOUT1	Power supply for the source driver liquid crystal drive unit and VCOM drive. Connect to VLOUT1. DDVDH = 4.5V ~ 6.0V
VLOUT2	1	O	Stabilizing capacitor, VGH	Output voltage from the step-up circuit 2, generated from VCI1 and DDVDH. The step-up factor is set by BT. Make sure to connect to stabilizing capacitor. VLOUT2 = max 15.0V
VGH	1	I	VLOUT2	Liquid crystal drive power supply. Connect to VLOUT2.
VLOUT3	1	O	Stabilizing capacitor, VGL	Output voltage from the step-up circuit 2, generated from VCI1 and DDVDH. The step-up factor is set by BT bits. Make sure to connect to stabilizing capacitor. VLOUT3 = min –12.5V

Signal	No. of pins	I/O	Connected with	Function
VGL	1	I	VLOUT3	Liquid crystal drive power supply. Connect to VLOUT3.
VLOUT4	1	O	Stabilizing capacitor, VCL	Output voltage from the step-up circuit 2, generated from VCI1 and DDVDH. The step-up factor is set by BT bits. Make sure to connect to stabilizing capacitor. VLOUT = -1.9V – 3.0V.
VCL	1	O	Stabilizing capacitor	VCOML drive power supply. Make sure to connect to stabilizing capacitor. VCL = -1.9V ~ -3.0V
VCILVL		I	Reference power supply	VCILVL must be at the same electrical potential as VCI. VCILVL = 2.5V ~ 3.1V. Connect to external power supply. In case of COG, connect to VCI on the FPC to prevent noise.
VPP1	1	I	Power supply or open	OTP power supply.
VPP2	1	I	Power supply or open	
VPP3A, 3B	2	I	Power supply or open	

Operation mode	VPP1	VPP2	VPP3
NVM Write	9V	7.5V	GND
NVM read	Open	Open	GND/Open

Source/Gate Driver and VCOM Signals				
G1~G432	432	O	LCD	Output gate driver signals, which has the swing from VGH to VGL
S1~S720	720	O	LCD	Output source driver signals. The D/A converted 64-gray-scale analog voltages are outputted.
VREG1 OUT	1	O	Stabilizing capacitor	Output voltage generated from the reference voltage (VCILVL or VCIR). The factor is determined by instruction (VRH bits). VREG1OUT is used for (1) source driver grayscale reference voltage, (2) VCOMH level reference voltage, and (3) VCOM amplitude reference voltage. Connect to a stabilizing capacitor when in use. VREG1OUT = 4.0V ~ (DDVDH – 0.5)V
VCOM	1	O	TFT panel common electrode	Power supply to TFT panel's common electrode. VCOM alternates between VCOMH and VCOML. The alternating cycle is set by internal register. Also, the VCOM output can be started and halted by register setting.
VCOMH	1	O	Stabilizing capacitor	The High level of VCOM amplitude. The output level can be adjusted by either external resistor (VCOMR) or electronic volume. Make sure to connect to stabilizing capacitor.
VCOML	1	O	Stabilizing capacitor	The Low level of VCOM amplitude. The output level can be adjusted by instruction (VDV bits). VCOML = (VCL+0.5)V ~ 0V. Make sure to connect to stabilizing capacitor.
VCOMR	1	I	Variable resistor or open	Connect a variable resistor when adjusting the VCOMH level between VREG1OUT and GND.
VGS	1	I	GND	Reference level for the grayscale voltage generating circuit.
VCC	1	-	Power supply	Internal logic power: VCC = 2.5V ~3.1V. VCC > IOVCC.
GND	1	-	Power supply	Internal logic GND: GND = 0V.
RGND	1	-	Power supply	Internal RAM GND. RGND must be at the same electrical potential as GND. In case of COG, connect to GND on the FPC to prevent noise.
VDD	1	O	Stabilizing capacitor	Internal logic regulator output, which is used as the power supply to internal logic. Connect a stabilizing capacitor.
IOVCC	1	-	Power supply	Power supply to the interface pins: RESET*, CS*, WR, RD*, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE. IOVCC = 1.65V ~ 3.3V. VCC ≥IOVCC. In case of COG, connect to VCC on the FPC if IOVCC=VCC, to prevent noise.

Signal	No. of pins	I/O	Connected with	Function
IOGND	1	-	Power supply	GND for the interface pins: RESET*, CS*, WR, RD*, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE. IOGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
AGND	1	-	Power supply	Analog GND (for logic regulator and liquid crystal power supply circuit): AGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
VCI	1	I	Power supply	Power supply to the liquid crystal power supply analog circuit. Connect to an external power supply of 2.5V ~ 3.1V.
VCILVL	1	I	Reference power supply	VCILVL must be at the same electrical potential as VCI. VCILVL = 2.5V ~ 3.1V. Connect to external power supply. In case of COG, connect to VCI on the FPC to prevent noise.
Misc. Signal				
V0T, V31T	2	I/O	Open	Test pins. Leave them open. SPFD5420A use these pins to do self-test. No signal on panel can cross these pins, otherwise function fail.
VTEST	1	I/O	Open	Test pins. Leave them open. SPFD5420A use these pins to do self-test. No signal on panel can cross these pins, otherwise function fail.
VREFC	1	I/O	Open	Test pins. Fix to the AGND level.
VREF	1	I/O	Open	Test pins. Leave them open.
VDDTEST	1	I/O	Open	Test pins. Fix to the AGND level.
VREFD	1	I/O	Open	Test pins. Leave them open. SPFD5420A use these pins to do self-test. No signal on panel can cross these pins, otherwise function fail.
VMON	1	I/O	Open	Test pins. Leave them open. SPFD5420A use these pins to do self-test. No signal on panel can cross these pins, otherwise function fail.
TESTA5	1	I/O	Open	Test pins. Leave them open. SPFD5420A use these pins to do self-test. No signal on panel can cross these pins, otherwise function fail.
IOVCCDUM1~2	2	I/O	Open	Test pins. Leave them open.
VCCDUM1	1	I/O	Open	Test pins. Leave them open.
IOGNDDUM1~3	3	I/O	Open	Test pins. Leave them open.
AGNDDUM1~5	5	I/O	Open	Test pins. Fix to VREFC, VDDTEST.
DUMMYR1~10	10	I/O	Open	Test pins. Leave them open. SPFD5420A use these pins to do self-test. No any signal on panel can cross these pins, otherwise function fail.
VGLDMY1~4	4	I/O	Open	Test pins. Leave them open.
TESTO1~18	18	I/O	Open	Test pins. Leave them open.
TEST1~3	3	I	IOGND	Test pins. Connect to IOGND.

6. INSTRUCTIONS

6.1. Outline

The SPFD5420A supports 18-bit data bus interface to access command register to configure system. When the command register accessing is desired, sending the command information to specify which index register would be accessed and following the data to that control register. Moreover, register accessing operation should cooperate with RS, /WR, /RD signal for SPFD5420A to recognize the control instruction. And command instruction can be accomplished by using all system interfaces (18-bit, 16-bit, 9-bit, 8-bit 80 system and SPI). The corresponding pin assignment of different system interface are shown in **Figure 6-1** to **Figure 6-6**

The instruction can be categorized into 8 groups. And the 8 groups are:

1. Specify the index of register
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal GRAM address
7. Transfer data to and from the internal GRAM
8. Internal grayscale γ-correction

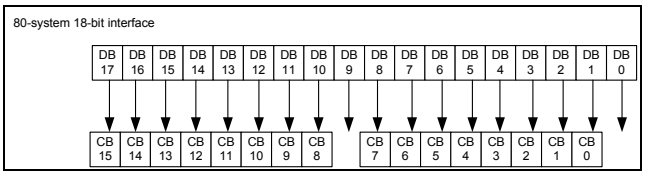


Figure 6-1

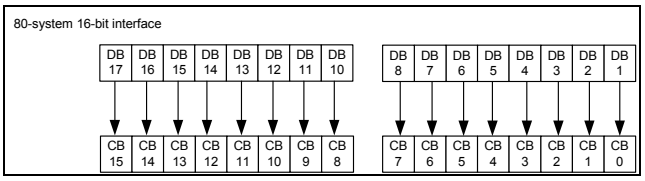


Figure 6-2

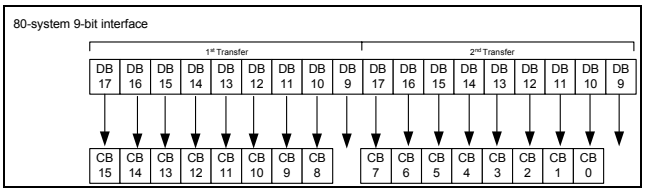


Figure 6-3

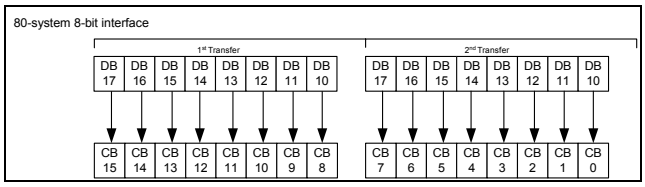


Figure 6-4

Serial interface Data Format

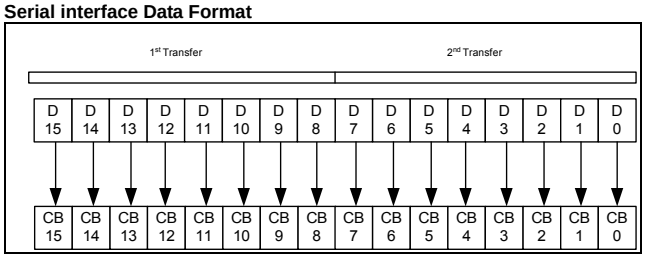


Figure 6-5

Serial interface Data Transfer Format

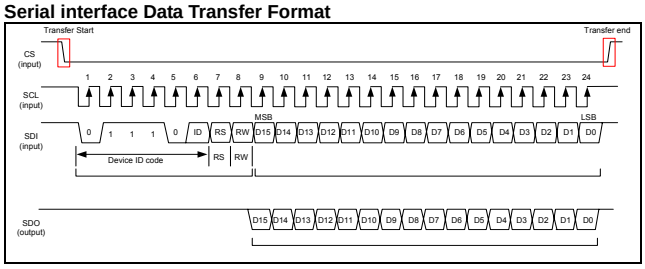


Figure 6-6

6.2. Instruction

Table 6-1 Instruction List Table

Register No	Register	Upper 8-bit								Lower 8-bit							
		CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
000h	ID Read	0	1	0	1	0	1	0	0	0	0	1	0	0	0	0	0
001h	Driver Output Control	0	0	0	0	0	SM (0)	0	SS (0)	0	0	0	0	0	0	0	0
002h	LCD Drive Waveform Control	0	0	0	0	0	0	0	B/C (0)	0	0	0	0	0	0	NW1 (0)	NW0 (0)
003h	Entry Mode	TRIREG (0)	DFM (0)	0	BGR (0)	0	0	HWM (0)	0	ORG (0)	0	I/D1 (1)	I/D0 (1)	AM (0)	0	EPF1 (0)	EPF0 (0)
004h-006h	Setting disabled																
007h	Display Control (1)	0	0	PTDE1 (0)	PTDE0 (0)	0	0	0	BASEE (0)	0	VON (0)	GON (0)	DTE (0)	0	0	D1 (0)	D0 (0)
008h	Display Control (2)	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)
009h	Low Power Control (1)	0	0	0	0	PTV (0)	PTS2 (0)	PTS1 (0)	PTS0 (0)	0	0	PTG1 (0)	PTG0 (0)	ISC3 (0)	ISC2 (0)	ISC1 (0)	ISC0 (0)
00Ah	Setting Disabled																
00Bh	Low Power Control (2)	0	0	0	0	0	0	0	0	0	0	0	VEM0 (0)	0	0	0	COL (0)
0Ch	External Display Controll (1)	0	ENC2 (0)	ENC1 (0)	ENC0 (0)	0	0	0	RM (0)	0	0	DM1 (0)	DM0 (0)	0	0	RIM1 (0)	RIM0 (0)
00Dh-00Eh	Setting Disabled																
00Fh	External Display Controll (2)	0	0	0	0	0	0	0	0	0	0	0	VSPL (0)	HSPL (0)	0	EPL (0)	DPL (0)
010h	Panel interface Control 1	0	0	0	0	0	0	DIVI1 (0)	DIVI0 (0)	0	0	0	RTNI4 (1)	RTNI3 (0)	RTNI2 (1)	RTNI1 (1)	RTNI0 (1)
011h	Panel interface Control 2	0	0	0	0	0	NOWI2 (0)	NOWI1 (0)	NOWI0 (0)	0	0	0	0	0	SDTI2 (0)	SDTI1 (0)	SDTI0 (0)
012h	Panel interface Control 3	0	0	0	0	0	0	VEQW11 (0)	VEQW10 (0)	0	0	0	0	0	0	0	0
013-01Fh	Setting Disabled																
020h	Panel Interface Control 4	0	0	0	0	0	0	DIVE1 (0)	DIVE0 (0)	0	RTNE6 (0)	RTNE5 (0)	RTNE4 (1)	RTNE3 (1)	RTNE2 (1)	RTNE1 (1)	RTNE0 (0)
021h	Panel Interface Control 5	0	0	0	0	NOWE3 (0)	NOWE2 (0)	NOWE1 (0)	NOWE0 (0)	0	0	0	0	SDTE3 (0)	SDTE2 (0)	SDTE1 (0)	SDTE0 (0)
022h	Panel Interface Control 6	0	0	0	0	0	VEQWE2 (0)	VEQWE1 (0)	VEQWE0 (0)	0	0	0	0	0	0	0	0
023h-08Fh	Setting Disabled																
090h	Frame Marker Control	FMI3 (0)	FMI2 (0)	FMI1 (0)	FMI0 (0)	0	0	0	FMP8 (0)	FMP7 (0)	FMP6 (0)	FMP5 (0)	FMP4 (0)	FMP3 (0)	FMP2 (0)	FMP1 (0)	FMP0 (0)
091h-0FFh	Setting disabled																
100h	Power Control (1)	0	0	0	SAP (0)	0	BT2 (0)	BT1 (0)	BT0 (0)	APE (0)	0	AP1 (0)	AP0 (0)	0	DSTB (0)	SLP (0)	0
101h	Power Control (2)	0	0	0	0	0	DC12 (0)	DC11 (0)	DC10 (0)	0	DC02 (0)	DC01 (0)	DC00 (0)	0	VC2 (0)	VC1 (0)	VC0 (0)
102h	Power Control (3)	0	0	0	0	0	0	0	VCMR0 (0)	VREG1R (0)	0	PSON (0)	PON (0)	VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)
103h	Power Control (4)	0	0	VCOMG (0)	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	0	0	0	0	0	0	0	0
104h-106h	Setting disabled																
107h	Power Control (5)	0	0	0	0	0	0	0	0	0	0	0	DCM0 (0)	DCT3 (0)	DCT2 (0)	DCT1 (0)	DCT0 (0)
108-10Fh	Setting disabled																
110h	Power Control(6)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PSE (0)
111-1ffh	Setting disabled																
200h	GRAM address Set Horizontal Address	0	0	0	0	0	0	0	0	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)
201h	GRAM address Set Vertical Address	0	0	0	0	0	0	0	AD16 (0)	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)
202h	Write Data to GRAM Read Data from GRAM	Data format is varied according to “interface”.															
203-20Fh	Setting disabled																
210h	Window Horzontal RAM Address Start	0	0	0	0	0	0	0	0	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)
211h	Window Horzontal RAM Address End	0	0	0	0	0	0	0	0	HEA7 (1)	HEA6 (1)	HEA5 (1)	HEA4 (0)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)
212h	Window Vertical RAM Address Start	0	0	0	0	0	0	0	VSA8 (0)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)
213h	Window Vertical RAM Address End	0	0	0	0	0	0	0	VEA8 (1)	VEA7 (0)	VEA6 (0)	VEA5 (1)	VEA4 (1)	VEA3 (1)	VEA2 (1)	VEA1 (1)	VEA0 (1)
214-27Fh	Setting Disabled																
280h	NVM Write/Read	0	0	0	0	0	0	0	0	0	0	0	0	UID3 (0)	UID2 (0)	UID1 (0)	UID0 (0)
281h	VCom high voltage 1	0	0	0	0	0	0	0	0	0	0	0	VCM14 (0)	VCM13 (0)	VCM12 (0)	VCM11 (0)	VCM10 (0)
282h	VCom high voltage 2	0	0	0	0	0	0	0	0	VCMSEL (0)	0	0	VCM24 (0)	VCM23 (0)	VCM22 (0)	VCM21 (0)	VCM20 (0)
283-2FFh	Setting disabled																
300h	γ Control (1)																
301h	γ Control (2)																

302h	γ Control (3)																
303h	γ Control (4)																
304h	γ Control (5)																
305h	γ Control (6)																
306h	γ Control (7)																
307h	γ Control (8)																
308h	γ Control (9)																
309h	γ Control (10)																
30Ah	γ Control (11)																
30Bh	γ Control (12)																
30Ch	γ Control (13)																
30Dh	γ Control (14)																
30Eh	γ Control (15)																
30Fh	γ Control (16)																
310-3FFh	Setting disabled																
400h	Size of base image	GS (0)	0	NL5 (0)	NL4 (0)	NL3 (0)	NL2 (0)	NL1 (0)	NL0 (0)	0	0	SCN5 (0)	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)
401h	Base image display control	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL (0)	VLE (0)	REV (0)
402-403h	Setting disabled																
404h	Vertical Scoll Control	0	0	0	0	0	0	0	VL8 (0)	VL7 (0)	VL6 (0)	VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	VL0 (0)
405-4FFh	Setting disabled																
500h	Display Position - Partial Display 1	0	0	0	0	0	0	0	PTDP08 (0)	PTDP07 (0)	PTDP06 (0)	PTDP05 (0)	PTDP04 (0)	PTDP03 (0)	PTDP02 (0)	PTDP01 (0)	PTDP00 (0)
501h	RAM Address Start - Partial Display 1	0	0	0	0	0	0	0	PTSA08 (0)	PTSA07 (0)	PTSA06 (0)	PTSA05 (0)	PTSA04 (0)	PTSA03 (0)	PTSA02 (0)	PTSA01 (0)	PTSA00 (0)
502h	RAM Address End - Partial Display 1	0	0	0	0	0	0	0	PTEA08 (0)	PTEA07 (0)	PTEA06 (0)	PTEA05 (0)	PTEA04 (0)	PTEA03 (0)	PTEA02 (0)	PTEA01 (0)	PTEA00 (0)
503h	Display Position - Partial Display 2	0	0	0	0	0	0	0	PTDP18 (0)	PTDP17 (0)	PTDP16 (0)	PTDP15 (0)	PTDP14 (0)	PTDP13 (0)	PTDP12 (0)	PTDP11 (0)	PTDP10 (0)
504h	RAM Address Start - Partial Display 2	0	0	0	0	0	0	0	PTSA18 (0)	PTSA17 (0)	PTSA16 (0)	PTSA15 (0)	PTSA14 (0)	PTSA13 (0)	PTSA12 (0)	PTSA11 (0)	PTSA10 (0)
505h	RAM Address End - Partial Display 2	0	0	0	0	0	0	0	PTEA18 (0)	PTEA17 (0)	PTEA16 (0)	PTEA15 (0)	PTEA14 (0)	PTEA13 (0)	PTEA12 (0)	PTEA11 (0)	PTEA10 (0)
506-605h	Setting Disabled																
606h	i80-I/F Endian Control	0	0	0	0	0	0	0	TCREV1 (0)	0	0	0	0	0	0	0	TCREV0 (0)
607-6EFh	Setting disabled																
6F0h	NVM access control	0	0	0	0	0	0	0	0	TE (0)	0	EOP1 (0)	EOP0 (0)	0	0	EAD1 (0)	EAD0 (0)
6F1-FFFh	Setting disabled																

The following are detailed explanations of instructions with illustrations of instruction bits (CB15-0) assigned to each interface.

6.2.1. Index Register (IR)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	0	0	0	0	0	0	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the index (R000h ~ RFFFh) of a control register.

6.2.2. ID Read Register (R000h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R	0	0	1	0	1	0	1	0	0	0	0	1	0	0	0	0	0

The IC code of SPFD5420A can be accessed by read operation. ‘5408H can be read out when read ID operation is exectued.

6.2.3. Driver Output Control Register (R001h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	SM(0)	0	SS(0)	0	0	0	0	0	0	0	0

SS: Shift direction of the source driver output selection.

When SS = "0", source driver shifts from S1 to S720. When SS = "1", source driver shifts from S720 to S1. Moreover, SS can cooperate with BGR for different color filter configuration of LCD panel. The combination of SS and BGR bit are summarized at **Table 6-2.**

Table 6-2

SS=0;BGR=0;	S1	S2	S3	····▶	S718	S719	S720
SS=0;BGR=1;	S1	S2	S3	····▶	S718	S719	S720
SS=1,BGR=0;	S1	S2	S3	◀····	S718	S719	S720
SS=1,BGR=1;	S1	S2	S3	◀····	S718	S719	S720

SM: Set the scan mode of the gate driver output. Moreover, SM can cooperate with GS for different LCD panel gate line layout. The combination of GS and SM bit are summarized at **Table 6-3**.

Table 6-3

SM	GS	Shift Direction (begin,…..,end)
0	0	G1, G2, G3, G4……G429, G430, G431, G432
0	1	G432, G431, G430, G429……G4, G3, G2, G1
1	0	G1, G3, G5, …G429, G431, …G2, G4,... G430, G432
1	1	G432, G430, G428,..G4, G2, ..G429, G431,...G3, G1

6.2.4. LCD Driving Waveform Control (R002h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	1	B/C(0)	0	0	0	0	0	0	0	NW1(0)	NW0(0)

NW1-NW0: SPFD5420A provides 1-line inversion for Vcom.

B/C: This bit .is to set the Vcom toggle at frame rate format of N-line inversion format.

B/C=0: Frame inversion.

B/C=1: 1-line inversion.

6.2.5. Entry Mode (R003h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	TRI REG(0)	DFM (0)	0	BGR (0)	0	0	HWM (0)	0	ORG (0)	0	I/D1 (1)	I/D0 (1)	AM (0)	0	EPF1 (0)	EPF0 (0)

Table 6-4

Operation mode	ORG	AM	I/D1	I/D0	Function
Mode 1	0	0	0	0	Replace horizontal data
Mode2	0	1	0	1	Replace vertical data
Mode3	1	0	1	0	Conditionally replace horizontal data
Mode4	1	1	1	1	Conditionally replace vertical data

AM: To set the update direction when writing data to GRAM. If AM=1, data will write in vertical direction. If AM=0, data will write in horizontal direction. Moreover, if a fixed window GRAM accessing is desired, the writing direction can be set by I/D1-0 and AM bits.

I/D1-0: To specify address counter increment /decrement automatically function while GRAM is accessing. I/D[0] indicates the increment or decrement in horizontal direction. I/D[1] indicates the increment or decrement in vertical direction.

I/D[0]=0: decrement in horizontal direction automatically

I/D[0]=1: increment in horizontal direction automatically

I/D[1]=0: decrement in vertical direction automatically

I/D[1]=1: increment in vertical direction automatically

ID[1-0] setting can cooperate with AM bit to set the data updating direction.

ORG: SPFD5420A provides the option of start address definition when window function is selected.

ORG=1: RAM address setting should set to (00000h) no matter where the window start address is. In this case, the window start postion is treated as (00000h), regardless the physical location in GRAM.

ORG=0: RAM address setting should set to the address.

HWM: SPFD5420A provides a high speed GRAM accessing mode that updated GRAM data in 1-line unit. Be aware that data can be written to GRAM only if accessing GRAM operation is halted after writing enough data for 1-line. Make sure the AM is set to “0”, when HWM function is set to “1”.

BGR: To set the order of RGB dot location in GRAM.

BGR=0: same assignment of RGB allocation of DB17-0

BGR=1: inverse assignment of RGB allocation of DB17-0

DFM: In combination with TRIREG setting to set the different data transfer mode.

TRIREG: to set 1–3 time transfer mode for system interface. TRIREG bit should cooperate with DFM to meet the specific transfer mode.

For 8-bit databus interface mode:

TRIREG=0: 2 time transfer mode for 16-bit GRAM data.

TRIREG=1: 3 time transfer mode for 18-bit GRAM data

For 16-bit databus interface mode:

TRIREG=0: 1 time transfer mode for 16-bit GRAM data.

TRIREG=1: 2 time transfer mode for 18-bit GRAM data

Note: Set TRIREG=0, when using neither 8-bit nor 16-bit.

EPF1-0: To select the algorithm of expanding 8/16 bits to 18 bits. This setting is valid only when 16-bit or 8-bit interfaces are in use.

6.2.6. Display Control 1 (R007h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	PTDE1 (0)	PTDE0 (0)	0	0	0	BASEE (0)	0	VON (0)	GON (0)	DTE (0)	0	0	D1 (0)	D0 (0)

D1-0: To set the internal operation, source driver output and VCOM output function. When D1-0=00; SPFD5420A is set to standby mode. The combination of D1-0 and BASEE bit is summarized at **Table 6-5**.

Table 6-5

D1	D0	BASEE	Source, VCOM output	Internal Operation	FLM
0	0	*	GND	Terminated	OFF
0	1	*	GND	Normal Operation	ON
1	0	*	Non-lit display	Normal Operation	ON
1	1	0	Non-lit display	Normal Operation	ON
		1	Normal display	Normal Operation	ON

DTE, GON: Specify the high/low level of gate driver output signal. The combination of DTE and GON bit is summarized at **Table 6-6**.

Table 6-6

APE	GON	DTE	Gate Output
0	*	*	VGL(=GND)
1	0	0	VGH
	0	1	VGH
	1	0	VGL
	1	1	VGH/VGL

VON: To Control VCOM output signal. The combination of APE, AP[1:0] , VON and VCOMG bit is summarized at **Table 6-7.**

Table 6-7

APE	AP [1:0]	VON	VCOMG	VCOM Output
0	*	*	*	GND
1	00	0	0	GND
	00	1	0-1	Setting Disabled
	00	0	1	Setting Disabled
	01-11	0	0	GND
	01-11	0	1	VCOML
	01-11	1	0	VCOMH/GND
	01-11	1	1	VCOMH/VCOML

BASEE: To enable Base image display

BASEE	
0	(1) Non-lit display (2) Partial image display
1	Base image is display on the LCD

PTDE1-0: To set the partial-display enables function.

PTDE [0]: “0” Partial image 1 display “Off”.
“1” Partial image 1 display “On”.

PTDE [1]: “0” Partial image 2 display “Off”.
“1” Partial image 2 display “On”.

6.2.7. Display Control 2 (R008h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)

FP3-0: Set the amount of blank period of front porch

BP3-0: Set the amount of blank period of back porch

Table 6-8 summarized the function of FP3-0/BP3-0 setting. When setting this register, make sure that:

BP + FP ≤ 16 lines

FP ≥ 2 lines

BP ≥ 2 lines

In external display interface mode, a back porch (BP) period starts on the falling edge of the VSYNC signal, followed by a display operation period. After driving the number of lines set with NL bits, a front porch period starts. After the front porch period, a blank period continues until the next input of VSYNC signal. Be aware that different interface mode, has different BP/ FP setting. **Table 6-9** summarized the setting for each interface mode.

Table 6-8

FP3	FP2	FP1	FP0	Number of lines for the Front Porch
BP3	BP2	BP1	BP0	Number of lines for the Back Porch
0	0	0	0	Setting disabled
0	0	0	1	Setting disabled
0	0	1	0	2 lines
0	0	1	1	3 lines
0	1	0	0	4 lines
0	1	0	1	5 lines
0	1	1	0	6 lines
0	1	1	1	7 lines
1	0	0	0	8 lines
1	0	0	1	9 lines
1	0	1	0	10 lines
1	0	1	1	11 lines
1	1	0	0	12 lines
1	1	0	1	13 lines
1	1	1	0	14 lines
1	1	1	1	Setting disabled

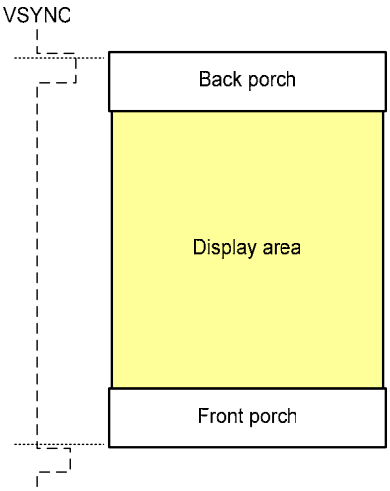


Figure 6-7 Front porch and back porch function diagram

Table 6-9

Operation of Internal clock	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP ≤ 16 lines
RGB interface	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP ≤ 16 lines
VSYNC interface	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP = 16 lines

6.2.8. Display Control 3 (R009h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	PTV (0)	PTS2 (0)	PTS1 (0)	PTS0 (0)	0	0	PTG1 (0)	PTG0 (0)	ISC3 (0)	ISC2 (0)	ISC1 (0)	ISC0 (0)

ISC3-0: To set the gate driver scan cycle in non-display area. **Table 6-10** summarized the function of ISC3-0 setting

Table 6-10

ISC3	ISC2	ISC1	ISC0	Scan cycle	fFLM=60Hz
0	0	0	0	Setting disable	
0	0	0	1	3frames	50 ms
0	0	1	0	5 frames	84 ms
0	0	1	1	7 frames	117 ms
0	1	0	0	9 frames	150 ms
0	1	0	1	11 frames	184 ms
0	1	1	0	13 frames	217 ms
0	1	1	1	15 frames	251 ms
1000-1111				Setting Disabled	

PTG1-0: To set the gate driver scan mode in non-display area. **Table 6-11** summarized the function of PTG1-0 setting

Table 6-11

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	VCOM output
0	0	Normal scan	Based on the PTS2-0 bits setting	VCOMH/VCOML
0	1	Setting Disable		
1	0	Interval scan	Based on the PTS2-0 bits setting	VCOMH/VCOML
1	1	Setting Disable		

PTS2-0: To set the source driver output level in non-display area of partial display mode. **Table 6-12** summarized the function of PTS2-0 setting.

Table 6-12

PTS2	PTS1	PTS0	Source output in non-display area		Operation amplifier in non-display area
			+ve polarity	-ve polarity	
0	0	0	V31	V0	V0-V31
001-011			Setting inhibited		
1	0	0	V31	V0	V0-V31
101-111			Setting inhibited		

PTV: To set VCOM output in non-display area, Vcom operates normally when PTV = 1, and stops operation when PTV = 0.

6.2.9. Low Power Control (R00Bh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VEM0 (0)	0	0	0	COL (0)

COL:

COL = 0: 262,144 colors

COL = 1: 8 colors.

In 8-color mode, the source output is either connected to VREGIOUT or GND.

VEM0: VEM0 = 1, when VCOM is switched from VCOMH to VCOML, it will dropped to GND level in the intermediate stage.

6.2.10. External Display Interface Control 1 (R00Ch)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	ENC2 (0)	ENC1 (0)	ENC0 (0)	0	0	0	RM (0)	0	0	DM1 (0)	DM0 (0)	0	0	RIM1 (0)	RIM0 (0)

RIM1-0: To set the different transfer modes of RGB interface.

Table 6-13 summarized the function of RIM1-0 setting.

Table 6-13

RIM1	RIM0	RGB Interface Mode	Colors	Data Bus
0	0	18-bit RGB interface (one transfer/pixel)	262K	DB 17-0
0	1	16-bit RGB interface (one transfer/pixel)	65K	DB 17-13; DB 11-1
1	0	6-bit RGB interface (three transfers/pixel)	262K	DB17-12
1	1	Setting disabled	-	-

DM1-0: To specify the display interface mode.

Table 6-14summarized the function of DM1-0 setting.

Table 6-14

DM1	DM0	Display Interface
0	0	Internal clock operation
0	1	RGB interface
1	0	VSYNC interface
1	1	Setting disabled

RM: Select the interface to access the SPFD5420A's internal GRAM. The setting of RM should be consistent with DM1-0. **Table 6-15** summarized the function of RM bit setting.

Table 6-15

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

ENC2-0: Set the RAM data write cycle in RGB interface mode. **Table 6-16** summarized the function of ENC2-0 setting.

Table 6-16

ECN2	ECN1	ECN0	RAM data write cycle
0	0	0	1 frame
0	0	1	2 frames
0	1	0	3 frames
0	1	1	4 frames
1	0	0	5 frames
1	0	1	6 frames
1	1	0	7 frames
1	1	1	8 frames

6.2.11. External Display Interface Control 2 (R00Fh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL (0)	HSPL (0)	0	EPL (0)	DPL (0)

DPL: Select the data latch edge of the DOTCLK signal in RGB interface mode.
DPL = ”0”: rising edge of the DOTCLK.
DPL =”1”: falling edge of the DOTCLK.

HSPL: The polarity of HSYNC signal selection in RGB interface mode.
HSPL = ”0”: Low active.
HSPL = ”1”: High active.

EPL: The polarity of ENABLE signal selection in RGB interface mode.
EPL = “0”: ENABLE: Low active
EPL = ”1”: ENABLE: High active

VSPL: The polarity of VSYNC signal selection in RGB interface mode.
VSPL = ”0”: Low active.
VSPL = ”1”: High active.

6.2.12. Panel Interface Control 1 (R010h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	DIVI1 (0)	DIVI0 (0)	0	0	0	RTNI4 (1)	RTNI3 (0)	RTNI2 (1)	RTNI1 (1)	RTNI0 (1)

RTNI4-0: Set the clock cycle per line **Table 6-17** summarized the function of RTNI4-0 setting.

Table 6-17

RTNI4	RTNI3	RTNI2	RTNI1	RTNI0	Clock Cycles per line
0	0	0	0	0	Setting disable
Setting disable					
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks

DIVI1-0: To specified the division ratio of internal operation clock frequency. Set the RTN and DIVI bits to adjust frame frequency. Be aware of that if the number of lines for driving liquid crystal is changed, the frame frequency must also be adjusted. Moreover, In RGB interface mode, the DIVI1-0 bits are disabled. **Table 6-18** summarized the function of DIVI1-0 setting.

Table 6-18

DIVI1	DIVI0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

fosc =Frequency of RC oscillation

Formula to calculate frame frequency

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Clock cycles per line} \times \text{division ratio} \times (\text{Line} + \text{BP} + \text{FP})} \quad [\text{Hz}]$$

fosc: frequency of RC oscillation

Line: number of lines for driving liquid crystal (NL bits)

Division ratio: DIVI bits

Clock cycles per line: RTNI bits

FP: the number of lines for the front porch period

BP: the number of lines for the back porch period

6.2.13. Panel Interface Control 2 (R011h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	NOWI2 (0)	NOWI1 (0)	NOWI0 (0)	0	0	0	0	0	SDTI2 (0)	SDTI1 (0)	SDTI0 (0)

NOWI [2:0]: Set the adjacent gate driver output non-overlap period. **Table 6-19** summarized the function of NOWI2-0 setting.

Table 6-19

NOWI2	NOWI1	NOWI0	Gate output non-overlap period Internal Operation (reference clock: internal oscillator)
0	0	0	0 clock
0	0	1	1 clocks
0	1	0	2 clocks
0	1	1	3 clocks
1	0	0	4 clocks
1	0	1	5 clocks
1	1	0	6 clocks
1	1	1	7 clocks

SDTI2-0: Set the delay of source output in every line.

Table 6-20

SDTI2	SDTI1	SDTI0	Source output delay period Internal Operation (reference clock: internal oscillator)
0	0	0	0 clock
0	0	1	1 clocks
0	1	0	2 clocks
0	1	1	3 clocks
1	0	0	4 clocks
1	0	1	5 clocks
1	1	0	6 clocks
1	1	1	7 clocks

6.2.14. Panel Interface control 3 (R012h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	VEQW1 (0)	VEQW0 (0)	0	0	0	0	0	0	0	0	0

VEQWI[1:0]: Set VCOM equalize period.

Table 6-21

VEQWI1	VEQWI0	VCOM Equalize Period
0	0	0 clock
0	1	1 clock
1	0	2 clocks
1	1	3 clocks

6.2.15. Panel Interface control 4 (R020h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	DIVE1 (1)	DIVE0 (0)	0	RTNE6 (0)	RTNE5 (0)	RTNE4 (1)	RTNE3 (1)	RTNE2 (1)	RTNE1 (1)	RTNE0 (0)

RTNE6-0: Set the clock cycle per line **Table 6-22** summarized the function of RTNE5-0 setting.

Table 6-22

RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0	Clock Cycles per line
0	0	0	0	0	0	Setting disable
Setting disable						
0	1	0	0	0	0	16 clocks
0	1	0	0	0	1	17 clocks
0	1	0	0	1	0	18 clocks
0	1	0	0	1	1	19 clocks
0	1	0	1	0	0	20 clocks
0	1	0	1	0	1	21 clocks
0	1	0	1	1	0	22 clocks
0	1	0	1	1	1	23 clocks
0	1	1	0	0	0	24 clocks
0	1	1	0	0	1	25 clocks
0	1	1	0	1	0	26 clocks
0	1	1	0	1	1	27 clocks
0	1	1	1	0	0	28 clocks
0	1	1	1	0	1	29 clocks
0	1	1	1	1	0	30 clocks
0	1	1	1	1	1	31 clocks
1	1	0	0	0	0	32 clocks
1	1	0	0	0	1	33 clocks
1	1	0	0	1	0	34 clocks

RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0	Clock Cycles per line
1	1	0	0	1	1	35 clocks
1	1	0	1	0	0	36 clocks
1	1	0	1	0	1	37 clocks
1	1	0	1	1	0	38 clocks
1	1	0	1	1	1	39 clocks
1	1	1	0	0	0	40 clocks
1	1	1	0	0	1	41 clocks
1	1	1	0	1	0	42 clocks
1	1	1	0	1	1	43 clocks
1	1	1	1	0	0	44 clocks
1	1	1	1	0	1	45 clocks
1	1	1	1	1	0	46 clocks
1	1	1	1	1	1	47 clocks
1	1	0	0	0	0	48 clocks
1	1	0	0	0	1	49 clocks
1	1	0	0	1	0	50 clocks
1	1	0	0	1	1	51 clocks
1	1	0	1	0	0	52 clocks
1	1	0	1	0	1	53 clocks
1	1	0	1	1	0	54 clocks
1	1	0	1	1	1	55 clocks
1	1	1	0	0	0	56 clocks
1	1	1	0	0	1	57 clocks
1	1	1	0	1	0	58 clocks
1	1	1	0	1	1	59 clocks
1	1	1	1	0	0	60 clocks
1	1	1	1	0	1	61 clocks
1	1	1	1	1	0	62 clocks
1	1	1	1	1	1	63 clocks

DIVE1-0: To specified the division ratio of internal operation clock frequency. Set the RTNE and DIVE bits to adjust frame frequency. Be aware of that if the number of lines for driving liquid crystal is changed, the frame frequency must also be adjusted. Moreover, In RGB interface mode, the DIVE1-0 bits are disabled. **Table 6-23** summarized the function of DIVE1-0 setting.

Table 6-23

DIVE1	DIVE0	Division Ratio	Internal Operation Clock Frequency (16 bit, one time transfer)	Internal Operation Clock Frequency(8 bit, three time transfer)
0	0	Setting disable		
0	1	4	fosc / 4	fosc / 12
1	0	8	fosc / 8	fosc / 24
1	1	16	fosc / 16	fosc / 48

fosc =Frequency of RC oscillation

6.2.16. Panel Interface Control 5 (021Rh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	NOWE3(0)	NOWE2(0)	NOWE1(0)	NOWE0(0)	0	0	0	0	SDTE3(0)	SDTE2(0)	SDTE1(0)	SDTE0(0)

NOWE [3:0]: Set the adjacent gate driver output non-overlap period in RGB interface. **Table 6-24** summarized the function of NOWE3-0 setting.

Table 6-24

NOWE3	NOWE2	NOWE1	NOWE0	Gate output non-overlap period Internal Operation (reference clock: internal oscillator)
0	0	0	0	0 clock
0	0	0	1	1 clocks
0	0	1	0	2 clocks
0	0	1	1	3 clocks
0	1	0	0	4 clocks
0	1	0	1	5 clocks
0	1	1	0	6 clocks
0	1	1	1	7 clocks
1	0	0	0	8 clocks
1	0	0	1	9 clocks
1	0	1	0	10 clocks
1	0	1	1	11 clocks
1	1	0	0	12 clocks
1	1	0	1	13 clocks
1	1	1	0	14 clocks
1	1	1	1	15 clocks

SDTE: Set the source output delay in RGB interface.

Table 6-25

SDTE3	SDTE 2	SDTE 1	SDTE 0	Source output period Internal Operation (reference clock: internal oscillator)
0	0	0	0	0 clock
0	0	0	1	1 clocks
0	0	1	0	2 clocks
0	0	1	1	3 clocks
0	1	0	0	4 clocks
0	1	0	1	5 clocks
0	1	1	0	6 clocks
0	1	1	1	7 clocks
1	0	0	0	8 clocks
1	0	0	1	9 clocks
1	0	1	0	10 clocks
1	0	1	1	11 clocks
1	1	0	0	12 clocks

1	1	0	1	13 clocks
1	1	1	0	14 clocks
1	1	1	1	15 clocks

6.2.17. Panel Interface Control 6 (R022h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	VEQ WE2(0)	VEQ WE1(0)	VEQ WE0(0)	0	0	0	0	0	0	0	0

VEQWE2-0: To set the drive period of low power VCOM, which is valid when the operation is synchronized with RGB interface signals.

Table 6-26

VEQWE2	VEQWE1	VEQWE0	Source Output Delay Perios
0	0	0	0 clock
0	0	1	1 clocks
0	1	0	2 clocks
0	1	1	3 clocks
1	0	0	4 clocks
1	0	1	5 clocks
1	1	0	6 clocks
1	1	1	7 clocks

6.2.18. Frame Marker Control (R090h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	FMI2 (0)	FMI1 (0)	FMI0 (0)	0	0	0	FMP8 (0)	FMP7 (0)	FMP6 (0)	FMP5 (0)	FMP4 (0)	FMP3 (0)	FMP2 (0)	FMP1 (0)	FMP0 (0)

FMP8-0: Set the position of the frame marker. 0 ≤ FMP ≤ BP + NL + FP

Table 6-27

FMP8-0	Frame Marker Position
000000000	**0**
000000001	**1**
000000010	**2**
000000011	**3**
…	**…**
110111100	**444**
110111101	**445**
110111110	**446**
110111111	**447**

FMI2-0: Set the period of the Frame Marker.

Table 6-28

FMI2	FMI1	FMI0	Period of FMARK
0	0	0	1 frame
0	1	1	2 frames
1	0	1	4 frames
1	1	1	6 frames

6.2.19. Power Control 1 (R100h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	SAP (0)	0	BT2 (0)	BT1 (0)	BT0 (0)	APE (0)	0	AP1 (0)	AP0 (0)	0	DSTB (0)	SLP (0)	0

SLP: Sleep mode selection. When SLP =1, SPFD5420A set to sleep mode. In sleep mode, all internal operations are terminated except internal RC oscillation. Be sure that a display off sequence should be executed before set SLP to "1". In sleep mode, no instruction can be accepted. Set STB=0 can exit sleep mode. Moreover, when exit from sleep mode, data in GRAM and in instruction registers are remained unchanged.

DSTB: Deep Standby mode selection. When DSTB =1, SPFD5420A set to deep standby mode. In this mode, all internal operations are terminated including internal RC oscillation. Be sure that a display off sequence should be executed before set DSTB to "1". Set DSTB=0 can exit standby mode. Be sure that start oscillation following by 10ms delay should be executed before set DSTB to "0". Moreover, when exit from deep standby mode, data in GRAM and register would be lost, reset and re-sending command and data into GRAM are necessary.

AP1-0: Operational amplifier DC bias current adjustment. Set AP1-0 = "00" to stop operational amplifier and DC/DC charge pump circuits to reduce current consumption during non display period. **Table 6-29** summarized the function of AP1-0 setting. Please note that the values listed in the table are the ratios of the currents of the corresponding settings to the current at the max rank.

Table 6-29

AP1	AP0	Constant current in power supply circuit	Constant current in Gamma circuit
0	0	Halt	Halt
0	1	0.5	0.62
1	0	0.75	0.71
1	1	1	1

APE: Enable bit for both liquid crystal power supply and gamma voltage generation circuit.

APE="0", Halt liquid crystal power supply and gamma voltage generation circuit

APE="1", Enable liquid crystal power supply and gamma voltage generation circuit.

BT3-0: Set the voltage level of DDVDH, VGH, VGL and VCL.

Table 6-30 summarized the function of BT2-0 setting

BT2	BT1	BT0	DDVDH	VGH	VGL	VCL	Capacitor connection pins
0	0	0	VCI1 x 2 [VCI1x2]	DDVDH x 3 [VCI1 x 6]	-(VCI1+DDVDHx 2) [VCI1x -5]	-VCI1 [VCI1x-1]	C23 can be eliminated
0	0	1	Setting Disabled	Setting Disabled	Setting Disabled	Setting Disabled	Setting Disabled
0	1	0	Setting Disabled	Setting Disabled	Setting Disabled	Setting Disabled	Setting Disabled
0	1	1	VCI1 x 2 [x2]	DDVDH x 3 + VCI1 [VCI1 x 7]	-(VCI1+DDVDHx 2) [VCI1x -5]	-VCI1	
1	0	0	VCI1 x 2 [x2]	DDVDH x 3 + VCI1 [VCI1 x 7]	-(DDVDHx 2) [VCI1x -4]	-VCI1	
1	0	1	VCI1 x 2 [x2]	DDVDH x 3 + VCI1 [VCI1 x 7]	-(VCI1+DDVDH) [VCI1x -3]	-VCI1	
1	1	0	VCI1 x 2 [x2]	DDVDH x 3 [VCI1 x 6]	-(DDVDHx 2) [VCI1x -4]	-VCI1	C23 can be eliminated
1	1	1	VCI1 x 2 [x2]	DDVDH x 3 [VCI1 x 6]	-(VCI1+DDVDH) [VCI1x -3]	-VCI1	C23 can be eliminated

SAP: Enable bit for gamma voltage generation circuit.

SAP="0", Halt gamma voltage generation circuit.

SAP="1", Enable gamma voltage generation circuit.

6.2.20. Power Control 2 (R101h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	DC12 (1)	DC11 (1)	DC10 (0)	0	DC02 (1)	DC01 (1)	DC00 (0)	0	VC2 (0)	VC1 (0)	VC0 (0)

VC2-0: Set the voltage of VCIOUT. VCIOUT is generated by VCILVL. **Table 6-31** summarized the function of VC2-0 setting

Table 6-31

VC2	VC1	VC0	VCIOUT
0	0	0	0.94 x VCILVL
0	0	1	0.89 x VCILVL
0	1	0	Setting Disable
0	1	1	Setting Disable
1	0	0	0.76 x VCILVL
1	0	1	Setting Disable
1	1	0	Setting Disable
1	1	1	1.00 x VCILVL

DC02-00: Set DC/DC charge pump circuit 1 operating frequency. **Table 6-32** summarized the function of DC02-00 setting

Table 6-32

DC02	DC01	DC00	DC/DC charge pump circuit 1 frequency (fDCDC1)
0	0	0	Oscillation clock
0	0	1	Oscillation clock / 2
0	1	0	Oscillation clock / 4
0	1	1	Oscillation clock / 8
1	0	0	Oscillation clock / 16
1	0	1	Invalid Setting
1	1	0	Halt Step-up Circuit 1
1	1	1	Invalid Setting

DC12-10: Set DC/DC charge pump circuit 2 operating frequency. **Table 6-33** summarized the function of DC02-00 setting

Table 6-33

DC12	DC11	DC10	Step-up circuit 2 step-up frequency (fDCDC2)
0	0	0	Oscillation clock / 16
0	0	1	Oscillation clock / 32
0	1	0	Oscillation clock / 64
0	1	1	Oscillation clock / 128
1	0	0	Oscillation clock / 256
1	0	1	Setting disabled
1	1	0	Halt Step-up Circuit 2
1	1	1	Setting disabled

6.2.21. Power Control 3 (R102h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VCM R0(0)	VRE G1R(0	0	PSON ()	PON (0)	VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)

VRH3-0: Set the voltage level of VREG1OUT, which generated from VCILVL. **Table 6-34** summarized the function of VRH3-0 setting

Table 6-34

VRH3	VRH2	VRH1	VRH0	VREG1OUT voltage		VRH3	VRH2	VRH1	VRH0	VREG1OUT voltage	
				VCILVL	VCIR					VCILVL	VCIR
0	0	0	0	Halt	Halt	1	0	0	0	VCILVLx1.6	2.5Vx1.6
0	0	0	1	Halt	Halt	1	0	0	1	VCILVLx1.65	2.5Vx1.65
0	0	1	0	Halt	Halt	1	0	1	0	VCILVLx1.7	2.5Vx1.7
0	0	1	1	Halt	Halt	1	0	1	1	VCILVLx1.75	2.5Vx1.75
0	1	0	0	Setting disable	Setting disable	1	1	0	0	VCILVLx1.8	2.5Vx1.8
0	1	0	1	Setting disable	Setting disable	1	1	0	1	VCILVLx1.85	2.5Vx1.85
0	1	1	0	Setting disable	Setting disable	1	1	1	0	VCILVLx1.9	2.5Vx1.9
0	1	1	1	Setting disable	Setting disable	1	1	1	1	Setting disable	Setting disable

PON: VLOUT3 ON/OFF control. Set PON = “0” to stop VLOUT3. Set PON = “1” to start VLOUT3.

PSON: Power Supply control bit for ON/OFF. When turning on power supply, Set PSE = “1” and then set PSON = “1” to start internal power supply operation..

VREG1R: Select reference voltage for VREG1OUT

VREG1R = “0” (default): VCILVL (External) as reference voltage for VREG1OUT.

VREG1R = ”1”: VCIR (internal) as reference voltage for VREG1OUT.

VCMR[0]: Select VCOMH external resistance or internal setting for VCOMH voltage level.

VCMR[0] = “0” use VCOMR (External) setting as VCOMH voltage.

VCMR[0] = ”1”: use register (Internal) setting as VCOMH voltage.

6.2.22. Power Control 4 (R103h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	VCOMG(0)	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	0	0	0	0	0	0	0	0

VDV4-0: Set the Vcom amplitude. Vcom amplitude is generated from VREG1OUT, the coefficient is valid from 0.7 to 1.24.

Table 6-35

VDV4	VDV3	VDV2	VDV1	VDV0	Vcom amplitude
0	0	0	0	0	VREG1OUT x 0.70
0	0	0	0	1	VREG1OUT x 0.72
0	0	0	1	0	VREG1OUT x 0.74
0	0	0	1	1	VREG1OUT x 0.76
0	0	1	0	0	VREG1OUT x 0.78
0	0	1	0	1	VREG1OUT x 0.80
0	0	1	1	0	VREG1OUT x 0.82
0	0	1	1	1	VREG1OUT x 0.84
0	1	0	0	0	VREG1OUT x 0.86
0	1	0	0	1	VREG1OUT x 0.88
0	1	0	1	0	VREG1OUT x 0.90
0	1	0	1	1	VREG1OUT x 0.92
0	1	1	0	0	VREG1OUT x 0.94
0	1	1	0	1	VREG1OUT x 0.96
0	1	1	1	0	VREG1OUT x 0.98
0	1	1	1	1	VREG1OUT x 1.00
1	0	0	0	0	VREG1OUT x 1.02
1	0	0	0	1	VREG1OUT x 1.04
1	0	0	1	0	VREG1OUT x 1.06
1	0	0	1	1	VREG1OUT x 1.08
1	0	1	0	0	VREG1OUT x 1.10
1	0	1	0	1	VREG1OUT x 1.12
1	0	1	1	0	VREG1OUT x 1.14
1	0	1	1	1	VREG1OUT x 1.16
1	1	0	0	0	VREG1OUT x 1.18
1	1	0	0	1	VREG1OUT x 1.20
1	1	0	1	0	VREG1OUT x 1.22
1	1	0	1	1	VREG1OUT x 1.24
1	1	1	0	0	Setting Disabled
1	1	1	0	1	
1	1	1	1	0	
1	1	1	1	1	

VCOMG: Set the value of VcomL.
When VCOMG = 0, VcomL equals to GND.
When VCOMG = 0, VcomL is set by VDV4-0.

6.2.23. Power Control 5 (R107h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	DCM0 (0)	0	0	0	0

6.2.24. Power Control 6(R110h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PSE

PSE: Power supply enable bit

PSE = “1”, and set PSON can start SPFD5408 power supply system.

PSE = ”0”, power supply system reset. .

6.2.25. GRAM Address Set (Horizontal Address) (R200h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

See R201h.

6.2.26. GRAM Address Set (Vertical Address) (R201h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

AD16–0: To set the initial address counter for GRAM address. Based on AM and I/D[1:0] setting, the address counter is automatically increment or decrement while data are written to the internal GRAM There is no need to updated AD16-0 every data transfer if AD16-0 was set in the beginning of one frame graphic data. Be aware that address counter is not automatically updated if reading data from the internal GRAM instruction is executed. Moreover, the address counter cannot be accessed when the SPFD5420A is in standby mode.

Table 6-36 summarized the function of AD15-0 setting

Note1: The address AD16-0 should be set in the address counter every frame on the falling edge of VSYNC if RGB interface mode is selected.

Note2: The address AD16-0 should be set when executing an instruction if system or VSYNC interface mode is selected.

Table 6-36

AD16–AD0	GRAM Setting
“00000”H – “000EF”H	Bitmap data for G1
“00100”H – “001EF”H	Bitmap data for G2
“00200”H – “002EF”H	Bitmap data for G3
“00300”H – “003EF”H	Bitmap data for G4
:	:
“1AC00”H – “1ACEF”H	Bitmap data for G399
“1AD00”H – “1ADEF”H	Bitmap data for G430
“1AE00”H – “1AEEF”H	Bitmap data for G431
“1AF00”H – “1AFEF”H	Bitmap data for G432

6.2.27. Write Data to GRAM (R202h)

R/W	RS	CB15 CB14 CB13 CB12 CB11 CB10 CB9 CB8 CB7 CB6 CB5 CB4 CB3 CB2 CB1 CB0
W	1	RAM write data (WD17-0) The DB17-0 pin assignment is different in different transferring modes.

WD17-0: SPFD5420A supports 18 bits data format. However, if only 16-bit (565format) is input to GRAM, SPFD5420A will expand the 16 bit data into 18-bit format. Same case when RGB interface is selected. Based on the graphic data in GRAM, the grayscale voltage of source driver is selected. **Table 6-37** summarized the source driver grayscale voltage output versus graphic data in GRAM. **Figure 6-8 ~ Figure 6-18** illustrates the pin assignment among data bus (DB17-0), (WD17-0) and GRAM.

Table 6-37

Data in GRAM	Source Driver Grayscale Output – REV=1 (REV=0)	
RGB	**Negative(Postive)**	**Positive(Negative)**
000000	V31	V0
000001	(V30+V31)/2	(V1+V0)/2
000010	V30	V1
000011	(V29+V30)/2	(V2+V1)/2
000100	V29	V2
000101	(V29+V28)/2	(V3+V2)/2
000110	V28	V3
000111	(V28+V27)/2	(V4+V3)/2
001000	V27	V4
001001	(V27+V26)/2	(V5+V4)/2
001010	V26	V5
001011	(V26+V25)/2	(V6+V5)/2
001100	V25	V6
001101	(V25+V24)/2	(V7+V6)/2
001110	V24	V7
001111	(V24+V23)/2	(V8+V7)/2
010000	V23	V8
010001	(V23+V22)/2	(V9+V8)/2
010010	V22	V9
010011	(V22+V21)/2	(V10+V9)/2
010100	V21	V10
010101	(V21+V20)/2	(V11+V10)/2
010110	V20	V11
010111	(V20+V19)/2	(V12+V11)/2
011000	V19	V12
011001	(V19+V18)/2	(V12+V11)/2
011010	V18	V13
011011	(V18+V17)/2	(V13+V12)/2
011100	V17	V14
011101	(V17+V16)/2	(V14+V13)/2
011110	V16	V15
011111	(V16+V15)/2	(V16+V15)/2
100000	V15	V16
100001	(V15+V14)/2	(V17+V16)/2
100010	V14	V17
100011	(V14+V13)/2	(V18+V17)/2
100100	V13	V18
100101	(V13+V12)/2	(V19+V18)/2
100110	V12	V19
100111	(V12+V11)/2	(V20+V19)/2
101000	V11	V20
101001	(V11+V10)/2	(V21+V20)/2
101010	V10	V21
101011	(V10+V9)/2	(V22+V21)/2
101100	V9	V22
101101	(V9+V8)/2	(V23+V22)/2
101110	V8	V23
101111	(V8+V7)/2	(V24+V23)/2
110000	V7	V24
110001	(V7+V6)/2	(V25+V24)/2
110010	V6	V25
110011	(V6+V5)/2	(V26+V25)/2
110100	V5	V26
110101	(V5+V4)/2	(V27+V26)/2
110110	V4	V27
110111	(V4+V3)/2	(V28+V27)/2
111000	V3	V28
111001	(V3+V2)/2	(V29+V28)/2
111010	V2	V29
111011	(V2+V1)/2	(V29+V30)/2
111100	V1	V30
111101	(V1+V0)/2	(V30+V31)/2
111110	(V1+2V0)/2	(V30+2V31)/2
111111	V0	V31

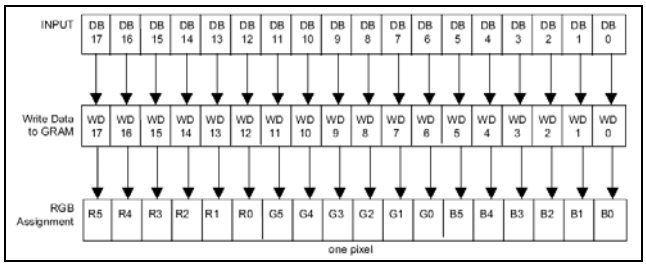


Figure 6-8 18-bit interface (262,144 colors)

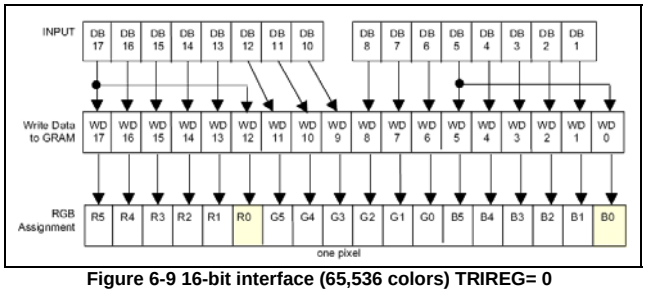


Figure 6-9 16-bit interface (65,536 colors) TRIREG= 0

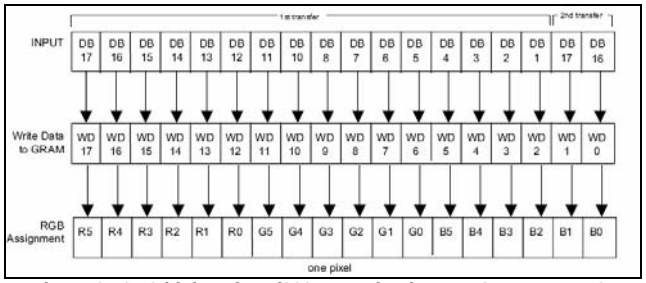


Figure 6-10 16-bit interface (262,144 colors) TRIREG = 1, DFM = 0

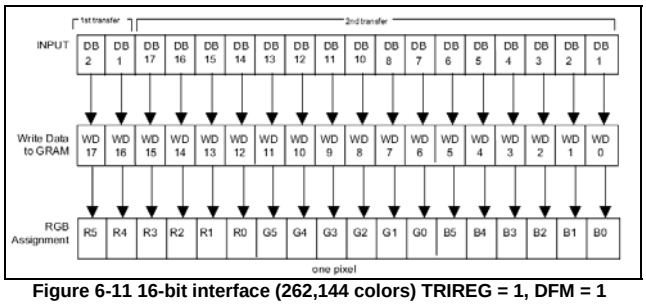


Figure 6-11 16-bit interface (262,144 colors) TRIREG = 1, DFM = 1

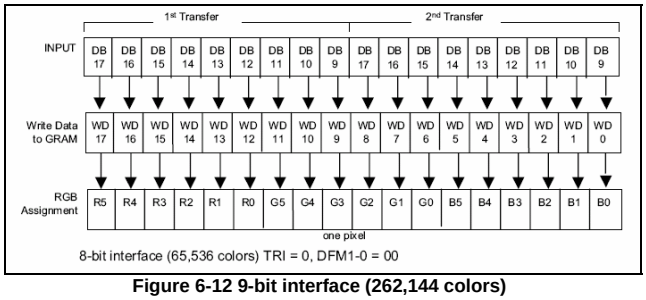


Figure 6-12 9-bit interface (262,144 colors)

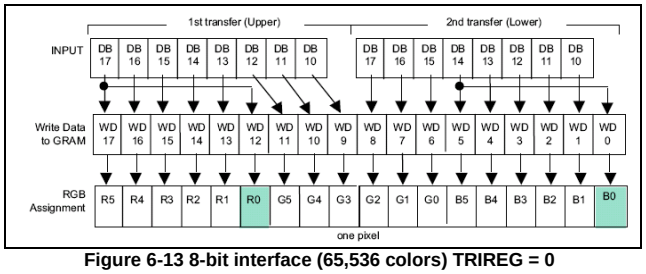


Figure 6-13 8-bit interface (65,536 colors) TRIREG = 0

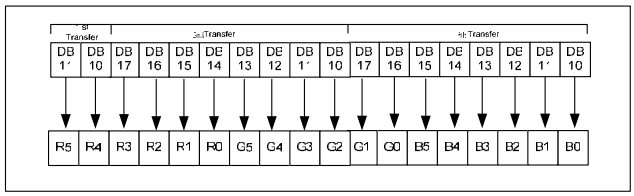


Figure 6-14 8-bit interface 262 colors) TRIREG = 1, DFM=0.

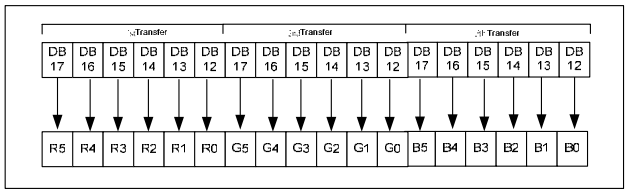


Figure 6-15 8-bit interface (262K colors) TRIREG = 1, DFM=1

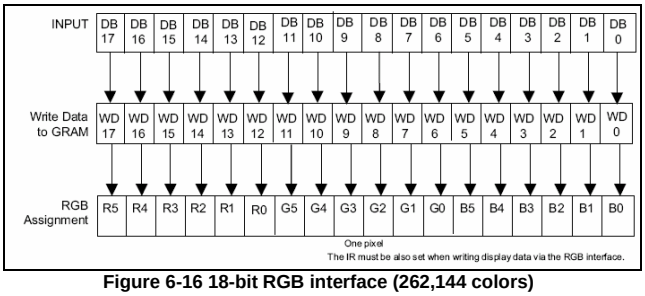


Figure 6-16 18-bit RGB interface (262,144 colors)

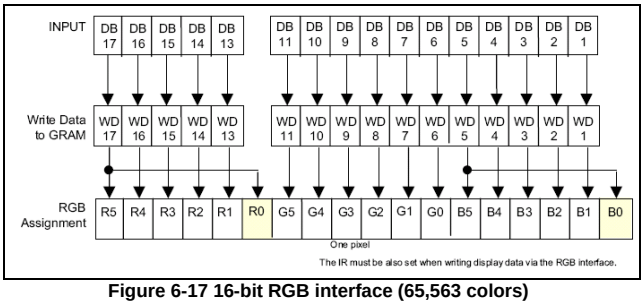


Figure 6-17 16-bit RGB interface (65,563 colors)

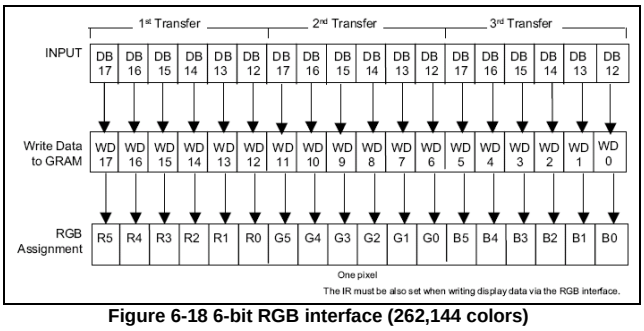


Figure 6-18 6-bit RGB interface (262,144 colors)

SPFD5420A supports external (RGB) interface. In RGB interface mode, all graphic data are stored in GRAM. To meet the diverse requirement of small size LCD panel, SPFD5420A also supports in a fix window using RGB interface and outside the window still use system interface.

In RGB interface mode, data writing to the internal RAM is synchronized with DOTCLK during ENABLE = "Low". Set ENABLE "High" to terminate writing data to RAM. Wait for a write/read bus cycle time. If accessing internal RAM using the RGB interface is desired after accessing the RAM via the system interface. **Figure 6-19** illustrates the timing diagram while RGB and system interface are both use in the same time.

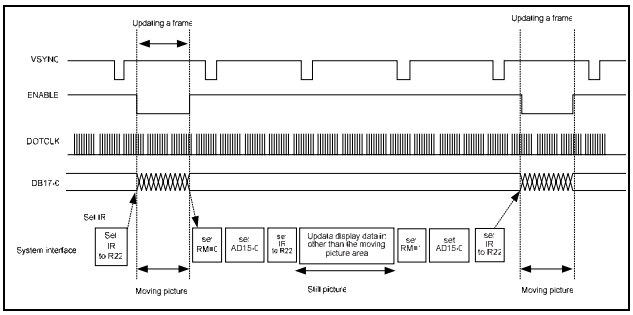


Figure 6-19

6.2.28. Read Data Read from GRAM (R202h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	RAM Read data (RD17-0) The DB17-0 pin assignment is different in different transferring modes.															

R202 also served as a register, which store the data read out from GRAM. When data are read out from the GRAM is desired, first sets the RAM address and executes first word read, and issues second word read. When first word read instruction is issued, Invalid data are sent to the data bus DB17-0. Valid data are sent to the data bus as second word data is executed.

The LSBs of R and B dots cannot read out, when the 8 or 16-bit interface is selected,

Note: This register is not available with the RGB interface. **Figure 6-20** and
Figure 6-23**Figure 6-23** illustrates the pin assignment among data bus (DB17-0), R22 (RD17-0) and GRAM in read data instruction.

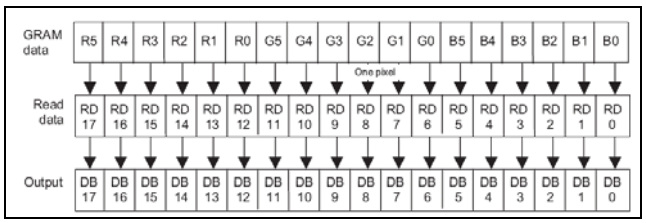


Figure 6-20 18-bit interface

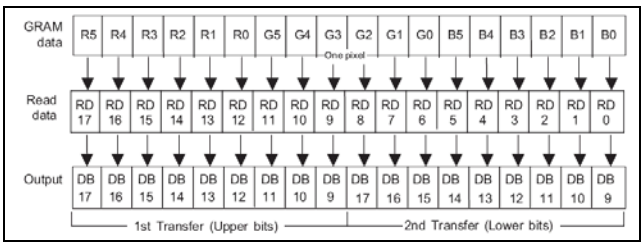


Figure 6-22 9-bit interface

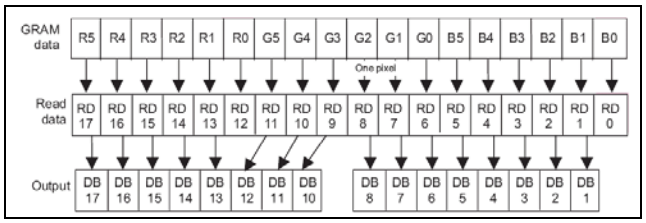


Figure 6-21 16-bit interface

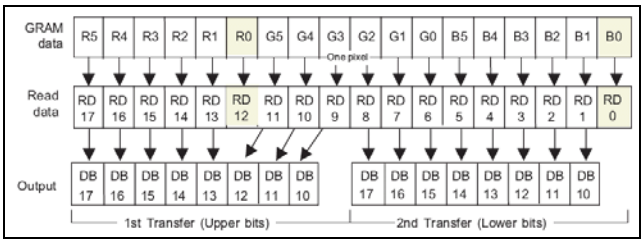


Figure 6-23 8-bit interface / SPI

6.2.29. NVM read data 1 (R280h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	UID3 (0)	UID2 (0)	UID1 (0)	UID0 (0)

See R282h

6.2.30. NVM read data 2 (R281h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VCM 14(0)	VCM 13(0)	VCM 12(0)	VCM 11(0)	VCM 10(0)

See R282h

6.2.31. NVM read data 3 (R282h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	VCM SEL	0	0	VCM 24(0)	VCM 23(0)	VCM 22(0)	VCM 21(0)	VCM 20(0)

UID[3:0]: SPFD5420A provides a 4-bit identification code UID[3:0] for user to use. UID[3:0] can be write / read from NVM. UID can be read out via R280h.

VCM1 [4:0]: These pins are to set the factor for generating VCOMH when VCMSEL="0". **Table 6-38** summarized the the factor of VERG1OUT

Table 6-38

VCM1[4:0]	VCOMH voltage
5'h00	VREG1OUT x 0.69
5'h01	VREG1OUT x 0.70
5'h02	VREG1OUT x 0.71
5'h03	VREG1OUT x 0.72
5'h04	VREG1OUT x 0.73
5'h05	VREG1OUT x 0.74
5'h06	VREG1OUT x 0.75
5'h07	VREG1OUT x 0.76
5'h08	VREG1OUT x 0.77
5'h09	VREG1OUT x 0.78
5'h0A	VREG1OUT x 0.79
5'h0B	VREG1OUT x 0.80
5'h0C	VREG1OUT x 0.81
5'h0D	VREG1OUT x 0.82
5'h0E	VREG1OUT x 0.83
5'h0F	VREG1OUT x 0.84
5'h10	VREG1OUT x 0.85
5'h11	VREG1OUT x 0.86
5'h12	VREG1OUT x 0.87
5'h13	VREG1OUT x 0.88
5'h14	VREG1OUT x 0.89
5'h15	VREG1OUT x 0.90
5'h16	VREG1OUT x 0.91
5'h17	VREG1OUT x 0.92
5'h18	VREG1OUT x 0.93
5'h19	VREG1OUT x 0.94
5'h1A	VREG1OUT x 0.95
5'h1B	VREG1OUT x 0.96
5'h1C	VREG1OUT x 0.97
5'h1D	VREG1OUT x 0.98
5'h1E	VREG1OUT x 0.99
5'h1F	VREG1OUT x 1.00

VCM2 [4:0]: These pins are to set the factor for generating VCOMH when VCMSEL="1". **Table 6-39** summarized the the factor of VERG1OUT

Table 6-39

VCM2[4:0]	VCOMH voltage
5'h00	VREG1OUT x 0.69
5'h01	VREG1OUT x 0.70
5'h02	VREG1OUT x 0.71
5'h03	VREG1OUT x 0.72
5'h04	VREG1OUT x 0.73
5'h05	VREG1OUT x 0.74
5'h06	VREG1OUT x 0.75
5'h07	VREG1OUT x 0.76
5'h08	VREG1OUT x 0.77
5'h09	VREG1OUT x 0.78
5'h0A	VREG1OUT x 0.79
5'h0B	VREG1OUT x 0.80
5'h0C	VREG1OUT x 0.81
5'h0D	VREG1OUT x 0.82
5'h0E	VREG1OUT x 0.83
5'h0F	VREG1OUT x 0.84
5'h10	VREG1OUT x 0.85
5'h11	VREG1OUT x 0.86
5'h12	VREG1OUT x 0.87
5'h13	VREG1OUT x 0.88
5'h14	VREG1OUT x 0.89
5'h15	VREG1OUT x 0.90
5'h16	VREG1OUT x 0.91
5'h17	VREG1OUT x 0.92
5'h18	VREG1OUT x 0.93
5'h19	VREG1OUT x 0.94
5'h1A	VREG1OUT x 0.95
5'h1B	VREG1OUT x 0.96
5'h1C	VREG1OUT x 0.97
5'h1D	VREG1OUT x 0.98
5'h1E	VREG1OUT x 0.99
5'h1F	VREG1OUT x 1.00

VCMSEL: VCMSEL is to select VCM1 or VCM2; When VCMSEL="0", VCM1 is selected while VCMSEL="1", VCM2 is selected.

6.2.32. Window Horizontal RAM Address Start (R210h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HAS (0)2	HSA1 (0)	HSA0 (0)

See R213h.

6.2.33. Window Horziontal RAM Address End (R211h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	HEA7 (1)	HEA6 (1)	HEA5 (1)	HEA4 (1)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)

See R213h.

6.2.34. Window Vertical RAM Address Start (R212h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VSA8 (0)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)

See R213h.

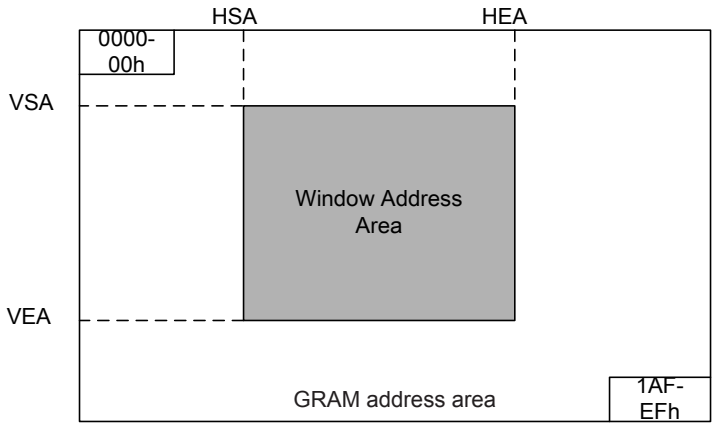
6.2.35. Window Vertical RAM Address End (R213h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VEA8 (1)	VEA7 (1)	VEA6 (1)	VEA5 (1)	VEA4 (1)	VEA3 (1)	VEA2 (1)	VEA1 (1)	VEA0 (1)

HSA7-0/HEA7-0: SPFD5420A provides window access function. Set HSA7-0 and HEA7-0 represent the start address and end address of the window function in horizontal direction. To use window-accessing function, HSA and HEA bits must be set before starting RAM write operation. Be aware that “00”h ≤ HSA7-0< HEA7-0 ≤ “EF”h and HEA-HAS>=”04h”.

VSA8-0/VEA8-0: SPFD5420A provides window access function. Set VSA8-0 and VEA8-0 represent the start address and end address of the window in vertical direction. To use window-accessing function, VSA and VEA bits must be set before starting RAM write operation. Be aware that “00”h ≤ VSA8-0< VEA8-0 ≤ 9’h1AF.

Figure 6-24 illustrates the window-accessing function.



6.2.36. γ Control (R300h to R30Dh)

T.B.D.

6.2.37. Base Image Number of Line (R400h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	GS (0)	0	NL5 (0)	NL4 (0)	NL3 (0)	NL2 (0)	NL1 (0)	NL0 (0)	0	0	SCN5 (0)	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)

SCN5-0: Set the SCN5-0 bits can specify the starting position of the gate driver. The start position of gate driver is determined by the combination of the setting of GS and SM. **Table 6-40** summarized the starting position for each SCN5-0 setting.

Table 6-40 (whenSM=0)

SCN5	SCN4	SCN3	SCN2	SCN1	SCN0	Scan Start Position (Gate line)	
						GS = "0"	GS = "1"
0	0	0	0	0	0	G1	G432
0	0	0	0	0	1	G9	G424
0	0	0	0	1	0	G17	G416
0	0	0	0	1	1	G25	G408
0	0	0	1	0	0	G33	G400
0	0	0	1	0	1	G41	G392
0	0	0	1	1	0	G49	G384
0	0	0	1	1	1	G57	G376
0	0	1	0	0	0	G65	G368
0	0	1	0	0	1	G73	G360
0	0	1	0	1	0	G81	G352
0	0	1	0	1	1	G89	G344
0	0	1	1	0	0	G97	G336
0	0	1	1	0	1	G105	G328
0	0	1	1	1	0	G113	G320
0	0	1	1	1	1	G121	G312
0	1	0	0	0	0	G129	G304
0	1	0	0	0	1	G137	G296
0	1	0	0	1	0	G145	G288
0	1	0	0	1	1	G153	G280
0	1	0	1	0	0	G161	G272
0	1	0	1	0	1	G169	G264
0	1	0	1	1	0	G177	G256
0	1	0	1	1	1	G185	G248
0	1	1	0	0	0	G193	G240
0	1	1	0	0	1	G201	G232
0	1	1	0	1	0	G209	G224
0	1	1	0	1	1	G217	G216
0	1	1	1	0	0	G225	G208
0	1	1	1	0	1	G233	G200
0	1	1	1	1	0	G241	G192
0	1	1	1	1	1	G249	G184
1	0	0	0	0	0	G257	G176
1	0	0	0	0	1	G265	G168
1	0	0	0	1	0	G273	G160
1	0	0	0	1	1	G281	G152
1	0	0	1	0	0	G289	G144
1	0	0	1	0	1	G297	G136
1	0	0	1	1	0	G305	G128
1	0	0	1	1	1	G313	G120
1	0	1	0	0	0	G321	G112
1	0	1	0	0	1	G329	G104
1	0	1	0	1	0	G337	G96
1	0	1	0	1	1	G345	G88
1	0	1	1	0	0	G353	G80
1	0	1	1	0	1	G361	G72
1	0	1	1	1	0	G369	G64
1	0	1	1	1	1	G377	G56
1	1	0	0	0	0	G385	G48
1	1	0	0	0	1	G393	G40
1	1	0	0	1	0	G401	G32
1	1	0	0	1	1	G409	G24
1	1	0	1	0	0	G417	G16
1	1	0	1	0	1	G425	G8
1	1	0	1	1	0	Setting disabled	
Setting disabled							
1	1	1	1	1	1	Setting disabled	

Table 6-41 (whenSM=1)

SC N5	SC N4	SC N3	SC N2	SC N1	SC N0	Scan Start Position (Gate line)	
						GS = "0"	GS = "1"
0	0	0	0	0	0	G1	G432
0	0	0	0	0	1	G17	G416
0	0	0	0	1	0	G33	G400
0	0	0	0	1	1	G49	G384
0	0	0	1	0	0	G65	G368
0	0	0	1	0	1	G81	G352
0	0	0	1	1	0	G97	G336
0	0	0	1	1	1	G113	G320
0	0	1	0	0	0	G129	G304
0	0	1	0	0	1	G145	G288
0	0	1	0	1	0	G161	G272
0	0	1	0	1	1	G177	G256
0	0	1	1	0	0	G193	G240
0	0	1	1	0	1	G209	G224
0	0	1	1	1	0	G225	G208
0	0	1	1	1	1	G241	G192
0	1	0	0	0	0	G257	G176
0	1	0	0	0	1	G273	G160
0	1	0	0	1	0	G289	G144
0	1	0	0	1	1	G305	G128
0	1	0	1	0	0	G321	G112
0	1	0	1	0	1	G337	G96
0	1	0	1	1	0	G353	G80
0	1	0	1	1	1	G369	G64
0	1	1	0	0	0	G385	G48
0	1	1	0	0	1	G401	G32
0	1	1	0	1	0	G417	G16
0	1	1	0	1	1	G2	G431
0	1	1	1	0	0	G18	G415
0	1	1	1	0	1	G34	G399
0	1	1	1	1	0	G50	G383
0	1	1	1	1	1	G66	G367
1	0	0	0	0	0	G82	G351
1	0	0	0	0	1	G98	G335
1	0	0	0	1	0	G114	G319
1	0	0	0	1	1	G130	G303
1	0	0	1	0	0	G146	G287
1	0	0	1	0	1	G162	G271
1	0	0	1	1	0	G178	G255
1	0	0	1	1	1	G194	G239
1	0	1	0	0	0	G210	G223
1	0	1	0	0	1	G226	G207
1	0	1	0	1	0	G242	G191
1	0	1	0	1	1	G258	G175
1	0	1	1	0	0	G274	G159
1	0	1	1	0	1	G290	G143
1	0	1	1	1	0	G306	G127
1	0	1	1	1	1	G322	G111
1	1	0	0	0	0	G338	G95
1	1	0	0	0	1	G354	G79
1	1	0	0	1	0	G370	G63
1	1	0	0	1	1	G386	G47
1	1	0	1	0	0	G402	G31
1	1	0	1	0	1	G418	G15
1	1	0	1	1	0	Setting disabled	
Setting disabled							
1	1	1	1	1	1		

NL5-0: Set the number of gate lines for different resolution of display panel. The combination of NL5-NL0 represents the gate line number are summarized at **Table 6-42**.

Table 6-42

NL5	NL4	NL3	NL2	NL1	NL0	Display Size	No. of Lines	Driven gate lines
0	0	0	0	0	0	Setting disabled	Setting disabled	Setting disabled
0	0	0	0	0	1	720 x 16 dots	16	G1 ~ G16
0	0	0	0	1	0	720 x 24 dots	24	G1 ~ G24
0	0	0	0	1	1	720 x 32 dots	32	G1 ~ G32
0	0	0	1	0	0	720 x 40 dots	40	G1 ~ G40
0	0	0	1	0	1	720 x 48 dots	48	G1 ~G48
0	0	0	1	1	0	720 x 56 dots	56	G1 ~ G56
0	0	0	1	1	1	720 x 64 dots	64	G1 ~ G64
0	0	1	0	0	0	720 x 72 dots	72	G1 ~ G72
0	0	1	0	0	1	720 x 80 dots	80	G1 ~ G80
0	0	1	0	1	0	720 x 88 dots	88	G1 ~ G88
0	0	1	0	1	1	720 x 96 dots	96	G1 ~ G96
0	0	1	1	0	0	720 x 104 dots	104	G1 ~ G104
0	0	1	1	0	1	720 x 112 dots	112	G1 ~ 112
0	0	1	1	1	0	720 x 120 dots	120	G1 ~ 120
0	0	1	1	1	1	720 x 128 dots	128	G1 ~ 128
0	1	0	0	0	0	720 x 136 dots	136	G1 ~ 136
0	1	0	0	0	1	720 x 144 dots	144	G1 ~ 144
0	1	0	0	1	0	720 x 152 dots	152	G1 ~ 152
0	1	0	0	1	1	720 x 160 dots	160	G1 ~ 160
0	1	0	1	0	0	720 x 168 dots	168	G1 ~ 168
0	1	0	1	0	1	720 x 176 dots	176	G1 ~ 176
0	1	0	1	1	0	720 x 184 dots	184	G1 ~ 184
0	1	0	1	1	1	720 x 192 dots	192	G1 ~ 192
0	1	1	0	0	0	720 x 200 dots	200	G1 ~ 200
0	1	1	0	0	1	720 x 208 dots	208	G1 ~ 208
0	1	1	0	1	0	720 x 216 dots	216	G1 ~ 216
0	1	1	0	1	1	720 x 224 dots	224	G1 ~ 224
0	1	1	1	0	0	720 x 232 dots	232	G1 ~ 232
0	1	1	1	0	1	720 x 240 dots	240	G1 ~ 240
0	1	1	1	1	0	720 x 248 dots	248	G1 ~ 248
0	1	1	1	1	1	720 x 256 dots	256	G1 ~ 256
1	0	0	0	0	0	720 x 264 dots	264	G1 ~ 264
1	0	0	0	0	1	720 x 272 dots	272	G1 ~ 272
1	0	0	0	1	0	720 x 280 dots	280	G1 ~ 280
1	0	0	0	1	1	720 x 288 dots	288	G1 ~ 288
1	0	0	1	0	0	720 x 296 dots	296	G1 ~ 296
1	0	0	1	0	1	720 x 304 dots	304	G1 ~ 304
1	0	0	1	1	0	720 x 312 dots	312	G1 ~ 312
1	0	0	1	1	1	720 x 320 dots	320	G1 ~ 320
1	0	1	0	0	0	720 x 328 dots	328	G1 ~ 328

NL5	NL4	NL3	NL2	NL1	NL0	Display Size	No. of Lines	Driven gate lines
1	0	1	0	0	1	720 x 336 dots	336	G1 ~ 336
1	0	1	0	1	0	720 x 344 dots	344	G1 ~ 344
1	0	1	0	1	1	720 x 352 dots	352	G1 ~ 352
1	0	1	1	0	0	720 x 360 dots	360	G1 ~ 360
1	0	1	1	0	1	720 x 368 dots	368	G1 ~ 368
1	0	1	1	1	0	720 x 376 dots	376	G1 ~ 376
1	0	1	1	1	1	720 x 384 dots	384	G1 ~ 384
1	1	0	0	0	0	720 x 392 dots	392	G1 ~ 392
1	1	0	0	0	1	720 x 400 dots	400	G1 ~ 400
1	1	0	0	1	0	720 x 408 dots	408	G1 ~ 408
1	1	0	0	1	1	720 x 416 dots	416	G1 ~ 416
1	1	0	1	0	0	720 x 424 dots	424	G1 ~ 424
1	1	0	1	0	1	720 x 430 dots	430	G1 ~ 430
Setting Disabled								

Note: Back porch and a front porch (set with BP/FP bits respectively) are inserted before/ after driving all gate lines.

GS: Shift direction of the gate driver output selection. When
GS="0", gate driver shift from G1 to G320. When GS = "1", gate driver shift from G432 to G1.

6.2.38. Base Image Display Control (R401h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL (0)	VLE (0)	REV (0)

REV: To set the grayscale corresponding to normally white or normally black LCD panel from same data input. **Table 6-43** summarized REV bit function.

Table 6-43

REV	GRAM data	Source Driver Output	
		Positive Polarity	Negative Polarity
0	18'h00000 ⋮ 18'h3FFFF	V63 ⋮ V0	V0 ⋮ V63
1	18'h00000 ⋮ 18'h3FFFF	V0 ⋮ V63	V63 ⋮ V0

VLE: SPFD5408 provides vertical scrolling function which can be set by VLE bit.
VLE = "1", vertical scrolling function enable. The amout of scrolling line from the first line is determined by VL[8:0].
VLE = "0", normal display.

NDL: set the source driver output level in non-lit area..
NDL = "1", Positive = V0, Negative = V31;
NDL = "0", Postive = V31 and Negative = V0.

6.2.39. Based Image Vertical Scroll Control (R404h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VL8 (0)	VL7 (0)	VL6 (0)	VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	VL0 (0)

VL8-0: SPFD5420A provides scrolling function. The start position for displaying the image is shifted vertically by the number of lines based on the setting of the VL8-0 bits. Be aware that the vertical scrolling function is not available in the external (RGB) display interface mode. **Table 6-44** summarized the function of VL8-0 setting.

Table 6-44

VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Scrolling lines
0	0	0	0	0	0	0	0	0	0 line
0	0	0	0	0	0	0	0	1	1 line
0	0	0	0	0	0	0	1	0	2 lines
	:	:	:	:	:	:	:	:	:
1	1	0	1	0	1	1	1	0	431 lines
1	1	0	1	0	1	1	1	1	432 lines

Note: VL8-0 bits cannot set more than 432 lines.

6.2.40. Display Position - Partial Display 1 (R500h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTD P08	PTD P07	PTD P06	PTD P05	PTD P04	PTD P03	PTD P02	PTD P01	PTD P00

See R505h.

6.2.41. RAM Address Start – Partial Display 1 (R501h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTS A08	PTS A07	PTS A06	PTS A05	PTS A04	PTS A03	PTS A02	PTS A01	PTS A00

See R505h.

6.2.42. RAM Address End – Partail Display 1 (R502h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTE A08	PTE A07	PTE A06	PTE A05	PTE A04	PTE A03	PTE A02	PTE A01	PTE A00

See R505h.

6.2.43. Display Position – Partial Display 2 (R503h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTD P18	PTD P17	PTD P16	PTD P15	PTD P14	PTD P13	PTD P12	PTD P11	PTD P10

See R505h.

6.2.44. RAM Address Start – Partial Display 2 (R504h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTSA18	PTSA17	PTSA16	PTSA15	PTSA14	PTSA13	PTSA12	PTSA11	PTSA10

See R505h.

6.2.45. RAM Address End – Partial Display 2 (R505h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTEA18	PTEA17	PTEA16	PTEA15	PTEA14	PTEA13	PTEA12	PTEA11	PTEA10

PTDP0[8:0]: Set the physical starting position of partial display 1 on the LCD panel

PTDP1[8:0]: Set the physical starting position of partial display 2 on the LCD panel

The partial display 1 and partial display 2 should not overlap with each other. And make sure the PTDP0[8:0] < PTDP1[8:0].

PTSA0[8:0]: Set the start line address of display RAM of partial display 1 which will be display according to PTDP0[8:0].

PTEA0[8:0]: Set the end line address of display RAM of partial display 1 which will be display according to PTDP0[8:0].

Make sure PTSA0≤PTEA0.

PTSA1[8:0]: Set the start line address of display RAM of partial display2 which will be display according to PTDP1[8:0].

PTEA1[8:0]: Set the end line address of display RAM of partial display2 which will be display according to PTDP1[8:0]

Make sure PTSA1≤PTEA1.

6.2.46. Pin Control (R606h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	TCREV1(0)	0	0	0	0	0	0	0	TCREV0(0)

TCREV1-0: Set the order of receiving data when using i80 interface.

TCREV1-0	2 Transfers/Pixel	3 Transfers/Pixel
00	1st to 2nd	1st to 3rd
01 – 10	Setting Disabled	
11	2nd to 1st	3rd to 1st

Note 1: During read operation, the setting of TCREV is ignored; data is transferred from 1st to 2nd/1st to 3rd.

Note 2: Reset TCREV after reset and power-on.

6.2.47. NVM Access Control (R6F0h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	TE	0	EOP1 (0)	EOP0 (0)	0	0	EAD1 (0)	EAD0 (0)

EDA1 – 0: Determine the address of the NVM.

EAD1 – 0	Data written into NVM
00	UID(3 – 0)
01	VCM1(4 – 0)
10	VCMSEL, VCM2(4 – 0)
11	Setting Disabled

EOP: EOP = 00: Halt the write operation; EOP = 01: Enable the write operation.

TE: TE = 1, Enable the NVM control sequence.

7. GRAM

Table 7-1 GRAM address and display panel position (SS = "0")

S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	....	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	DB17-0			DB17-0			DB17-0			DB17-0			....	DB17-0			DB17-0			DB17-0			DB17-0		
G1	G400	"00000"H			"00001"H			"00002"H			"00003"H			....	"000EC"H			"000ED"H			"000EE"H			"000EF"H		
G2	G399	"00100"H			"00101"H			"00102"H			"00103"H			....	"001EC"H			"001ED"H			"001EE"H			"001EF"H		
G3	G398	"00200"H			"00201"H			"00202"H			"00203"H			....	"002EC"H			"002ED"H			"002EE"H			"002EF"H		
G4	G397	"00300"H			"00301"H			"00302"H			"00303"H			....	"003EC"H			"003ED"H			"003EE"H			"003EF"H		
G5	G396	"00400"H			"00401"H			"00402"H			"00403"H			....	"004EC"H			"004ED"H			"004EE"H			"004EF"H		
G6	G395	"00500"H			"00501"H			"00502"H			"00503"H			....	"005EC"H			"005ED"H			"005EE"H			"005EF"H		
G7	G394	"00600"H			"00601"H			"00602"H			"00603"H			....	"006EC"H			"06ED"H			"06EE"H			"06EF"H		
G8	G393	"00700"H			"00701"H			"00702"H			"00703"H			....	"007EC"H			"007ED"H			"007EE"H			"007EF"H		
G9	G392	"00800"H			"00801"H			"00802"H			"00803"H			....	"008EC"H			"008ED"H			"008EE"H			"008EF"H		
G10	G391	"00900"H			"00901"H			"00902"H			"00903"H			....	"009EC"H			"009ED"H			"009EE"H			"009EF"H		
G11	G390	"00E00"H			"00E01"H			"00E02"H			"00E03"H			....	"00EEC"H			"00EED"H			"00EEE"H			"00EEF"H		
G12	G389	"00B00"H			"00B01"H			"00B02"H			"00B03"H			....	"00BEC"H			"00BED"H			"00BEE"H			"00BEF"H		
G13	G388	"00C00"H			"00C01"H			"00C02"H			"00C03"H			....	"00CEC"H			"00CED"H			"00CEE"H			"00CEF"H		
G14	G387	"00D00"H			"00D01"H			"00D02"H			"00D03"H			....	"00DEC"H			"00DED"H			"00DEE"H			"00DEF"H		
G15	G386	"00E00"H			"00E01"H			"00E02"H			"00E03"H			....	"00EEC"H			"00EED"H			"00EEE"H			"00EEF"H		
G16	G385	"00F00"H			"00F01"H			"00F02"H			"00F03"H			....	"00FEC"H			"00FED"H			"00FEE"H			"00FEF"H		
G17	G384	"01000"H			"01001"H			"01002"H			"01003"H			....	"010EC"H			"010ED"H			"010EE"H			"010EF"H		
G18	G383	"01100"H			"01101"H			"01102"H			"01103"H			....	"011EC"H			"011ED"H			"011EE"H			"011EF"H		
G19	G382	"01200"H			"01201"H			"01202"H			"01203"H			....	"012EC"H			"012ED"H			"012EE"H			"012EF"H		
G20	G381	"01300"H			"01301"H			"01302"H			"01303"H			....	"013EC"H			"013ED"H			"013EE"H			"013EF"H		
:	:	:			:			:			:				:			:			:			:		
:	:	:			:			:			:				:			:			:			:		
G393	G8	"1A900"H			"1A801"H			"1A802"H			"1A803"H			....	"1A8EC"H			"1A8ED"H			"1A8EE"H			"1A8EF"H		
G394	G7	"1AA00"H			"1A901"H			"1A902"H			"1A903"H			....	"1A9EC"H			"1A9ED"H			"1A9EE"H			"1A9EF"H		
G395	G6	"1AB00"H			"1AA01"H			"1AA02"H			"1AA03"H			....	"1AAEC"H			"1AAED"H			"1AAEE"H			"1AAEF"H		
G396	G5	"1AC00"H			"1AB01"H			"1AB02"H			"1AB03"H			....	"1ABEC"H			"1ABED"H			"1ABEE"H			"1ABEF"H		
G397	G4	"1AD00"H			"1AC01"H			"1AC02"H			"1AC03"H			....	"1ACEC"H			"1ACED"H			"1ACEE"H			"1ACEF"H		
G398	G3	"1AD00"H			"1AD01"H			"1AD02"H			"1AD03"H			....	"1ADEC"H			"1ADED"H			"1ADEE"H			"1ADEF"H		
G399	G2	"1AE00"H			"1AE01"H			"1AE02"H			"1AE03"H			....	"1AEEC"H			"1AEED"H			"1AEEE"H			"1AEEF"H		
G400	G1	"1AF00"H			"1AF01"H			"1AF02"H			"1AF03"H			....	"1AFEC"H			"1AFED"H			"1AFEE"H			"1AFEF"H		

Table 7-2 GRAM address and display panel position (SS = "1")

S/G pin		S1	S2	S3	S4	S5	…	S7	S8	S9	S10	S11	S12	….	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	DB17-0			DB17-0			DB17-0			DB17-0			….	DB17-0			DB17-0			DB17-0			DB17-0		
G1	G432	"000EF"H			"000EE"H			"000ED"H			"000EC"H			….	"00003"H			"00002"H			"00001"H			"00000"H		
G2	G431	"001EF"H			"001EE"H			"001ED"H			"001EC"H			….	"00103"H			"00102"H			"00101"H			"00100"H		
G3	G430	"002EF"H			"002AE"H			"002ED"H			"002EC"H			….	"00203"H			"00202"H			"00201"H			"00200"H		
G4	G429	"003EF"H			"003EE"H			"003ED"H			"003EC"H			….	"00303"H			"00302"H			"00301"H			"00300"H		
G5	G428	"004EF"H			"004EE"H			"004ED"H			"004EC"H			….	"00403"H			"00402"H			"00401"H			"00400"H		
G6	G427	"005EF"H			"005EE"H			"005ED"H			"005EC"H			….	"00503"H			"00502"H			"00501"H			"00500"H		
G7	G426	"006EF"H			"006EE"H			"006ED"H			"006EC"H			….	"00603"H			"00602"H			"00601"H			"00600"H		
G8	G425	"007EF"H			"007EE"H			"007ED"H			"007EC"H			….	"00703"H			"00702"H			"00701"H			"00700"H		
G9	G424	"008EF"H			"008EE"H			"008ED"H			"008EC"H			….	"00803"H			"00802"H			"00801"H			"00800"H		
G10	G423	"009EF"H			"009EE"H			"009ED"H			"009EC"H			….	"00903"H			"00902"H			"00901"H			"00900"H		
G11	G422	"00AEF"H			"00AEE"H			"00AED"H			"00AEC"H			….	"00E03"H			"00A02"H			"00A01"H			"00A00"H		
G12	G421	"00BEF"H			"00BEE"H			"00BED"H			"00BEC"H			….	"00B03"H			"00B02"H			"00B01"H			"00B00"H		
G13	G420	"00CEF"H			"00CEE"H			"00CED"H			"00CEC"H			….	"00C03"H			"00C02"H			"00C01"H			"00C00"H		
G14	G419	"00DEF"H			"00DEE"H			"00DED"H			"00DEC"H			….	"00D03"H			"00D02"H			"00D01"H			"00D00"H		
G15	G418	"00EEF"H			"00EEE"H			"00EED"H			"00EEC"H			….	"00E03"H			"00E02"H			"00E01"H			"00E00"H		
G16	G417	"00FEF"H			"00FEE"H			"00FED"H			"00FEC"H			….	"00F03"H			"00F02"H			"00F01"H			"00F00"H		
G17	G416	"010EF"H			"010EE"H			"010ED"H			"010EC"H			….	"01003"H			"01002"H			"01001"H			"01000"H		
G18	G415	"011EF"H			"011EE"H			"011ED"H			"011EC"H			….	"01103"H			"01102"H			"01101"H			"01100"H		
G19	G414	"012EF"H			"012EE"H			"012ED"H			"012EC"H			….	"01203"H			"01202"H			"01201"H			"01200"H		
G20	G413	"013EF"H			"013EE"H			"013ED"H			"013EC"H			….	"01303"H			"01302"H			"01301"H			"01300"H		
:	:	:			:			:			:				:			:			:			:		
:	:	:			:			:			:				:			:			:			:		
G425	G8	"1A8EF"H			"1A8EE"H			"1A8ED"H			"1A8EC"H			….	"1A803"H			"1A802"H			"1A801"H			"1A900"H		
G426	G7	"1A9EF"H			"1A9EE"H			"1A9ED"H			"1A9EC"H			….	"1A903"H			"1A902"H			"1A901"H			"1AA00"H		
G427	G6	"1AAEF"H			"1AAEE"H			"1AAED"H			"1AAEC"H			….	"1AA03"H			"1AA02"H			"1AA01"H			"1AB00"H		
G428	G5	"1ABEF"H			"1ABEE"H			"1ABED"H			"1ABEC"H			….	"1AB03"H			"1AB02"H			"1AB01"H			"1AC00"H		
G429	G4	"1ACEF"H			"1ACEE"H			"1ACED"H			"1ACEC"H			….	"1AC03"H			"1AC02"H			"1AC01"H			"1AD00"H		
G430	G3	"1ADEF"H			"1ADEE"H			"1ADED"H			"1ADEC"H			….	"1AD03"H			"1AD02"H			"1AD01"H			"1AD00"H		
G431	G2	"1AEEF"H			"1AEEE"H			"1AEED"H			"1AEEC"H			….	"1AE03"H			"1AE02"H			"1AE01"H			"1AE00"H		
G432	G1	"1AFEF"H			"1AFEE"H			"1AFED"H			"1AFEC"H			….	"1AF03"H			"1AF02"H			"1AF01"H			"1AF00"H		

8. INTERFACES

The SPFD5420A provides different interfaces to meet the diverse need of small/medium size LCD. Based on the application requirement, there are three different display modes which are most used in end product.

1. Still picture display
2. Moving picture display.
3. Re-writing still pictures while moving picture are display.

For above three different display requirements, SPFD5420A provides different interfaces to meet the requirement.

1. System interface
2. External interface (RGB interface)
3. VSYNC interface

System interface is suitable for still picture display while RGB interface and VSYNC interface are suitable for moving picture display. Be aware that RGB or VSYNC interface still can used to display still picture and system interface can also display moving picture. **Table 8-1** summarized different interfaces for different display requirement.

Table 8-1

Operation Mode	Display Mode	RAM Access Setting (RM)	Display Operation Mode (DM1-0)
System	Still picture	System interface (RM = 0)	Internal operating clock (DM1-0 = 00)
RGB interface (1)	Moving picture	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
RGB interface (2)	Rewriting still pictures while displaying moving pictures	System interface (RM = 0)	RGB interface (DM1-0 = 01)
VSYNC interface	Moving pictures	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

8.1. System Interface

The system interfaces of SPFD5420A can support 8-bit, 9-bit, 16-bit, 18-bit 80-system Interface and Serial Peripheral Interface (SPI), which can be set by the IM2/1/0 pins. The system interface can set instructions and access RAM. **Table 8-2** summarized the interface corresponding to IM2-0 setting.

Table 8-2

IM2	IM1	IM0	MPU-Interface Mode	DB Pin in use
0	0	0	80-system 18-bit interface	DB17 to 0
0	0	1	80-system 9-bit interface	DB17 to 9
0	1	0	80-system 16-bit interface	DB17 to 10 and 8 to 1
0	1	1	80-system 8-bit interface	DB17 to 10
1	0	*	Serial peripheral interface (SPI)	DB1 to 0
1	1	0	Setting disabled	-
1	1	1	Setting disabled	-

8.1.1. 80-system 18-bit interface

The instruction and GRAM accessing format of 80-system 18-bit interface are shown in **Figure 8-1** and **Figure 8-2**, respectively.

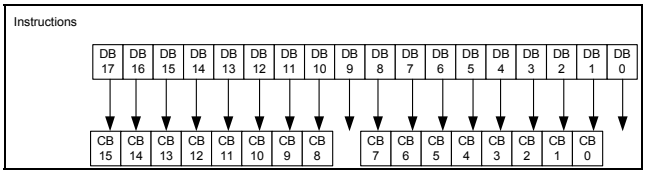


Figure 8-1

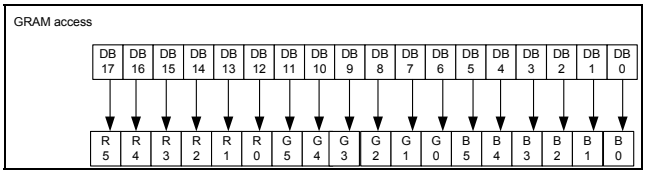


Figure 8-2

8.1.2. 80-system 16-bit interface

The instruction and GRAM accessing format of 80-system 16-bit interface are shown in **Figure 8-3** and **Figure 8-4**, respectively.

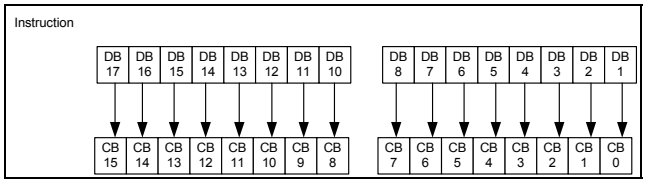


Figure 8-3

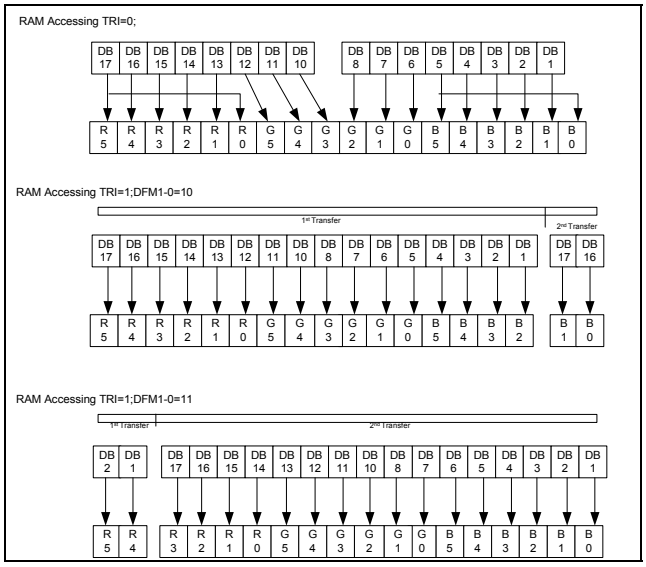


Figure 8-4

8.1.3. 80-system 9-bit interface

The instruction and GRAM accessing format of 80-system 9-bit interface are shown in **Figure 8-5** and **Figure 8-6**, respectively.

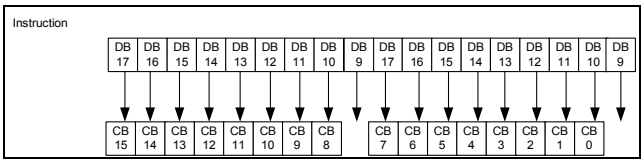


Figure 8-5

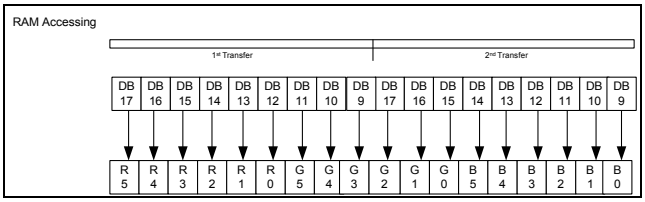


Figure 8-6

8.1.4. 80-system 8-bit interface

The instruction and GRAM accessing format of 80-system 8-bit interface are shown in **Figure 8-7** and **Figure 8-8**, respectively.

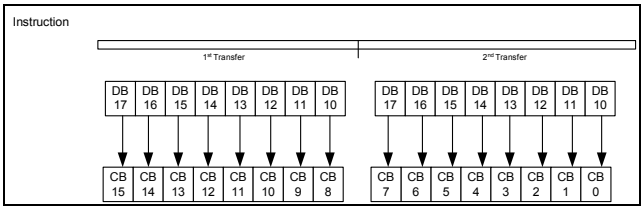


Figure 8-7

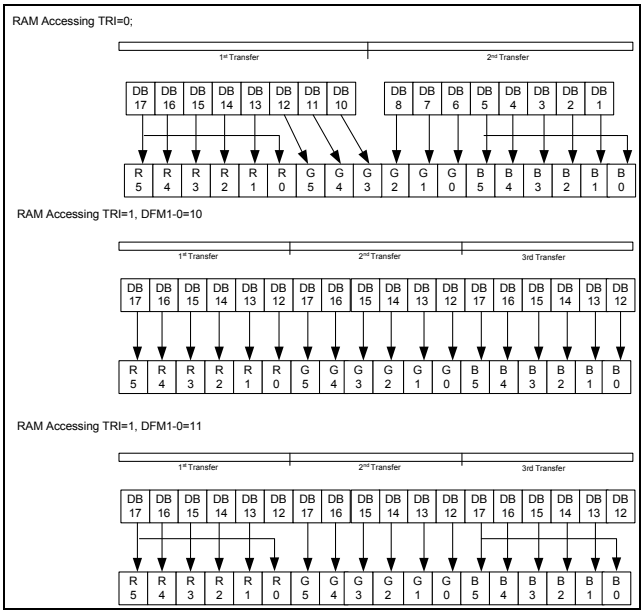


Figure 8-8

8.1.5. Serial Peripheral interface (SPI)

The system interface of SPFD5420A also includes the Serial Peripheral Interface (SPI). In SPI mode, /CS, SCL, SDI and SDO are used to transfer data between MCU and SPFD5420A. IM0/ID pin served as the ID pin. **Figure 8-9** illustrates the detail timing while using SPI. Be aware that the unused pins such as DB17-0 pins must be fixed at either IOVCC or GND level.

The instruction and GRAM accessing format of SPI interface are shown in **Figure 8-10** and **Figure 8-11**, respectively.

When read operation is desired In SPI mode, valid data are read out as the SPFD5420A reads out the 6th byte data from the internal GRAM. The RAM data transfer in SPI mode, in SPI mode with TRI=1/ DFM1-0=10 and status read are illustrated in **Figure 8-12**, **Figure 8-13** and **Figure 8-14**, respectively.

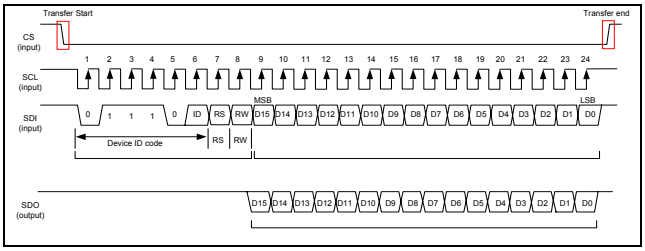


Figure 8-9

Start Byte Format

Transferred bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note 1) ID bit is selected by setting the IM0/ID pin.

RS	R/W	Function
0	0	Set an index register
0	1	Read a status
1	0	Write an instruction or RAM data
1	1	Read an instruction or RAM data

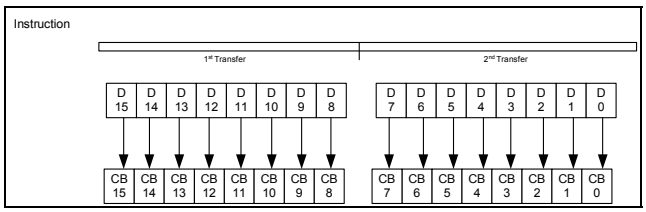


Figure 8-10

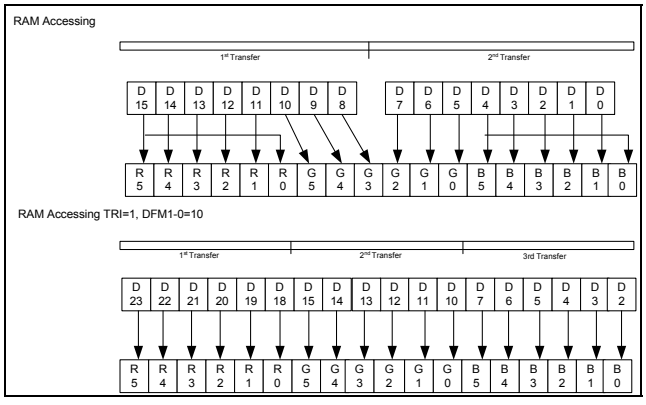


Figure 8-11

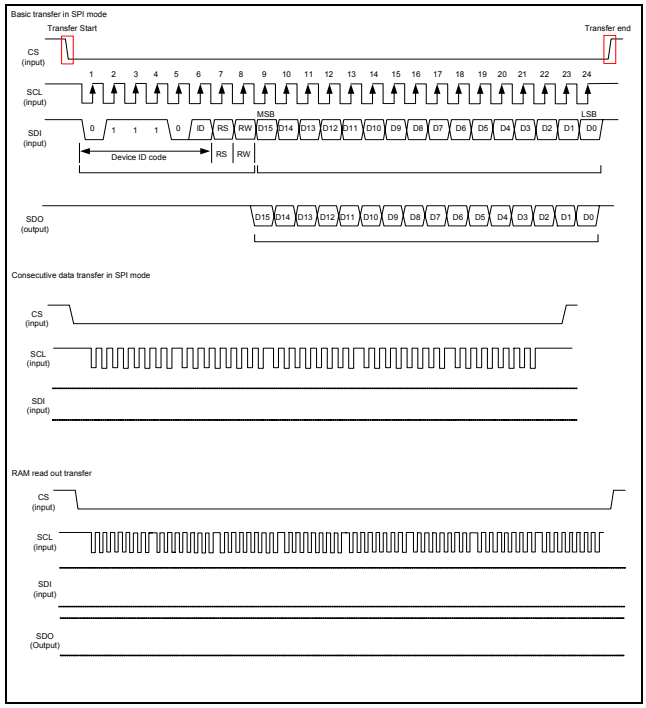


Figure 8-12

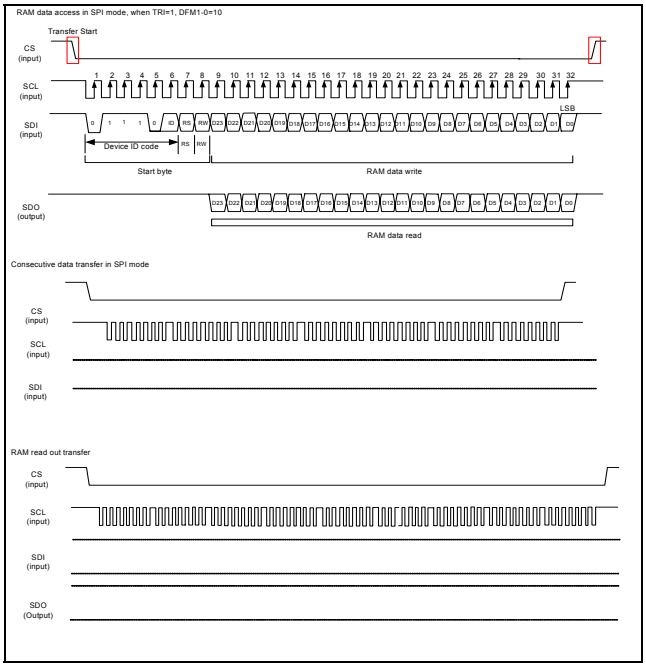


Figure 8-13

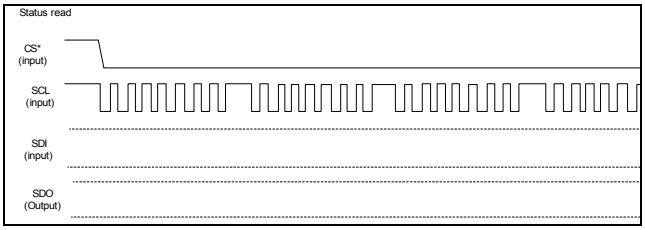


Figure 8-14

8.2. VSYNC Interface

The SPFD5420A also supports VSYNC interface for moving picture display, which is the system interface in synchronization with the frame-synchronizing signal (VSYNC). The VSYNC interface can display a moving picture without tremendous modification.

DM1-0 = “10” and RM = “0” can initialized VSYNC interface. In VSYNC interface mode, the internal display operation is synchronized with the VSYNC signal. In VSYNC interface mode, the graphic data are stored in GRAM to minimize the data transfer to overwrite on the moving picture GRAM area. **Figure 8-15** illustrates moving picture data transfer through VSYNC interface.

In VSYNC mode, Internal operation is executed in synchronization with the internal clock generated from internal oscillators and VSYNC input. Therefore the frame rate is determined by the frequency of VSYNC. SPFD5420A can access the internal RAM in high speed with less power consumption in VSYNC interface mode while using high-speed write mode

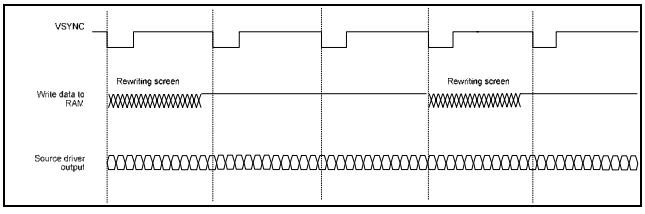


Figure 8-15

In VSYNC interface mode, the formula for Internal clock frequency and frame rate is shown below:

Input clock frequency = FrameRate x (DisplayLines + FrontPorch + BackPorch) x 16 x variance

Due to the possible cause of variances while set the internal clock frequency; be sure to complete the display operation in one VSYNC cycle.

8.3. External Display Interface

SPFD5420A also includes external (RGB) interface for displaying moving picture. External interface can be set by RIM1-0 bit. **Table 8-3** summarized the corresponding types of RGB interface with RM1-0 setting.

Table 8-3

RIM1	RIM0	RGB Interface	DB Pin
0	0	18-bit RGB interface	DB17-0
0	1	16-bit RGB interface	DB17-13, 11-1
1	0	6-bit RGB interface	DB17-12
1	1	Setting disabled	

RGB interface cab access SPFD5420A by VSYNC, HSYNC, ENABLE, DOTCLK and DB17-0 signals, where VSYNC is used for frame synchronization; HSYNC is used for line synchronization and ENABLE is served as the valid data synchronized signals. The RGB interface can be rewriting minimum necessary data to the GRAM area which need to be overwritten with use of window address function and high-speed write mode. It is necessary for RGB interface to set front and back porch periods after and before a display period, respectively. **Figure 8-16** illustrates the general timing for RGB interface. There are some constrain while using RGB interface. The following summarized the conditions,

(a) Partial display/ scroll function / interlace and graphics operation function are not available for RGB interface.

(b) In RGB interface VSYNC, HSYNC, and DOTCLK signals must be input through a display operation period.

(c) The setting of the NO1-0 bits, STD1-0 bits and EQ1-0 bits are based on DOTCLK in RGB interface mode. In 6-bit RGB interface mode, it takes 3 DOTCLK inputs to transfer one pixel. Be aware data transfer in units of 3 DOTCLK inputs in 6-bit RGB interface mode is necessary. Set the cycle of each signal in 6-bit interface mode (VSYNC, HSYNC ENABLE, DB17-0) to input 3x clock to complete data transfer in units of pixels.

(d) In RGB-I/F mode, while writing data to the internal RAM make sure to use the high-speed write mode (HWM = “1”)

(e) In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.

(f) In RGB interface mode, a GRAM address (DB17-0) is set in the address counter every frame on the falling edge of VSYNC.

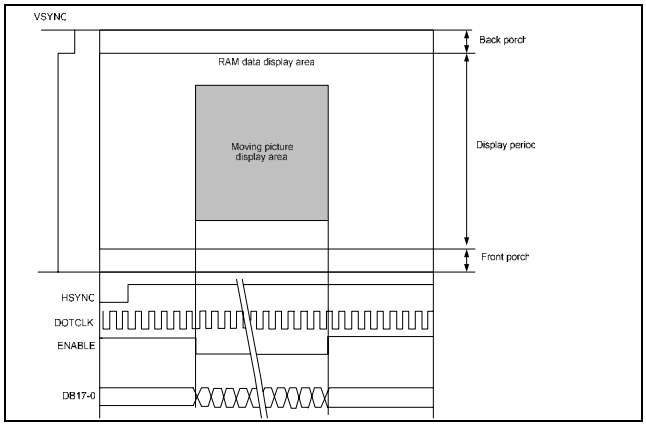


Figure 8-16

RGB interface includes ENABLE signal served as valid data synchronized signals. Moreover, the active level for ENABLE can be set by EPL. The EPL bit inverts the polarity of ENABLE signal. **Table 8-4** summarized the setting of EPL and ENABLE active level for GRAM accessing. Setting both EPL and ENABLE bits to automatically update RAM address in the AC is necessary while writing data to the GRAM.

Table 8-4

EPL	ENABLE	RAM Write	RAM Address
0	0	Enabled	Updated
0	1	Disabled	Retained
1	0	Disabled	Retained
1	1	Enabled	Updated

SPFD5420A can support 18-bit, 16-bit and 6-bit RGB interface. The detail timing diagram for 18-bit, 16-bit and 6-bit RGB interfaces are shown in **Figure 8-17** and **Figure 8-18** respectively.

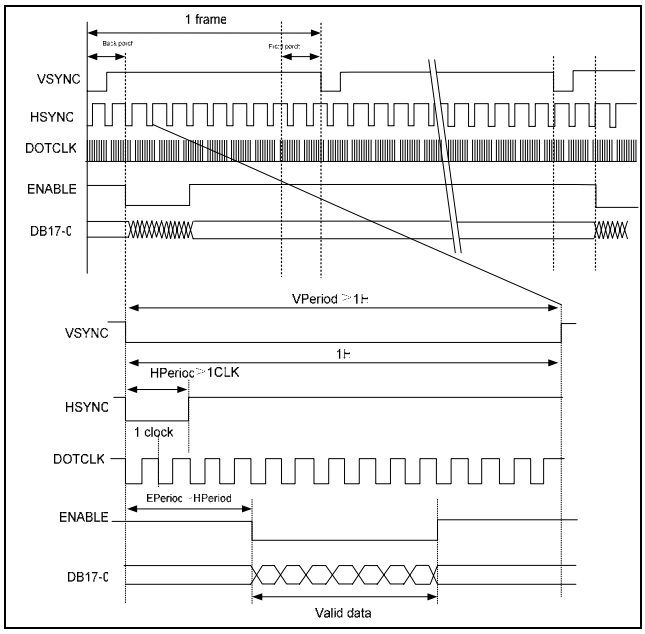


Figure 8-17

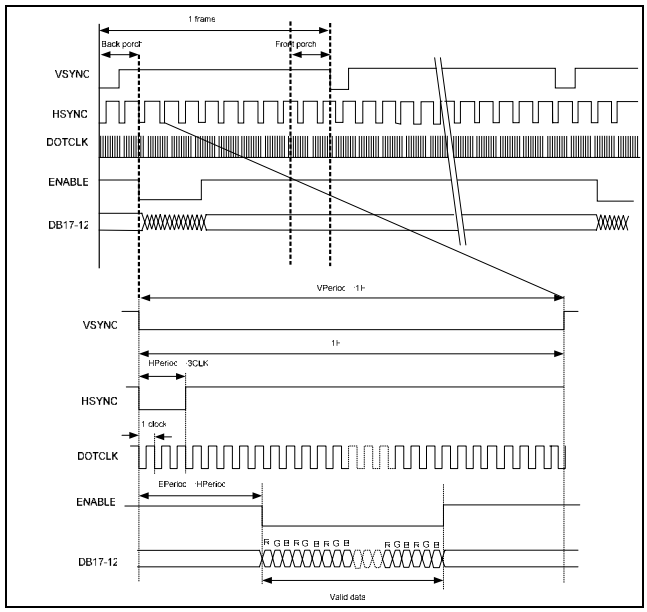


Figure 8-18

The RGB interface also has the window address function to transfer only minimum necessary data on the moving picture GRAM area, which can lower the power consumption and still can use system interface to rewrite data in still picture RAM area while displaying a moving picture. Setting RM = 0 while in RGB interface mode can make GRAM access CBIe through the system interface. When RGB interface accessing GRAM is desired, wait for one read/write bus cycle following by RM = 1 setting.

Figure 8-19 illustrates the timing diagram when displaying a moving picture through the RGB interface and rewriting data in the still picture GRAM area through the system interface.

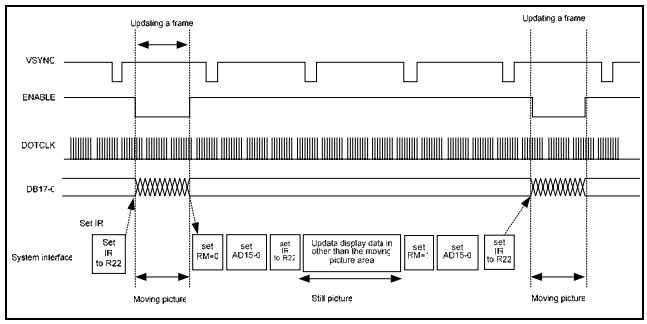


Figure 8-19

8.3.1. 6-bit RGB interface

RAM accessing format and data transmission synchronization of 6-bit RGB interface are shown in **Figure 8-20** and **Figure 8-21**, respectively.

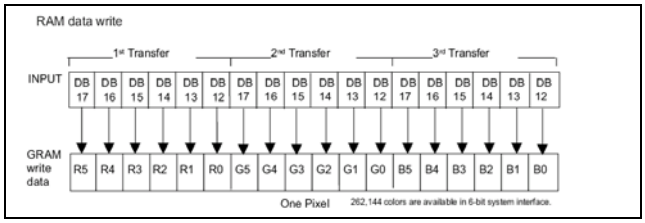


Figure 8-20

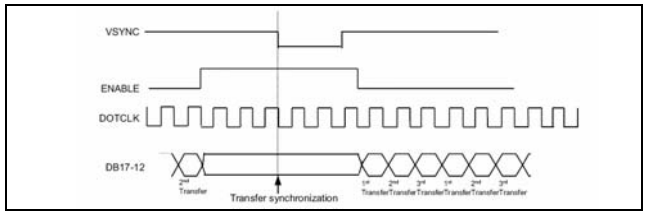


Figure 8-21

8.3.2. 16-bit RGB interface

RAM accessing format of 16-bit RGB interface are shown in **Figure 8-22**.

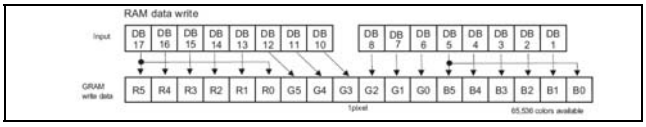


Figure 8-22

8.3.3. 18-bit RGB interface

RAM accessing format of 18-bit RGB interface are shown in **Figure 8-23**.

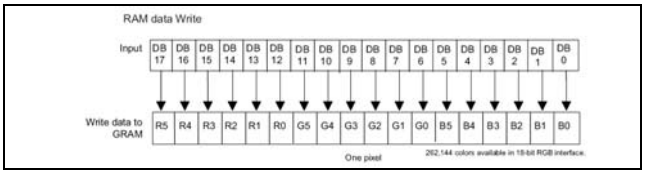


Figure 8-23

9. Display Feature Function:

9.1. FMARK function:

SPFDF5408A provided FMARK function which output signal to alert host MCU via FMARK I/O pad so that LCD display can avoid flicker effect. FMARK output position and onterval can be set by FMP[8:0] and FMI[2:0], respectively.

Figure 9-1 illustrated the FMARK output position when FMP[8:0]=9'h008.

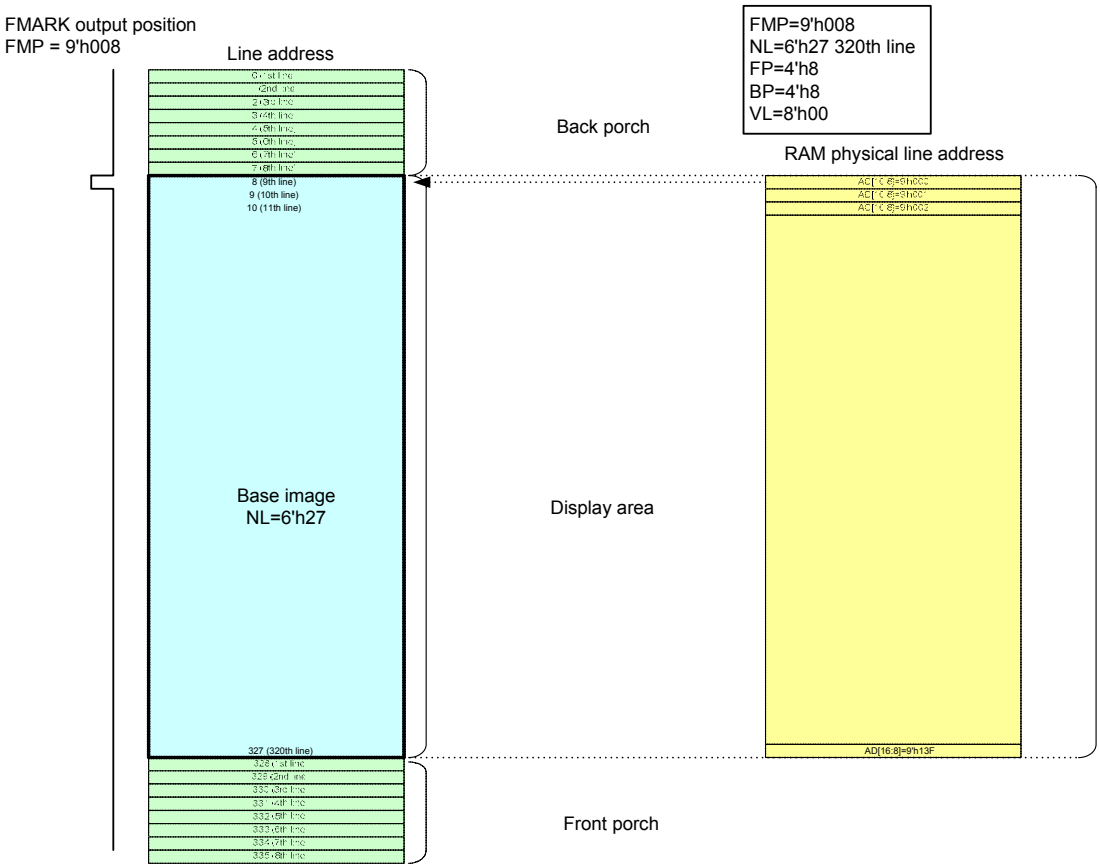
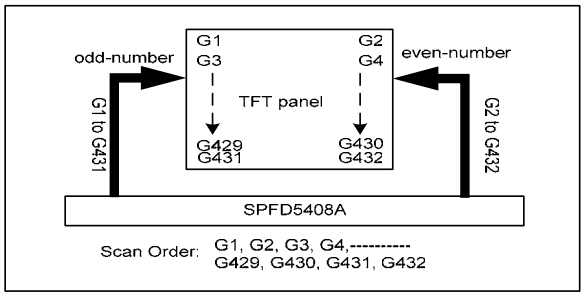
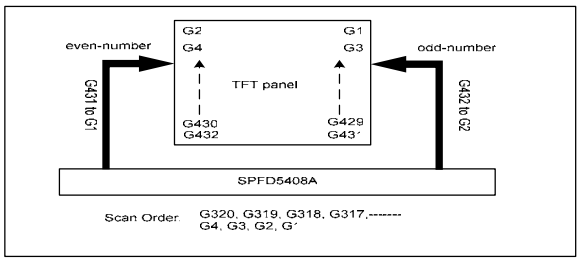
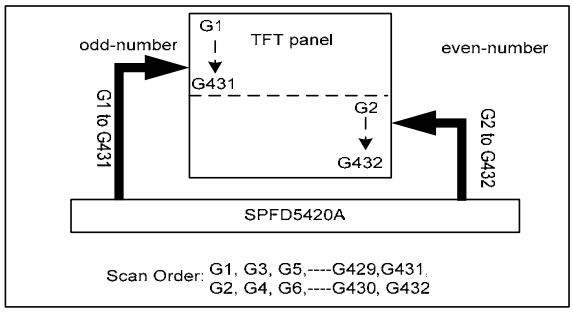
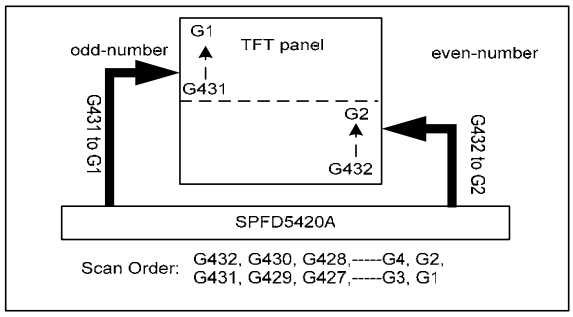


Figure 9-1 Example of FMARK signal.

9.2. Scan Mode function:

SM	GS	Scan Direction
0	0	
0	1	
1	0	
1	1	

9.3. Partial Display function:

SPFD5408 has partial display function feature which can provide only partial display for power saving purpose. Partial display function can be accessed by setting BSEE="0",. Moreover, 2 partial display area (partial image 1/ partial image 2) can be initialized by setted PTDE0="1" and PTDE1="1", respectively. The partial display area for partial image 1 and partial 2 can be set by PTSA0 / PTEA0 and PTSA1/ PTEA1, respectively. **Table 9-1** and **Figure 9-2** summarized the full and partial display function.

Table 9-1 Partial display function summary table

Case	Function Setting	Display area setting	Display Position
Full dsiplay	**BASEE="1" PTDE0="x" PTDE1="x"**	**(BSA,BEA)**	**-**
Partail image1:0n Partial image2:Off	**BASEE="0" PTDE0="1" PTDE1="0"**	**(PTSA0,PTEA0)**	**PTDP0**
Partail image1:Off Partial image2:On	**BASEE="0" PTDE0="0" PTDE1="1"**	**(PTSA1,PTEA1)**	**PTDP1**
Partail image1:On Partial image2:On	**BASEE="0" PTDE0="1" PTDE1="1"**	**(PTSA0,PTEA0) (PTSA1,PTEA1)**	**PTDP0 & PTDP1**

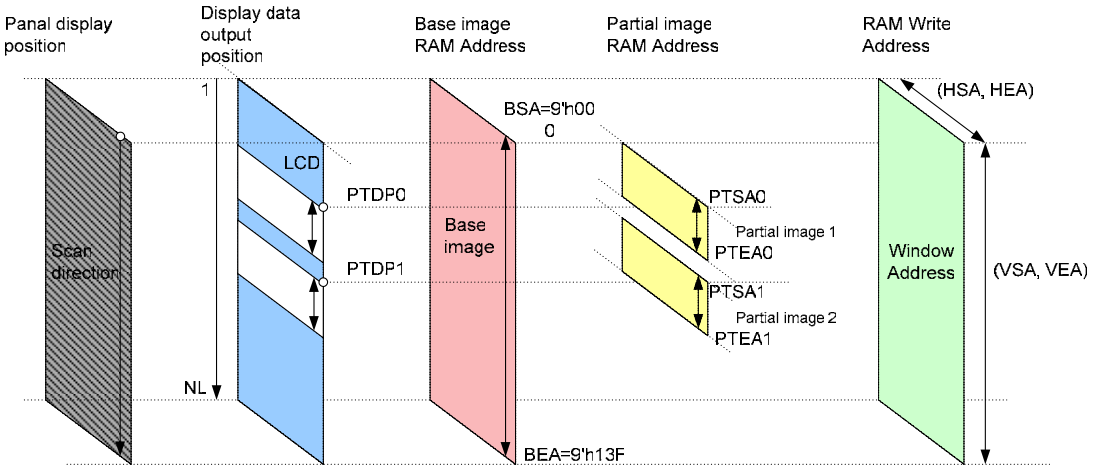


Figure 9-2 Partial display function diagram

Figure 9-3 indicated the case of NL[5:0] setting is < 6'h35 which active line is less than 432. Partial display image data can stored in not active area.

Figure 9-4 indicated the partial display area start position. The partial display area and start position can be set by (**PTSA0, PTEA0 , PTSA1, PTEA1) and (PTDP0, PTDP1).**

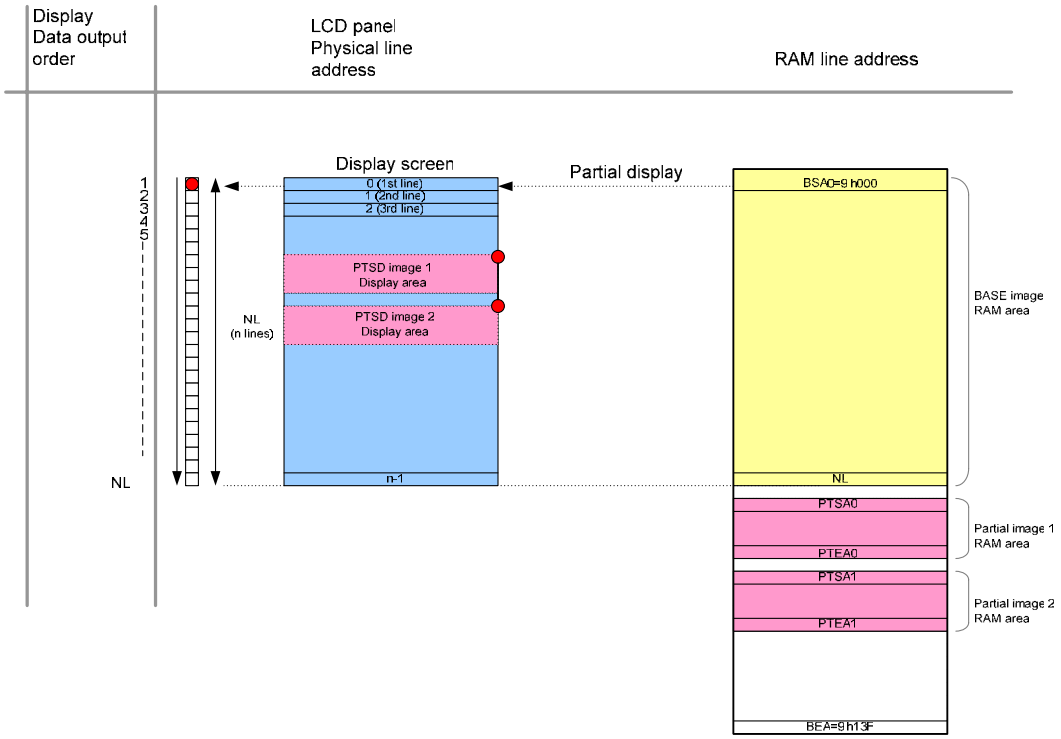


Figure 9-3 Example of NL[5:0] setting is < 6'h35 case

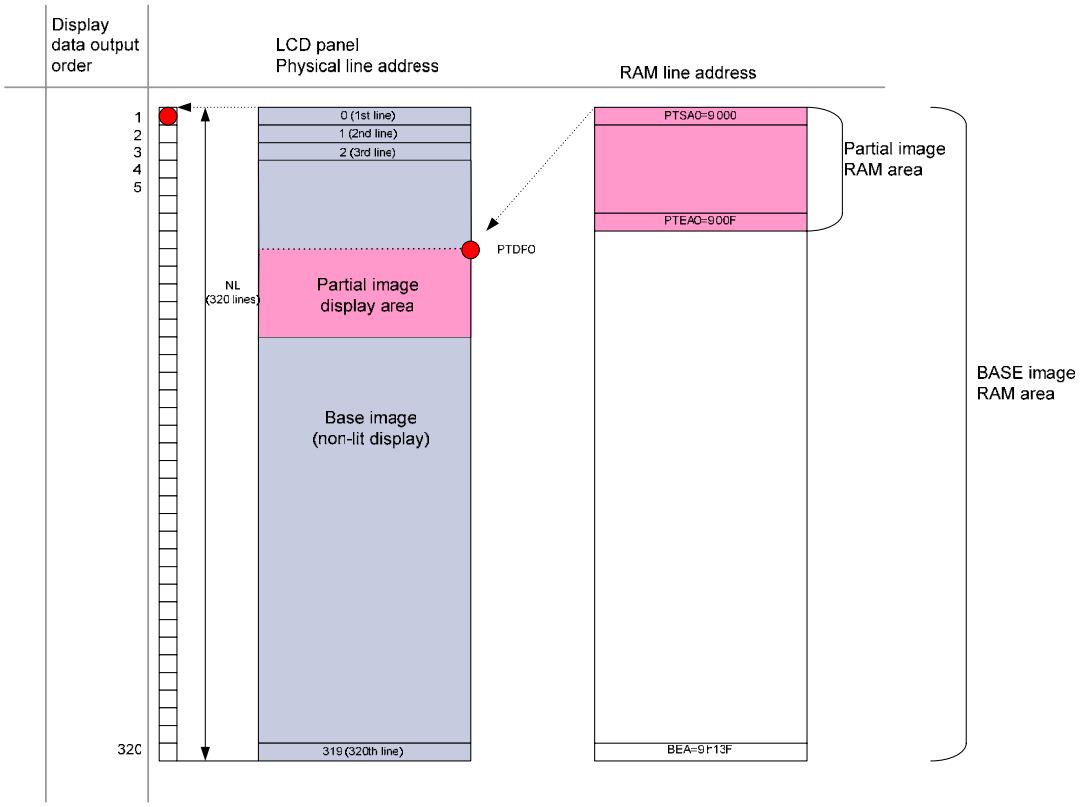


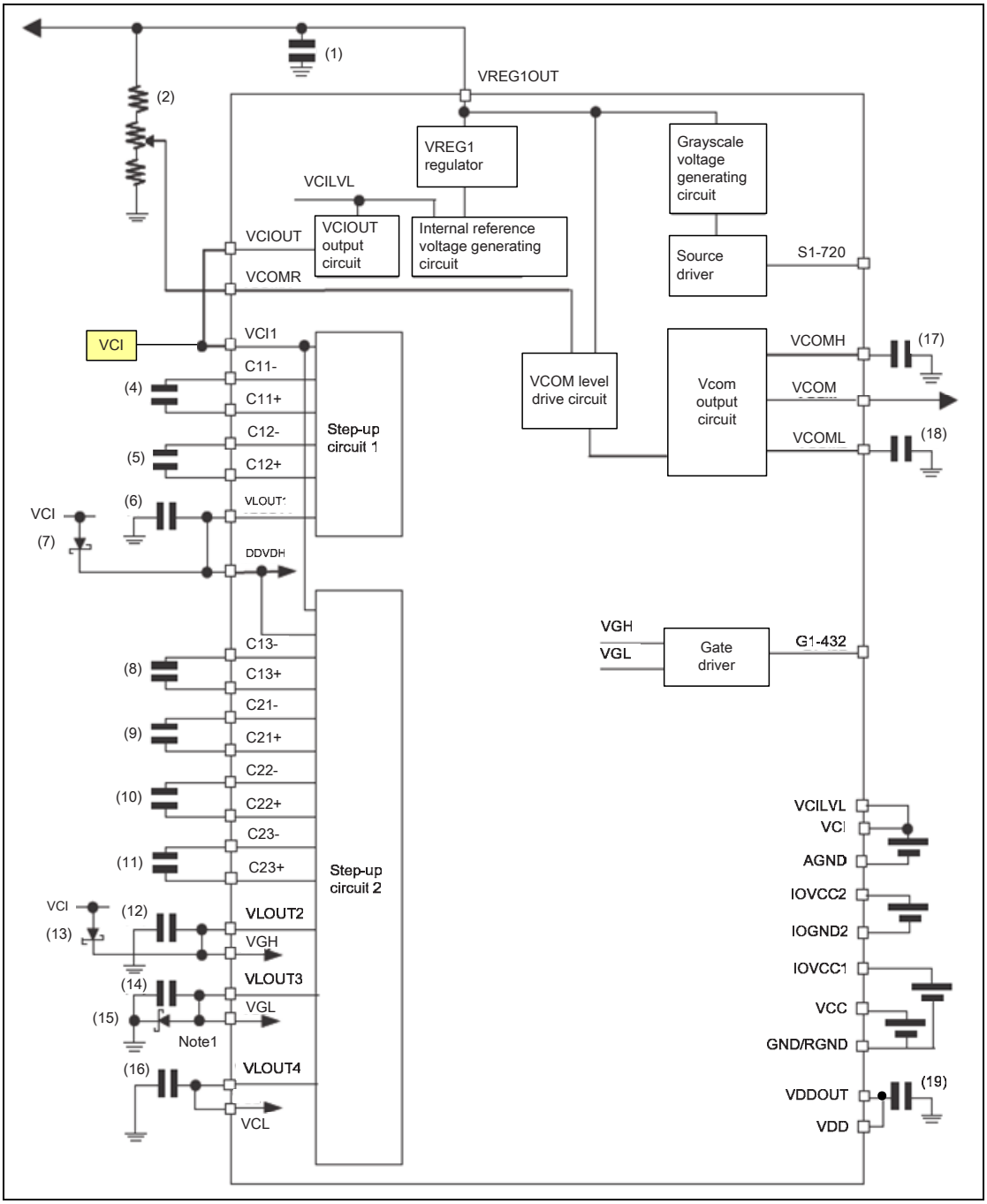
Figure 9-4 indicated the partial display area start position.

9.4. Gamma Correction functions:

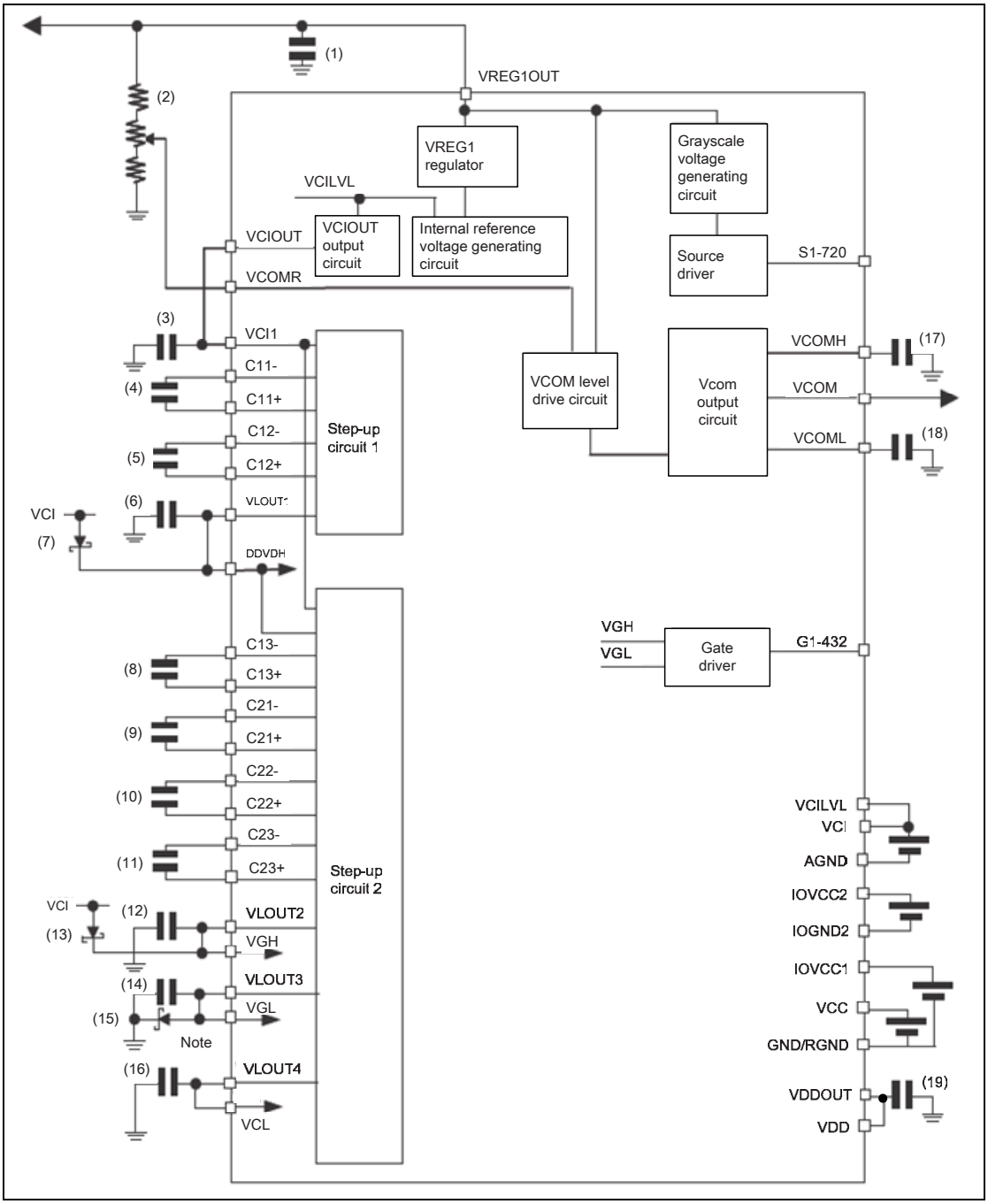
T.B.D.

10. Power Management System:

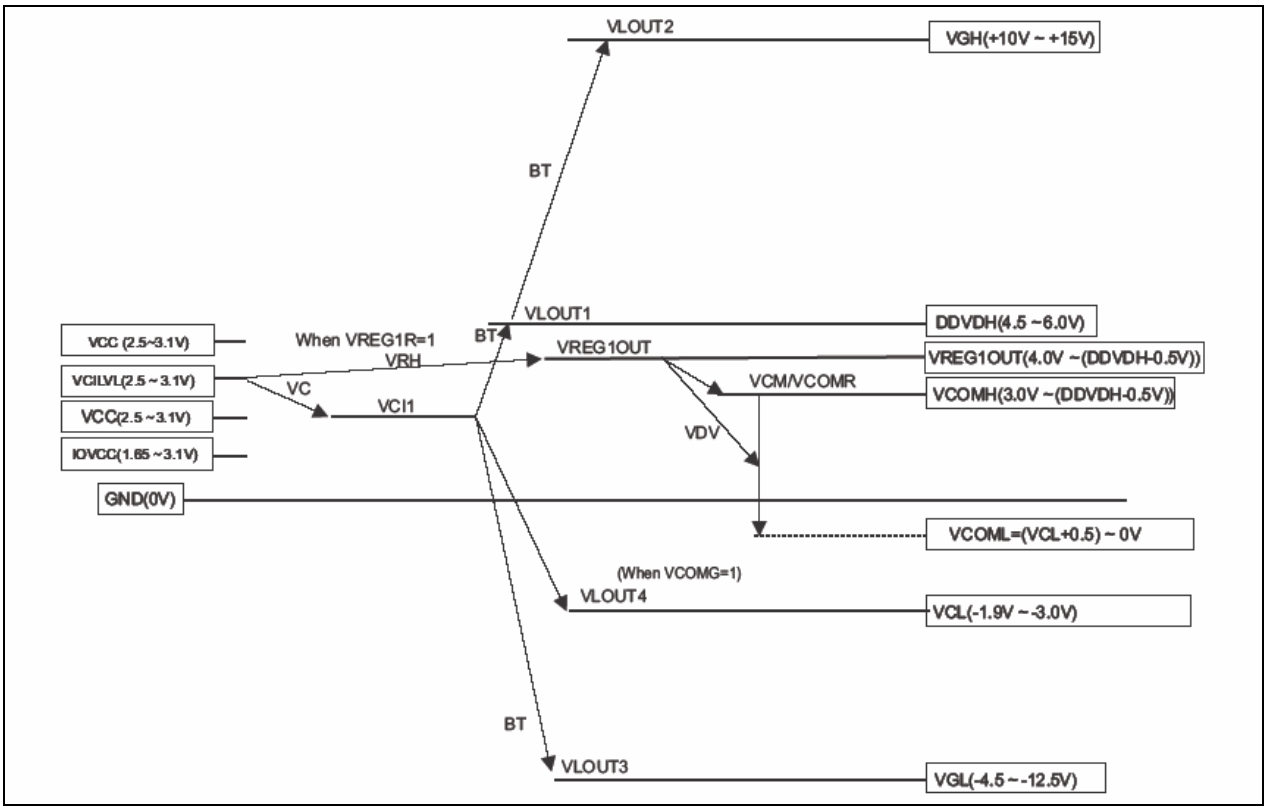
(a) VCI1=VCI direct input



(b) VCI1=VCIOUT



(c) Voltage Generation Diagram



11. Application circuits:

T.B.D.

12. Initial Code:

T.B.D.

13. Electrical Characteristics:

13.1. Absolute Maximum Ratings:

Table 13-1

Item	Symbol	Unit	Value	Note
Power Supply Voltage1	VCC,IOVCC	V	-0.3 ～+4.6	
Power Supply Voltage 2	VCI – AGND	V	-0.3 ～+4.6	
Power Supply Voltage 3	DDVDH – AGND	V	-0.3 ～+6.5	
Power Supply Voltage4	AGND – VCL	V	-0.3 ～+4.6	
Power Supply Voltage 5	DDVDH – VCL	V	-0.3 ～+9.0	
Power Supply Voltage7	AGND – VGL	V	-0.3 ～+14.0	
Power Supply Voltage 8	VGH– VGL	V	-0.3 ～+30.0	
Input Voltage	Vt	V	-0.3 ～IOVCC + 0.3	
Operating Temperature	Topr	℃	-40 ～+85	
Storage Temperature	Tstg	℃	-55 ～+110	

13.2. DC Characteristics

Table 13-2 VCC= 2.50V～3.10V，IOVCC=1.65V～ 3.10V，Ta=-40℃～+85℃

Item	Sym bol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input High level voltage	VIH	V	IOVCC=1.65V～3.10V	0.8xIOVCC	-	IOVCC	
Input Low level voltage	VIL	V	IOVCC=1.65V～3.10V	-0.3	-	0.2xIOVCC	
Output ”High” level voltage 1 （DB0-17）	VOH	V	IOVCC=1.65V～3.10V, IOH=-0.1mA	0.8xIOVCC	-	-	
Output ”Low” level voltage 1 （DB0-17）	VOL	V	IOVCC=1.65V～3.10V, IOL=0.1mA	-	-	0.2xIOVCC	
I/O leak current	ILI1	μA	Vin=0～IOVCC1	-1	-	1	
Current Consumption (IOVCC-IOGND)+(VCC-GND) Normal operation mode (262k-colors, display operation)	IOP1	μA	fosc=678kHz (432 line drive), IOVCC=VCC=3.00V fFLM=60Hz Ta=25℃ RAM data: 18’h000000	-	175	-	
Current Consumption (IOVCC-IOGND)+(VCC-GND) 8-color mode, 64-line, partial display operation	Iop2	μA	fosc=376kHz (64-line, partial display), IOVCC=VCC=3.00V, fFLM=40Hz Ta=25℃ RAM data: 18h’000000	-	140	-	

13.3. AC Characteristics

VCC= 2.50V～3.10V，IOVCC=1.65V～3.10V，Ta=-40℃～+85℃

13.3.1. Clock Characteristics

Table 13-3

Item	Symbol	Unit	Timing Diagram	Min.	Typ.	Max.	Note
RC Oscillation clock	fosc	kHz	IOVCC = VCC = 3.0V, 25°C	611	678	745	

13.3.2. 80-System Bus Interface Timing Characteristics

Table 13-4 Normal write operation (HWM=0), IOVCC=1.65V~3.10V

Item	Symbol		Unit	Min.	Typ.	Max.
Bus cycle time	Write	tCYCW	ns	150	-	-
	Read	tCYCR	ns	450	-	-
Write low-level pulse width		PWLW	ns	55	-	-
Read low-level pulse width		PWLR	ns	170	-	-
Write high-level pulse width		PWHW	ns	70	-	-
Read high-level pulse width		PWHR	ns	250	-	-
Write/Read rise/ fall time		tWRr, WRf	ns	-	-	10
Setup time	Write (RS to CS*,WR*)	tAS	ns	0	-	-
	Read (RS to CS*, RD*)		ns	10	-	-
Address Hold Time		tAH	ns	2	-	-
Write data setup time		tDSW	ns	25	-	-
Write data hold time		tH	ns	10	-	-
Read data delay time		tDDR	ns	-	-	150
Read data hold time		tDHR	ns	5	-	-

13.3.3. Clock-synchronized Serial Interface Timing Characteristics

Normal Write Function (HWM=0), High-speed Write Function (HWM=1), IOVCC=1.65~3.10V)

Table 13-5

Item	Symbol		Unit	Min.	Typ.	Max.
SerialTime Clock Cycle	Write (received)	tSCYC	ns	100	-	20.000
	Read (transmitted)	tSCYC	ns	350	-	20.000
Serial Clock high-level width	Write (received)	tSCH	ns	40	-	-
	Read (transmitted)	tSCH	ns	150	-	-
Serial Clock low-level width	Write (received)	tSCL	ns	40	-	-
	Read (transmitted)	tSCL	ns	150	-	-
Serial clock rise/fall time		tSCr, tSCf	ns	-	-	20
Chip select setup time		tCSU	ns	20	-	-
Chip select hold time		tCH	ns	60	-	-
Serial input data setup time		tSISU	ns	30	-	-
Serial input data hold time		tSIH	ns	30	-	-
Serial output data delay time		tSOD	ns	-	-	130
Serial output data hold time		tSOH	ns	5	-	-

13.3.4. Reset Timing Characteristics (IOVCC=1.65~3.10V)

Table 13-6

Item	Symbol	Unit	Min.	Typ.	Max.
Reset low-level width	tRES	ms	1	—	—
Reset rise time	trRES	μs	—	—	10

13.3.5. RGB Interface Timing Characterics

18-/ 16- bit RGB interface (HWM= 1), IOVCC=1.65~3.10V

Table 13-7

Item	Symbol	Unit	Min.	Typ.	Max.
VSYNC/HSYNC Setup time	TSYNCS	clock	0	-	1
ENABLE Setup time	TENS	ns	10	-	-
ENABLE Hold time	TENH	ns	20	-	-
DOTCLK low-level pulse width	PWDL	ns	40	-	-
DOTCLK high-level pulse width	PWDH	ns	40	-	-
DOTCLK cycle time	TCYCD	ns	100	-	-
Data setup time	TPDS	ns	10	-	-
Data hold time	TPDH	ns	40	-	-
DOTCLK, VSYNC and HSYNC rise/fall time	Trgbr Trgbf	ns	-	-	25

6-bit RGB interface (HWM = 1), IOVCC=1.65~3.10V

Table 13-8

Item	Symbol	Unit	Min.	Typ.	Max.
VSYNC/HSYNC setup time	TSYNCS	clock	0	-	1
ENABLE setup time	TENS	ns	10	-	-
ENABLE hold time	TENH	ns	25	-	-
DOTCLK low-level pulse width	PWDL	ns	25	-	-
DOTCLK high-level pulse width	PWDH	ns	25	-	-
DOTCLK cycle time	TCYCD	ns	60	-	-
Data setup-time	TPDS	ns	10	-	-
Data hold time	TPDH	ns	25	-	-
DOTCLK, VSYNC, and HSYNC rise/fall time	Trgb Ttrgbf	ns	-	-	25