



# ***Crystalfontz America, Incorporated***

## GRAPHIC LCD MODULE SPECIFICATIONS



One-inch diagonal active area. ZIF connector cable is shown folded behind the module.

Crystalfontz Model Number	<b>CFAO4265A-TFK</b>
Hardware Version	<b>Version A, October 2011</b>
Data Sheet Version	<b>Version 1.0, October 2011</b>
Product Pages	<a href="http://www.crystalfontz.com/product/CFAO4265ATFK.html">www.crystalfontz.com/product/CFAO4265ATFK.html</a>

### **Crystalfontz America, Incorporated**

12412 East Saltese Avenue  
Spokane Valley, WA 99216-0357

Phone: (888) 206-9720

Fax: (509) 892-1203

Email: [techinfo@crystalfontz.com](mailto:techinfo@crystalfontz.com)

URL: [www.crystalfontz.com](http://www.crystalfontz.com)



## REVISION HISTORY

HARDWARE	
2011/10/21	Current hardware version: <b>vA</b> New module.

DATA SHEET	
2011/10/21	Data Sheet version: <b>v1.0</b> New Data Sheet.

### The Fine Print

Certain applications using CrystalFontz America, Inc. products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications"). CRYSTALFONTZ AMERICA, INC. PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. Inclusion of CrystalFontz America, Inc. products in such applications is understood to be fully at the risk of the customer. In order to minimize risks associated with customer applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazard. Please contact us if you have any questions concerning potential risk applications.

CrystalFontz America, Inc. assumes no liability for applications assistance, customer product design, software performance, or infringements of patents or services described herein. Nor does CrystalFontz America, Inc. warrant or represent that any license, either express or implied, is granted under any patent right, copyright, or other intellectual property right of CrystalFontz America, Inc. covering or relating to any combination, machine, or process in which our products or services might be or are used.

The information in this publication is deemed accurate but is not guaranteed.

Company and product names mentioned in this publication are trademarks or registered trademarks of their respective owners.

Copyright © 2011 by CrystalFontz America, Inc., 12412 East Saltese Avenue, Spokane Valley, WA 99216-0357 U.S.A.



# CONTENTS

<b>MAIN FEATURES</b>	<b>5</b>
Features	5
Module Classification Information	5
Ordering Information	6
<b>MECHANICAL SPECIFICATIONS</b>	<b>7</b>
Physical Characteristics	7
Module Outline DrawingS	8
ZIF Connectors	10
<b>ELECTRICAL SPECIFICATIONS</b>	<b>11</b>
System Block Diagram	11
Driving Methods	12
Absolute Maximum Ratings	12
DC Characteristics	13
Details of Interface Pin Functions	14
Photo with Pins Labeled (Contact Side of FFC)	16
ESD (Electro-Static Discharge)	17
Sitronix ST7565P Controller	17
<b>OPTICAL SPECIFICATIONS</b>	<b>17</b>
Test Conditions and Definitions for Optical Characteristics	17
<b>LED BACKLIGHT</b>	<b>20</b>
Location of A (LED+) and K (LED-)	20
Backlight Characteristics	21
Circuit Example Using LED Driver NCP5007	22
<b>PRODUCT RELIABILITY</b>	<b>23</b>
Module Reliability	23
Module Longevity (EOL / Replacement Policy)	23
<b>CARE AND HANDLING PRECAUTIONS</b>	<b>24</b>
ESD (Electro-Static Discharge)	24
Design and Mounting	24
Avoid Shock, Impact, Torque, or Tension	25
Cleaning	25
Operation	25
Storage and Recycling	25
<b>APPENDIX A: QUALITY ASSURANCE STANDARDS</b>	<b>26</b>
<b>APPENDIX B: SITRONIX ST7565P CONTROLLER SPECIFICATION SHEET</b>	<b>29</b>



## LIST OF FIGURES

Figure 1. Module Outline Drawings (2 pages) -----	8
Figure 2. System Block Diagram -----	11
Figure 3. Photo with Pins Labeled (Contact Side of FFC)-----	16
Figure 4. Definition of Operation Voltage ( $V_{OP}$ ) (Positive)-----	18
Figure 5. Definition of Response Time ( $T_r$ , $T_f$ ) (Positive) -----	18
Figure 6. Definition of Horizontal and Vertical Viewing Angles ( $CR>2$ )-----	19
Figure 7. 6:00 O’Clock and 12:00 O’Clock Viewing Angles-----	19
Figure 8. Location of Backlight Tabs A and K -----	20
Figure 9. Circuit Example Using LED Driver NCP5007 -----	22
Figure 10. Limit FFC Bend Radius-----	24



# MAIN FEATURES

## FEATURES

- ☐ 42 x 65 module consists of an LCD panel, a COG (Chip On Glass) driver IC, and an FFC (Flat Flexible Cable) that mates with [ZIF Connectors \(Pg. 10\)](#).
- ☐ Module Dimensions.
  - Active Area is 13.84 (W) x 21.43 (H) millimeters.
  - Overall dimension in millimeters is 22.40 (W) x 34.00 FFC folded (H) x 4.8 maximum excluding backlight tabs (D).
- ☐ Built-in [Sitronix ST7565P](#) or compatible controller.
- ☐ SPI (4-wire Serial Peripheral Interface) interface.
- ☐ White edge-lit LED backlight with FSTN light-grey glass positive transfective mode display. Displays dark pixels on an illuminated white background.
- ☐ Wide temperature range for operation is -20°C to +70°C.
- ☐ Positive mode display is sunlight readable and also readable in dark areas.
- ☐ RoHS compliant.
- ☐ Factories have ISO certification.
- ☐ Our partner manufacturer has completed a Declaration of Conformity Data Request: 2002/95/EC Restriction of Hazardous Substances (RoHS) and REACH EC/1097-2006 SVHC Annex 1.

## MODULE CLASSIFICATION INFORMATION



CFA   O   42   65   A   -   T   F   K  
①   ②   ③   ④   ⑤   -   ⑥   ⑦   ⑧

①	Brand	CrystalFontz America, Inc.
②	Display Type	O – Chip On Glass
③	Number of Pixels (Width)	42 Pixels
④	Number of Pixels (Height)	65 Pixels
⑤	Model Identifier	A
⑥	Backlight Type & Color	T – LED, white
⑦	Fluid Type, Image (Positive or Negative), & LCD Glass Color	F – FSTN, positive light grey
⑧	Polarizer Film Type, Wide Temperature (WT) Range, & View Angle (O 'Clock)	K – Transfective, WT, 12:00 <sup>1</sup>

<sup>1</sup>Note: For more information on Viewing Angle, see [Definition of 6:00 O'clock and 12:00 O'clock Viewing Angles \(Pg. 19\)](#).



## ORDERING INFORMATION

PART NUMBER	FLUID	LCD GLASS COLOR	IMAGE	POLARIZER FILM	BACKLIGHT COLOR/TYPE
CFAO4265A-TFK	FSTN	light grey	positive	transflective	white edge LEDs 
<i>Additional variants (same form factor, different LCD mode or backlight):</i>					
CFAO4265A-TTL	FSTN	black	negative	transmissive	white edge LEDs 



## MECHANICAL SPECIFICATIONS

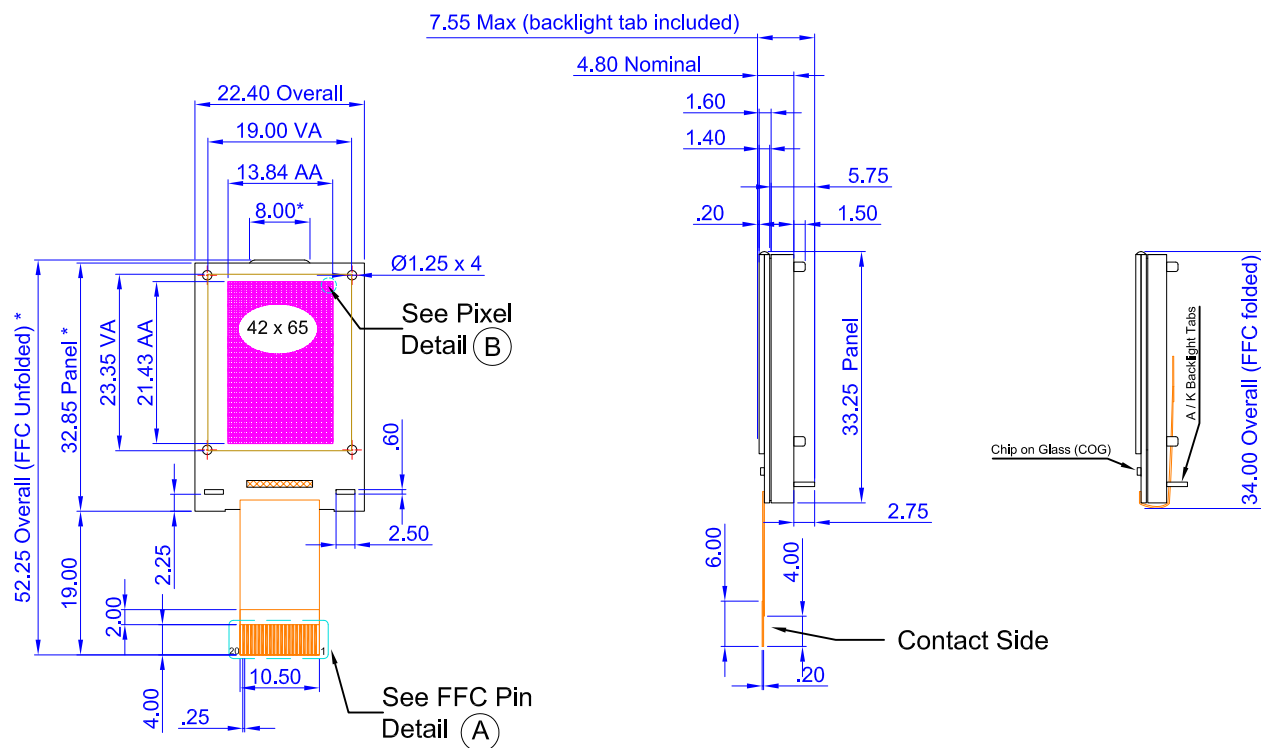
---

### PHYSICAL CHARACTERISTICS

ITEM	SIZE
Pixels	
Number of Pixels	42 x 65 = 2,730 pixels
Pixel Size	0.02 (W) x 0.02 (H) mm
Pixel Pitch	0.31 (W) x 0.31 (H) mm
Viewing Area Width and Height	Millimeters: 19.0 (W) x 23.35 (H) mm Inches: 0.75" (W) x 0.92" (H)
Active Area Diagonal	Millimeters: 25.5 mm Inches: 1.00"
Active Area Width and Height	Millimeters: 13.84 (W) x 21.43 (H) mm Inches: 0.54" (W) x 0.84" (H)
Overall Module Outline Width	Millimeters: 22.40 (W) mm Inches: 0.88" (W)
Overall Module Outline Height	<i>With FFC folded:</i> Millimeters: 34.00 (H) mm Inches: 1.33" (H)  <i>With FFC unfolded:</i> Millimeters: 52.25 (H) mm Inches: 2.06" (H)
Module Depth	<i>Nominal (excludes backlight tabs):</i> Millimeters: 4.80 (D) mm Inches: 0.19" (D)  <i>Maximum (includes backlight tabs):</i> Millimeters: 7.55 (D) mm Inches: 0.30" (D)
FFC Bend Radius	≥R2.0 mm
Weight	6 grams (typical)

## MODULE OUTLINE DRAWINGS

Figure 1. Module Outline Drawings (2 pages)

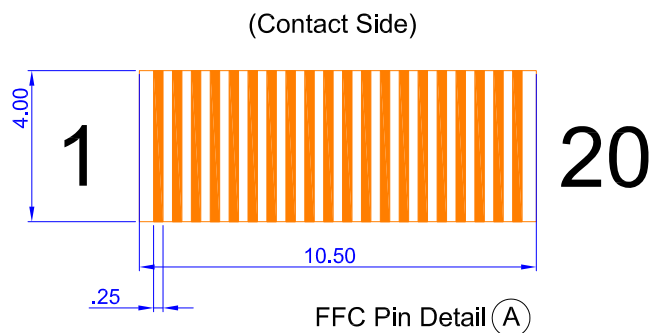


Note:

1. Tolerance is  $\pm 0.3$  mm unless specified
2. FFC = Flat Flexible Cable (Shape may vary slightly)
3. VA = Viewing Area
4. AA = Active Area
5. 1" Diagonal Viewing Area
6. \* Tolerances for bump at top may vary

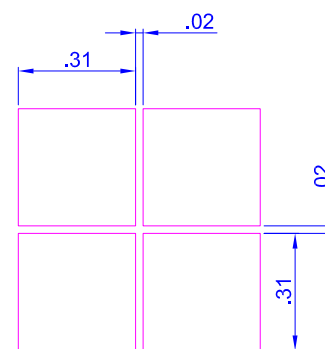
TOLERANCE	
>0-6 ±0,10	>120-300 ±0,50
>6-30 ±0,20	>300-500 ±0,80
>30-120 ±0,30	>500 ±1,20
ANGLE: ±3,0°	





PIN DESCRIPTION:

PIN	SYMBOL
1	CS
2	RST
3	A0
4	SCL
5	SI
6	VDD (V <sub>Logic</sub> )
7	VDD (V <sub>Logic</sub> )
8	VSS (GND)
9	VSS (GND)
10	V <sub>OUT</sub>
11	CAP3P
12	CAP1N
13	CAP1P
14	CAP2P
15	CAP2N
16	V4
17	V3
18	V2
19	V1
20	V0



Note:

1. Tolerance is  $\pm 0.3$  mm unless specified
2. FFC = Flat Flexible Cable (Shape may vary slightly)
3. VA = Viewing Area
4. AA = Active Area
5. 1" Diagonal Viewing Area

Copyright Crystalfontz America, Inc.



copyright © 2010 by  
**Crystalfontz America, Inc.**  
[www.crystalfontz.com/products/](http://www.crystalfontz.com/products/)

Part No.(s): CFAO4265A-TFK  
CFAO4265A-TTL

Scale:  
Not to scale  
Units:  
Millimeters

Drawing Number:  
CFAO4265A\_master  
Date:  
2011/10/21

Hardware Rev.:  
vA  
Sheet:  
2 of 2



## ZIF CONNECTORS

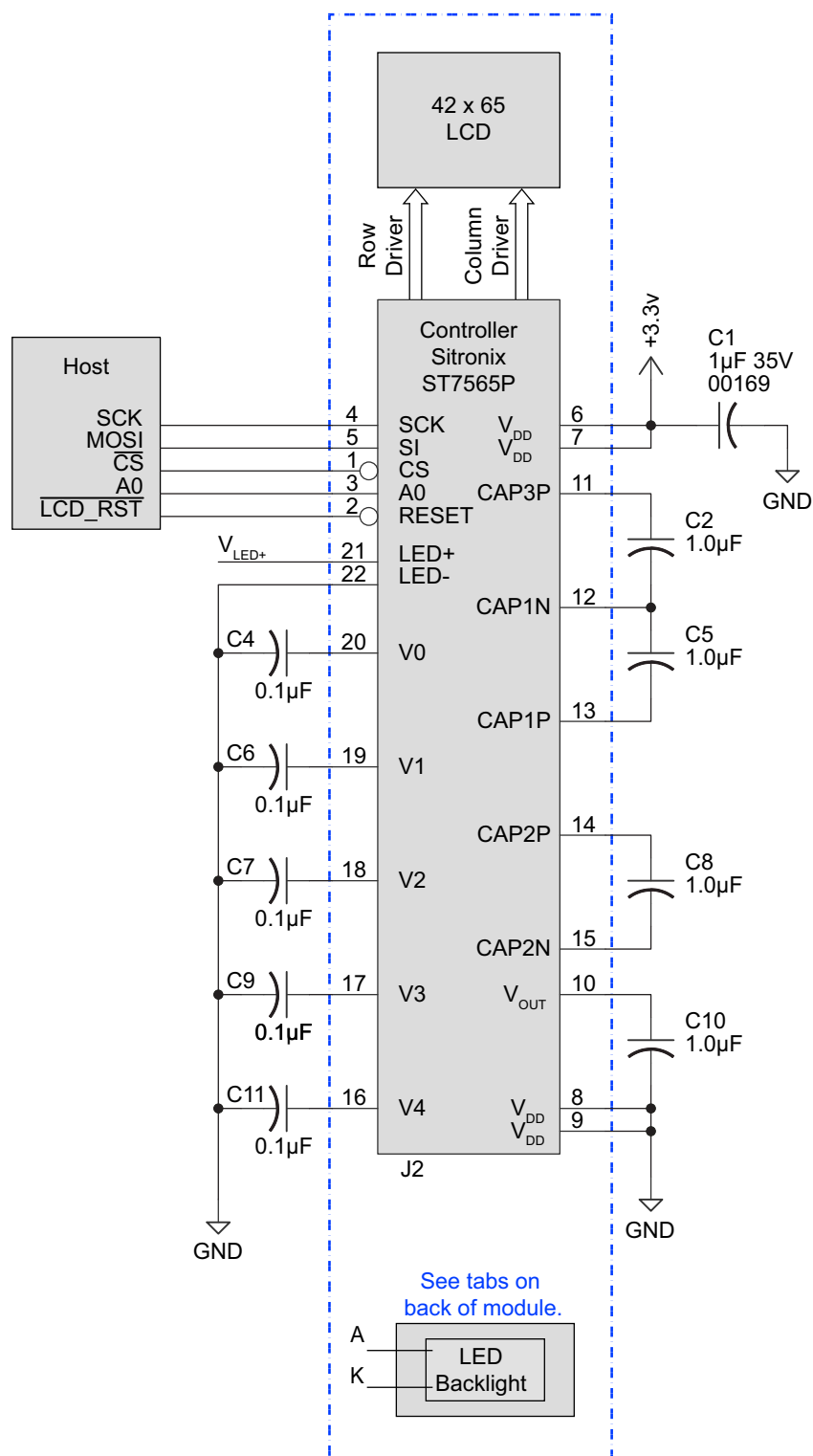
Choices for ZIF connectors include these Hirose connectors from Digi-Key:

- [Digi-Key HFN420CT-ND, Hirose Electric Co Ltd. FH19C-20S-0.5SH\(05\)](#)
- [Digi-Key HFK120CT-ND, Hirose Electric Co Ltd. FH12A-20S-0.5SH\(55\)](#)
- [Digi-Key HFJ120CT-ND, Hirose Electric Co Ltd. FH12-20S-0.5SH\(55\)](#)



## ELECTRICAL SPECIFICATIONS

### SYSTEM BLOCK DIAGRAM



You must provide and connect capacitors C1 to C11 in order for the Sitronix ST7565 controller to generate the supply voltages for the LCD.

Figure 2. System Block Diagram

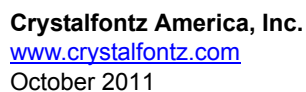


## DRIVING METHODS

DRIVING METHOD	SPECIFICATION
Duty	1/65
Bias	1/9

## ABSOLUTE MAXIMUM RATINGS

ABSOLUTE MAXIMUM RATINGS	SYMBOL	MINIMUM	MAXIMUM
Operating Temperature*	$T_{OP}$	-20°C	+70°C
Storage Temperature*	$T_{ST}$	-30°C	+80°C
Humidity (Noncondensing)	RH	0%	90%
Input Voltage	$V_I$	0v	$V_{LOGIC}$
Supply Voltage for Logic	$V_{DD}$	-0.3v	+3.6v
Supply Voltage for LCD	$V_{DD}-V_O$	-0.3v	+14.5v
<i>Note: Extended exposure to the absolute maximum ratings listed above may affect device reliability. Stresses beyond those listed above can cause permanent damage.</i>			



	DC CHARACTERISTICS	TEST CONDITIONS	SYMBOL	MINIMUM	TYPICAL	MAXIMUM
CONTROLLER AND BOARD	Supply Voltage for Logic	TOP = -20°C to +70°C	$V_{DD} - GND$		+3.0v	+3.3v
	Input High Voltage	$V_{DD} = +3.0$	$V_{IH}$	+2.0v		$V_{Logic}$ ( $V_{DD}$ )
		$V_{DD} = +3.0v$		+0.8 * $V_{DD}$ $V_{DD} = +3.0v$ $V_{IH} = +2.4v$		
	Input Low Voltage		$V_{IL}$	0v (GND)		+0.2v
	Output High Voltage		$V_{OH}$	+0.8 * $V_{DD}$ $V_{DD} = +3.0v$ $V_{IH} = +2.4v$		$V_{Logic}$ ( $V_{DD}$ )
	Output Low Voltage		$V_{OL}$	0v (GND)		+0.2v
	Supply Current	Logic only, not including backlight	$V_{LOGIC}$	0.6 mA	0.8 mA	1.5 mA
LCD GLASS	Supply voltage for driving LCD	$T_A = +25^\circ C$			+9.5v	

For detailed information, see DC Characteristics in [APPENDIX B: SITRONIX ST7565P CONTROLLER SPECIFICATION SHEET \(Pg. 29\)](#).



## DETAILS OF INTERFACE PIN FUNCTIONS

PIN	SIGNAL	LEVEL	DIRECTION	DESCRIPTION
1	$\overline{CS}$	H/L	I	<p><i>Low:</i> Controller chip is selected. Communications with the host is possible.</p> <p><i>High:</i> Controller chip is not selected. Host interface signals are ignored by the controller.</p>
2	$\overline{RST}$	L	I	<p>Reset signal input.</p> <p><i>Low:</i> Display controller is reset. The <math>\overline{RST}</math> pin should be pulsed low shortly after power is applied.</p> <p><i>High:</i> The <math>\overline{RST}</math> pin should be brought high for normal operation.</p>
3	A0	H/L	I	<p><i>R/W = Low:</i></p> <p>A0 = High: Command Write.</p> <p>A0 = Low: Data Write.</p> <p><i>R/W = High:</i></p> <p>A0 = High: Status Read.</p> <p>A0 = Low: Data Read.</p>
4	SCL		I	Display clock input.
5	SI		I	Serial data input.
6-7	V <sub>DD</sub> (V <sub>LOGIC</sub> )	+3.3v	–	Supply voltage for logic.
8-9	V <sub>SS</sub> (GND)	0v	–	Ground. Must be connected to an external ground.
10	V <sub>OUT</sub>		O	DC/DC voltage converter. Connect a capacitor between this terminal and V <sub>SS</sub> (GND) or V <sub>DD</sub> (V <sub>LOGIC</sub> ).
11	CAP3P			DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
12	CAP1N			DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1P terminal.
13	CAP1P			DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
14	CAP2P			DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.



PIN	SIGNAL	LEVEL	DIRECTION	DESCRIPTION
15	CAP2N			DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2P terminal.
16-20	V4-V0			Multilevel power supply to drive the LCD. The voltage settings are selected using the LCD bias set command.
<i>Note: Backlight pins A (LED+) and K (LED-) are separate tabs on the back of the module. See figure <a href="#">Location of Backlight Tabs A and K (Pg. 20)</a>.</i>				



## PHOTO WITH PINS LABELED (CONTACT SIDE OF FFC)

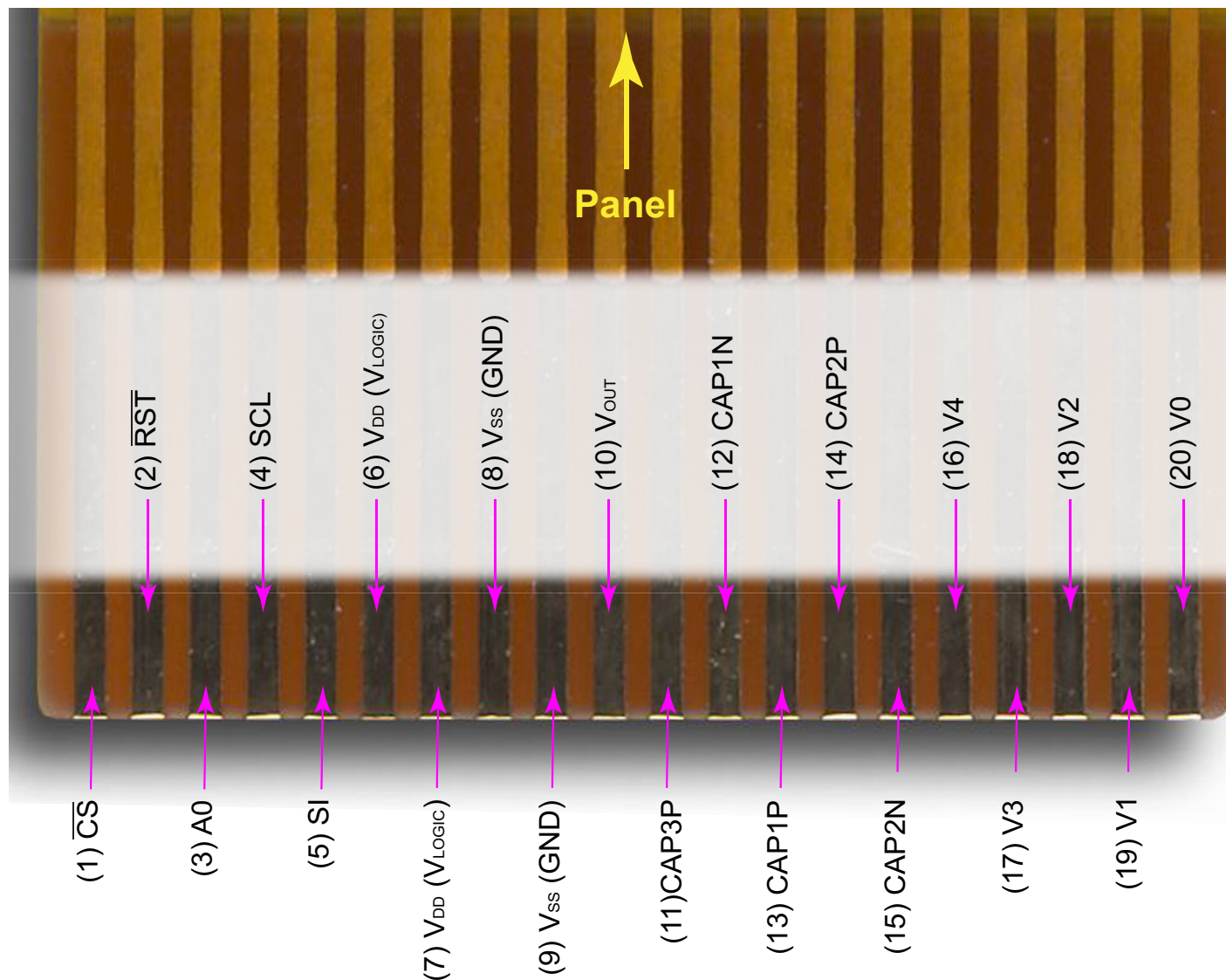


Figure 3. Photo with Pins Labeled (Contact Side of FFC)

For location of backlight connections, see A (LED+) and K (LED+) on tabs in [LED BACKLIGHT \(Pg. 20\)](#).





## ESD (ELECTRO-STATIC DISCHARGE)

The circuitry is industry standard CMOS logic and susceptible to ESD damage. Please use industry standard antistatic precautions as you would for any other static sensitive devices such as expansion cards, motherboards, or integrated circuits. Ground your body, work surfaces, and equipment.

## SITRONIX ST7565P CONTROLLER

The CFAO4265A-TFK uses a Sitronix ST7565P controller. For your reference, the Sitronix ST7565P *65 x 132 Dot Matrix LCD Controller/Driver* specifications (February 23, 2009, 71 pages) are included as an appendix in this Data Sheet. See [APPENDIX B: SITRONIX ST7565P CONTROLLER SPECIFICATION SHEET \(Pg. 29\)](#).

Here are links to some of the commonly used sections:

- For description of functions, see [page 23 in Appendix C](#).
- For display control instruction, see [Commands on page 42 of Appendix C](#).
- For initialization parameters, see [page 52 in Appendix C](#).
- For DC characteristics, see [page 58 in Appendix C](#).
- For host interface timing characteristics (read and write operation sequence), see [pages 65-67 of Appendix C](#).

## OPTICAL SPECIFICATIONS

ITEM	SYMBOL	TEST CONDITION	MINIMUM	TYPICAL	MAXIMUM
View Angle (Vertical, Horizontal)	(V) $\theta$	CR $\geq$ 2	-40°		+40°
Contrast Ratio	CR		2	4	
LCD Response Time*	T rise	Ta = 25°C		200 ms	200 ms
	T fall	Ta = 25°C		300 ms	300 ms
*Response Time: The amount of time it takes a liquid crystal cell to go from active to inactive or back again.					

## TEST CONDITIONS AND DEFINITIONS FOR OPTICAL CHARACTERISTICS

We work to continuously improve our products, including backlights that are brighter and last longer. Slight color variations from module to module and batch to batch are normal. If you need modules with consistent color, please ask for a custom order.

Test Conditions.

- Operating Voltage (V<sub>LCD</sub>): V<sub>OP</sub>
- Viewing Angle
  - Vertical (V) $\theta$ : 0°



- Horizontal ( $H_\phi$ ):  $0^\circ$
- Frame Frequency: 64 Hz (nominal)
- Driving  $W_a$
- Waveform: 1/65 Duty, 1/9 Bias
- Ambient Temperature ( $T_a$ ):  $25^\circ\text{C}$

## Definition of Operation Voltage ( $V_{op}$ )

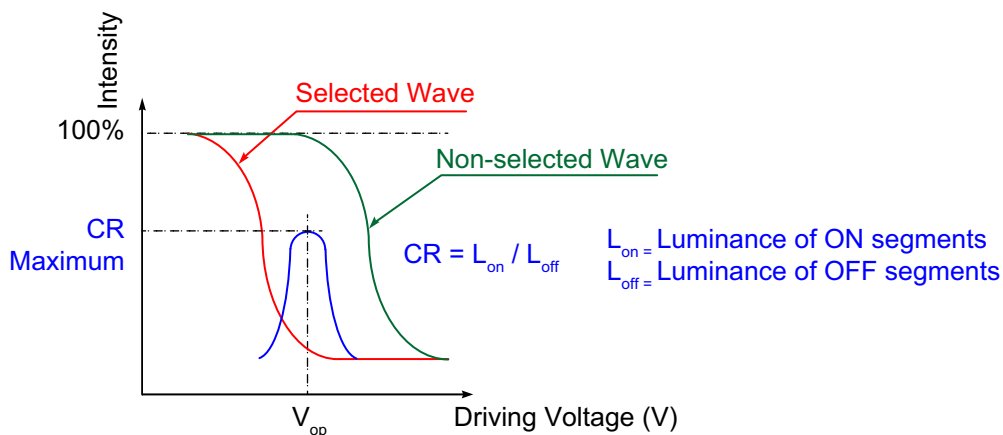


Figure 4. Definition of Operation Voltage ( $V_{op}$ ) (Positive)

## Definition of Response Time ( $T_r$ , $T_f$ )

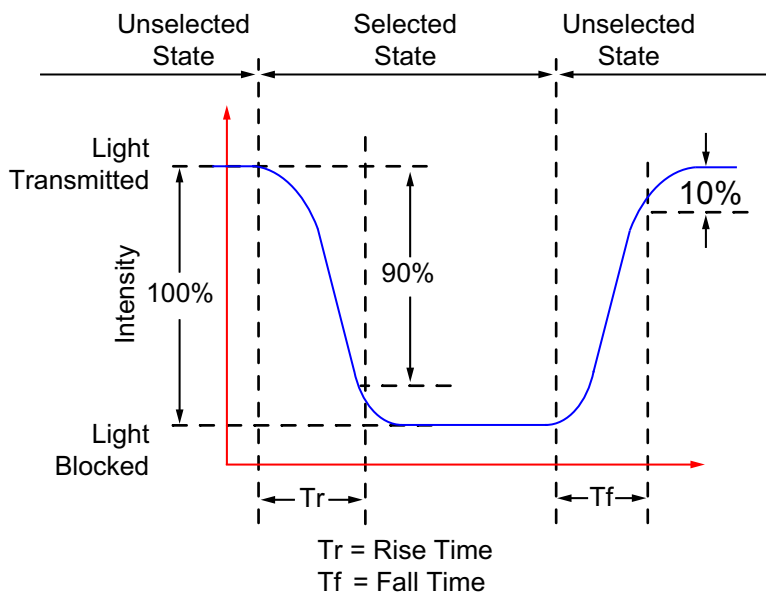


Figure 5. Definition of Response Time ( $T_r$ ,  $T_f$ ) (Positive)



## Definition of Horizontal and Vertical Viewing Angles (CR>2)

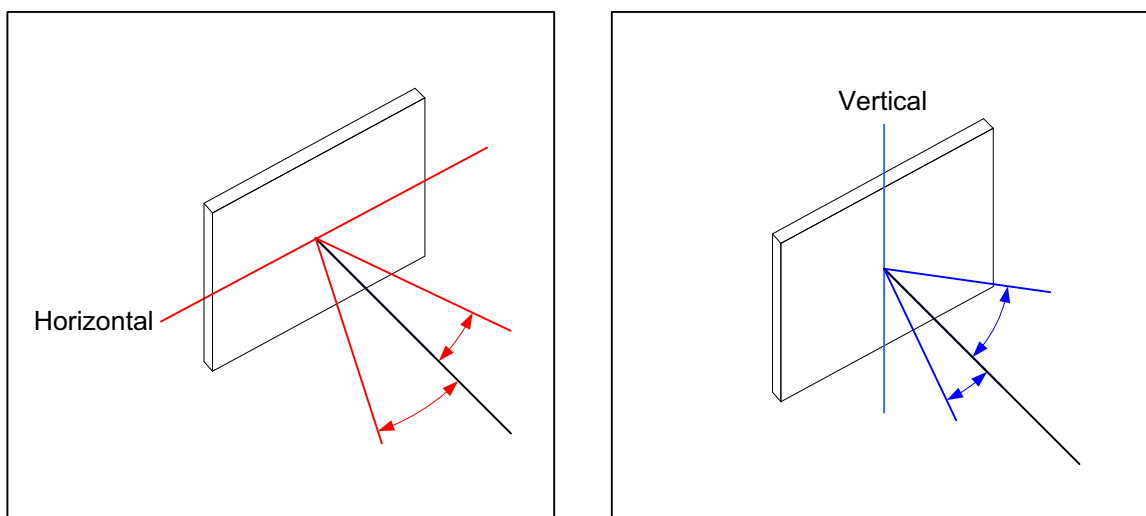


Figure 6. Definition of Horizontal and Vertical Viewing Angles (CR>2)

## Definition of 6:00 O'clock and 12:00 O'clock Viewing Angles

A 6:00 o'clock viewing angle is a bottom viewing angle like what you would see when looking at a cell phone or calculator. (Display is above eye level.) A 12:00 o'clock viewing angle is a top viewing angle like what you would see when looking at the gauges in a golf cart or airplane. (Display is below eye level.)

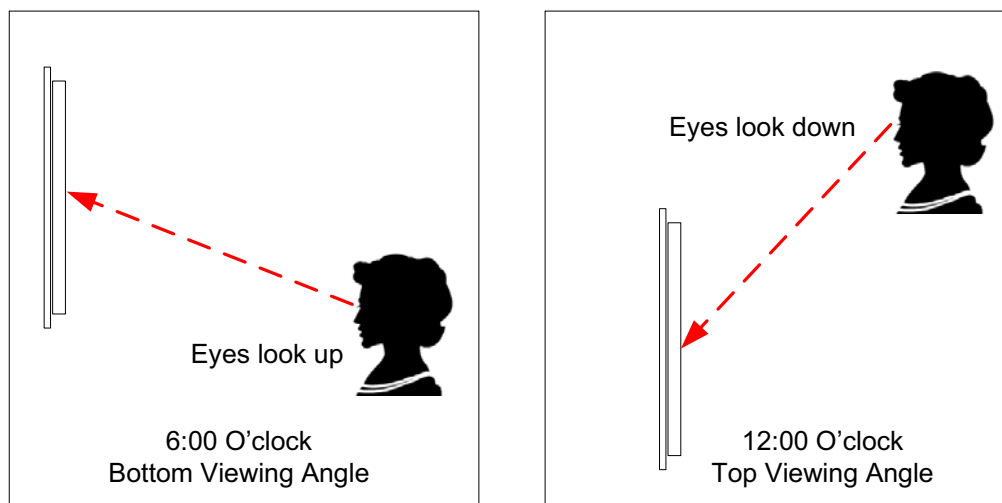


Figure 7. 6:00 O'Clock and 12:00 O'Clock Viewing Angles



## LED BACKLIGHT

---

### LOCATION OF A (LED+) AND K (LED-)

Make connections to your PCB using the tabs A (LED+) and K (LED-) on the back of the module.

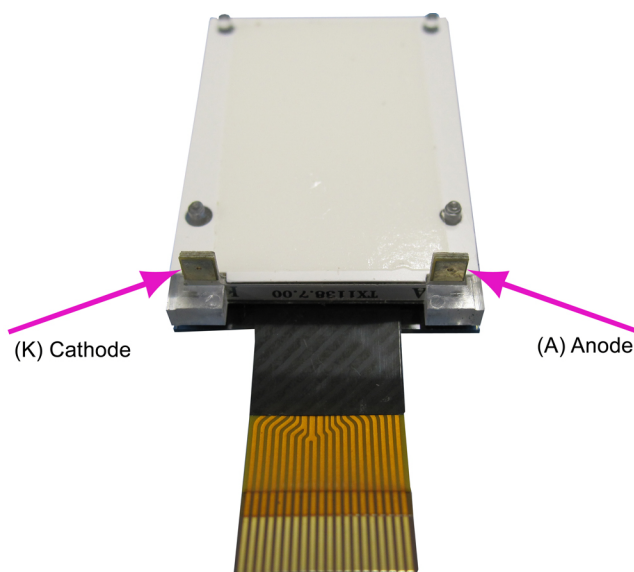


Figure 8. Location of Backlight Tabs A and K



## BACKLIGHT CHARACTERISTICS

<b>LED Backlight Characteristics</b> <i>Edge-lit LED backlight has three LEDs.</i> <i>White LED backlight displays dark pixels on an illuminated white background).</i>					
ITEM	SYMBOL	TEST CONDITION	MINIMUM	TYPICAL	MAXIMUM
Forward Current	$I_{LED}$			12 mA	15 mA
<i>Driving the backlight above 20 mA will shorten its lifetime.</i>					
Forward Voltage	$V_{LED}$			+9.6v	+10.8v
Reverse Voltage ( $V_R$ )	$V_R$				+15v
White Chromaticity	x	CIE (1931)	0.27	0.31	0.35
	y		0.25	0.30	0.35
Luminous Intensity*	IV	$I_{LED} = 15 \text{ mA}$	150 cd/m <sup>2</sup>	180 cd/m <sup>2</sup>	
Uniformity (minimum/maximum x 100%)	C		70%		
<i>*The backlight is measured through the LCD. Direct backlight measurement is significantly brighter.</i>					

The CFAO4265A-TFK backlight uses LEDs. The backlight is easy to use properly but it is also easily damaged by abuse.

### **NOTE**

Do not connect +5v directly to the backlight terminals. This will ruin the backlight.

### **NOTE**

We recommend that the white LED backlight be dimmed or turned off during periods of inactivity to conserve the LEDs' lifetime.

LEDs are "current" devices. The brightness is controlled by the current flowing through it, not the voltage across it. Ideally, a current source would be used to drive the LEDs. In practice, a simple current limiting resistor will work well in most applications and is much less complex than a current source.



## CIRCUIT EXAMPLE USING LED DRIVER NCP5007

The CFAO4265A-TFK uses series connected white LEDs for its backlight. The overall series forward voltage is 9.6v to 10.8v. For long life, we recommend driving the backlight at 12mA. The best way to drive the backlight is to use a switching supply designed to control current. We have used the [NCP5007](#) LED driver on many designs with good results.

Here is an example circuit:

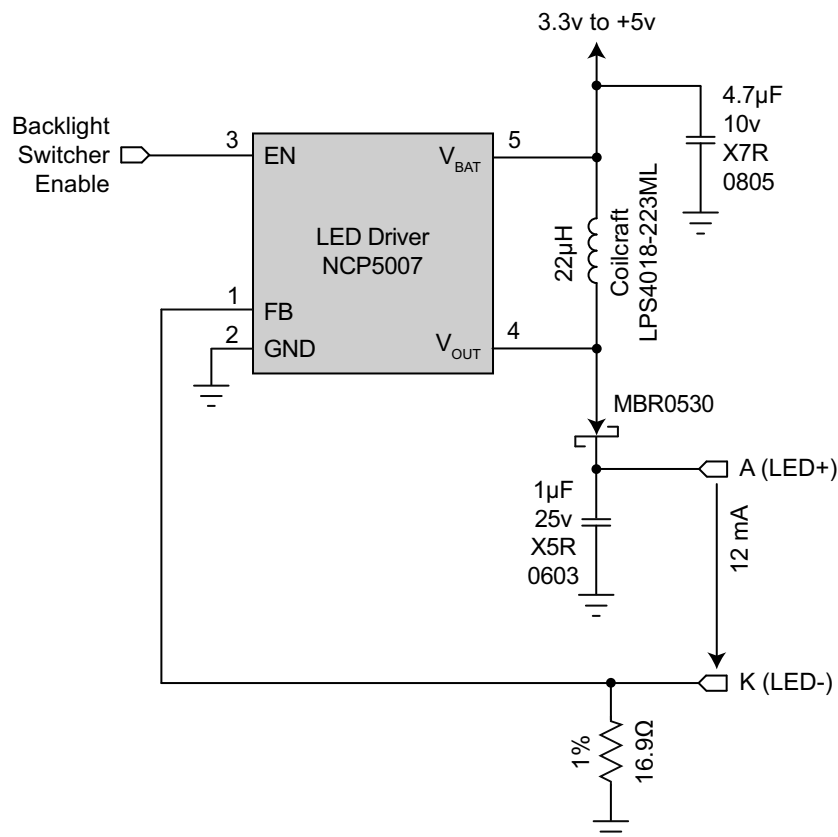


Figure 9. Circuit Example Using LED Driver NCP5007



# PRODUCT RELIABILITY

## MODULE RELIABILITY

ITEM	SPECIFICATION	
Module, excluding backlight.	50,000 to 100,000 hours (typical)	
White LED Backlight ( $I_{LED} < 15 \text{ mA}$ ) <i>* We recommend that the backlight of the white LED backlit modules be dimmed or turned off during periods of inactivity to conserve the white LED backlight lifetime.</i>	<i>Power-On Hours</i>	<i>% of Initial Brightness</i>
	<10,000	>70%
	<50,000	>50%
<i>Conditions: under operating and storage temperature specification limitations, humidity (noncondensing) RH up to 65%, and no exposure to direct sunlight.</i>		

White LEDs do not have the extremely long lifetime typical of red or green LEDs. The white LEDs dim over time, especially if driven with high currents. The dimming may not be noticeable when a single display is installed. However, if a new display is installed next to a display that has been on continuously for a very long time, you will see the difference. To preserve the lifetime of white LEDs, we recommend that white LED backlights be dimmed or turned off when not needed. Also, please do not use more current than you need to achieve your brightness requirements.

## MODULE LONGEVITY (EOL / REPLACEMENT POLICY)

CrystalFontz is committed to making all of our LCD modules available for as long as possible. For each module we introduce, we intend to offer it indefinitely. We do not preplan a module's obsolescence. The majority of modules we have introduced are still available.

We recognize that discontinuing a module may cause problems for some customers. However, rapidly changing technologies, component availability, or low customer order levels may force us to discontinue ("End of Life", EOL) a module. For example, we must occasionally discontinue a module when a supplier discontinues a component or a manufacturing process becomes obsolete. When we discontinue a module, we will do our best to find an acceptable replacement module with the same fit, form, and function.

In most situations, you will not notice a difference when comparing a "fit, form, and function" replacement module to the discontinued module it replaces. However, sometimes a change in component or process for the replacement module results in a slight variation, perhaps an improvement, over the previous design.

Although the replacement module is still within the stated Data Sheet specifications and tolerances of the discontinued module, changes may require modification to your circuit and/or firmware. Possible changes include:

- *LCD fluid, polarizers, or the LCD manufacturing process.* These items may change the appearance of the display, requiring an adjustment to  $V_O$ . See [Sitronix ST7565P Controller \(Pg. 17\)](#).
- *Backlight LEDs.* Brightness may be affected (perhaps the new LEDs have better efficiency) or the current they draw may change (new LEDs may have a different VF).
- *Controller.* A new controller may require minor changes in your code.
- *Component tolerances.* Module components have manufacturing tolerances. In extreme cases, the tolerance stack can change the visual or operating characteristics.



Please understand that we avoid changing a module whenever possible; we only discontinue a module if we have no other option. We will post Part Change Notices on the product's webpage as soon as possible. If interested, you can subscribe to future part change notifications.

## CARE AND HANDLING PRECAUTIONS

For optimum operation of the module and to prolong its life, please follow the precautions below. Excessive voltage will shorten the life of the module. You must drive the display within the specified voltage limit. See [Absolute Maximum Ratings \(Pg. 12\)](#).

### ESD (ELECTRO-STATIC DISCHARGE)

The circuitry is industry standard CMOS logic and susceptible to ESD damage. Please use industry standard antistatic precautions as you would for any other static sensitive devices such as expansion cards, motherboards, or integrated circuits. Ground your body, work surfaces, and equipment.

### DESIGN AND MOUNTING

- The exposed surface of the "glass" is actually a polarizer laminated on top of the glass. To protect the soft plastic polarizer from damage, the module ships with a protective film over the polarizer. Please peel off the protective film slowly. Peeling off the protective film abruptly may generate static electricity.
- The polarizer is made out of soft plastic and is easily scratched or damaged. When handling the module, avoid touching the polarizer. Finger oils are difficult to remove.
- To protect the soft plastic polarizer from damage, place a transparent plate (for example, acrylic, polycarbonate, or glass) in front of the module, leaving a small gap between the plate and the display surface. We use GE HP-92 Lexan, which is readily available and works well.
- Do not disassemble or modify the module.
- The display can be mounted vertically onto a front panel using a variety of methods. If the enclosure is plastic, it can be molded to have the display snap into place. A metal enclosure can use a milled faceplate with mounting tabs to secure the module. Adhesives can be used, as long as they are not similar to "super-glue" because these emit vapors that can damage the display over time.
- Do not reverse polarity to the power supply connections. Reversing polarity will immediately ruin the module.
- Use care to keep the exposed terminals clean.
- Sharp bends can damage the LCD panel. Do not crease the cables. Do not bend the cables tightly against the edge of the panel. Do not repeatedly bend the cable beyond its elastic region. Limit bend radius to at least R2.00 mm.

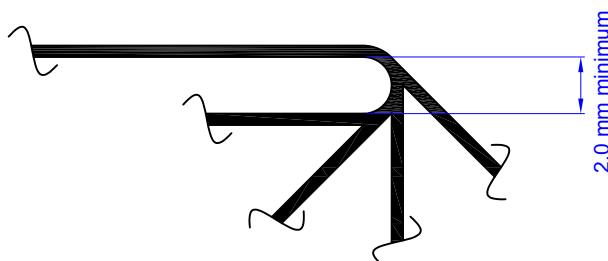


Figure 10. Limit FFC Bend Radius





## AVOID SHOCK, IMPACT, TORQUE, OR TENSION

- Do not expose the module to strong mechanical shock, impact, torque, or tension.
- Do not drop, toss, bend, or twist the module.
- Do not place weight or pressure on the module.

## CLEANING

- The polarizer (laminated to the glass) is soft plastic. The soft plastic is easily scratched or damaged. Be very careful when you clean the polarizer.
- Do not clean the polarizer with liquids. Do not wipe the polarizer with any type of cloth or swab (for example, Q-tips).
- Use the removable protective film to remove smudges (for example, fingerprints) and any foreign matter. If you no longer have the protective film, use standard transparent office tape (for example, Scotch® brand "Crystal Clear Tape"). If the polarizer is dusty, you may carefully blow it off with clean, dry, oil-free compressed air.

## OPERATION

- We do not recommend connecting this module to a PC's parallel port as an "end product." This module is not "user friendly" and connecting it to a PC's parallel port is often difficult, frustrating, and can result in a "dead" display due to mishandling. For more information, see our forum thread at <http://www.crystalfontz.com/forum/showthread.php?s=&threadid=3257>.
- Your circuit should be designed to protect the module from ESD and power supply transients.
- Observe the operating temperature limitations: from -20°C minimum to +70°C maximum with minimal fluctuations. Operation outside of these limits may shorten the life and/or harm the display.
- Operate away from dust, moisture, and direct sunlight.

## STORAGE AND RECYCLING

- Store in an ESD-approved container away from dust, moisture, and direct sunlight, fluorescent lamps, or any ultraviolet ray.
- Observe the storage temperature limitations: from -30°C minimum to +80°C maximum with minimal fluctuations. Rapid temperature changes can cause moisture to form, resulting in permanent damage.
- Do not allow weight to be placed on the modules while they are in storage.
- Please recycle your outdated CrystalFontz modules at an approved facility.



## APPENDIX A: QUALITY ASSURANCE STANDARDS

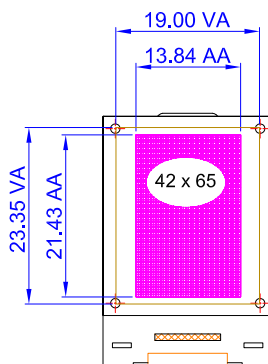
### INSPECTION CONDITIONS

- Environment
  - Temperature:  $25 \pm 5^{\circ}\text{C}$
  - Humidity: 30~85% RH (noncondensing)
- For visual inspection of active display area
  - Source lighting: two 20-Watt or one 40-Watt fluorescent light
  - Display adjusted for best contrast
  - Viewing distance:  $30 \pm 5$  cm (about 12 inches)
  - Viewing angle: inspect at  $45^{\circ}$  angle of vertical line right and left, top and bottom

### COLOR DEFINITIONS

We try to describe the appearance of our LCD modules as accurately as possible. For the photos, we adjust the backlight (if any) and contrast for optimal appearance. Actual display appearance may vary due to (1) different operating conditions, (2) small variations of component tolerances, (3) inaccuracies of our camera, (4) color interpretation of the photos on your monitor, and/or (5) personal differences in the perception of color.

### DEFINITION OF ACTIVE AREA AND VIEWING AREA



### ACCEPTANCE SAMPLING

DEFECT TYPE	AQL*
Major	$\leq .65\%$
Minor	$< 1.0\%$
* Acceptable Quality Level: maximum allowable error rate or variation from standard	

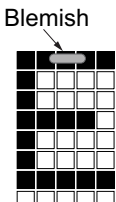
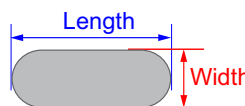
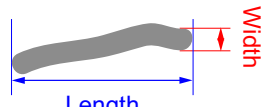


## DEFECTS CLASSIFICATION

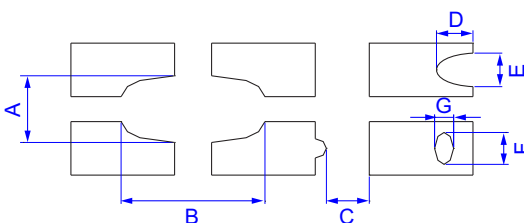
Defects are defined as:

- Major Defect: results in failure or substantially reduces usability of unit for its intended purpose
- Minor Defect: deviates from standards but is not likely to reduce usability for its intended purpose

## ACCEPTANCE STANDARDS

#	DEFECT TYPE	CRITERIA			MAJOR / MINOR
1	Electrical defects	1. No display, display malfunctions, or shorted segments. 2. Current consumption exceeds specifications.			Major
2	Viewing area defect	Viewing area does not meet specifications.			Major
3	Contrast adjustment defect	Contrast adjustment fails or malfunctions.			Major
4	Blemishes or foreign matter on display segments		Defect Size	Acceptable Qty	Minor
			≤0.30 mm	3	
			≤2 defects within 10 mm of each other		
5	Blemishes or foreign matter outside of display segments	Defect Size = (Width + Length)/2 	Defect Size	Acceptable Qty	Minor
			≤0.15 mm	Ignore	
			0.15 to 0.20 mm	3	
			0.20 to 0.25 mm	2	
			> 0.30 mm	1	
6	Dark lines or scratches in display area 	Defect Width	Defect Length	Acceptable Qty	Minor
		≤0.03 mm	≤3.0 mm	3	
		0.03 to 0.05	≤2.0 mm	2	
		0.05 to 0.08	≤2.0 mm	1	
		0.08 to 0.10	≤3.0 mm	0	
		≥0.10	>3.0 mm	0	



#	DEFECT TYPE	CRITERIA		MAJOR / MINOR
7	Bubbles between polarizer film and glass	Defect Size	Acceptable Qty	Minor
		≤0.20 mm	Ignore	
		0.20 to 0.40 mm	3	
		0.40 to 0.60 mm	2	
		≥0.60 mm	0	
8	Display pattern defect			Minor
		Dot Size	Acceptable Qty	
		$((A+B)/2) \leq 0.20 \text{ mm}$	$\leq 3 \text{ total defects}$ $\leq 2 \text{ pinholes per digit}$	
		C > 0 mm		
		$((D+E)/2) \leq 0.25 \text{ mm}$		
		$((F+G)/2) \leq 0.25 \text{ mm}$		
9	Backlight defects	1. Light fails or flickers.* 2. Color and luminance do not correspond to specifications.* 3. Exceeds standards for display's blemishes, foreign matter, dark lines or scratches. *Minor if display functions correctly. Major if the display fails.		Minor
10	PCB defects (if module has PCB)	1. Oxidation or contamination on connectors.* 2. Wrong parts, missing parts, or parts not in specification.* 3. Jumpers set incorrectly. 4. Solder (if any) on bezel, LED pad, zebra pad, or screw hole pad is not smooth. *Minor if display functions correctly. Major if the display fails.		Minor
11	Soldering defects	1. Unmelted solder paste. 2. Cold solder joints, missing solder connections, or oxidation.* 3. Solder bridges causing short circuits.* 4. Residue or solder balls. 5. Solder flux is black or brown. *Minor if display functions correctly. Major if the display fails.		Minor



## APPENDIX B: SITRONIX ST7565P CONTROLLER SPECIFICATION SHEET

---

The complete *Sitronix ST7565P 65 x 132 Dot Matrix LCD Controller/Driver* specifications v2.1a (February 23, 2009, 71 pages) follows.

## FEATURES

- Directly display RAM data through Display Data RAM
- RAM capacity : 65 x 132 = 8580 bits
- Display duty selectable by select pin
  - 1/65 duty : 65 common x 132 segment
  - 1/49 duty : 49 common x 132 segment
  - 1/33 duty : 33 common x 132 segment
  - 1/55 duty : 55 common x 132 segment
  - 1/53 duty : 53 common x 132 segment
- High-speed 8-bit MPU interface:  
ST7565P can be connected directly to both the 80x86 series MPUs and the 6800 series MPUs. Serial interface (SPI-4) is also supported.
- Abundant command functions:  
Display data read/write, display ON/OFF, Normal/Reverse display mode, page address set, display start line set, column address set, status read, display all points ON, LCD bias set, electronic volume, read-modify-write, set segment driver direction, power save mode, set common output direction, set V0 regulator internal resistor ratio.
- Built-in low power consumption power circuits:  
Booster, Regulator and Follower.
- Booster circuit supports 2X/3X/4X/5X/6X boost level. External reference voltage (VDD2) for booster circuits.
- High-accuracy Regulator with contrast control (EV) and built-in V0 voltage regulator resistors. (Thermal gradient = -0.05%/°C)
- Built-in Follower for LCD bias voltages.
- Embedded R-C oscillation circuit. Support external clock input.
- Extremely low power consumption:  
60uA (operating, bare chip with internal power) (V<sub>DD</sub>-V<sub>SS</sub> = V<sub>DD2</sub>-V<sub>SS</sub> = 3V, Booster x4, V0 = 11V ). Condition: display pattern is "OFF"; use normal mode.
- Wide application voltage range:  
Logic power: V<sub>DD</sub> - V<sub>SS</sub> = 1.8V to 3.3V (typical)  
Analog power: V<sub>DD2</sub> - V<sub>SS</sub> = 2.4V to 3.3V (typical)  
Maximum Booster limitation: V<sub>OUT</sub> = 13.5V  
LCD Vop: V0 - V<sub>SS</sub> = 3.0V to 12.0V
- Wide operation temperature range: -30 to 85°C
- CMOS process.
- Package type: Bare chip (COG) and TCP.
- ST7565P is not designed for resistance to light or resistance to radiation.

## GENERAL DESCRIPTION

ST7565P is a single-chip dot-matrix LCD driver that can be connected directly to a microprocessor bus. 8-bit parallel or serial display data sent from the microprocessor is stored in the internal Display Data RAM and this chip generates LCD driving signals independent of the microprocessor. Each data bits (65x132) of the internal Display Data RAM is 1-to-1 correspondence with each pixels (65x132) on the LCD panel, therefore, ST7565P enables displays with a high degree of freedom.

Moreover, the display area can be extended horizontally by using Master/Slave feature.

With the abundant embedded circuits (2~6 times booster circuit, V0 regulator with contrast control for LCD voltage adjustment, voltage follower with bias selection and R-C oscillation circuit), ST7565P can be used to create a display system with the lowest power consumption and the fewest external components for high-performance portable devices.

PART NO.	VRS temperature gradient	VRS range
ST7565P	-0.05%/°C	2.1V ± 0.03V

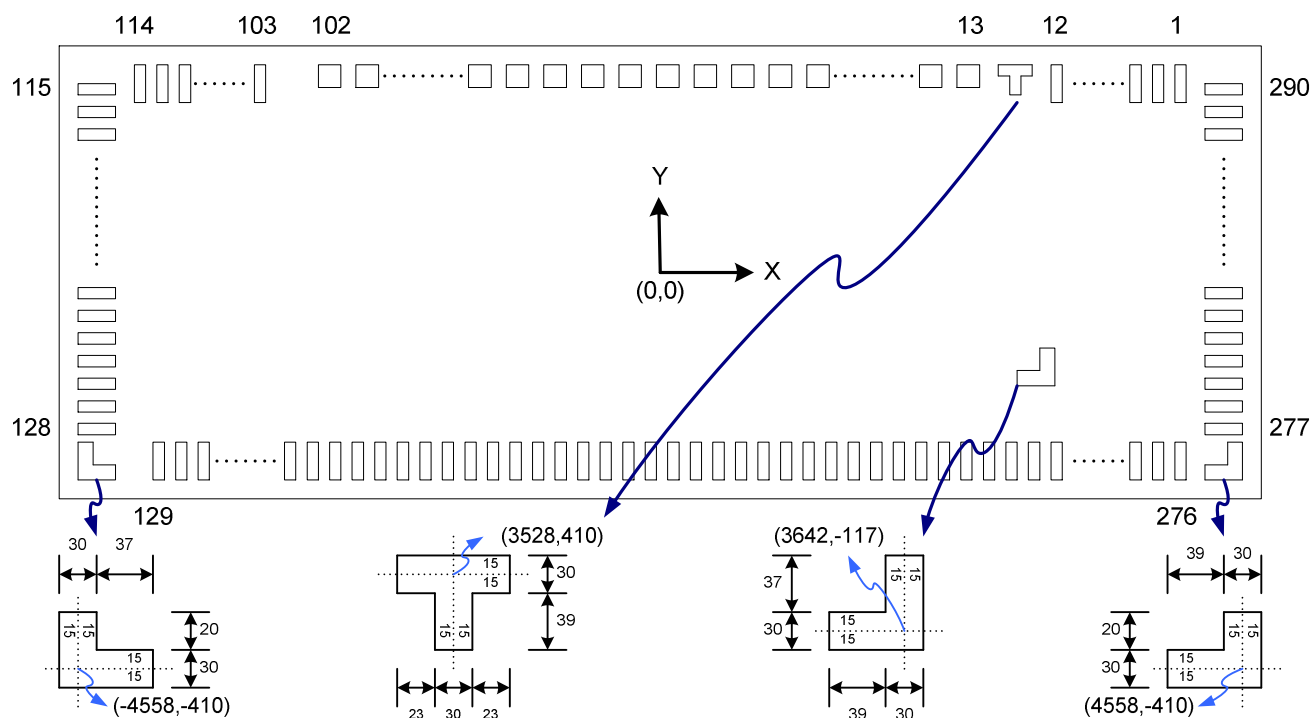
<b>ST7565P</b>	<b>6800 , 8080 , 4-Line interface</b>	
----------------	---------------------------------------	---

Sitronix Technology Corp. reserves the right to change the contents in this document without prior notice.

## ST7565P Pad Arrangement(COG)

PAD No	Bump Size
001~012, 103~114, 129~276	40μm x 90μm
013~102	56μm x 60μm
115, 290	90μm x 25.5μm
116~128, 277~289	90μm x 40μm

Chip Size
9,336μm x 1,000μm
Bump Pitch
58μm (Min.)
Bump Height
17μm (Typ)
Chip Thickness
635μm



Use select pin to define display duty as following table:

SEL 3, 2, 1	DUTY	BIAS
0, 0, 0	1/65	1/9 or 1/7
0, 0, 1	1/49	1/8 or 1/6
0, 1, 0	1/33	1/6 or 1/5
0, 1, 1	1/55	1/8 or 1/6
1, 0, 0	1/53	1/8 or 1/6
1, X, X	-----	-----

## Pad Center Coordinates (1/65 Duty)

Units:  $\mu\text{m}$

PAD No.	PIN Name	X	Y
1	COM[53]	4241	374
2	COM[54]	4183	374
3	COM[55]	4125	374
4	COM[56]	4067	374
5	COM[57]	4009	374
6	COM[58]	3951	374
7	COM[59]	3893	374
8	COM[60]	3835	374
9	COM[61]	3777	374
10	COM[62]	3719	374
11	COM[63]	3661	374
12	COMS1	3603	374
13	FRS	3443	389
14	FR	3369	389
15	CL	3295	389
16	/DOF	3221	389
17	VSS	3147	389
18	/CS1	3073	389
19	CS2	2999	389
20	VDD	2925	389
21	/RES	2851	389
22	A0	2777	389
23	VSS	2703	389
24	/WR(R/W)	2629	389
25	/RD(E)	2555	389
26	VDD	2481	389
27	D0	2407	389
28	D1	2333	389
29	D2	2259	389
30	D3	2185	389
31	D4	2111	389
32	D5	2037	389
33	D6	1963	389
34	D7	1889	389
35	VDD	1815	389
36	VDD2	1741	389
37	VDD2	1667	389
38	VSS	1593	389
39	VSS	1519	389
40	VSS	1445	389
41	VSS	1371	389
42	VOUT	1297	389
43	VOUT	1223	389
44	CAP5P	1149	389
45	CAP5P	1075	389
46	CAP1N	1001	389
47	CAP1N	927	389

PAD No.	PIN Name	X	Y
48	CAP3P	853	389
49	CAP3P	779	389
50	CAP1N	705	389
51	CAP1N	631	389
52	CAP1P	557	389
53	CAP1P	483	389
54	CAP2P	409	389
55	CAP2P	335	389
56	CAP2N	261	389
57	CAP2N	187	389
58	CAP4P	113	389
59	CAP4P	39	389
60	VSS	-35	389
61	VSS	-109	389
62	VRS	-183	389
63	VRS	-257	389
64	VDD2	-331	389
65	VDD	-405	389
66	V4	-479	389
67	V4	-553	389
68	V3	-627	389
69	V3	-701	389
70	V2	-775	389
71	V2	-849	389
72	V1	-923	389
73	V1	-997	389
74	V0	-1071	389
75	V0	-1145	389
76	VR	-1219	389
77	VR	-1293	389
78	VDD	-1367	389
79	VDD2	-1441	389
80	TEST0	-1515	389
81	TEST1	-1589	389
82	TEST2	-1663	389
83	TEST3	-1737	389
84	TEST4	-1811	389
85	TEST5	-1885	389
86	VDD	-1959	389
87	M/S	-2033	389
88	CLS	-2107	389
89	VSS	-2181	389
90	C86	-2255	389
91	P/S	-2329	389
92	VDD	-2403	389
93	/HPM	-2477	389
94	VSS	-2551	389



PAD No.	PIN Name	X	Y
95	IRS	-2625	389
96	VDD	-2699	389
97	SEL1	-2773	389
98	VSS	-2847	389
99	SEL2	-2921	389
100	VDD	-2995	389
101	SEL3	-3069	389
102	VSS	-3143	389
103	COM[31]	-3606	374
104	COM[30]	-3664	374
105	COM[29]	-3722	374
106	COM[28]	-3780	374
107	COM[27]	-3838	374
108	COM[26]	-3896	374
109	COM[25]	-3954	374
110	COM[24]	-4012	374
111	COM[23]	-4070	374
112	COM[22]	-4128	374
113	COM[21]	-4186	374
114	COM[20]	-4244	374
115	(NC)	-4542	404
116	COM[19]	-4542	351
117	COM[18]	-4542	293
118	COM[17]	-4542	235
119	COM[16]	-4542	177
120	COM[15]	-4542	119
121	COM[14]	-4542	61
122	COM[13]	-4542	3
123	COM[12]	-4542	-55
124	COM[11]	-4542	-113
125	COM[10]	-4542	-171
126	COM[9]	-4542	-229
127	COM[8]	-4542	-287
128	COM[7]	-4542	-345
129	COM[6]	-4267	-374
130	COM[5]	-4209	-374
131	COM[4]	-4151	-374
132	COM[3]	-4093	-374
133	COM[2]	-4035	-374
134	COM[1]	-3977	-374
135	COM[0]	-3919	-374
136	COMS2	-3861	-374
137	SEG[0]	-3803	-374
138	SEG[1]	-3745	-374
139	SEG[2]	-3687	-374
140	SEG[3]	-3629	-374
141	SEG[4]	-3571	-374
142	SEG[5]	-3513	-374
143	SEG[6]	-3455	-374
144	SEG[7]	-3397	-374
145	SEG[8]	-3339	-374
146	SEG[9]	-3281	-374

PAD No.	PIN Name	X	Y
147	SEG[10]	-3223	-374
148	SEG[11]	-3165	-374
149	SEG[12]	-3107	-374
150	SEG[13]	-3049	-374
151	SEG[14]	-2991	-374
152	SEG[15]	-2933	-374
153	SEG[16]	-2875	-374
154	SEG[17]	-2817	-374
155	SEG[18]	-2759	-374
156	SEG[19]	-2701	-374
157	SEG[20]	-2643	-374
158	SEG[21]	-2585	-374
159	SEG[22]	-2527	-374
160	SEG[23]	-2469	-374
161	SEG[24]	-2411	-374
162	SEG[25]	-2353	-374
163	SEG[26]	-2295	-374
164	SEG[27]	-2237	-374
165	SEG[28]	-2179	-374
166	SEG[29]	-2121	-374
167	SEG[30]	-2063	-374
168	SEG[31]	-2005	-374
169	SEG[32]	-1947	-374
170	SEG[33]	-1889	-374
171	SEG[34]	-1831	-374
172	SEG[35]	-1773	-374
173	SEG[36]	-1715	-374
174	SEG[37]	-1657	-374
175	SEG[38]	-1599	-374
176	SEG[39]	-1541	-374
177	SEG[40]	-1483	-374
178	SEG[41]	-1425	-374
179	SEG[42]	-1367	-374
180	SEG[43]	-1309	-374
181	SEG[44]	-1251	-374
182	SEG[45]	-1193	-374
183	SEG[46]	-1135	-374
184	SEG[47]	-1077	-374
185	SEG[48]	-1019	-374
186	SEG[49]	-961	-374
187	SEG[50]	-903	-374
188	SEG[51]	-845	-374
189	SEG[52]	-787	-374
190	SEG[53]	-729	-374
191	SEG[54]	-671	-374
192	SEG[55]	-613	-374
193	SEG[56]	-555	-374
194	SEG[57]	-497	-374
195	SEG[58]	-439	-374
196	SEG[59]	-381	-374
197	SEG[60]	-323	-374
198	SEG[61]	-265	-374

PAD No.	PIN Name	X	Y
199	SEG[62]	-207	-374
200	SEG[63]	-149	-374
201	SEG[64]	-91	-374
202	SEG[65]	-33	-374
203	SEG[66]	25	-374
204	SEG[67]	83	-374
205	SEG[68]	141	-374
206	SEG[69]	199	-374
207	SEG[70]	257	-374
208	SEG[71]	315	-374
209	SEG[72]	373	-374
210	SEG[73]	431	-374
211	SEG[74]	489	-374
212	SEG[75]	547	-374
213	SEG[76]	605	-374
214	SEG[77]	663	-374
215	SEG[78]	721	-374
216	SEG[79]	779	-374
217	SEG[80]	837	-374
218	SEG[81]	895	-374
219	SEG[82]	953	-374
220	SEG[83]	1011	-374
221	SEG[84]	1069	-374
222	SEG[85]	1127	-374
223	SEG[86]	1185	-374
224	SEG[87]	1243	-374
225	SEG[88]	1301	-374
226	SEG[89]	1359	-374
227	SEG[90]	1417	-374
228	SEG[91]	1475	-374
229	SEG[92]	1533	-374
230	SEG[93]	1591	-374
231	SEG[94]	1649	-374
232	SEG[95]	1707	-374
233	SEG[96]	1765	-374
234	SEG[97]	1823	-374
235	SEG[98]	1881	-374
236	SEG[99]	1939	-374
237	SEG[100]	1997	-374
238	SEG[101]	2055	-374
239	SEG[102]	2113	-374
240	SEG[103]	2171	-374
241	SEG[104]	2229	-374
242	SEG[105]	2287	-374
243	SEG[106]	2345	-374
244	SEG[107]	2403	-374
245	SEG[108]	2461	-374

PAD No.	PIN Name	X	Y
246	SEG[109]	2519	-374
247	SEG[110]	2577	-374
248	SEG[111]	2635	-374
249	SEG[112]	2693	-374
250	SEG[113]	2751	-374
251	SEG[114]	2809	-374
252	SEG[115]	2867	-374
253	SEG[116]	2925	-374
254	SEG[117]	2983	-374
255	SEG[118]	3041	-374
256	SEG[119]	3099	-374
257	SEG[120]	3157	-374
258	SEG[121]	3215	-374
259	SEG[122]	3273	-374
260	SEG[123]	3331	-374
261	SEG[124]	3389	-374
262	SEG[125]	3447	-374
263	SEG[126]	3505	-374
264	SEG[127]	3563	-374
265	SEG[128]	3621	-374
266	SEG[129]	3679	-374
267	SEG[130]	3737	-374
268	SEG[131]	3795	-374
269	COM[32]	3853	-374
270	COM[33]	3911	-374
271	COM[34]	3969	-374
272	COM[35]	4027	-374
273	COM[36]	4085	-374
274	COM[37]	4143	-374
275	COM[38]	4201	-374
276	COM[39]	4259	-374
277	COM[40]	4542	-345
278	COM[41]	4542	-287
279	COM[42]	4542	-229
280	COM[43]	4542	-171
281	COM[44]	4542	-113
282	COM[45]	4542	-55
283	COM[46]	4542	3
284	COM[47]	4542	61
285	COM[48]	4542	119
286	COM[49]	4542	177
287	COM[50]	4542	235
288	COM[51]	4542	293
289	COM[52]	4542	351
290	(NC)	4542	404

**Pad Center Coordinates (1/49 Duty)**Units:  $\mu\text{m}$ 

PAD No.	PIN Name	X	Y
1	COM[37]	4241	374
2	COM[38]	4183	374
3	COM[39]	4125	374
4	COM[40]	4067	374
5	COM[41]	4009	374
6	COM[42]	3951	374
7	COM[43]	3893	374
8	COM[44]	3835	374
9	COM[45]	3777	374
10	COM[46]	3719	374
11	COM[47]	3661	374
12	COMS1	3603	374
13	FRS	3443	389
14	FR	3369	389
15	CL	3295	389
16	/DOF	3221	389
17	VSS	3147	389
18	/CS1	3073	389
19	CS2	2999	389
20	VDD	2925	389
21	/RES	2851	389
22	A0	2777	389
23	VSS	2703	389
24	/WR(R/W)	2629	389
25	/RD(E)	2555	389
26	VDD	2481	389
27	D0	2407	389
28	D1	2333	389
29	D2	2259	389
30	D3	2185	389
31	D4	2111	389
32	D5	2037	389
33	D6	1963	389
34	D7	1889	389
35	VDD	1815	389
36	VDD2	1741	389
37	VDD2	1667	389
38	VSS	1593	389
39	VSS	1519	389
40	VSS	1445	389
41	VSS	1371	389
42	VOUT	1297	389
43	VOUT	1223	389
44	CAP5P	1149	389
45	CAP5P	1075	389
46	CAP1N	1001	389
47	CAP1N	927	389

PAD No.	PIN Name	X	Y
48	CAP3P	853	389
49	CAP3P	779	389
50	CAP1N	705	389
51	CAP1N	631	389
52	CAP1P	557	389
53	CAP1P	483	389
54	CAP2P	409	389
55	CAP2P	335	389
56	CAP2N	261	389
57	CAP2N	187	389
58	CAP4P	113	389
59	CAP4P	39	389
60	VSS	-35	389
61	VSS	-109	389
62	VRS	-183	389
63	VRS	-257	389
64	VDD2	-331	389
65	VDD	-405	389
66	V4	-479	389
67	V4	-553	389
68	V3	-627	389
69	V3	-701	389
70	V2	-775	389
71	V2	-849	389
72	V1	-923	389
73	V1	-997	389
74	V0	-1071	389
75	V0	-1145	389
76	VR	-1219	389
77	VR	-1293	389
78	VDD	-1367	389
79	VDD2	-1441	389
80	TEST0	-1515	389
81	TEST1	-1589	389
82	TEST2	-1663	389
83	TEST3	-1737	389
84	TEST4	-1811	389
85	TEST5	-1885	389
86	VDD	-1959	389
87	M/S	-2033	389
88	CLS	-2107	389
89	VSS	-2181	389
90	C86	-2255	389
91	P/S	-2329	389
92	VDD	-2403	389
93	/HPM	-2477	389
94	VSS	-2551	389

PAD No.	PIN Name	X	Y
95	IRS	-2625	389
96	VDD	-2699	389
97	SEL1	-2773	389
98	VSS	-2847	389
99	SEL2	-2921	389
100	VDD	-2995	389
101	SEL3	-3069	389
102	VSS	-3143	389
103	Reserve	-3606	374
104	Reserve	-3664	374
105	Reserve	-3722	374
106	Reserve	-3780	374
107	Reserve	-3838	374
108	Reserve	-3896	374
109	Reserve	-3954	374
110	Reserve	-4012	374
111	COM[23]	-4070	374
112	COM[22]	-4128	374
113	COM[21]	-4186	374
114	COM[20]	-4244	374
115	(NC)	-4542	404
116	COM[19]	-4542	351
117	COM[18]	-4542	293
118	COM[17]	-4542	235
119	COM[16]	-4542	177
120	COM[15]	-4542	119
121	COM[14]	-4542	61
122	COM[13]	-4542	3
123	COM[12]	-4542	-55
124	COM[11]	-4542	-113
125	COM[10]	-4542	-171
126	COM[9]	-4542	-229
127	COM[8]	-4542	-287
128	COM[7]	-4542	-345
129	COM[6]	-4267	-374
130	COM[5]	-4209	-374
131	COM[4]	-4151	-374
132	COM[3]	-4093	-374
133	COM[2]	-4035	-374
134	COM[1]	-3977	-374
135	COM[0]	-3919	-374
136	COMS2	-3861	-374
137	SEG[0]	-3803	-374
138	SEG[1]	-3745	-374
139	SEG[2]	-3687	-374
140	SEG[3]	-3629	-374
141	SEG[4]	-3571	-374
142	SEG[5]	-3513	-374
143	SEG[6]	-3455	-374
144	SEG[7]	-3397	-374
145	SEG[8]	-3339	-374
146	SEG[9]	-3281	-374

PAD No.	PIN Name	X	Y
147	SEG[10]	-3223	-374
148	SEG[11]	-3165	-374
149	SEG[12]	-3107	-374
150	SEG[13]	-3049	-374
151	SEG[14]	-2991	-374
152	SEG[15]	-2933	-374
153	SEG[16]	-2875	-374
154	SEG[17]	-2817	-374
155	SEG[18]	-2759	-374
156	SEG[19]	-2701	-374
157	SEG[20]	-2643	-374
158	SEG[21]	-2585	-374
159	SEG[22]	-2527	-374
160	SEG[23]	-2469	-374
161	SEG[24]	-2411	-374
162	SEG[25]	-2353	-374
163	SEG[26]	-2295	-374
164	SEG[27]	-2237	-374
165	SEG[28]	-2179	-374
166	SEG[29]	-2121	-374
167	SEG[30]	-2063	-374
168	SEG[31]	-2005	-374
169	SEG[32]	-1947	-374
170	SEG[33]	-1889	-374
171	SEG[34]	-1831	-374
172	SEG[35]	-1773	-374
173	SEG[36]	-1715	-374
174	SEG[37]	-1657	-374
175	SEG[38]	-1599	-374
176	SEG[39]	-1541	-374
177	SEG[40]	-1483	-374
178	SEG[41]	-1425	-374
179	SEG[42]	-1367	-374
180	SEG[43]	-1309	-374
181	SEG[44]	-1251	-374
182	SEG[45]	-1193	-374
183	SEG[46]	-1135	-374
184	SEG[47]	-1077	-374
185	SEG[48]	-1019	-374
186	SEG[49]	-961	-374
187	SEG[50]	-903	-374
188	SEG[51]	-845	-374
189	SEG[52]	-787	-374
190	SEG[53]	-729	-374
191	SEG[54]	-671	-374
192	SEG[55]	-613	-374
193	SEG[56]	-555	-374
194	SEG[57]	-497	-374
195	SEG[58]	-439	-374
196	SEG[59]	-381	-374
197	SEG[60]	-323	-374
198	SEG[61]	-265	-374

PAD No.	PIN Name	X	Y
199	SEG[62]	-207	-374
200	SEG[63]	-149	-374
201	SEG[64]	-91	-374
202	SEG[65]	-33	-374
203	SEG[66]	25	-374
204	SEG[67]	83	-374
205	SEG[68]	141	-374
206	SEG[69]	199	-374
207	SEG[70]	257	-374
208	SEG[71]	315	-374
209	SEG[72]	373	-374
210	SEG[73]	431	-374
211	SEG[74]	489	-374
212	SEG[75]	547	-374
213	SEG[76]	605	-374
214	SEG[77]	663	-374
215	SEG[78]	721	-374
216	SEG[79]	779	-374
217	SEG[80]	837	-374
218	SEG[81]	895	-374
219	SEG[82]	953	-374
220	SEG[83]	1011	-374
221	SEG[84]	1069	-374
222	SEG[85]	1127	-374
223	SEG[86]	1185	-374
224	SEG[87]	1243	-374
225	SEG[88]	1301	-374
226	SEG[89]	1359	-374
227	SEG[90]	1417	-374
228	SEG[91]	1475	-374
229	SEG[92]	1533	-374
230	SEG[93]	1591	-374
231	SEG[94]	1649	-374
232	SEG[95]	1707	-374
233	SEG[96]	1765	-374
234	SEG[97]	1823	-374
235	SEG[98]	1881	-374
236	SEG[99]	1939	-374
237	SEG[100]	1997	-374
238	SEG[101]	2055	-374
239	SEG[102]	2113	-374
240	SEG[103]	2171	-374
241	SEG[104]	2229	-374
242	SEG[105]	2287	-374
243	SEG[106]	2345	-374
244	SEG[107]	2403	-374
245	SEG[108]	2461	-374

PAD No.	PIN Name	X	Y
246	SEG[109]	2519	-374
247	SEG[110]	2577	-374
248	SEG[111]	2635	-374
249	SEG[112]	2693	-374
250	SEG[113]	2751	-374
251	SEG[114]	2809	-374
252	SEG[115]	2867	-374
253	SEG[116]	2925	-374
254	SEG[117]	2983	-374
255	SEG[118]	3041	-374
256	SEG[119]	3099	-374
257	SEG[120]	3157	-374
258	SEG[121]	3215	-374
259	SEG[122]	3273	-374
260	SEG[123]	3331	-374
261	SEG[124]	3389	-374
262	SEG[125]	3447	-374
263	SEG[126]	3505	-374
264	SEG[127]	3563	-374
265	SEG[128]	3621	-374
266	SEG[129]	3679	-374
267	SEG[130]	3737	-374
268	SEG[131]	3795	-374
269	Reserve	3853	-374
270	Reserve	3911	-374
271	Reserve	3969	-374
272	Reserve	4027	-374
273	Reserve	4085	-374
274	Reserve	4143	-374
275	Reserve	4201	-374
276	Reserve	4259	-374
277	COM[24]	4542	-345
278	COM[25]	4542	-287
279	COM[26]	4542	-229
280	COM[27]	4542	-171
281	COM[28]	4542	-113
282	COM[29]	4542	-55
283	COM[30]	4542	3
284	COM[31]	4542	61
285	COM[32]	4542	119
286	COM[33]	4542	177
287	COM[34]	4542	235
288	COM[35]	4542	293
289	COM[36]	4542	351
290	(NC)	4542	404

**Pad Center Coordinates (1/33 Duty)**Units:  $\mu\text{m}$ 

PAD No.	PIN Name	X	Y
1	COM[21]	4241	374
2	COM[22]	4183	374
3	COM[23]	4125	374
4	COM[24]	4067	374
5	COM[25]	4009	374
6	COM[26]	3951	374
7	COM[27]	3893	374
8	COM[28]	3835	374
9	COM[29]	3777	374
10	COM[30]	3719	374
11	COM[31]	3661	374
12	COMS1	3603	374
13	FRS	3443	389
14	FR	3369	389
15	CL	3295	389
16	/DOF	3221	389
17	VSS	3147	389
18	/CS1	3073	389
19	CS2	2999	389
20	VDD	2925	389
21	/RES	2851	389
22	A0	2777	389
23	VSS	2703	389
24	/WR(R/W)	2629	389
25	/RD(E)	2555	389
26	VDD	2481	389
27	D0	2407	389
28	D1	2333	389
29	D2	2259	389
30	D3	2185	389
31	D4	2111	389
32	D5	2037	389
33	D6	1963	389
34	D7	1889	389
35	VDD	1815	389
36	VDD2	1741	389
37	VDD2	1667	389
38	VSS	1593	389
39	VSS	1519	389
40	VSS	1445	389
41	VSS	1371	389
42	VOUT	1297	389
43	VOUT	1223	389
44	CAP5P	1149	389
45	CAP5P	1075	389
46	CAP1N	1001	389
47	CAP1N	927	389

PAD No.	PIN Name	X	Y
48	CAP3P	853	389
49	CAP3P	779	389
50	CAP1N	705	389
51	CAP1N	631	389
52	CAP1P	557	389
53	CAP1P	483	389
54	CAP2P	409	389
55	CAP2P	335	389
56	CAP2N	261	389
57	CAP2N	187	389
58	CAP4P	113	389
59	CAP4P	39	389
60	VSS	-35	389
61	VSS	-109	389
62	VRS	-183	389
63	VRS	-257	389
64	VDD2	-331	389
65	VDD	-405	389
66	V4	-479	389
67	V4	-553	389
68	V3	-627	389
69	V3	-701	389
70	V2	-775	389
71	V2	-849	389
72	V1	-923	389
73	V1	-997	389
74	V0	-1071	389
75	V0	-1145	389
76	VR	-1219	389
77	VR	-1293	389
78	VDD	-1367	389
79	VDD2	-1441	389
80	TEST0	-1515	389
81	TEST1	-1589	389
82	TEST2	-1663	389
83	TEST3	-1737	389
84	TEST4	-1811	389
85	TEST5	-1885	389
86	VDD	-1959	389
87	M/S	-2033	389
88	CLS	-2107	389
89	VSS	-2181	389
90	C86	-2255	389
91	P/S	-2329	389
92	VDD	-2403	389
93	/HPM	-2477	389
94	VSS	-2551	389

PAD No.	PIN Name	X	Y
95	IRS	-2625	389
96	VDD	-2699	389
97	SEL1	-2773	389
98	VSS	-2847	389
99	SEL2	-2921	389
100	VDD	-2995	389
101	SEL3	-3069	389
102	VSS	-3143	389
103	Reserve	-3606	374
104	Reserve	-3664	374
105	Reserve	-3722	374
106	Reserve	-3780	374
107	Reserve	-3838	374
108	Reserve	-3896	374
109	Reserve	-3954	374
110	Reserve	-4012	374
111	Reserve	-4070	374
112	Reserve	-4128	374
113	Reserve	-4186	374
114	Reserve	-4244	374
115	(NC)	-4542	404
116	Reserve	-4542	351
117	Reserve	-4542	293
118	Reserve	-4542	235
119	Reserve	-4542	177
120	COM[15]	-4542	119
121	COM[14]	-4542	61
122	COM[13]	-4542	3
123	COM[12]	-4542	-55
124	COM[11]	-4542	-113
125	COM[10]	-4542	-171
126	COM[9]	-4542	-229
127	COM[8]	-4542	-287
128	COM[7]	-4542	-345
129	COM[6]	-4267	-374
130	COM[5]	-4209	-374
131	COM[4]	-4151	-374
132	COM[3]	-4093	-374
133	COM[2]	-4035	-374
134	COM[1]	-3977	-374
135	COM[0]	-3919	-374
136	COMS2	-3861	-374
137	SEG[0]	-3803	-374
138	SEG[1]	-3745	-374
139	SEG[2]	-3687	-374
140	SEG[3]	-3629	-374
141	SEG[4]	-3571	-374
142	SEG[5]	-3513	-374
143	SEG[6]	-3455	-374
144	SEG[7]	-3397	-374
145	SEG[8]	-3339	-374
146	SEG[9]	-3281	-374

PAD No.	PIN Name	X	Y
147	SEG[10]	-3223	-374
148	SEG[11]	-3165	-374
149	SEG[12]	-3107	-374
150	SEG[13]	-3049	-374
151	SEG[14]	-2991	-374
152	SEG[15]	-2933	-374
153	SEG[16]	-2875	-374
154	SEG[17]	-2817	-374
155	SEG[18]	-2759	-374
156	SEG[19]	-2701	-374
157	SEG[20]	-2643	-374
158	SEG[21]	-2585	-374
159	SEG[22]	-2527	-374
160	SEG[23]	-2469	-374
161	SEG[24]	-2411	-374
162	SEG[25]	-2353	-374
163	SEG[26]	-2295	-374
164	SEG[27]	-2237	-374
165	SEG[28]	-2179	-374
166	SEG[29]	-2121	-374
167	SEG[30]	-2063	-374
168	SEG[31]	-2005	-374
169	SEG[32]	-1947	-374
170	SEG[33]	-1889	-374
171	SEG[34]	-1831	-374
172	SEG[35]	-1773	-374
173	SEG[36]	-1715	-374
174	SEG[37]	-1657	-374
175	SEG[38]	-1599	-374
176	SEG[39]	-1541	-374
177	SEG[40]	-1483	-374
178	SEG[41]	-1425	-374
179	SEG[42]	-1367	-374
180	SEG[43]	-1309	-374
181	SEG[44]	-1251	-374
182	SEG[45]	-1193	-374
183	SEG[46]	-1135	-374
184	SEG[47]	-1077	-374
185	SEG[48]	-1019	-374
186	SEG[49]	-961	-374
187	SEG[50]	-903	-374
188	SEG[51]	-845	-374
189	SEG[52]	-787	-374
190	SEG[53]	-729	-374
191	SEG[54]	-671	-374
192	SEG[55]	-613	-374
193	SEG[56]	-555	-374
194	SEG[57]	-497	-374
195	SEG[58]	-439	-374
196	SEG[59]	-381	-374
197	SEG[60]	-323	-374
198	SEG[61]	-265	-374



PAD No.	PIN Name	X	Y
199	SEG[62]	-207	-374
200	SEG[63]	-149	-374
201	SEG[64]	-91	-374
202	SEG[65]	-33	-374
203	SEG[66]	25	-374
204	SEG[67]	83	-374
205	SEG[68]	141	-374
206	SEG[69]	199	-374
207	SEG[70]	257	-374
208	SEG[71]	315	-374
209	SEG[72]	373	-374
210	SEG[73]	431	-374
211	SEG[74]	489	-374
212	SEG[75]	547	-374
213	SEG[76]	605	-374
214	SEG[77]	663	-374
215	SEG[78]	721	-374
216	SEG[79]	779	-374
217	SEG[80]	837	-374
218	SEG[81]	895	-374
219	SEG[82]	953	-374
220	SEG[83]	1011	-374
221	SEG[84]	1069	-374
222	SEG[85]	1127	-374
223	SEG[86]	1185	-374
224	SEG[87]	1243	-374
225	SEG[88]	1301	-374
226	SEG[89]	1359	-374
227	SEG[90]	1417	-374
228	SEG[91]	1475	-374
229	SEG[92]	1533	-374
230	SEG[93]	1591	-374
231	SEG[94]	1649	-374
232	SEG[95]	1707	-374
233	SEG[96]	1765	-374
234	SEG[97]	1823	-374
235	SEG[98]	1881	-374
236	SEG[99]	1939	-374
237	SEG[100]	1997	-374
238	SEG[101]	2055	-374
239	SEG[102]	2113	-374
240	SEG[103]	2171	-374
241	SEG[104]	2229	-374
242	SEG[105]	2287	-374
243	SEG[106]	2345	-374
244	SEG[107]	2403	-374
245	SEG[108]	2461	-374

PAD No.	PIN Name	X	Y
246	SEG[109]	2519	-374
247	SEG[110]	2577	-374
248	SEG[111]	2635	-374
249	SEG[112]	2693	-374
250	SEG[113]	2751	-374
251	SEG[114]	2809	-374
252	SEG[115]	2867	-374
253	SEG[116]	2925	-374
254	SEG[117]	2983	-374
255	SEG[118]	3041	-374
256	SEG[119]	3099	-374
257	SEG[120]	3157	-374
258	SEG[121]	3215	-374
259	SEG[122]	3273	-374
260	SEG[123]	3331	-374
261	SEG[124]	3389	-374
262	SEG[125]	3447	-374
263	SEG[126]	3505	-374
264	SEG[127]	3563	-374
265	SEG[128]	3621	-374
266	SEG[129]	3679	-374
267	SEG[130]	3737	-374
268	SEG[131]	3795	-374
269	Reserve	3853	-374
270	Reserve	3911	-374
271	Reserve	3969	-374
272	Reserve	4027	-374
273	Reserve	4085	-374
274	Reserve	4143	-374
275	Reserve	4201	-374
276	Reserve	4259	-374
277	Reserve	4542	-345
278	Reserve	4542	-287
279	Reserve	4542	-229
280	Reserve	4542	-171
281	Reserve	4542	-113
282	Reserve	4542	-55
283	Reserve	4542	3
284	Reserve	4542	61
285	COM[16]	4542	119
286	COM[17]	4542	177
287	COM[18]	4542	235
288	COM[19]	4542	293
289	COM[20]	4542	351
290	(NC)	4542	404



**Pad Center Coordinates (1/55 Duty)**Units:  $\mu\text{m}$ 

PAD No.	PIN Name	X	Y
1	COM[43]	4241	374
2	COM[44]	4183	374
3	COM[45]	4125	374
4	COM[46]	4067	374
5	COM[47]	4009	374
6	COM[48]	3951	374
7	COM[49]	3893	374
8	COM[50]	3835	374
9	COM[51]	3777	374
10	COM[52]	3719	374
11	COM[53]	3661	374
12	COMS1	3603	374
13	FRS	3443	389
14	FR	3369	389
15	CL	3295	389
16	/DOF	3221	389
17	VSS	3147	389
18	/CS1	3073	389
19	CS2	2999	389
20	VDD	2925	389
21	/RES	2851	389
22	A0	2777	389
23	VSS	2703	389
24	/WR(R/W)	2629	389
25	/RD(E)	2555	389
26	VDD	2481	389
27	D0	2407	389
28	D1	2333	389
29	D2	2259	389
30	D3	2185	389
31	D4	2111	389
32	D5	2037	389
33	D6	1963	389
34	D7	1889	389
35	VDD	1815	389
36	VDD2	1741	389
37	VDD2	1667	389
38	VSS	1593	389
39	VSS	1519	389
40	VSS	1445	389
41	VSS	1371	389
42	VOUT	1297	389
43	VOUT	1223	389
44	CAP5P	1149	389
45	CAP5P	1075	389
46	CAP1N	1001	389
47	CAP1N	927	389

PAD No.	PIN Name	X	Y
48	CAP3P	853	389
49	CAP3P	779	389
50	CAP1N	705	389
51	CAP1N	631	389
52	CAP1P	557	389
53	CAP1P	483	389
54	CAP2P	409	389
55	CAP2P	335	389
56	CAP2N	261	389
57	CAP2N	187	389
58	CAP4P	113	389
59	CAP4P	39	389
60	VSS	-35	389
61	VSS	-109	389
62	VRS	-183	389
63	VRS	-257	389
64	VDD2	-331	389
65	VDD	-405	389
66	V4	-479	389
67	V4	-553	389
68	V3	-627	389
69	V3	-701	389
70	V2	-775	389
71	V2	-849	389
72	V1	-923	389
73	V1	-997	389
74	V0	-1071	389
75	V0	-1145	389
76	VR	-1219	389
77	VR	-1293	389
78	VDD	-1367	389
79	VDD2	-1441	389
80	TEST0	-1515	389
81	TEST1	-1589	389
82	TEST2	-1663	389
83	TEST3	-1737	389
84	TEST4	-1811	389
85	TEST5	-1885	389
86	VDD	-1959	389
87	M/S	-2033	389
88	CLS	-2107	389
89	VSS	-2181	389
90	C86	-2255	389
91	P/S	-2329	389
92	VDD	-2403	389
93	/HPM	-2477	389
94	VSS	-2551	389

PAD No.	PIN Name	X	Y
95	IRS	-2625	389
96	VDD	-2699	389
97	SEL1	-2773	389
98	VSS	-2847	389
99	SEL2	-2921	389
100	VDD	-2995	389
101	SEL3	-3069	389
102	VSS	-3143	389
103	Reserve	-3606	374
104	Reserve	-3664	374
105	Reserve	-3722	374
106	Reserve	-3780	374
107	Reserve	-3838	374
108	COM[26]	-3896	374
109	COM[25]	-3954	374
110	COM[24]	-4012	374
111	COM[23]	-4070	374
112	COM[22]	-4128	374
113	COM[21]	-4186	374
114	COM[20]	-4244	374
115	(NC)	-4542	404
116	COM[19]	-4542	351
117	COM[18]	-4542	293
118	COM[17]	-4542	235
119	COM[16]	-4542	177
120	COM[15]	-4542	119
121	COM[14]	-4542	61
122	COM[13]	-4542	3
123	COM[12]	-4542	-55
124	COM[11]	-4542	-113
125	COM[10]	-4542	-171
126	COM[9]	-4542	-229
127	COM[8]	-4542	-287
128	COM[7]	-4542	-345
129	COM[6]	-4267	-374
130	COM[5]	-4209	-374
131	COM[4]	-4151	-374
132	COM[3]	-4093	-374
133	COM[2]	-4035	-374
134	COM[1]	-3977	-374
135	COM[0]	-3919	-374
136	COMS2	-3861	-374
137	SEG[0]	-3803	-374
138	SEG[1]	-3745	-374
139	SEG[2]	-3687	-374
140	SEG[3]	-3629	-374
141	SEG[4]	-3571	-374
142	SEG[5]	-3513	-374
143	SEG[6]	-3455	-374
144	SEG[7]	-3397	-374
145	SEG[8]	-3339	-374
146	SEG[9]	-3281	-374

PAD No.	PIN Name	X	Y
147	SEG[10]	-3223	-374
148	SEG[11]	-3165	-374
149	SEG[12]	-3107	-374
150	SEG[13]	-3049	-374
151	SEG[14]	-2991	-374
152	SEG[15]	-2933	-374
153	SEG[16]	-2875	-374
154	SEG[17]	-2817	-374
155	SEG[18]	-2759	-374
156	SEG[19]	-2701	-374
157	SEG[20]	-2643	-374
158	SEG[21]	-2585	-374
159	SEG[22]	-2527	-374
160	SEG[23]	-2469	-374
161	SEG[24]	-2411	-374
162	SEG[25]	-2353	-374
163	SEG[26]	-2295	-374
164	SEG[27]	-2237	-374
165	SEG[28]	-2179	-374
166	SEG[29]	-2121	-374
167	SEG[30]	-2063	-374
168	SEG[31]	-2005	-374
169	SEG[32]	-1947	-374
170	SEG[33]	-1889	-374
171	SEG[34]	-1831	-374
172	SEG[35]	-1773	-374
173	SEG[36]	-1715	-374
174	SEG[37]	-1657	-374
175	SEG[38]	-1599	-374
176	SEG[39]	-1541	-374
177	SEG[40]	-1483	-374
178	SEG[41]	-1425	-374
179	SEG[42]	-1367	-374
180	SEG[43]	-1309	-374
181	SEG[44]	-1251	-374
182	SEG[45]	-1193	-374
183	SEG[46]	-1135	-374
184	SEG[47]	-1077	-374
185	SEG[48]	-1019	-374
186	SEG[49]	-961	-374
187	SEG[50]	-903	-374
188	SEG[51]	-845	-374
189	SEG[52]	-787	-374
190	SEG[53]	-729	-374
191	SEG[54]	-671	-374
192	SEG[55]	-613	-374
193	SEG[56]	-555	-374
194	SEG[57]	-497	-374
195	SEG[58]	-439	-374
196	SEG[59]	-381	-374
197	SEG[60]	-323	-374
198	SEG[61]	-265	-374

PAD No.	PIN Name	X	Y
199	SEG[62]	-207	-374
200	SEG[63]	-149	-374
201	SEG[64]	-91	-374
202	SEG[65]	-33	-374
203	SEG[66]	25	-374
204	SEG[67]	83	-374
205	SEG[68]	141	-374
206	SEG[69]	199	-374
207	SEG[70]	257	-374
208	SEG[71]	315	-374
209	SEG[72]	373	-374
210	SEG[73]	431	-374
211	SEG[74]	489	-374
212	SEG[75]	547	-374
213	SEG[76]	605	-374
214	SEG[77]	663	-374
215	SEG[78]	721	-374
216	SEG[79]	779	-374
217	SEG[80]	837	-374
218	SEG[81]	895	-374
219	SEG[82]	953	-374
220	SEG[83]	1011	-374
221	SEG[84]	1069	-374
222	SEG[85]	1127	-374
223	SEG[86]	1185	-374
224	SEG[87]	1243	-374
225	SEG[88]	1301	-374
226	SEG[89]	1359	-374
227	SEG[90]	1417	-374
228	SEG[91]	1475	-374
229	SEG[92]	1533	-374
230	SEG[93]	1591	-374
231	SEG[94]	1649	-374
232	SEG[95]	1707	-374
233	SEG[96]	1765	-374
234	SEG[97]	1823	-374
235	SEG[98]	1881	-374
236	SEG[99]	1939	-374
237	SEG[100]	1997	-374
238	SEG[101]	2055	-374
239	SEG[102]	2113	-374
240	SEG[103]	2171	-374
241	SEG[104]	2229	-374
242	SEG[105]	2287	-374
243	SEG[106]	2345	-374
244	SEG[107]	2403	-374
245	SEG[108]	2461	-374

PAD No.	PIN Name	X	Y
246	SEG[109]	2519	-374
247	SEG[110]	2577	-374
248	SEG[111]	2635	-374
249	SEG[112]	2693	-374
250	SEG[113]	2751	-374
251	SEG[114]	2809	-374
252	SEG[115]	2867	-374
253	SEG[116]	2925	-374
254	SEG[117]	2983	-374
255	SEG[118]	3041	-374
256	SEG[119]	3099	-374
257	SEG[120]	3157	-374
258	SEG[121]	3215	-374
259	SEG[122]	3273	-374
260	SEG[123]	3331	-374
261	SEG[124]	3389	-374
262	SEG[125]	3447	-374
263	SEG[126]	3505	-374
264	SEG[127]	3563	-374
265	SEG[128]	3621	-374
266	SEG[129]	3679	-374
267	SEG[130]	3737	-374
268	SEG[131]	3795	-374
269	Reserve	3853	-374
270	Reserve	3911	-374
271	Reserve	3969	-374
272	Reserve	4027	-374
273	Reserve	4085	-374
274	COM[27]	4143	-374
275	COM[28]	4201	-374
276	COM[29]	4259	-374
277	COM[30]	4542	-345
278	COM[31]	4542	-287
279	COM[32]	4542	-229
280	COM[33]	4542	-171
281	COM[34]	4542	-113
282	COM[35]	4542	-55
283	COM[36]	4542	3
284	COM[37]	4542	61
285	COM[38]	4542	119
286	COM[39]	4542	177
287	COM[40]	4542	235
288	COM[41]	4542	293
289	COM[42]	4542	351
290	(NC)	4542	404

**Pad Center Coordinates (1/53 Duty)**Units:  $\mu\text{m}$ 

PAD No.	PIN Name	X	Y
1	COM[41]	4241	374
2	COM[42]	4183	374
3	COM[43]	4125	374
4	COM[44]	4067	374
5	COM[45]	4009	374
6	COM[46]	3951	374
7	COM[47]	3893	374
8	COM[48]	3835	374
9	COM[49]	3777	374
10	COM[50]	3719	374
11	COM[51]	3661	374
12	COMS1	3603	374
13	FRS	3443	389
14	FR	3369	389
15	CL	3295	389
16	/DOF	3221	389
17	VSS	3147	389
18	/CS1	3073	389
19	CS2	2999	389
20	VDD	2925	389
21	/RES	2851	389
22	A0	2777	389
23	VSS	2703	389
24	/WR(R/W)	2629	389
25	/RD(E)	2555	389
26	VDD	2481	389
27	D0	2407	389
28	D1	2333	389
29	D2	2259	389
30	D3	2185	389
31	D4	2111	389
32	D5	2037	389
33	D6	1963	389
34	D7	1889	389
35	VDD	1815	389
36	VDD2	1741	389
37	VDD2	1667	389
38	VSS	1593	389
39	VSS	1519	389
40	VSS	1445	389
41	VSS	1371	389
42	VOUT	1297	389
43	VOUT	1223	389
44	CAP5P	1149	389
45	CAP5P	1075	389
46	CAP1N	1001	389
47	CAP1N	927	389

PAD No.	PIN Name	X	Y
48	CAP3P	853	389
49	CAP3P	779	389
50	CAP1N	705	389
51	CAP1N	631	389
52	CAP1P	557	389
53	CAP1P	483	389
54	CAP2P	409	389
55	CAP2P	335	389
56	CAP2N	261	389
57	CAP2N	187	389
58	CAP4P	113	389
59	CAP4P	39	389
60	VSS	-35	389
61	VSS	-109	389
62	VRS	-183	389
63	VRS	-257	389
64	VDD2	-331	389
65	VDD	-405	389
66	V4	-479	389
67	V4	-553	389
68	V3	-627	389
69	V3	-701	389
70	V2	-775	389
71	V2	-849	389
72	V1	-923	389
73	V1	-997	389
74	V0	-1071	389
75	V0	-1145	389
76	VR	-1219	389
77	VR	-1293	389
78	VDD	-1367	389
79	VDD2	-1441	389
80	TEST0	-1515	389
81	TEST1	-1589	389
82	TEST2	-1663	389
83	TEST3	-1737	389
84	TEST4	-1811	389
85	TEST5	-1885	389
86	VDD	-1959	389
87	M/S	-2033	389
88	CLS	-2107	389
89	VSS	-2181	389
90	C86	-2255	389
91	P/S	-2329	389
92	VDD	-2403	389
93	/HPM	-2477	389
94	VSS	-2551	389

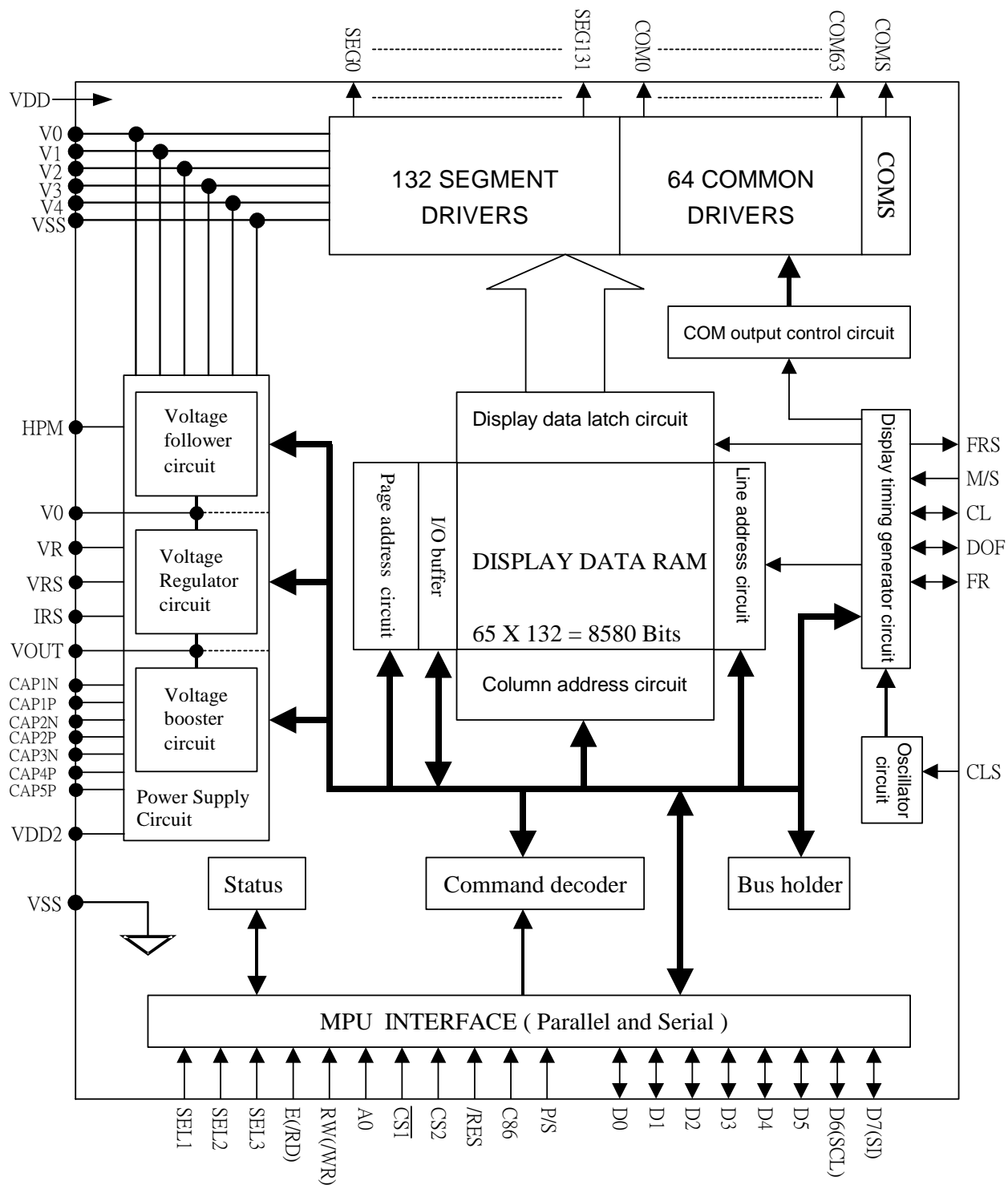
PAD No.	PIN Name	X	Y
95	IRS	-2625	389
96	VDD	-2699	389
97	SEL1	-2773	389
98	VSS	-2847	389
99	SEL2	-2921	389
100	VDD	-2995	389
101	SEL3	-3069	389
102	VSS	-3143	389
103	Reserve	-3606	374
104	Reserve	-3664	374
105	Reserve	-3722	374
106	Reserve	-3780	374
107	Reserve	-3838	374
108	Reserve	-3896	374
109	COM[25]	-3954	374
110	COM[24]	-4012	374
111	COM[23]	-4070	374
112	COM[22]	-4128	374
113	COM[21]	-4186	374
114	COM[20]	-4244	374
115	(NC)	-4542	404
116	COM[19]	-4542	351
117	COM[18]	-4542	293
118	COM[17]	-4542	235
119	COM[16]	-4542	177
120	COM[15]	-4542	119
121	COM[14]	-4542	61
122	COM[13]	-4542	3
123	COM[12]	-4542	-55
124	COM[11]	-4542	-113
125	COM[10]	-4542	-171
126	COM[9]	-4542	-229
127	COM[8]	-4542	-287
128	COM[7]	-4542	-345
129	COM[6]	-4267	-374
130	COM[5]	-4209	-374
131	COM[4]	-4151	-374
132	COM[3]	-4093	-374
133	COM[2]	-4035	-374
134	COM[1]	-3977	-374
135	COM[0]	-3919	-374
136	COMS2	-3861	-374
137	SEG[0]	-3803	-374
138	SEG[1]	-3745	-374
139	SEG[2]	-3687	-374
140	SEG[3]	-3629	-374
141	SEG[4]	-3571	-374
142	SEG[5]	-3513	-374
143	SEG[6]	-3455	-374
144	SEG[7]	-3397	-374
145	SEG[8]	-3339	-374
146	SEG[9]	-3281	-374

PAD No.	PIN Name	X	Y
147	SEG[10]	-3223	-374
148	SEG[11]	-3165	-374
149	SEG[12]	-3107	-374
150	SEG[13]	-3049	-374
151	SEG[14]	-2991	-374
152	SEG[15]	-2933	-374
153	SEG[16]	-2875	-374
154	SEG[17]	-2817	-374
155	SEG[18]	-2759	-374
156	SEG[19]	-2701	-374
157	SEG[20]	-2643	-374
158	SEG[21]	-2585	-374
159	SEG[22]	-2527	-374
160	SEG[23]	-2469	-374
161	SEG[24]	-2411	-374
162	SEG[25]	-2353	-374
163	SEG[26]	-2295	-374
164	SEG[27]	-2237	-374
165	SEG[28]	-2179	-374
166	SEG[29]	-2121	-374
167	SEG[30]	-2063	-374
168	SEG[31]	-2005	-374
169	SEG[32]	-1947	-374
170	SEG[33]	-1889	-374
171	SEG[34]	-1831	-374
172	SEG[35]	-1773	-374
173	SEG[36]	-1715	-374
174	SEG[37]	-1657	-374
175	SEG[38]	-1599	-374
176	SEG[39]	-1541	-374
177	SEG[40]	-1483	-374
178	SEG[41]	-1425	-374
179	SEG[42]	-1367	-374
180	SEG[43]	-1309	-374
181	SEG[44]	-1251	-374
182	SEG[45]	-1193	-374
183	SEG[46]	-1135	-374
184	SEG[47]	-1077	-374
185	SEG[48]	-1019	-374
186	SEG[49]	-961	-374
187	SEG[50]	-903	-374
188	SEG[51]	-845	-374
189	SEG[52]	-787	-374
190	SEG[53]	-729	-374
191	SEG[54]	-671	-374
192	SEG[55]	-613	-374
193	SEG[56]	-555	-374
194	SEG[57]	-497	-374
195	SEG[58]	-439	-374
196	SEG[59]	-381	-374
197	SEG[60]	-323	-374
198	SEG[61]	-265	-374

PAD No.	PIN Name	X	Y
199	SEG[62]	-207	-374
200	SEG[63]	-149	-374
201	SEG[64]	-91	-374
202	SEG[65]	-33	-374
203	SEG[66]	25	-374
204	SEG[67]	83	-374
205	SEG[68]	141	-374
206	SEG[69]	199	-374
207	SEG[70]	257	-374
208	SEG[71]	315	-374
209	SEG[72]	373	-374
210	SEG[73]	431	-374
211	SEG[74]	489	-374
212	SEG[75]	547	-374
213	SEG[76]	605	-374
214	SEG[77]	663	-374
215	SEG[78]	721	-374
216	SEG[79]	779	-374
217	SEG[80]	837	-374
218	SEG[81]	895	-374
219	SEG[82]	953	-374
220	SEG[83]	1011	-374
221	SEG[84]	1069	-374
222	SEG[85]	1127	-374
223	SEG[86]	1185	-374
224	SEG[87]	1243	-374
225	SEG[88]	1301	-374
226	SEG[89]	1359	-374
227	SEG[90]	1417	-374
228	SEG[91]	1475	-374
229	SEG[92]	1533	-374
230	SEG[93]	1591	-374
231	SEG[94]	1649	-374
232	SEG[95]	1707	-374
233	SEG[96]	1765	-374
234	SEG[97]	1823	-374
235	SEG[98]	1881	-374
236	SEG[99]	1939	-374
237	SEG[100]	1997	-374
238	SEG[101]	2055	-374
239	SEG[102]	2113	-374
240	SEG[103]	2171	-374
241	SEG[104]	2229	-374
242	SEG[105]	2287	-374
243	SEG[106]	2345	-374
244	SEG[107]	2403	-374
245	SEG[108]	2461	-374

PAD No.	PIN Name	X	Y
246	SEG[109]	2519	-374
247	SEG[110]	2577	-374
248	SEG[111]	2635	-374
249	SEG[112]	2693	-374
250	SEG[113]	2751	-374
251	SEG[114]	2809	-374
252	SEG[115]	2867	-374
253	SEG[116]	2925	-374
254	SEG[117]	2983	-374
255	SEG[118]	3041	-374
256	SEG[119]	3099	-374
257	SEG[120]	3157	-374
258	SEG[121]	3215	-374
259	SEG[122]	3273	-374
260	SEG[123]	3331	-374
261	SEG[124]	3389	-374
262	SEG[125]	3447	-374
263	SEG[126]	3505	-374
264	SEG[127]	3563	-374
265	SEG[128]	3621	-374
266	SEG[129]	3679	-374
267	SEG[130]	3737	-374
268	SEG[131]	3795	-374
269	Reserve	3853	-374
270	Reserve	3911	-374
271	Reserve	3969	-374
272	Reserve	4027	-374
273	Reserve	4085	-374
274	Reserve	4143	-374
275	COM[26]	4201	-374
276	COM[27]	4259	-374
277	COM[28]	4542	-345
278	COM[29]	4542	-287
279	COM[30]	4542	-229
280	COM[31]	4542	-171
281	COM[32]	4542	-113
282	COM[33]	4542	-55
283	COM[34]	4542	3
284	COM[35]	4542	61
285	COM[36]	4542	119
286	COM[37]	4542	177
287	COM[38]	4542	235
288	COM[39]	4542	293
289	COM[40]	4542	351
290	(NC)	4542	404

## BLOCK DIAGRAM



## PIN DESCRIPTIONS

### Power Supply Pins

Pin Name	I/O	Function	No. of Pins																														
VDD	Power Supply	Power supply	13																														
VDD2	Power Supply	Power supply	10																														
VSS	Power Supply	Ground	2																														
VRS	Power Supply	This is the internal-output VREG power supply for the LCD power supply voltage regulator.	2																														
V0, V1, V2, V3, V4,Vss	Power Supply	<p>This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on Vss, and must maintain the relative magnitudes shown below.</p> <p><math>V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq Vss</math></p> <p>When the power supply turns ON, the internal power supply circuits produce the V1 to V4 voltages shown below. The voltage settings are selected using the LCD bias set command.</p> <table><tr><td></td><td>1/65 DUTY</td><td>1/49 DUTY</td><td>1/33 DUTY</td><td>1/55 DUTY</td><td>1/53 DUTY</td></tr><tr><td>V1</td><td>8/9*V0,6/7*V0</td><td>7/8*V0,5/6*V0</td><td>5/6*V0,4/5*V0</td><td>7/8*V0,5/6*V0</td><td>7/8*V0,5/6*V0</td></tr><tr><td>V2</td><td>7/9*V0,5/7*V0</td><td>6/8*V0,4/6*V0</td><td>4/6*V0,3/5*V0</td><td>6/8*V0,4/6*V0</td><td>6/8*V0,4/6*V0</td></tr><tr><td>V3</td><td>2/9*V0,2/7*V0</td><td>2/8*V0,2/6*V0</td><td>2/6*V0,2/5*V0</td><td>2/8*V0,2/6*V0</td><td>2/8*V0,2/6*V0</td></tr><tr><td>V4</td><td>1/9*V0,1/7*V0</td><td>1/8*V0,1/6*V0</td><td>1/6*V0,1/5*V0</td><td>1/8*V0,1/6*V0</td><td>1/8*V0,1/6*V0</td></tr></table>		1/65 DUTY	1/49 DUTY	1/33 DUTY	1/55 DUTY	1/53 DUTY	V1	8/9*V0,6/7*V0	7/8*V0,5/6*V0	5/6*V0,4/5*V0	7/8*V0,5/6*V0	7/8*V0,5/6*V0	V2	7/9*V0,5/7*V0	6/8*V0,4/6*V0	4/6*V0,3/5*V0	6/8*V0,4/6*V0	6/8*V0,4/6*V0	V3	2/9*V0,2/7*V0	2/8*V0,2/6*V0	2/6*V0,2/5*V0	2/8*V0,2/6*V0	2/8*V0,2/6*V0	V4	1/9*V0,1/7*V0	1/8*V0,1/6*V0	1/6*V0,1/5*V0	1/8*V0,1/6*V0	1/8*V0,1/6*V0	10
	1/65 DUTY	1/49 DUTY	1/33 DUTY	1/55 DUTY	1/53 DUTY																												
V1	8/9*V0,6/7*V0	7/8*V0,5/6*V0	5/6*V0,4/5*V0	7/8*V0,5/6*V0	7/8*V0,5/6*V0																												
V2	7/9*V0,5/7*V0	6/8*V0,4/6*V0	4/6*V0,3/5*V0	6/8*V0,4/6*V0	6/8*V0,4/6*V0																												
V3	2/9*V0,2/7*V0	2/8*V0,2/6*V0	2/6*V0,2/5*V0	2/8*V0,2/6*V0	2/8*V0,2/6*V0																												
V4	1/9*V0,1/7*V0	1/8*V0,1/6*V0	1/6*V0,1/5*V0	1/8*V0,1/6*V0	1/8*V0,1/6*V0																												

### LCD Power Supply Pins

Pin Name	I/O	Function	No. of Pins
CAP1P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.	4
CAP1N	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1P terminal.	2
CAP2P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.	2
CAP2N	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2P terminal.	2
CAP3P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.	2
CAP4P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.	2
CAP5P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.	2
VOOUT	O	DC/DC voltage converter. Connect a capacitor between this terminal and VSS or VDD	2
VR	I	<p>Output voltage regulator terminal. Provides the voltage between VSS and V0 through a resistive voltage divider.</p> <p>IRS = "L" : the V0 voltage regulator internal resistors are not used.</p> <p>IRS = "H" : the V0 voltage regulator internal resistors are used.</p>	2



## System Bus Connection Pins

Pin Name	I/O	Function	No. of Pins															
D5 to D0 D6 (SCL) D7 (SI)	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface (SPI-4) is selected (P/S = "L") : D7 : serial data input (SI) ; D6 : the serial clock input (SCL). D0 to D5 should be connected to VDD or floating. When the chip select is not active, D0 to D7 are set to high impedance.	8															
A0	I	This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or command. A0 = "H": Indicates that D0 to D7 are display data. A0 = "L": Indicates that D0 to D7 are control data.	1															
/RES	I	When /RES is set to "L", the register settings are initialized (cleared). The reset operation is performed by the /RES signal level.	1															
/CS1 CS2	I	This is the chip select signal. When /CS1 = "L" and CS2 = "H", then the chip select becomes active, and data/command I/O is enabled.	2															
/RD (E)	I	• When connected to 8080 series MPU, this pin is treated as the "/RD" signal of the 8080 MPU and is LOW-active. The data bus is in an output status when this signal is "L". • When connected to 6800 series MPU, this pin is treated as the "E" signal of the 6800 MPU and is HIGH-active. This is the enable clock input terminal of the 6800 Series MPU.	1															
/WR (R/W)	I	• When connected to 8080 series MPU, this pin is treated as the "/WR" signal of the 8080 MPU and is LOW-active. The signals on the data bus are latched at the rising edge of the /WR signal. • When connected to 6800 series MPU, this pin is treated as the "R/W" signal of the 6800 MPU and decides the access type : When R/W = "H": Read. When R/W = "L": Write.	1															
C86	I	This is the MPU interface selection pin. C86 = "H": 6800 Series MPU interface. C86 = "L": 8080 Series MPU interface.	1															
P/S	I	<div><div>This pin configures the interface to be parallel mode or serial mode. P/S = "H": Parallel data input/output. P/S = "L": Serial data input. The following applies depending on the P/S status:</div><table><tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial Clock</th></tr><tr><td>"H"</td><td>A0</td><td>D0 to D7</td><td>/RD, /WR</td><td>X</td></tr><tr><td>"L"</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td>SCL (D6)</td></tr></table><div>When P/S = "L", D0 to D5 must be fixed to "H". /RD (E) and /WR (R/W) are fixed to either "H" or "L". The serial access mode does NOT support read operation.</div></div>	P/S	Data/Command	Data	Read/Write	Serial Clock	"H"	A0	D0 to D7	/RD, /WR	X	"L"	A0	SI (D7)	Write only	SCL (D6)	1
P/S	Data/Command	Data	Read/Write	Serial Clock														
"H"	A0	D0 to D7	/RD, /WR	X														
"L"	A0	SI (D7)	Write only	SCL (D6)														

Pin Name	I/O	Function	No. of Pins																																			
CLS	I	Selection pin to enable or disable the internal display clock oscillator circuit. CLS = "H" : use internal oscillator circuit . CLS = "L" : use external clock input (internal oscillator is disabled). When CLS = "L", input the external display clock through the CL terminal.	1																																			
M/S	I	<div>This terminal selects the master/slave operation for the ST7565P Series chips. Master operation outputs the timing signals that are required for the LCD display, while slave operation input the timing signals required for the liquid crystal display. That synchronized the liquid crystal display system between Master and Slave. M/S = "H" Master operation M/S = "L" Slave operation</div> <table><tr><th>M/S</th><th>CLS</th><th>Oscillator Circuit</th><th>Power Supply Circuit</th><th>CL</th><th>FR</th><th>DOF</th></tr><tr><td>"H"</td><td>"H"</td><td>Enabled</td><td>Enabled</td><td>Output</td><td>Output</td><td>Output</td></tr><tr><td>"H"</td><td>"L"</td><td>Disabled</td><td>Enabled</td><td>Input</td><td>Output</td><td>Output</td></tr><tr><td>"L"</td><td>"H"</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Input</td></tr><tr><td>"L"</td><td>"L"</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Input</td></tr></table>	M/S	CLS	Oscillator Circuit	Power Supply Circuit	CL	FR	DOF	"H"	"H"	Enabled	Enabled	Output	Output	Output	"H"	"L"	Disabled	Enabled	Input	Output	Output	"L"	"H"	Disabled	Disabled	Input	Input	Input	"L"	"L"	Disabled	Disabled	Input	Input	Input	1
M/S	CLS	Oscillator Circuit	Power Supply Circuit	CL	FR	DOF																																
"H"	"H"	Enabled	Enabled	Output	Output	Output																																
"H"	"L"	Disabled	Enabled	Input	Output	Output																																
"L"	"H"	Disabled	Disabled	Input	Input	Input																																
"L"	"L"	Disabled	Disabled	Input	Input	Input																																
CL	I/O	<div>This is the display clock input terminal The following is true depending on the M/S and CLS status.</div> <table><tr><th>M/S</th><th>CLS</th><th>CL</th></tr><tr><td>"H"</td><td>"H"</td><td>Output</td></tr><tr><td>"H"</td><td>"L"</td><td>Input</td></tr><tr><td>"L"</td><td>"H"</td><td>Input</td></tr><tr><td>"L"</td><td>"L"</td><td>Input</td></tr></table>	M/S	CLS	CL	"H"	"H"	Output	"H"	"L"	Input	"L"	"H"	Input	"L"	"L"	Input	1																				
M/S	CLS	CL																																				
"H"	"H"	Output																																				
"H"	"L"	Input																																				
"L"	"H"	Input																																				
"L"	"L"	Input																																				
FR	O	This is the liquid crystal alternating current signal terminal.	1																																			
/DOF	O	This is the LCD blanking control terminal.	1																																			
FRS	O	Reserved	1																																			
IRS	I	This terminal selects the resistors for the V0 voltage level adjustment. IRS = "H": Use the internal resistors IRS = "L": Do not use the internal resistors. The V0 voltage level is regulated by an external resistive voltage divider attached to the VR terminal	1																																			
/HPM	I	This is the power control terminal for the power supply circuit for liquid crystal drive. /HPM = "H": Normal mode /HPM = "L": High power mode	1																																			
SEL3 SEL2 SEL1	I	<div>These pins are DUTY selection.</div> <table><tr><th>SEL 3 , 2 , 1</th><th>DUTY</th><th>BIAS</th></tr><tr><td>0 , 0 , 0</td><td>1/65</td><td>1/9 or 1/7</td></tr><tr><td>0 , 0 , 1</td><td>1/49</td><td>1/8 or 1/6</td></tr><tr><td>0 , 1 , 0</td><td>1/33</td><td>1/6 or 1/5</td></tr><tr><td>0 , 1 , 1</td><td>1/55</td><td>1/8 or 1/6</td></tr><tr><td>1 , 0 , 0</td><td>1/53</td><td>1/8 or 1/6</td></tr><tr><td>1, X , X</td><td>-----</td><td>-----</td></tr></table>	SEL 3 , 2 , 1	DUTY	BIAS	0 , 0 , 0	1/65	1/9 or 1/7	0 , 0 , 1	1/49	1/8 or 1/6	0 , 1 , 0	1/33	1/6 or 1/5	0 , 1 , 1	1/55	1/8 or 1/6	1 , 0 , 0	1/53	1/8 or 1/6	1, X , X	-----	-----	3														
SEL 3 , 2 , 1	DUTY	BIAS																																				
0 , 0 , 0	1/65	1/9 or 1/7																																				
0 , 0 , 1	1/49	1/8 or 1/6																																				
0 , 1 , 0	1/33	1/6 or 1/5																																				
0 , 1 , 1	1/55	1/8 or 1/6																																				
1 , 0 , 0	1/53	1/8 or 1/6																																				
1, X , X	-----	-----																																				
TEST0 ~ 5	I	These are terminals for IC testing. They are set to open.	6																																			

## LCD Driver Pins

Pin Name	I/O	Function	No. of Pins																										
SEG0 to SEG131	O	These are the LCD segment drive outputs. Through a combination of the contents of the display RAM and with the FR signal, a single level is selected from Vss, V3, V2 and V0.	132																										
		<table><tr><th rowspan="2">RAM DATA</th><th rowspan="2">FR</th><th colspan="2">Output Voltage</th></tr><tr><th>Normal Display</th><th>Reverse Display</th></tr><tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr><tr><td>H</td><td>L</td><td>Vss</td><td>V3</td></tr><tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr><tr><td>L</td><td>L</td><td>V3</td><td>Vss</td></tr><tr><td>Power save</td><td></td><td colspan="2">Vss</td></tr></table>		RAM DATA	FR	Output Voltage		Normal Display	Reverse Display	H	H	V0	V2	H	L	Vss	V3	L	H	V2	V0	L	L	V3	Vss	Power save		Vss	
		RAM DATA				FR	Output Voltage																						
				Normal Display	Reverse Display																								
		H		H	V0	V2																							
		H		L	Vss	V3																							
		L		H	V2	V0																							
		L		L	V3	Vss																							
Power save		Vss																											
COM0 to COMn	O	Through a combination of the contents of the scan data and with the FR signal, a single level is selected from Vss, V4, V1 and V0.	67																										
		<table><tr><th>Scan Data</th><th>FR</th><th>Output Voltage</th></tr><tr><td>H</td><td>H</td><td>Vss</td></tr><tr><td>H</td><td>L</td><td>V0</td></tr><tr><td>L</td><td>H</td><td>V1</td></tr><tr><td>L</td><td>L</td><td>V4</td></tr><tr><td>Power save</td><td></td><td>Vss</td></tr></table>		Scan Data	FR	Output Voltage	H	H	Vss	H	L	V0	L	H	V1	L	L	V4	Power save		Vss								
		Scan Data		FR	Output Voltage																								
		H		H	Vss																								
		H		L	V0																								
		L		H	V1																								
		L		L	V4																								
Power save		Vss																											
COMS	O	These are the COM output terminals for the indicator. Both terminals output the same signal. Leave these open if they are not used.	2																										

## ST7565P I/O PIN ITO Resister Limitation

PIN Name	ITO Resister
TEST0...5	Floating
V <sub>DD</sub> , V <sub>DD2</sub> , V <sub>SS</sub> , V <sub>OUT</sub> , VR, VRS	<100Ω
V0, V1, V2, V3, V4, CAP1P, CAP1N, CAP2P, CAP2N, CAP3P, CAP4P, CAP5P	<500Ω
/CS1, CS2, CL, E, R/W, A0, D0...D7,	<1KΩ
FR, /DOF, C86, P/S, M/S, /HPM, SEL1...SEL3, CLS, IRS	<5KΩ
/RES	<10KΩ

## DESCRIPTION OF FUNCTIONS

### The MPU Interface

#### Selecting the Interface Type

With the ST7565P chips, data transfers are done through an 8-bit parallel data bus (D7 to D0) or through a serial data input (SI). By setting the P/S terminal to “H” or “L”, it sets the

access mode to be either parallel or serial mode as shown in Table 1.

**Table 1**

P/S	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D5~D0
H: Parallel mode	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D5~D0
L: Serial mode	/CS1	CS2	A0	—	—	—	SI	SCL	(HZ)

“—” indicates fixed to either “H” or to “L”

### The Parallel Interface

When the parallel interface has been selected (P/S = “H”), the interface can be connected directly to either 8080 or

6800 Series MPU (as shown in Table 2) by setting the C86 terminal to either “H” or “L”.

**Table 2**

C86 (P/S=H)	/CS1	CS2	A0	E(/RD)	R/W(/WR)	D7~D0
H: 6800 Series	/CS1	CS2	A0	E	R/W	D7~D0
L: 8080 Series	/CS1	CS2	A0	/RD	/WR	D7~D0

Moreover, data bus signals are recognized according to the combination of A0, /RD (E), /WR (R/W) signals.

The functions are shown as below in Table 3.

**Table 3**

Shared	6800 Series	8080 Series		Function
A0	R/W	/RD	/WR	
1	1	0	1	Reads the display data
1	0	1	0	Writes the display data
0	1	0	1	Status read
0	0	1	0	Write control data (command)

## The Serial Interface

When the serial interface has been selected (P/S = "L") then when the chip is in active state (/CS1 = "L" and CS2 = "H") the serial data input (SI) and the serial clock input (SCL) can be received. The serial data is read from the serial data input pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits parallel data in the rising edge of the eighth serial clock for the processing.

The A0 input is used to determine whether or the serial data input is display data or command data; when A0 = "H", the data is display data, and when A0 = "L" then the data is command data. The A0 input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active. Figure 1 is a serial interface signal chart.

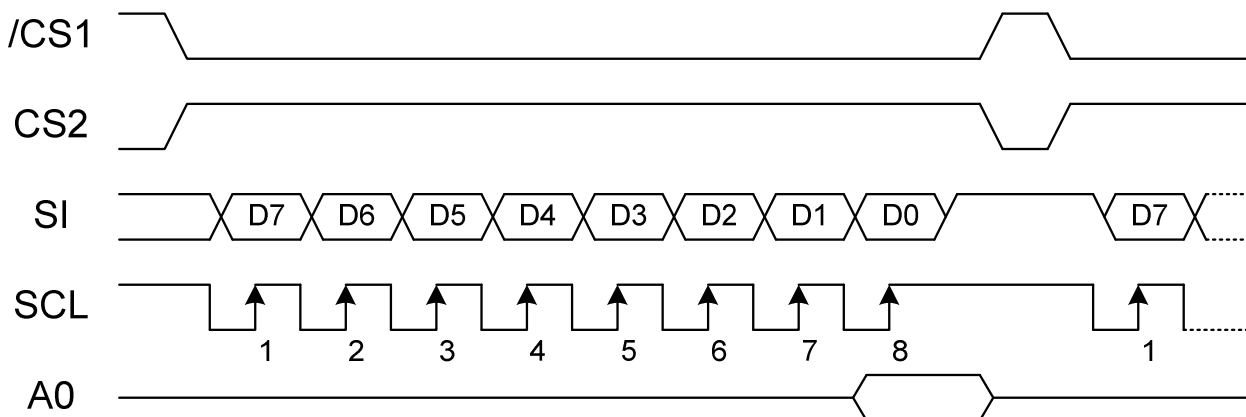


Figure 1

- \* When the chip is not active, the shift registers and the counter are reset to their initial states.
- \* Reading is not possible while in serial interface mode.
- \* Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend that operation be rechecked on the actual equipment.

## The Chip Select

The ST7565P have two chip select terminals: /CS1 and CS2. The MPU interface or the serial interface is enabled only when /CS1 = "L" and CS2 = "H".

When the chip select is inactive, D0 to D7 enter a high impedance state, and the A0, /RD, and /WR inputs are inactive. When the serial interface is selected, the shift register and the counter are reset.

## The Accessing the Display Data RAM and the Internal Registers

Data transfer at a higher speed is ensured since the MPU is required to satisfy the cycle time (tCYC) requirement alone in accessing the ST7565P. Wait time may not be considered. And, in the ST7565P, each time data is sent from the MPU, a type of pipeline process between LSIs is performed through the bus holder attached to the internal data bus. Internal data bus.

For example, when the MPU writes data to the display data RAM, once the data is stored in the bus holder, then it is written to the display data RAM before the next data write cycle. Moreover, when the MPU reads the display data RAM,

the first data read cycle (dummy) stores the read data in the bus holder, and then the data is read from the bus holder to the system bus at the next data read cycle.

There is a certain restriction in the read sequence of the display data RAM. Please be advised that data of the specified address is not generated by the read instruction issued immediately after the address setup. This data is generated in data read of the second time. Thus, a dummy read is required whenever the address setup or write cycle operation is conducted.

This relationship is shown in Figure 2.

The Busy Flag

When the busy flag is “1” it indicates that the ST7565P is running internal processes, and at this time no command aside from a status read will be received. The busy flag is outputted to D7 pin with the read instruction. If the cycle time

(tCYC) is maintained, it is not necessary to check for this flag before each command. This makes vast improvements in MPU processing capabilities possible.

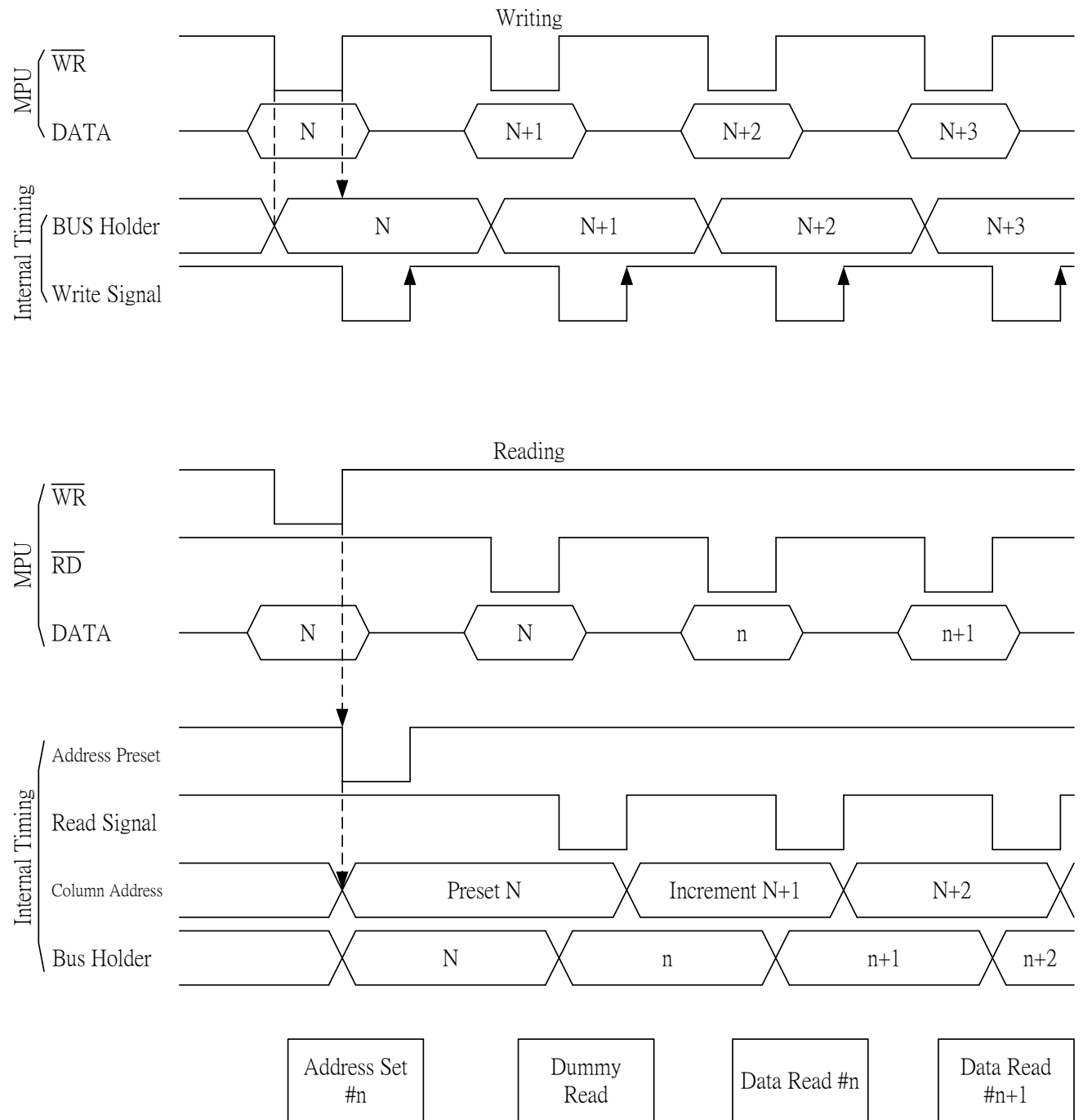


Figure 2

## Display Data RAM

The display data RAM stores the dot data for the LCD. It has a 65 (8 page x 8 bit +1) x 132 bit structure. As is shown in Figure 3, the D7 to D0 display data from the MPU corresponds to the LCD display common direction; there are few constraints at the time of display data transfer when multiple ST7565P are used, thus and display structures can be created easily and with a high degree of freedom.

D0	0	1	1	1		0
D1	1	0	0	0		0
D2	0	0	0	0		0
D3	0	1	1	1		0
D4	1	0	0	0		0
-						

Display data RAM

Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, it will not cause adverse effects on the display (such as flickering).

COM0						
COM1						
COM2						
COM3						
COM4						
-						

Liquid crystal display

Figure 3

## The Page Address Circuit

Page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access.

Page address 8 (D3, D2, D1, D0 = 1, 0, 0, 0) is a special RAM for icons, and only display data D0 is used (refer to Figure 4)

## The Column Addresses

The display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously. Moreover, the incrementing of column addresses stops with 83H. Because the column address is independent of the page address, when moving, for example, from page 0 column 83H to page 1 column 00H,

it is necessary to respective both the page address and the column address.

Furthermore, as is shown in Table 4, the ADC command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the LCD module is assembled can be minimized. As is shown in Figure 4.

Table 4

SEG Output ADC	SEG0	SEG 131
(D0) "0"	0 (H) → Column Address →	83 (H)
(D0) "1"	83 (H) ← Column Address ←	0 (H)

## The Line Address Circuit

The line address circuit, as shown in Table 4, specifies the line address relating to the COM output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified (this is the COM0 output when the common output mode is normal, and the COM63 output

for ST7565P, the detail is shown page.11 The display area is a 65 line area for the ST7565P. If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, etc. can be performed.

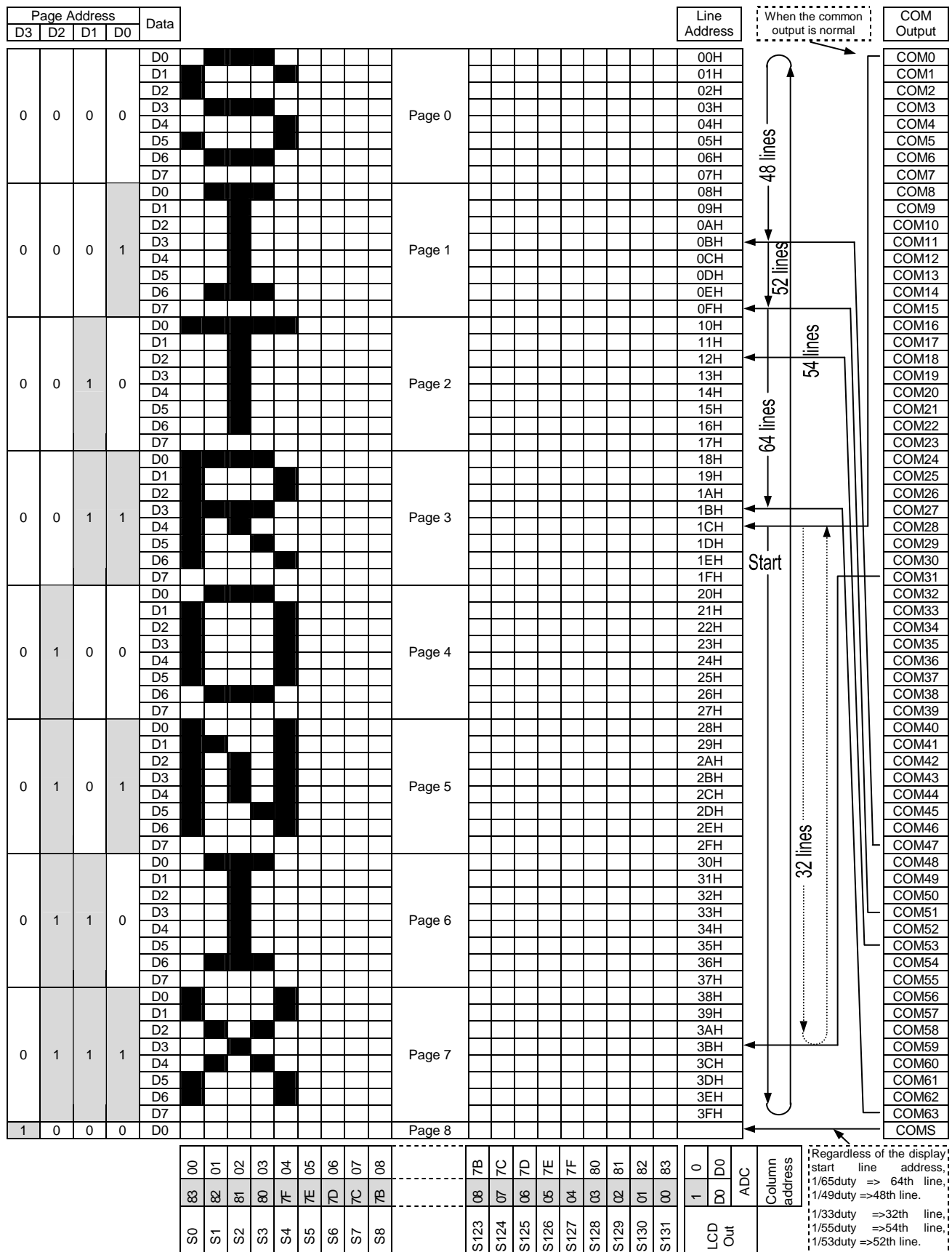


Figure 4



The Display Data Latch Circuit

The display data latch circuit is a latch that temporarily stores the display data that is output to the liquid crystal driver circuit from the display data RAM.

Because the display normal/reverse status, display ON/OFF status, and display all points ON/OFF commands control only the data within the latch, they do not change the data within the display data RAM itself.

The Oscillator Circuit

This is a CR-type oscillator that produces the display clock. The oscillator is only enabled when M/S= "H" and CLS = "H".

When CLS = "L" the oscillation stops, and the external clock is input through the CL terminal.

Display Timing Generator Circuit

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit using the display clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal. Reading to the display data liquid crystal driver circuits is completely independent of accesses to the display data RAM by the MPU. Consequently, even if the display data

RAM is accessed asynchronously during liquid crystal display, there is absolutely no adverse effect (such as flickering) on the display. Moreover, the display timing generator circuit generates the common timing and the liquid crystal alternating current signal (FR) from the display clock. It generates a drive wave form using a 2 frame alternating current drive method, as is shown in Figure 5, for the liquid crystal drive circuit.

Two-frame alternating current drive waveform

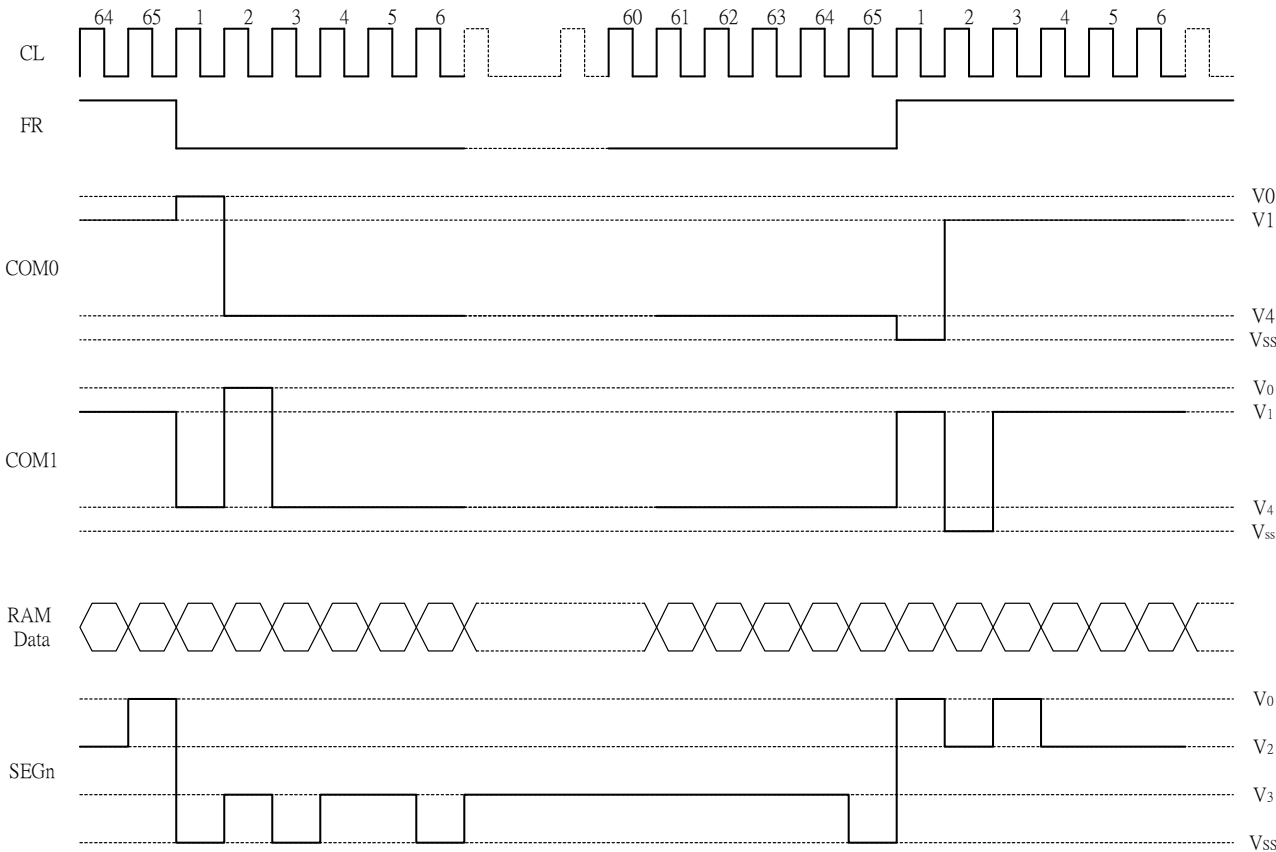


Figure 5

## The Common Output Status Select Circuit

In the ST7565P chips, the COM output scan direction can be selected by the common output status select command.

(See Table 6.) Consequently, the constraints in IC layout at the time of LCD module assembly can be minimized.

Table 6

Status	COM Scan Direction				
	1/65 DUTY	1/49 DUTY	1/33 DUTY	1/55 DUTY	1/53 DUTY
Normal	COM0 → COM63	COM0 → COM47	COM0 → COM31	COM0 → COM53	COM0 → COM51
Reverse	COM63 → COM0	COM47 → COM0	COM31 → COM0	COM53 → COM0	COM51 → COM0

Duty	COM dir	Common output pins							
		COM[0:15]	COM[16:23]	COM[24:26]	COM[27:36]	COM[37:39]	COM[40:47]	COM[48:63]	COMS
1/65	0	COM[0:63]							
	1	COM[63:0]							
1/49	0	COM[0:23]	reserve				COM[24:47]		COMS
	1	COM[47:24]	reserve				COM[23:0]		COMS
1/33	0	COM[0:15]	reserve					COM[16:31]	COMS
	1	COM[31:16]	reserve					COM[15:0]	COMS
1/55	0	COM[0:26]			reserve	COM[27:53]			COMS
	1	COM[53:27]			reserve	COM[26:0]			COMS
1/53	0	COM[0:25]			reserve	COM[26:51]			COMS
	1	COM[51:26]			reserve	COM[25:0]			COMS

## The LCD Driver Circuits

The LCD driver circuits generates four voltage levels to drive the LCD. The combination of the display data, the COM scan signal and the FR signal produces the drive voltage of LCD.

Figure 6 shows examples of the SEG and COM output wave form.

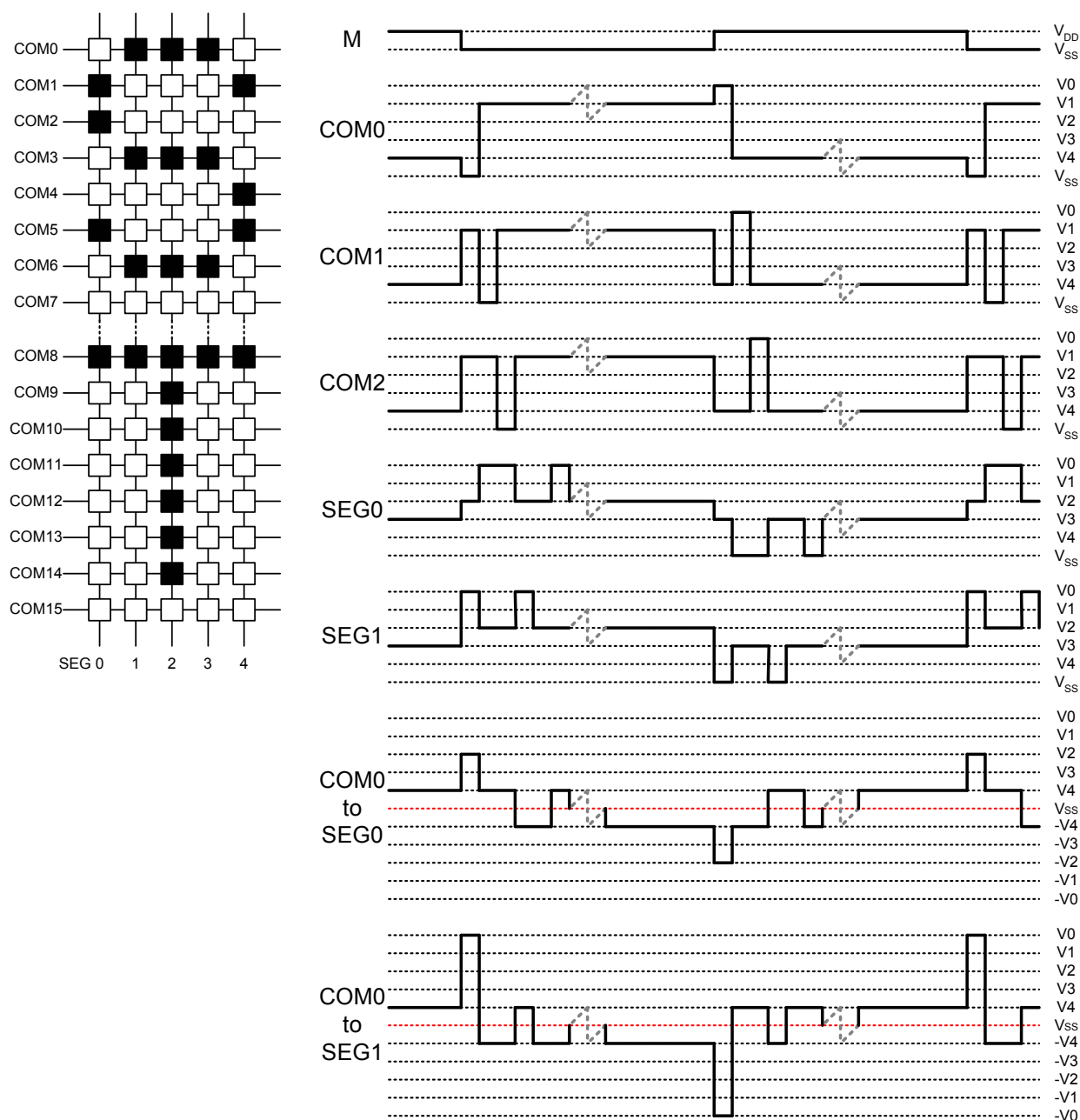


Figure 6

## The Power Supply Circuits

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for the LCD drivers. They are Booster circuits, voltage regulator circuits, and voltage follower circuits. They are only enabled in master operation. The power supply circuits can turn the Booster circuits, the voltage regulator circuits, and the

voltage follower circuits ON or OFF independently through the use of the Power Control Set command. Consequently, it is possible to make an external power supply and the internal power supply function somewhat in parallel. Table 7 shows the Power Control Set Command 3-bit data control function, and Table 8 shows reference combinations.

**Table 7**

bit	function	Status	
		"1"	"0"
D2	Booster circuit control bit	ON	OFF
D1	Voltage regulator circuit control bit (V/R circuit)	ON	OFF
D0	Voltage follower circuit control bit (V/F circuit)	ON	OFF

The Control Details of Each Bit of the Power Control Set Command

**Table 8**

Use Settings	D2	D1	D0	Voltage booster	Voltage regulator	Voltage follower	External voltage input	Step-up voltage
Only the internal power supply is used	1	1	1	ON	ON	ON	VDD2	Used
Only the voltage regulator circuit and the voltage follower circuit are used	0	1	1	OFF	ON	ON	VOUT, VDD2	Open
Only the V/F circuit is used	0	0	1	OFF	OFF	ON	V0, VDD2	Open
Only the external power supply is used	0	0	0	OFF	OFF	OFF	V0 to V4	Open

Reference Combinations

\* The "step-up system terminals" refer CAP1N, CAP1P, CAP2N, CAP2P, and CAP3N.

\* While other combinations, not shown above, are also possible, these combinations are not recommended because they have no practical use.

## The Step-up Voltage Circuits

Using the step-up voltage circuits equipped within the ST7565P chips it is possible to product a 2X,3X,4X,5X or 6X step-up of the VSS – VDD2 voltage levels.

The step-up voltage relationships are shown in Figure 7.

6X step-up: Connect capacitor C1 between CAP1N and CAP1P, between CAP2N and CAP2P, between CAP1N and CAP3P, between CAP2N and CAP4P, between CAP1N and CAP5P, and between VDD2 and VOUT, to produce a voltage level in the positive direction at the VOUT terminal that is 6 times the voltage level between VSS and VDD2.

5X step-up: Connect capacitor C1 between CAP1N and CAP1P, between CAP2N and CAP2P, between CAP1N and CAP3P, between CAP2N and CAP4P, and between VDD2 and VOUT, to produce a voltage level in the positive direction at the VOUT terminal that is 5 times the voltage level between VSS and VDD2.

4X step-up: Connect capacitor C1 between CAP1N and CAP1P, between CAP2N and CAP2P, between CAP1N and CAP3P, and between VDD2 and VOUT, to produce a voltage level in the positive direction at the VOUT terminal that is 4 times the voltage level between VSS and VDD2.

3X step-up: Connect capacitor C1 between CAP1N and CAP1P, between CAP2N and CAP2P and between VDD2 and VOUT, and short between CAP3P and VOUT to produce voltage level in the positive direction at the VOUT terminal that is 3 times the voltage difference between VSS and VDD2.

2X step-up: Connect capacitor C1 between CAP1N and CAP1P, and between VDD2 and VOUT, leave CAP2N open, and short between CAP2P, CAP3P and VOUT to produce a voltage in the positive direction at the VOUT terminal that is twice the voltage between VSS and VDD2.

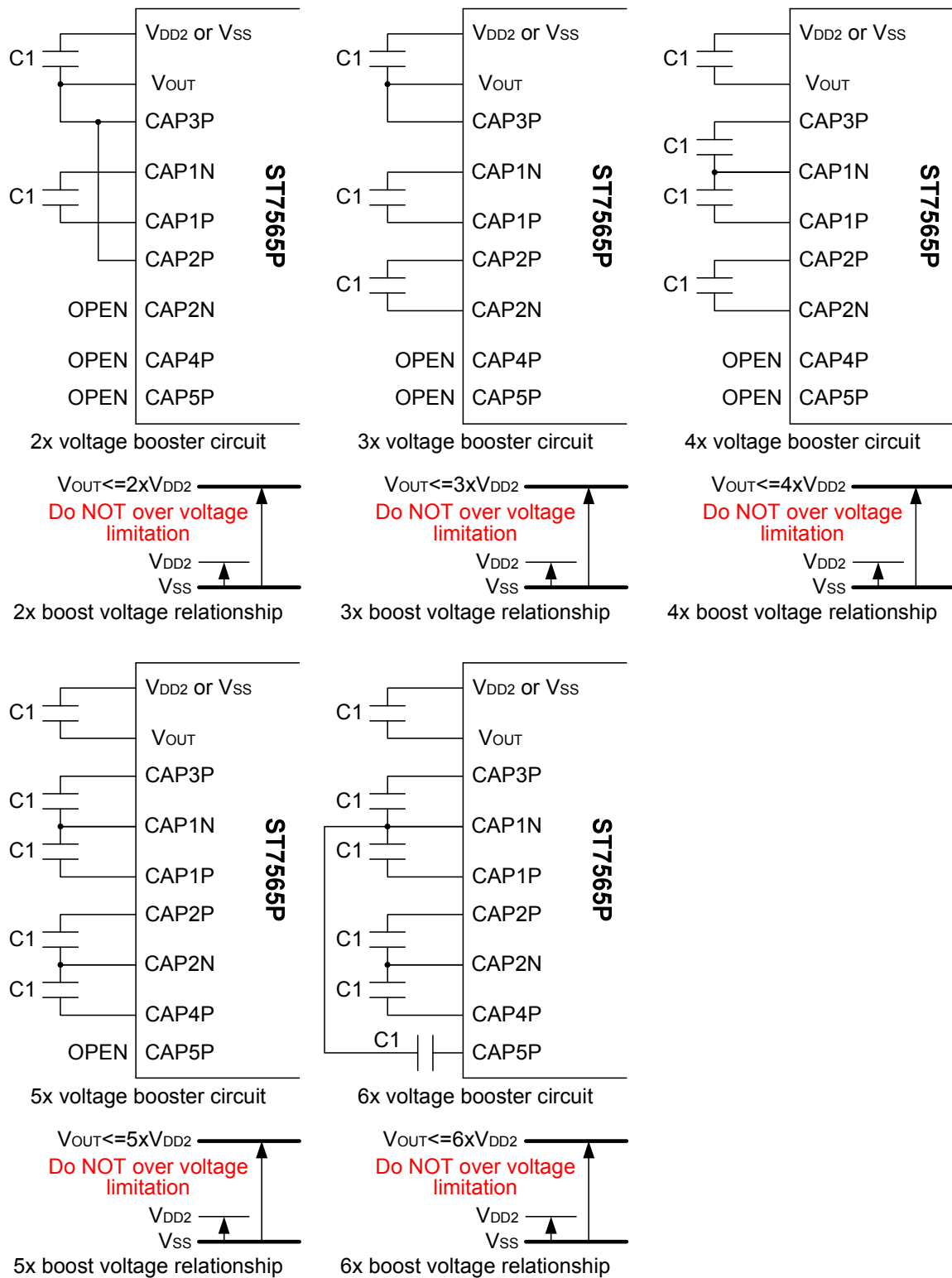


Figure 7

- \* The VDD2 voltage range must be set so that the VOUT terminal voltage does not exceed the absolute maximum rated value.
- \* The maximum voltage of the booster capacitor terminals are :  
VMAX: CAP5P > CAP4P > CAP3P > CAP2P > CAP1P > CAP2N = CAP1N.

## The Voltage Regulator Circuit

The step-up voltage generated at VOUT outputs the LCD driver voltage V0 through the voltage regulator circuit. Because the ST7565P chips have an internal high-accuracy fixed voltage power supply with a 64-level electronic volume

function and internal resistors for the V0 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components. (VREG thermal gradients approximate -0.05%/°C)

### (A) When the V0 Voltage Regulator Internal Resistors Are Used

Through the use of the V0 voltage regulator internal resistors and the electronic volume function the liquid crystal power supply voltage V0 can be controlled by commands alone (without adding any external resistors), making it possible to

adjust the liquid crystal display brightness. The V0 voltage can be calculated using equation A-1 over the range where  $|V_0| < |V_{OUT}|$ .

$$V_0 = \left(1 + \frac{R_b}{R_a}\right) \cdot V_{EV}$$

$$= \left(1 + \frac{R_b}{R_a}\right) \cdot \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG}$$

$$\left[ \because V_{EV} = \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG} \right]$$

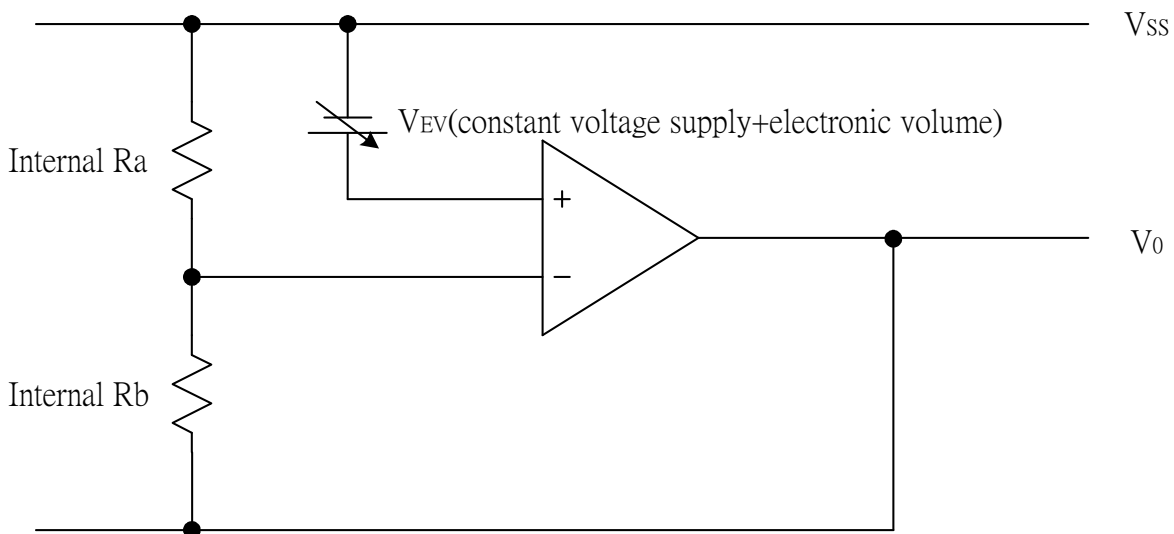


Figure 8

VREG is the IC-internal fixed voltage supply, and its voltage at  $T_a = 25^\circ\text{C}$  is as shown in Table 9.

**Table 9**

Part no.	Equipment Type	Thermal Gradient	VREG
ST7565P	Internal Power Supply	-0.05 %/°C	2.1V

$\alpha$  is set to 1 level of 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronic volume registers. Table 10 shows the value for  $\alpha$  depending on the electronic volume register settings.

Rb/Ra is the V0 voltage regulator internal resistor ratio, and can be set to 8 different levels through the V0 voltage regulator internal resistor ratio set command. The  $(1 + R_b/R_a)$  ratio assumes the values shown in Table 11 depending on the 3-bit data settings in the V0 voltage regulator internal resistor ratio register.

**Table 10**

D5	D4	D3	D2	D1	D0	$\alpha$
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
			$\vdots$			$\vdots$
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

V0 voltage regulator internal resistance ratio register value and  $(1 + R_b/R_a)$  ratio (Reference value)

**Table 11**

Register			ST7565P
D2	D1	D0	(1) -0.05 %/°C
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0
1	0	1	5.5
1	1	0	6.0
1	1	1	6.5

Figures 9, 10 show V0 voltage measured by values of the internal resistance ratio resistor for V0 voltage adjustment and electric volume resistor for each temperature grade model.

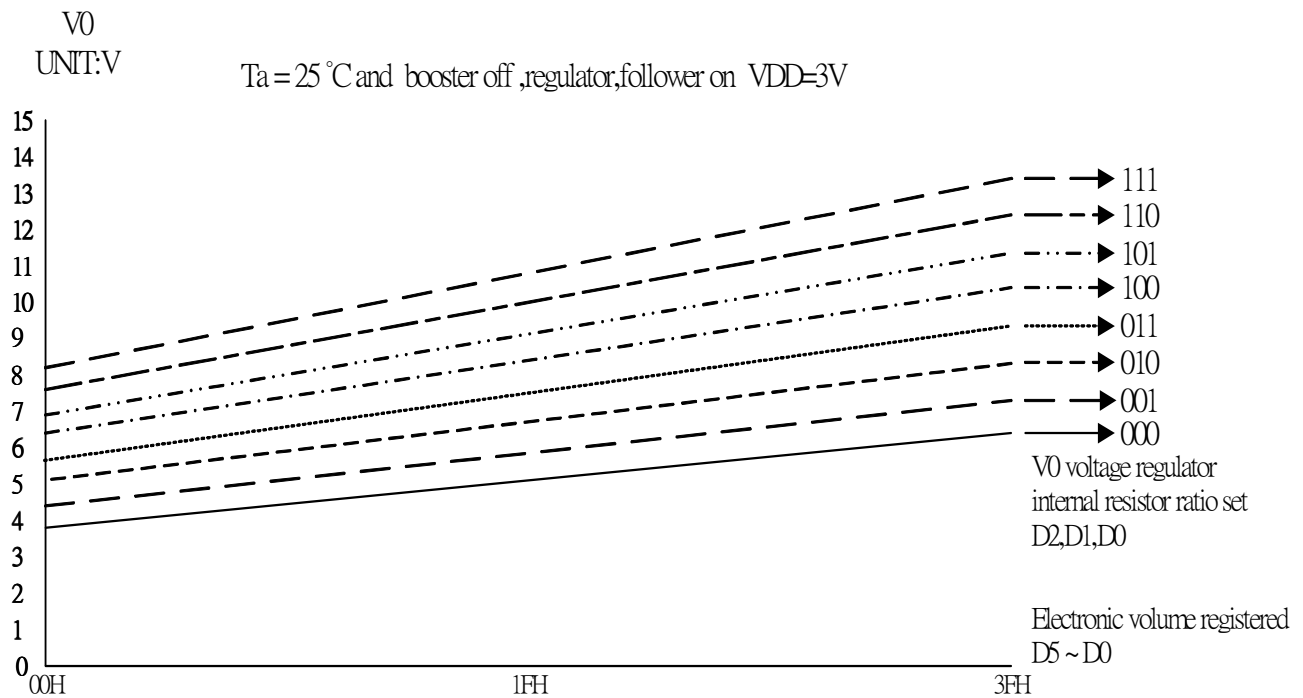


Figure 9 : (1) For ST7565P the Thermal Gradient = -0.05%/°C

The V0 voltage as a function of the V0 voltage regulator internal resistor ratio register and the electronic volume register.

Setup example: When selecting Ta = 25°C and V0 = 7V f or an ST7565P on which Temperature gradient = -0.05%/°C. Using Figure 9 and the equation A-1, the following setup is enabled.

At this time, the variable range and the notch width of the V0 voltage is, as shown Table 13, as dependent on the electronic volume.

Table 12

Contents	Register					
	D5	D4	D3	D2	D1	D0
For V0 voltage regulator	—	—	—	0	1	0
Electronic Volume	1	0	0	1	0	1

Table 13

V0	Min	Typ	Max	Units
Variable Range	5.1 (63 levels)	7.0 (central value)	8.4 (0 level)	[V]
Notch width		51		[mV]



## (B) When an External Resistance is Used (The V0 Voltage Regulator Internal Resistors Are Not Used) (1)

The liquid crystal power supply voltage V0 can also be set without using the V0 voltage regulator internal resistors (IRS terminal = "L") by adding resistors Ra' and Rb' between VDD and VR, and between VR and V0, respectively. When this is done, the use of the electronic volume function makes it possible to adjust the brightness of the liquid crystal display

by controlling the liquid crystal power supply voltage V0 through commands.

In the range where  $|V_0| < |V_{OUT}|$ , the V0 voltage can be calculated using equation B-1 based on the external resistances Ra' and Rb'.

$$V_0 = \left(1 + \frac{Rb'}{Ra'}\right) \cdot V_{EV}$$

$$= \left(1 + \frac{Rb'}{Ra'}\right) \cdot \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG}$$

$$\left[\because V_{EV} = \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG}\right]$$

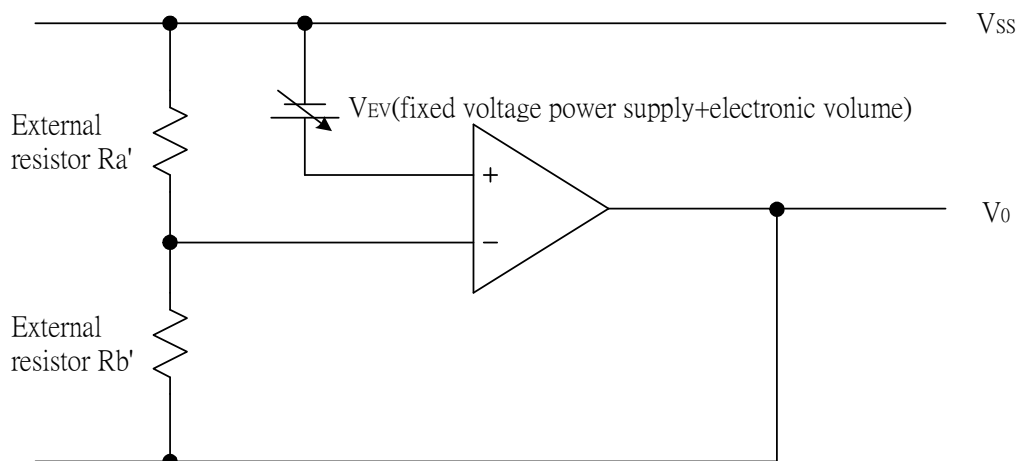


Figure 11

Setup example: When selecting Ta = 25°C and V0 = 7 V for ST7565P the temperature gradient = -0.05%/°C. When the central value of the electron volume register is (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0), then  $\alpha = 31$  and VREG = 2.1V so, according to equation B-1,

$$V_0 = \left(1 + \frac{Rb'}{Ra'}\right) \cdot \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG}$$

$$7V = \left(1 + \frac{Rb'}{Ra'}\right) \cdot \left(1 - \frac{31}{162}\right) \cdot (2.1)$$

Moreover, when the value of the current running through Ra' and Rb' is set to 5 uA, Ra' + Rb' = 1.4MΩ.....(Equation B-3)

Consequently, by equations B-2 and B-3,

$$\frac{Rb'}{Ra'} = 3.12$$

$$Ra' = 340k\Omega$$

$$Rb' = 1060k\Omega$$

At this time, the V0 voltage variable range and notch width, based on the electron volume function, is as given in Table 14.

Table 14

V0	Min	Typ	Max	Units
Variable Range	5.3 (63 levels)	7.0 (central value)	8.6 (0 level)	[V]
Notch width		52		[mV]

(C) When External Resistors are Used (The V0 Voltage Regulator Internal Resistors Are Not Used) (2)

When the external resistor described above are used, adding a variable resistor as well makes it possible to perform fine adjustments on Ra' and Rb', to set the liquid crystal drive voltage V0. In this case, the use of the electronic volume function makes it possible to control the liquid crystal power supply voltage V0 by commands to adjust the liquid crystal display brightness.

In the range where  $|V_0| < |V_{OUT}|$  the V0 voltage can be calculated by equation C-1 below based on the R1 and R2 (variable resistor) and R3 settings, where R2 can be subjected to fine adjustments ( $\Delta R2$ ).

$$\begin{aligned} V_0 &= \left(1 + \frac{R3+R2-\Delta R2}{R1+\Delta R2}\right) \cdot V_{EV} \\ &= \left(1 + \frac{R3+R2-\Delta R2}{R1+\Delta R2}\right) \cdot \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG} \\ \left[ \because V_{EV} &= \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG} \right] \end{aligned}$$

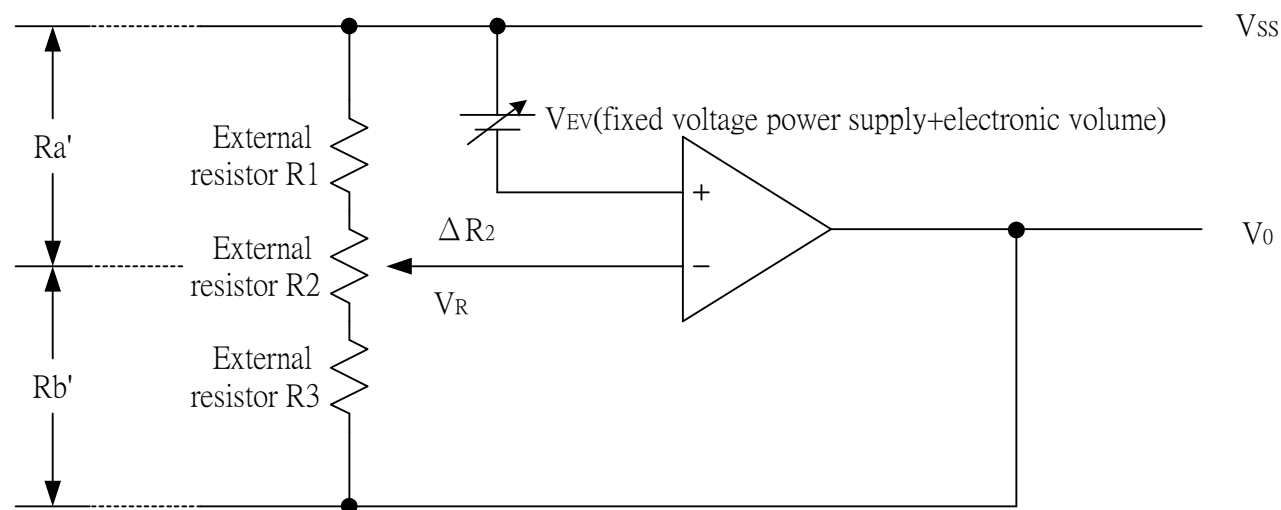


Figure 12

Setup example: When selecting Ta = 25°C and V0= 5 to 9 V (using R2) for an ST7565P the temperature gradient = -0.05%/°C. When the central value for the electronic volume register is set at (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0), then  $\alpha = 31$  and VREG = 2.1 V so, according to equation C-1, when  $\Delta R2 = 0 \Omega$ , in order to make V0 = 9 V,

$$9V = \left(1 + \frac{R3+R2}{R1}\right) \cdot \left(1 - \frac{31}{162}\right) \cdot (2.1)$$

When  $\Delta R2 = R2$ , in order to make V = -5 V,

$$5V = \left(1 + \frac{R3}{R1+R2}\right) \cdot \left(1 - \frac{31}{162}\right) \cdot (2.1)$$

When the current flowing VDD and V0 is set to 5 uA,  $R1 + R2 + R3 = 1.4M\Omega$ .....(Equation C-4)

With this, according to equation C-2, C-3 and C-4,

$$\begin{aligned} R1 &= 264k\Omega \\ R2 &= 211k\Omega \\ R3 &= 925k\Omega \end{aligned}$$

The V0 voltage variable range and notch width based on the electron volume function is as shown in Table 15.

Table 15

V0	Min	Typ	Max	Units
Variable Range	5.5 (63 levels)	7.3 (central value)	9 (0 level)	[V]
Notch width		56		[mV]

ST7565P

\* When the V0 voltage regulator internal resistors or the electronic volume function is used, it is necessary to at least set the voltage regulator circuit and the voltage follower circuit to an operating mode using the power control set commands. Moreover, it is necessary to provide a voltage from VOUT when the Booster circuit is OFF.

\* The VR terminal is enabled only when the V0 voltage regulator internal resistors are not used (i.e. the IRS terminal = "L"). When the V0 voltage regulator internal resistors are used (i.e. when the IRS terminal = "H"), then the VR terminal is left open.

\* Because the input impedance of the VR terminal is high, it is necessary to take into consideration short leads, shield cables, etc. to handle noise.

The LCD Voltage Generator Circuit

The V0 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V1, V2, V3, and V4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V1, V2, V3 and V4 to the liquid crystal drive circuit.

High Power Mode

The power supply circuit equipped in the ST7565P chips has very low power consumption (normal mode: HPM = "H"). However, for LCD panels with large loads (size), this low-power power supply may cause display quality to degrade. When this occurs, set the HPM terminal to "L" (high power mode) can improve the display quality.

SITRONIX recommends that the display should be checked on actual equipment to determine whether or not to use this mode. Moreover, if the improvement to the display is inadequate even after high power mode has been set, then it is necessary to add a liquid crystal drive power supply externally.

The Internal Power Supply Shutdown Command Sequence

The sequence shown in Figure 13 is recommended for shutting down the internal power supply, first placing the				power supply in power saver mode and then turning the power supply OFF.						
Sequence	Details (Command, status)	Command address D7 D6 D5 D4 D3 D2 D1 D0								
Step1	Display OFF	1	0	1	0	1	1	1	0	Power saver commands (compound)
Step2	Display all points ON	1	0	1	0	0	1	0	1	
End	Internal power supply OFF									

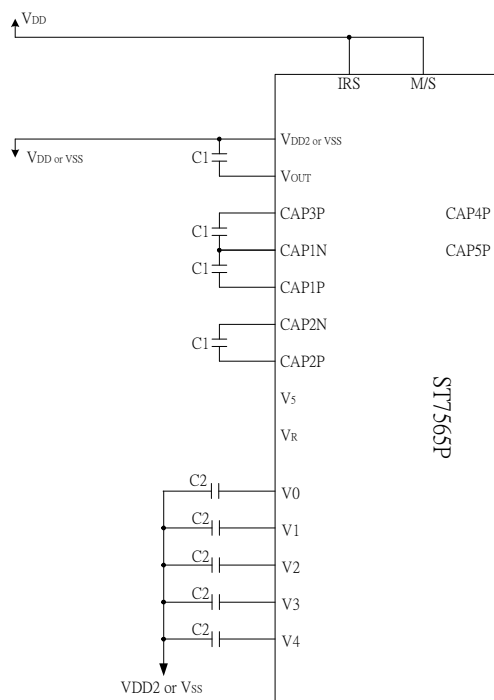
Figure 13

## Reference Circuit Examples

1. When used all of the step-up circuit, voltage regulating circuit and V/F circuit

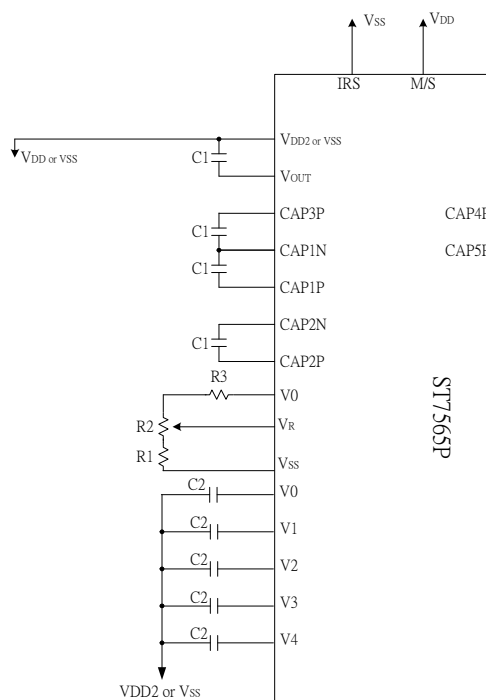
(1) When the voltage regulator internal resistor is used.

(Example where  $V_{DD2} = V_{DD}$ , with 4x step-up)



(2) When the voltage regulator internal resistor is not used.

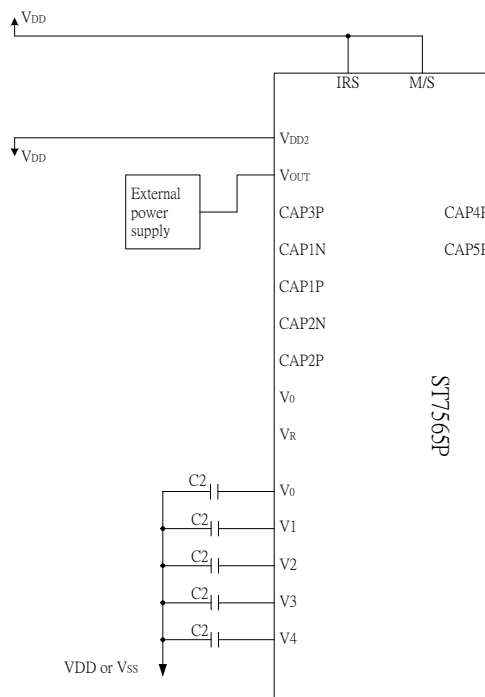
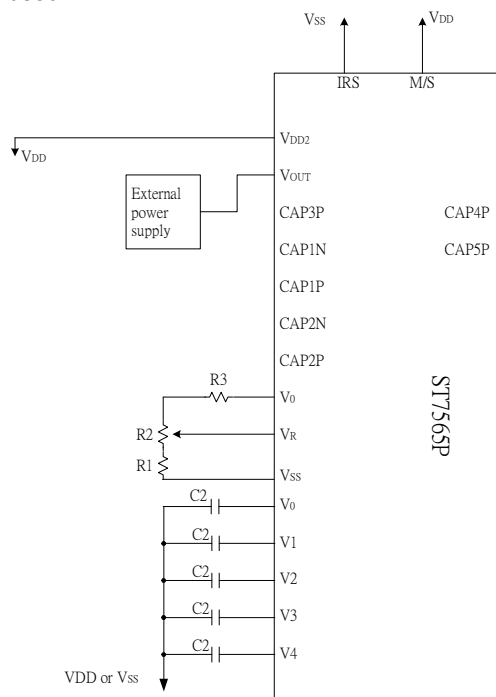
(Example where  $V_{DD2} = V_{DD}$ , with 4x step-up)



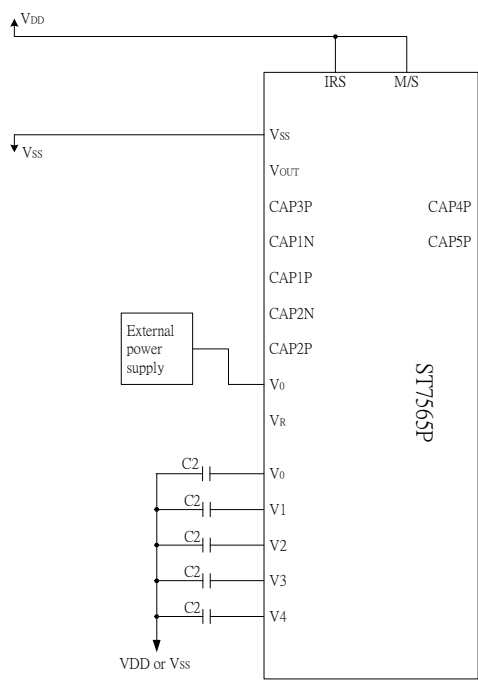
2. When the voltage regulator circuit and V/F circuit alone are used

(1) When the V0 voltage regulator internal resistor is NOT used.

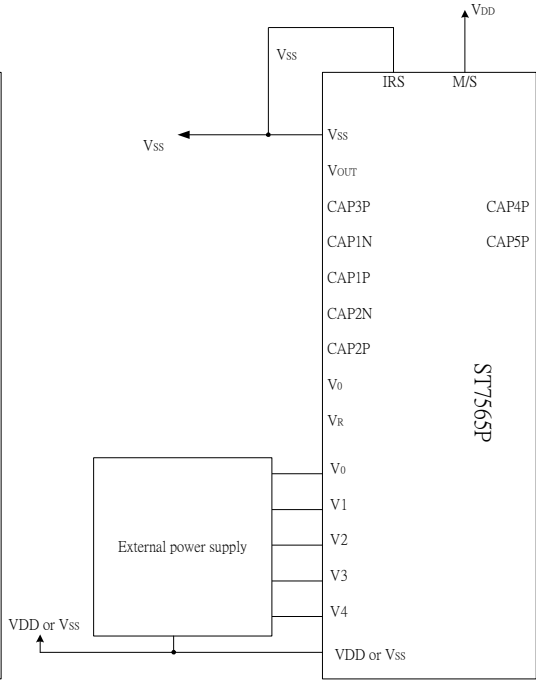
(2) When the V0 voltage regulator internal resistor is used.



(3) When the V/F circuit alone is used



(4) When the built-in power is not used



Item	Set value	units
C1	1.0 to 4.7	uF
C2	0.1 to 4.7	uF

C1 and C2 are determined by the size of the LCD being driven.

- \* 1. Because the VR terminal input impedance is high, use short leads and shielded lines.
- \* 2. C1 and C2 are determined by the size of the LCD being driven. Select a value that will stabilize the liquid crystal drive voltage.

Example of the process which determines the capacitor values:

- \* Turn the voltage regulator circuit and voltage follower circuit ON and supply a voltage to VOUT from the outside.
- \* Determine C2 by displaying an LCD pattern with a heavy load (such as horizontal stripes) and selecting a C2 that stabilizes the liquid crystal drive voltages (V0 to V4). Note that all C2 capacitors must have the same capacitance value.
- \* Next turn all the power supplies ON and determine C1.

## The Reset Circuit

When the /RES input comes to the "L" level, these LSIs return to the default state. Their default states are as follows:

1. Display OFF
2. Normal display
3. ADC select: Normal (ADC command D0 = "L")
4. Power control register: (D2, D1, D0) = (0, 0, 0)
5. Serial interface internal register data clear
6. LCD power supply bias rate:  
1/65 DUTY = 1/9 bias  
1/49, 1/55, 1/53 DUTY = 1/8 bias  
1/33 DUTY = 1/6 bias
7. All-indicator lamps-on OFF (All-indicator lamps ON/OFF command D0 = "L")
8. Power saving clear
9. V0 voltage regulator internal resistors Ra and Rb separation
10. Output conditions of SEG and COM terminals  
SEG=VSS, COM=VSS
11. Read modify write OFF
12. Display start line set to first line
13. Column address set to Address 0
14. Page address set to Page 0
15. Common output status normal
16. V0 voltage regulator internal resistor ratio set mode clear
17. Clear Electronic volume register :  
(D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0)
18. Test mode clear

On the other hand, when the reset command is used, the above default settings from 11 to 18 are only executed.

When the power is turned on, the IC internal state becomes unstable, and it is necessary to initialize it using the /RES terminal. After the initialization, each input terminal should be controlled normally.

Moreover, when the control signal from the MPU is in the high impedance, an over current may flow to the IC. After applying a current, it is necessary to take proper measures to prevent the input terminal from getting into the high impedance state.

If the internal liquid crystal power supply circuit is not used on ST7565P, it is necessary that /RES is "H" when the external liquid crystal power supply is turned on. This IC has the function to discharge V0 when /RES is "L," and the external power supply short-circuits to Vss when /RES is "L." While /RES is "L," the oscillator and the display timing generator stop, and the CL, FR and /DOF terminals are fixed to "H." The terminals D0 to D7 are not affected. The VSS level is output from the SEG and COM output terminals. This means that an internal resistor is connected between VSS and V0.

When the internal liquid crystal power supply circuit is not used on other models of ST7565P series, it is necessary that /RES is "L" when the external liquid crystal power supply is turned on.

While /RES is "L," the oscillator works but the display timing generator stops, and the CL, FR and /DOF terminals are fixed to "H." The terminals D0 to D7 are not affected.

## COMMANDS

The ST7565P identify the data bus signals by a combination of A0, /RD (E), /WR(R/W) signals. Command interpretation and execution does not depend on the external clock, but rather is performed through internal timing only, and thus the processing is fast enough that normally a busy check is not required.

In the 8080 MPU interface, commands are launched by inputting a low pulse to the RD terminal for reading, and inputting a low pulse to the /WR terminal for writing. In the 6800 Series MPU interface, the interface is placed in a read mode when an "H" signal is input to the R/W terminal and placed in a write mode when a "L" signal is input to the R/W terminal and then the command is launched by inputting a high pulse to the E terminal. Consequently, the 6800 Series MPU interface is different than the 80x86 Series MPU interface in that in the explanation of commands and the display commands the status read and display data read /RD (E) becomes "1(H)". In the explanations below the commands are explained using the 8080 Series MPU interface as the example. When the serial interface is selected, the data is input in sequence starting with D7.

<Explanation of Commands>

### Display ON/OFF

This command turns the display ON and OFF.

E R/W											Setting
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	1	1	1	1	Display ON Display OFF

When the display OFF command is executed when in the display all points ON mode, power saver mode is entered. See the section on the power saver for details.

### Display Start Line Set

This command is used to specify the display start line address of the display data RAM shown in Figure 4. For further details see the explanation of this function in "The Line Address Circuit".

E R/W											Line address
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	1	0	0	0	0	0	0	0
					0	0	0	0	0	1	1
					0	0	0	0	1	0	2
							↓				↓
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

### Page Address Set

This command specifies the page address corresponding to the low address when the MPU accesses the display data RAM (see Figure 4). Specifying the page address and column address enables to access a desired bit of the display data RAM. Changing the page address does not accompany a change in the status display.

E R/W											Page address
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							0	0	1	0	2
							↓				↓
							0	1	1	1	7
							1	0	0	0	8

## Column Address Set

This command specifies the column address of the display data RAM shown in Figure 4. The column address is split into two sections (the higher 4 bits and the lower 4 bits) when it is set (fundamentally, set continuously). Each time the display data RAM is accessed, the column address automatically increments (+1), making it possible for the MPU to continuously read from/write to the display data. The column address increment is topped at 83H. This does not change the page address continuously. See the function explanation in "The Column Address Circuit," for details.

	E R/W																			Column address
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	A7	A6	A5	A4	A3	A2	A1	A0	
High bits →	0	1	0	0	0	0	1	A7	A6	A5	A4	0	0	0	0	0	0	0	0	0
Low bits →							0	A3	A2	A1	A0	0	0	0	0	0	0	0	1	1
												0	0	0	0	0	0	1	0	2
												1	0	0	0	0	0	1	0	↓
												1	0	0	0	0	0	1	1	130
												1	0	0	0	0	0	1	1	131

## Status Read

E R/W												
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0		
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0		

BUSY	BUSY = 1: it indicates that either processing is occurring internally or a reset condition is in process. BUSY = 0: A new command can be accepted. if the cycle time can be satisfied, there is no need to check for BUSY conditions.
ADC	This shows the relationship between the column address and the segment driver. 0: Reverse (column address 131-n ↔ SEG n) 1: Normal (column address n ↔ SEG n) (The ADC command switches the polarity.)
ON/OFF	ON/OFF: indicates the display ON/OFF state. 0: Display ON 1: Display OFF (This display ON/OFF command switches the polarity.)
RESET	This indicates that the chip is in the process of initialization either because of a /RES signal or because of a reset command. 0: Operating state 1: Reset in progress

## Display Data Write

This command writes 8-bit data to the specified display data RAM address. Since the column address is automatically incremented by "1" after the write, the MPU can write the display data.

E R/W										
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							



## Display Data Read

This command reads 8-bit data from the specified display data RAM address. Since the column address is automatically incremented by "1" after the read, the CPU can continuously read multiple-word data. One dummy read is required immediately after the column address has been set. See the function explanation in "Display Data RAM" for the explanation of accessing the internal registers. When the serial interface is used, reading of the display data becomes unavailable.

E R/W										
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

## ADC Select (Segment Driver Direction Select)

This command can reverse the correspondence between the display RAM data column address and the segment driver output. Thus, sequence of the segment driver output pins may be reversed by the command. See the column address circuit for the detail. Increment of the column address (by "1") accompanying the reading or writing the display data is done according to the column address indicated in Figure 4.

E R/W											Setting
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

## Display Normal/Reverse

This command can reverse the lit and unlit display without overwriting the contents of the display data RAM. When this is done the display data RAM contents are maintained.

E R/W											Setting
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	0	1	1	0	RAM Data "H"
										1	LCD ON voltage (normal)
											RAM Data "L"
											LCD ON voltage (reverse)

## Display All Points ON/OFF

This command makes it possible to force all display points ON regardless of the content of the display data RAM. The contents of the display data RAM are maintained when this is done. This command takes priority over the display normal/reverse command.

E R/W											Setting
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	0	1	0	0	Normal display mode
										1	Display all points ON

When the display is in an OFF mode, executing the display all points ON command will place the display in power save mode. For details, see the Power Save section.

LCD Bias Set

This command selects the voltage bias ratio required for the liquid crystal display.

E		R/W									Select Status				
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	1/65duty	1/49duty	1/33duty	1/55duty	1/53duty
0	1	0	1	0	1	0	0	0	1	0	1/9 bias	1/8 bias	1/6 bias	1/8 bias	1/8 bias
											1/7 bias	1/6 bias	1/5 bias	1/6 bias	1/6 bias

Read/Modify/Write

This command is used paired with the “END” command. Once this command has been input, the display data read command does not change the column address, but only the display data write command increments (+1) the column address. This mode is maintained until the END command is input. When the END command is input, the column address returns to the address it was at when the read/modify/write command was entered. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blanking cursor.

E R/W												
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0		
0	1	0	1	1	1	0	0	0	0	0		

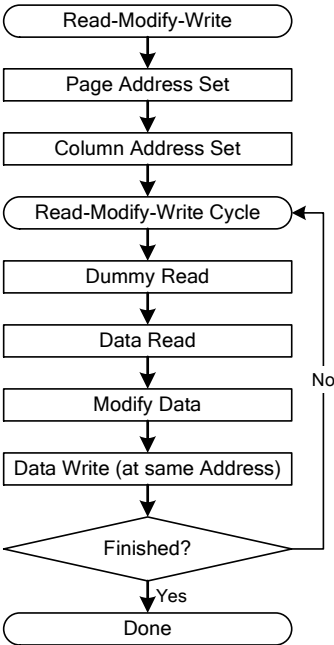


Figure 24 Command Sequence For read modify write

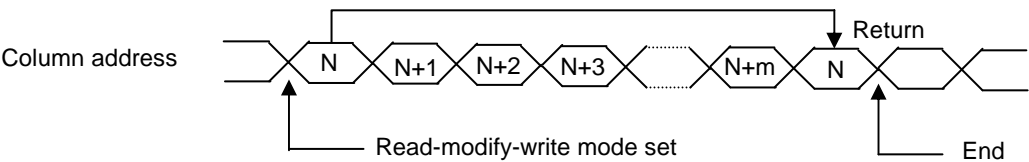


Figure 25

## End

This command releases the read/modify/write mode, and returns the column address to the address it was at when the mode was entered.

E R/W										
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

## Reset

This command initializes the display start line, the column address, the page address, the common output mode, the V0 voltage regulator internal resistor ratio, the electronic volume, and the static indicator are reset, and the read/modify/write mode and test mode are released. There is no impact on the display data RAM. See the function explanation in “Reset” for details. The reset operation is performed after the reset command is entered.

E R/W										
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The initialization when the power supply is applied must be done through applying a reset signal to the /RES terminal. The reset command must not be used instead.

## Common Output Mode Select

This command can select the scan direction of the COM output terminal. For details, see the function explanation in “Common Output Mode Select Circuit.”

E R/W											Selected Mode					
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0		1/65duty	1/49duty	1/33duty	1/55duty	1/53duty
0	1	0	1	1	0	0	0	*	*	*	Normal	COM0→COM63	COM0→COM47	COM0→COM31	COM0→COM53	COM0→COM51
							1				Reverse	COM63→COM0	COM47→COM0	COM31→COM0	COM53→COM0	COM51→COM0

\* Disabled bit

## Power Controller Set

This command sets the power supply circuit functions. See the function explanation in "The Power Supply Circuit," for details.

E R/W												
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode	
0	1	0	0	0	1	0	1	0			Booster circuit: OFF	
								1			Booster circuit: ON	
									0		Voltage regulator circuit: OFF	
									1		Voltage regulator circuit: ON	
										0	Voltage follower circuit: OFF	
										1	Voltage follower circuit: ON	

## V0 Voltage Regulator Internal Resistor Ratio Set

This command sets the V0 voltage regulator internal resistor ratio. For details, see the function explanation is "The Voltage Regulator circuit " and Table 11.

E R/W												
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Rb/Ra Ratio	
0	1	0	0	0	1	0	0	0	0	0	Small	
								0	0	1		
								0	1	0		
									↓			
								1	1	1		
								1	1	1	Large	

## The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the LCD drive voltage V0 through the output from the voltage regulator circuits of the internal liquid crystal power supply. This command is a two byte command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

## The Electronic Volume Mode Set

When this command is input, the electronic volume register set command becomes enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

E R/W										
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

## Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal drive voltage  $V_0$  assumes one of the 64 voltage levels. When this command is input, the electronic volume mode is released after the electronic volume register has been set.

E R/W											$V_0$
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	*	*	0	0	0	0	0	1	Small
			*	*	0	0	0	0	1	0	
			*	*	0	0	0	0	1	1	
			*	*	1	1	1	1	1	0	↓
			*	*	1	1	1	1	1	1	Large

\* Inactive bit (set "0")

When the electronic volume function is not used, set this to (1, 0, 0, 0, 0, 0)

## The Electronic Volume Register Set Sequence

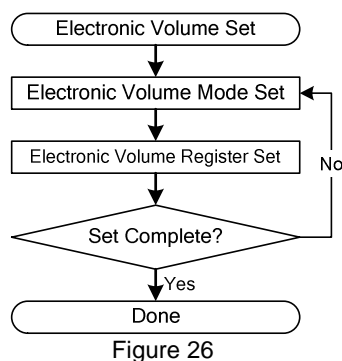


Figure 26

## Power Save (Compound Command)

When the display all points ON is performed while the display is in the OFF mode, the power saver mode is entered, thus greatly reducing power consumption.

The power saver mode has two different modes: the sleep mode and the standby mode. When the static indicator is OFF, it is the sleep mode that is entered. When the static indicator is ON, it is the standby mode that is entered. In the sleep mode and in the standby mode, the display data is saved as is the operating mode that was in effect before the power saver mode was initiated, and the MPU is still able to access the display data RAM. Refer to figure 28 for power save off sequence.

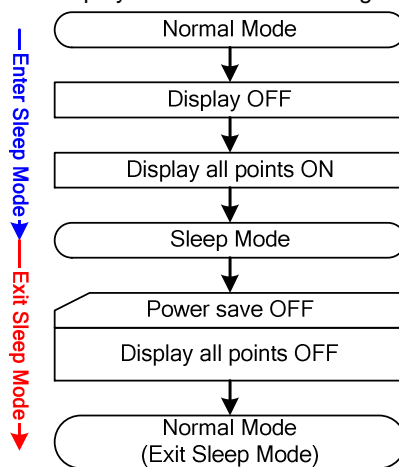


Figure 28

## Sleep Mode

This stops all operations in the LCD display system, and as long as there are no accesses from the MPU, the consumption current is reduced to a value near the static current. The internal modes during sleep mode are as follows:

1. The oscillator circuit and the LCD power supply circuit are halted.
2. All liquid crystal drive circuits are halted, and the segment in common drive outputs output a VSS level.
3. The static drive system does not operate.

## The Booster Ratio (Double Byte Command)

This command makes it possible to select step-up ratio. It is used when the power control set have turn on the internal booster circuit. This command is a two byte command used as a pair with the booster ratio select mode set command and the booster ratio register set command, and both commands must be issued one after the other.

## Booster Ratio Select Mode Set

When this command is input, the Booster ratio register set command becomes enabled. Once the booster ratio select mode has been set, no other command except for the booster ratio register command can be used. Once the booster ratio register set command has been used to set data into the register, then the booster ratio select mode is released.

E R/W										
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	1	0	0	0

## Booster Ratio Register Set

By using this command to set two bits of data to the booster ratio register, it can be select what kind of the booster ratio can be used. When this command is input, the booster ratio select mode is released after the booster ratio register has been set.

E R/W											Booster ratio select
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	*	*	*	*	*	*	0	0	2x,3x,4x
			*	*	*	*	*	*	0	1	5x
			*	*	*	*	*	*	1	1	6x

\* Inactive bit (set "0")

When the booster ratio select function is not used, set this to (0, 0) 2x,3x,4x step-up mode.

The booster ratio Register Set Sequence

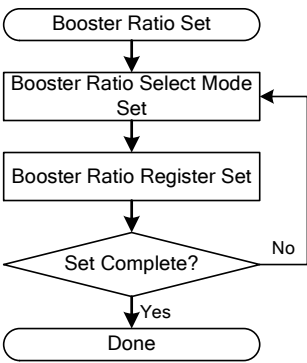


Figure 29

NOP

Non-Operation Command

E R/W										
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

Test

This is a command for IC chip testing. Please do not use it. If the test command is used by accident, it can be cleared by applying a “L” signal to the /RES input by the reset command or by using an NOP.

E R/W										
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	1	1	*	*

\* Inactive bit

Note: The ST7565P maintain their operating modes until something happens to change them. Consequently, excessive external noise, etc., can change the internal modes of the ST7565P . Thus in the packaging and system design it is necessary to suppress the noise or take measure to prevent the noise from influencing the chip. Moreover, it is recommended that the operating modes be refreshed periodically to prevent the effects of unanticipated noise.

**Table 16: Table of ST7565P Commands**

(Note) \*: disabled data

Command	Command Code										Function	
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1		D0
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address					Sets the display RAM display start line address	
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4) Column address set upper bit	0	1	0	0	0	0	1	Most significant column address Least significant column address				Sets the most significant 4 bits of the display RAM column address.
Column address set lower bit	0	1	0	0	0	0	0					Sets the least significant 4 bits of the display RAM column address.
(5) Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data							Writes to the display RAM	
(7) Display data read	1	0	1	Read data							Reads from the display RAM	
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (ST7565P)
(12) Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17) V0 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio(Rb/Ra) mode
(18) Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1	Set the V0 output voltage electronic volume register
Electronic volume register set				0	0	Electronic volume value						
(20) Booster ratio set	0	1	0	1	1	1	1	1	0	0	0 step-up value	select booster ratio 00: 2x,3x,4x 01: 5x 11: 6x
(21) Power saver												Display OFF and display all points ON compound command
(22) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(23) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command



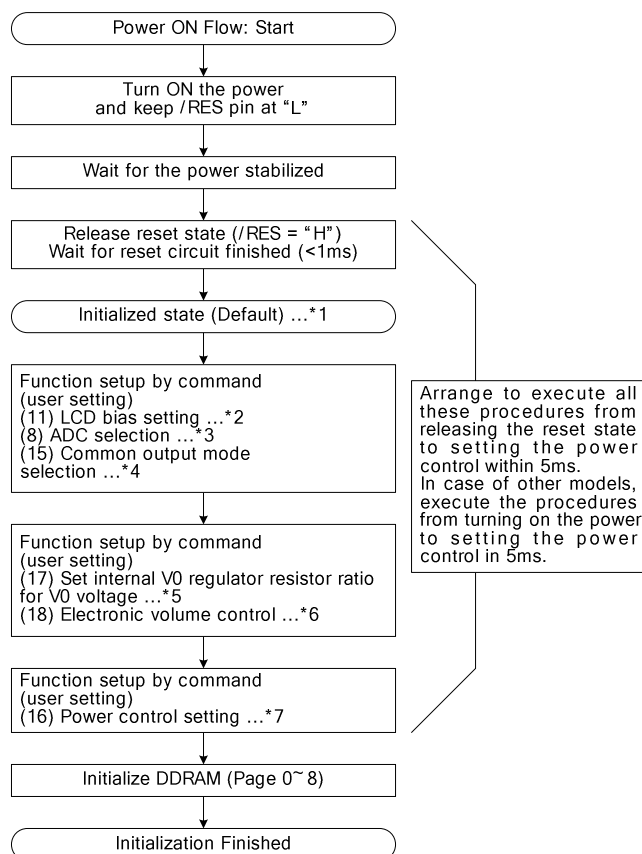
# COMMAND DESCRIPTION

## Instruction Setup: Reference

### (1) Initialization

Note: With this IC, when the power is applied, LCD driving non-selective potentials V2 and V3 (SEG pin) and V1 and V4 (COM pin) are output through the LCD driving output pins SEG and COM. When electric charge is remaining in the smoothing capacitor connecting between the LCD driving voltage output pins (V0 ~ V4) and the VSS pin, the picture on the display may become totally dark instantaneously when the power is turned on. To avoid occurrence of such a failure, we recommend the following flow when turning on the power.

#### 1. When the built-in power is being used immediately after turning on the power:



\* The target time of 5ms will result to vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

Notes: Refer to respective sections or paragraphs listed below.

\*1: Description of functions; Resetting circuit

\*2: Command description; LCD bias setting

\*3: Command description; ADC selection

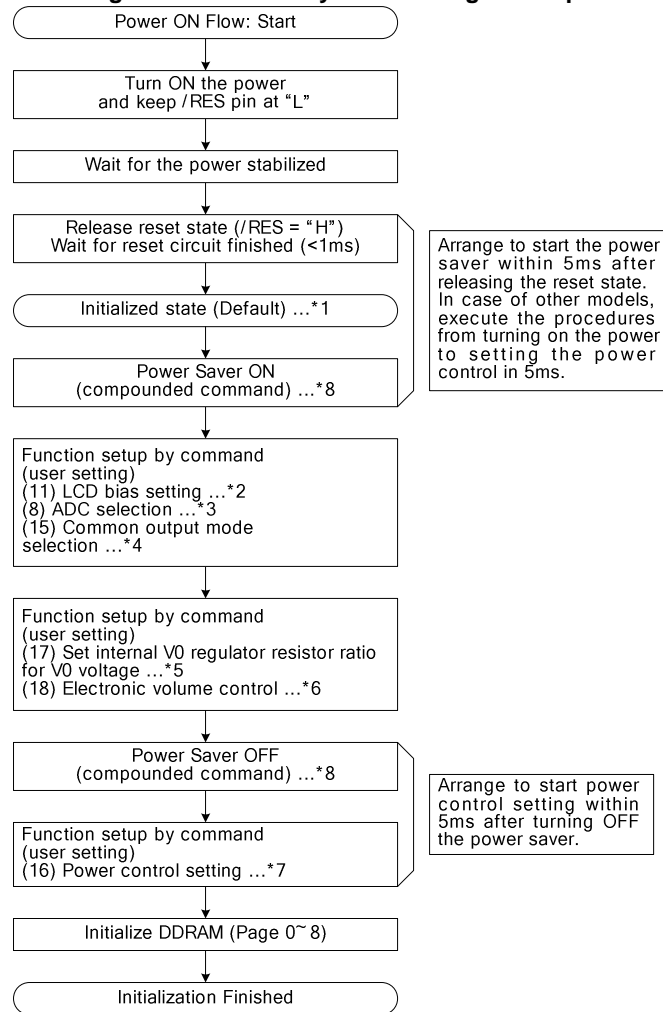
\*4: Command description; Common output state selection

\*5: Description of functions; Power circuit & Command description; Setting the built-in resistance ratio for regulation of the V0 voltage

\*6: Description of functions; Power circuit & Command description; Electronic volume control

\*7: Description of functions; Power circuit & Command description; Power control setting

## 2. When the built-in power is not being used immediately after turning on the power:



\* The target time of 5ms will result to vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

Notes: Refer to respective sections or paragraphs listed below.

\*1: Description of functions; Resetting circuit

\*2: Command description; LCD bias setting

\*3: Command description; ADC selection

\*4: Command description; Common output state selection

\*5: Description of functions; Power circuit & Command description; Setting the built-in resistance ratio for regulation of the V0 voltage

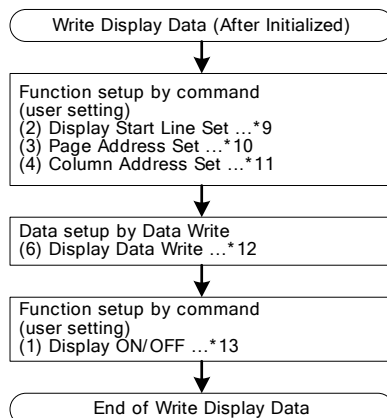
\*6: Description of functions; Power circuit & Command description; Electronic volume control

\*7: Description of functions; Power circuit & Command description; Power control setting

\*8: The power saver ON state can either be in sleep state or stand-by state.

Command description; Power saver START (multiple commands)

## (2) Data Display



Notes: Reference items

\*9: Command Description; Display start line set

\*10: Command Description; Page address set

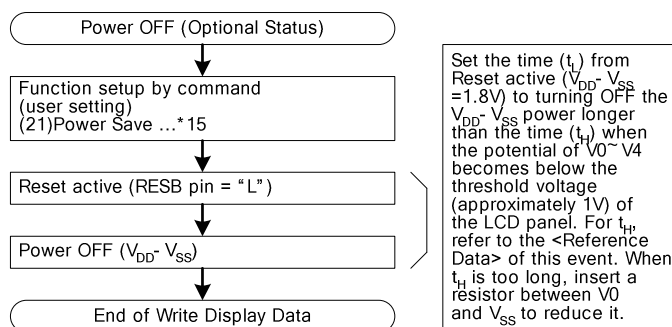
\*11: Command Description; Column address set

\*12: Command Description; Display data write

\*13: Command Description; Display ON/OFF

Avoid displaying all the data at the data display start (when the display is ON) in white.

## (3) Power OFF \*14



Notes: Reference items

\*14: The logic circuit of this IC's power supply  $V_{DD} - V_{SS}$  controls the driver of the LCD power supply  $V_{SS} - V_0$ . So, if the power supply  $V_{DD} - V_{SS}$  is cut off when the LCD power supply  $V_{SS} - V_0$  has still any residual voltage, the driver (COM. SEG) may output any uncontrolled voltage. When turning off the power, observe the following basic procedures:

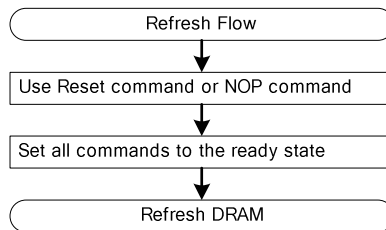
- After turning off the internal power supply, make sure that the potential  $V_0 \sim V_4$  has become below the threshold voltage of the LCD panel, and then turn off this IC's power supply ( $V_{DD} - V_{SS}$ ). 6. Description of Function, 6.7 Power Circuit

\*15: After inputting the power save command, be sure to reset the function using the /RES terminal until the power supply  $V_{DD} - V_{SS}$  is turned off. 7. Command Description (20) Power Save

\*16: After inputting the power save command, do not reset the function using the /RES terminal until the power supply  $V_{DD} - V_{SS}$  is turned off. 7. Command Description (20) Power Save

## Refresh

It is recommended to turn on the refresh sequence regularly at a specified interval.



## Precautions on Turning off the power

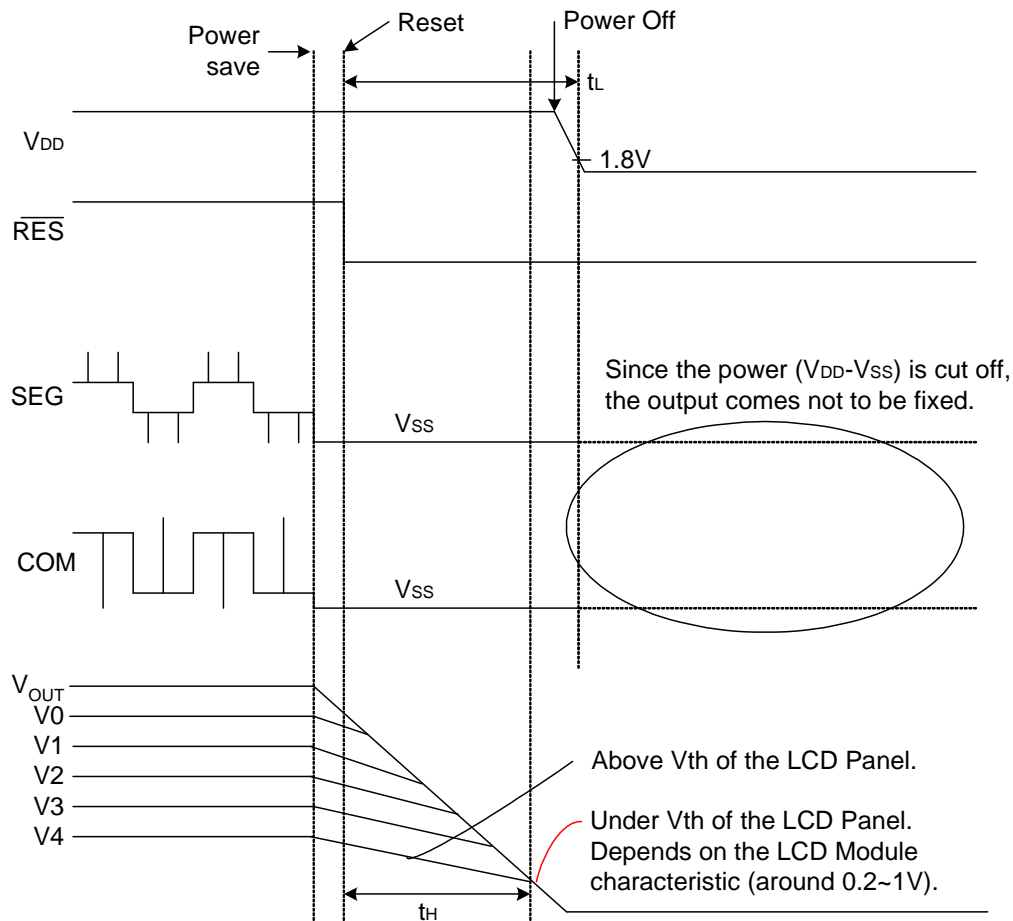
<Turning the power ( $V_{DD} - V_{SS}$ ) off>

1) Power Save (The LCD powers ( $V_0 - V_{SS}$ ) are off.) → Reset input → Power ( $V_{DD} - V_{SS}$ ) OFF

• Observe  $t_L > t_H$ .

• When  $t_L < t_H$ , an irregular display may occur.

Set  $t_L$  on the MPU according to the software.  $t_H$  is determined according to the external capacitor C2 (smoothing capacitor of  $V_0 \sim V_4$ ) and the driver's discharging capacity.



<Turning the power (VDD - VSS) off : When command control is not possible.>

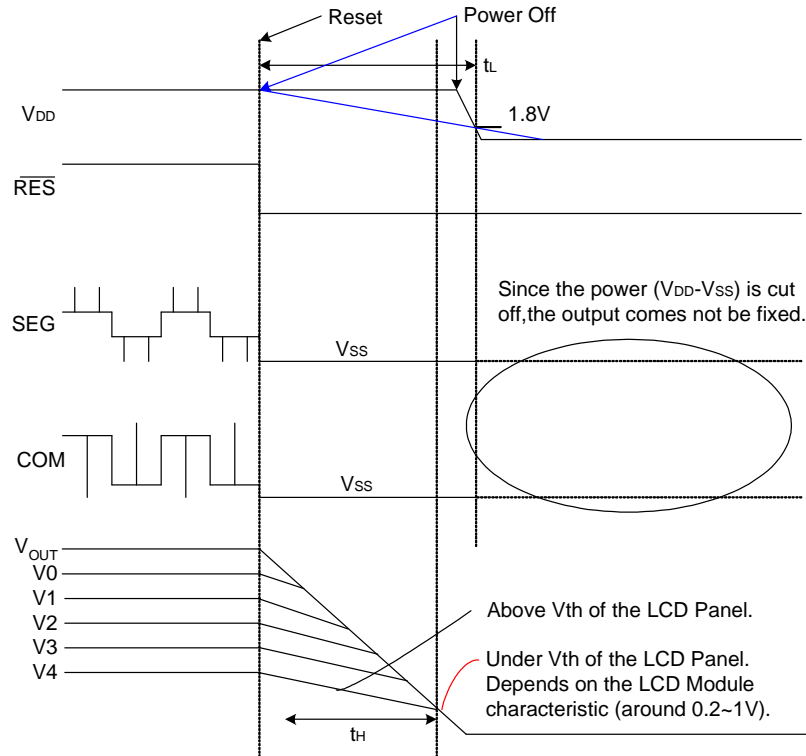
2) Reset (The LCD powers (VDD - Vss) are off.) → Power (VDD - Vss) OFF

• Observe  $t_L > t_H$ .

• When  $t_L < t_H$ , an irregular display may occur.

For  $t_L$ , make the power (VDD - Vss) falling characteristics longer or consider any other method.

$t_H$  is determined according to the external capacity C2 (smoothing capacity of V0 to V4) and the driver's discharging capacity.



<Reference Data>

V0 voltage falling (discharge) time ( $t_H$ ) after the process of operation → power save → reset.

V0 voltage falling (discharge) time ( $t_H$ ) after the process of operation → reset.

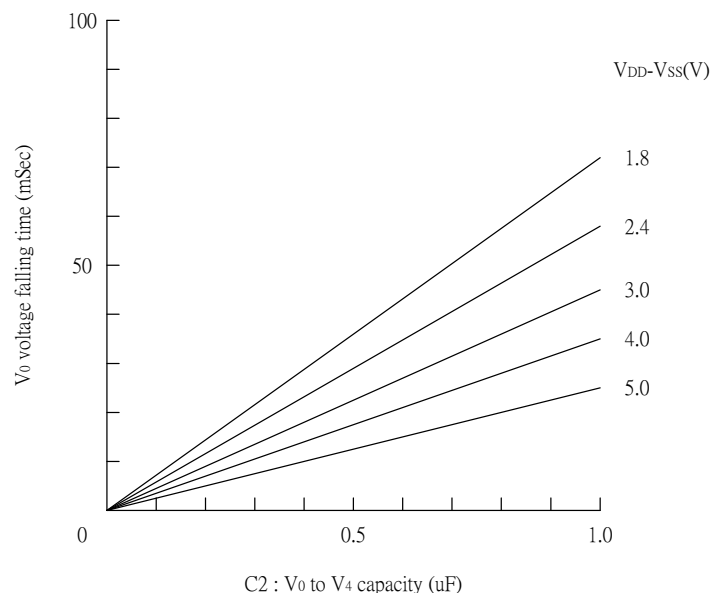


Figure 31

## ABSOLUTE MAXIMUM RATINGS

Unless otherwise specified,  $V_{SS} = 0V$

Parameter		Symbol	Conditions	Unit
Power Supply Voltage		$V_{DD}$	$-0.3 \sim 3.6$	V
Power supply voltage ( $V_{DD}$ standard)		$V_{DD2}$	$-0.3 \sim 3.6$	V
Power supply voltage ( $V_{DD}$ standard)		$V_0, V_{OUT}$	$-0.3 \sim 14.5$	V
Power supply voltage ( $V_{DD}$ standard)		$V_1, V_2, V_3, V_4$	$-0.3 \sim V_0+0.3$	V
Input Voltage	(Digital Pads)	$V_{IN}$	$-0.3 \sim V_{DD}+0.3$	V
Output Voltage		$V_O$	$-0.3 \sim V_{DD}+0.3$	V
Operating temperature	Bare chip	$T_{OPR}$	$-30$ to $+85$	°C
Storage temperature		$T_{STR}$	$-65$ to $+150$	°C

Table 17

### Notes and Cautions

1. The voltages are relative to  $V_{SS} = 0V$  unless otherwise specified.
2. The ranges listed in this section are stress only. It is recommended that the normal operating condition of this device should be in the ranges listed in "DC Characteristics" (the next section).
3. Stress over the listed ranges in "Absolute Maximum Ratings" may cause permanent damage to this device.
4. If this device is operated out of these conditions and ranges, it may not only result in malfunctions, but may have a negative impact on the reliability as well.
5. Insure that the voltage levels of  $V_1, V_2, V_3$ , and  $V_4$  are always such that  $V_{OUT} \geq V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4$ .

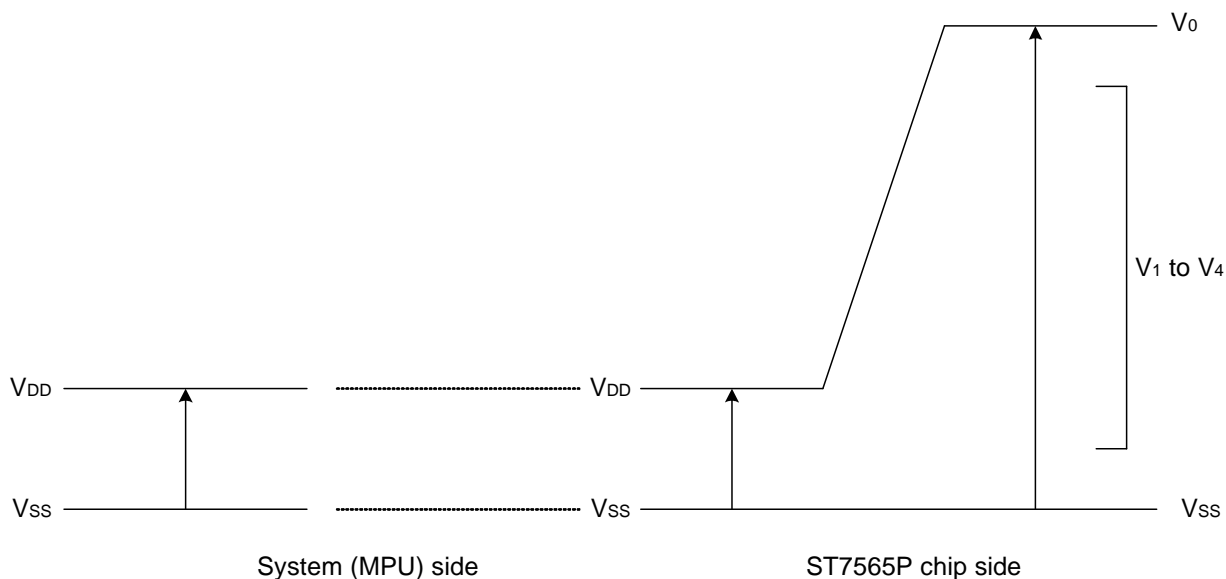


Figure 30

## DC CHARACTERISTICS

Unless otherwise specified,  $V_{SS} = 0\text{ V}$ ,  $V_{DD} = 3.0\text{ V} \pm 10\%$ ,  $T_a = -30\text{ to }85^\circ\text{C}$

Table 18

Item		Symbol	Condition		Rating			Units	Applicable Pin
					Min.	Typ.	Max.		
Operating Voltage (1)		V <sub>DD</sub>			1.8	—	3.3	V	V <sub>SS</sub> *1
Operating Voltage (2)		V <sub>DD2</sub>	(Related to V <sub>SS</sub> )		2.4	—	3.3	V	V <sub>SS</sub>
High-level Input Voltage		V <sub>IHC</sub>			0.8 x V <sub>DD</sub>	—	V <sub>DD</sub>	V	*3
Low-level Input Voltage		V <sub>ILC</sub>			V <sub>SS</sub>	—	0.2 x V <sub>DD</sub>	V	*3
High-level Output Voltage		V <sub>OHC</sub>	I <sub>OH</sub> = −1 mA		0.8 x V <sub>DD</sub>	—	V <sub>DD</sub>	V	*4
Low-level Output Voltage		V <sub>OLC</sub>	I <sub>OL</sub> = 1 mA		V <sub>SS</sub>	—	0.2 x V <sub>DD</sub>	V	*4
Input leakage current		I <sub>LI</sub>	V <sub>IN</sub> = VDD or VSS		−1.0	—	1.0	μA	*5
Output leakage current		I <sub>LO</sub>	V <sub>IN</sub> = VDD or VSS		−3.0	—	3.0	μA	*6
Liquid Crystal Driver ON Resistance		R <sub>ON</sub>	Ta = 25℃ (Related to V <sub>SS</sub> )	V0 = 13.0V	—	2.0	3.5	KΩ	SEGn COMn *7
				V0 = 8.0V	—	3.2	5.4		
Static Consumption Current		I <sub>SSQ</sub>	V0 = 13.0 V (Related to V <sub>SS</sub> )		—	0.01	2	μA	V <sub>DD</sub> , V <sub>DD2</sub>
Output Leakage Current		I <sub>5Q</sub>			—	0.01	10	μA	V0
Input Terminal Capacitance		C <sub>IN</sub>	Ta = 25℃ , f = 1 MHz		—	5.0	8.0	pF	
Oscillator Frequency	Internal Oscillator	f <sub>OSC</sub>	1/65 duty 1/33 duty	Ta = 25℃	17	20	24	kHz	*8
	External Input	f <sub>CL</sub>			17	20	24	kHz	CL
	Internal Oscillator	f <sub>OSC</sub>	1/49 duty 1/53 duty 1/55 duty	Ta = 25℃	25	30	35	kHz	*8
	External Input	f <sub>CL</sub>			25	30	35	kHz	CL

Table 19

Item	Symbol	Condition	Rating			Units	Applicable Pin
			Min.	Typ.	Max.		
Internal Power	Input voltage	V <sub>DD2</sub> (Relative to V <sub>SS</sub> )	2.4	—	3.3	V	V <sub>SS</sub>
	Supply Step-up output voltage Circuit	V <sub>OUT</sub> (Relative to V <sub>SS</sub> )	—	—	13.5	V	V <sub>OUT</sub>
	Voltage regulator Circuit Operating Voltage	V <sub>OUT</sub> (Relative to V <sub>SS</sub> )	6.0	—	13.5	V	V <sub>OUT</sub>
	Voltage Follower Circuit Operating Voltage	V <sub>O</sub> (Relative to V <sub>SS</sub> )	4.0	—	13.0	V	V <sub>O</sub> * 9
	Base Voltage	V <sub>R</sub> Ta = 25°C , (Relative to V <sub>SS</sub> ) -0.05%/°C	2.07	2.10	2.13	V	*10

- **Dynamic Consumption Current : During Display, with the Internal Power Supply OFF** Current consumed by total ICs when an external power supply is used .

Table 20

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern OFF	I <sub>DD</sub>	V <sub>DD</sub> = 3.0 V, V <sub>O</sub> - V <sub>SS</sub> = 11.0 V	—	16	27	μA	*11
Display Pattern Checker	I <sub>DD</sub>	V <sub>DD</sub> = 3.0 V, V <sub>O</sub> - V <sub>SS</sub> = 11.0 V	—	19	32	μA	*11

- **Dynamic Consumption Current : During Display, with the Internal Power Supply ON**

Table 21

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern OFF	I <sub>DD</sub>	V <sub>DD</sub> = 3.0 V, Quad step-up voltage. V <sub>O</sub> - V <sub>SS</sub> = 11.0 V	Normal Mode	—	90	μA	*12
			High-Power Mode	—	128		
Display Pattern Checker	I <sub>DD</sub>	V <sub>DD</sub> = 3.0 V, Quad step-up voltage. V <sub>O</sub> - V <sub>SS</sub> = 11.0 V	Normal Mode	—	100	μA	*12
			High-Power Mode	—	135		

- **Consumption Current at Time of Power Saver Mode : V<sub>SS</sub> = -3.0 V ± 10%**

Table 22

Item	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Sleep mode	I <sub>DD</sub>	Ta = 25°C	—	0.1	4	μA	
Standby Mode	I <sub>DD</sub>	Ta = 25°C	—	5	10		



• The Relationship Between Oscillator Frequency  $f_{OSC}$ , Display Clock Frequency  $f_{CL}$  and the Liquid Crystal Frame Rate Frequency  $f_{FR}$

Table 23

Item		$f_{CL}$	$f_{FR}$
1/65 DUTY	Used internal oscillator circuit	$f_{OSC} / 4$	$f_{OSC} / (4 \times 65)$
	Used <b>external</b> display clock	External input ( $f_{CL}$ )	$f_{CL} / 260$
1/49 DUTY	Used internal oscillator circuit	$f_{OSC} / 4$	$f_{OSC} / (4 \times 49)$
	Used <b>external</b> display clock	External input ( $f_{CL}$ )	$f_{CL} / 196$
1/33 DUTY	Used internal oscillator circuit	$f_{OSC} / 8$	$f_{OSC} / (8 \times 33)$
	Used <b>external</b> display clock	External input ( $f_{CL}$ )	$f_{CL} / 264$
1/55 DUTY	Used internal oscillator circuit	$f_{OSC} / 4$	$f_{OSC} / (4 \times 55)$
	Used <b>external</b> display clock	External input ( $f_{CL}$ )	$f_{CL} / 220$
1/53 DUTY	Used internal oscillator circuit	$f_{OSC} / 4$	$f_{OSC} / (4 \times 53)$
	Used <b>external</b> display clock	External input ( $f_{CL}$ )	$f_{CL} / 212$

( $f_{FR}$  is the liquid crystal alternating current period, and not the FR signal period.)

References for items market with \*

- \*1 While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.
- \*2 The operating voltage range for the  $V_{SS}$  system and the  $V_0$  system is. This applies when the external power supply is being used.
- \*3 The A0, D0 to D5, D6 (SCL), D7 (SI), /RD (E), /WR (R/W), /CS1, CS2, CLS, CL, FR, M/S, C86, P/S, /DOF, /RES, IRS, and /HPM terminals.
- \*4 The D0 to D7, FR, /DOF, and CL terminals.
- \*5 The A0, /RD (E), /WR (R/W), /CS1, CS2, CLS, M/S, C86, P/S, /RES, IRS, and /HPM terminals.
- \*6 Applies when the D0 to D5, D6 (SCL), D7 (SI), CL, FR, and /DOF terminals are in a high impedance state.
- \*7 These are the resistance values for when a 0.1 V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals ( $V_1$ ,  $V_2$ ,  $V_3$ , and  $V_4$ ). These are specified for the operating voltage (3) range.  $R_{ON} = 0.1 \text{ V} / \Delta I$  (Where  $\Delta I$  is the current that flows when 0.1 V is applied while the power supply is ON.)
- \*8 See Table 23 for the relationship between the oscillator frequency and the frame rate frequency.
- \*9 The  $V_0$  voltage regulator circuit regulates within the operating voltage range of the voltage follower.
- \*10 This is the internal voltage reference supply for the  $V_0$  voltage regulator circuit. In the ST7565P, the temperature range approximately  $-0.05\%/^{\circ}\text{C}$ .
- \*11, 12 It indicates the current consumed on ICs alone when the internal oscillator circuit and display are turned on. The ST7565P is 1/9 biased. Does not include the current due to the LCD panel capacity and wiring capacity. Applicable only when there is no access from the MPU.
- \*12 It is the value on a ST7565P having the VREG temperature gradient is  $-0.05\%/^{\circ}\text{C}$  when the  $V_0$  voltage regulator internal resistor is used.

## TIMING CHARACTERISTICS

## System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

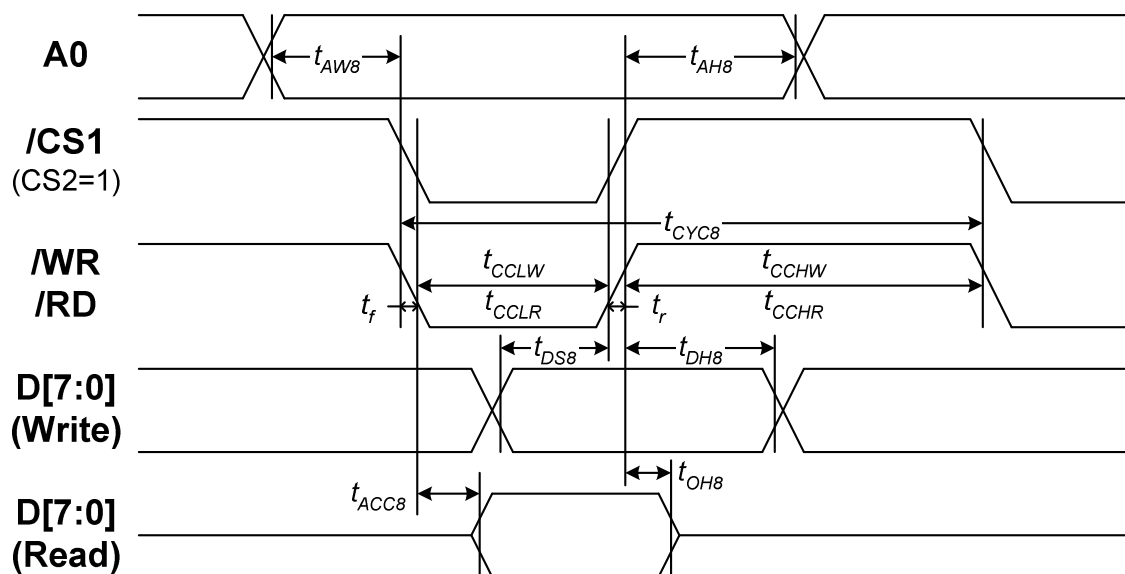


Figure 37

Table 24

(V<sub>DD</sub> = 3.3V, T<sub>a</sub> = -30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t <sub>AH8</sub>		0	—	Ns
Address setup time		t <sub>AW8</sub>		0	—	
System cycle time		t <sub>CYC8</sub>		240	—	
Write L pulse width	/WR	t <sub>CCLW</sub>		80	—	
Write H pulse width		t <sub>CCHW</sub>		80	—	
Read L pulse width	/RD	t <sub>CCLR</sub>		140	—	
Read H pulse width		t <sub>CCHR</sub>		80	—	
Write Data setup time	D0 to D7	t <sub>DS8</sub>		40	—	
Write Address hold time		t <sub>DH8</sub>		0	—	
Read access time		t <sub>ACC8</sub>	CL = 100 pF	—	70	
Read Output disable time		t <sub>OH8</sub>	CL = 100 pF	5	50	

Table 25

(V<sub>DD</sub> = 2.7V, Ta = -30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t <sub>AH8</sub>		0	—	ns
Address setup time		t <sub>AW8</sub>		0	—	
System cycle time		t <sub>CYC8</sub>		400	—	
Write L pulse width	WR	t <sub>CCLW</sub>		220	—	
Write H pulse width		t <sub>CCHW</sub>		180	—	
Read L pulse width	RD	t <sub>CCLR</sub>		220	—	
Read H pulse width		t <sub>CCHR</sub>		180	—	
Write Data setup time	D0 to D7	t <sub>DS8</sub>		40	—	
Write Address hold time		t <sub>DH8</sub>		0	—	
Read access time		t <sub>ACC8</sub>	CL = 100 pF	—	140	
Read Output disable time		t <sub>OH8</sub>	CL = 100 pF	10	100	

Table 26

(V<sub>DD</sub> = 1.8V, Ta = -30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t <sub>AH8</sub>		0	—	ns
Address setup time		t <sub>AW8</sub>		0	—	
System cycle time		t <sub>CYC8</sub>		640	—	
Write L pulse width	WR	t <sub>CCLW</sub>		360	—	
Write H pulse width		t <sub>CCHW</sub>		280	—	
Read L pulse width	RD	t <sub>CCLR</sub>		360	—	
Read H pulse width		t <sub>CCHR</sub>		280	—	
Write Data setup time	D0 to D7	t <sub>DS8</sub>		80	—	
Write Address hold time		t <sub>DH8</sub>		0	—	
Read access time		t <sub>ACC8</sub>	CL = 100 pF	—	240	
Read Output disable time		t <sub>OH8</sub>	CL = 100 pF	10	200	

\*1 The input signal rise time and fall time (t<sub>r</sub>, t<sub>f</sub>) is specified at 15 ns or less. When the system cycle time is extremely fast, (t<sub>r</sub> + t<sub>f</sub>) ≤ (t<sub>CYC8</sub> - t<sub>CCLW</sub> - t<sub>CCHW</sub>) for (t<sub>r</sub> + t<sub>f</sub>) ≤ (t<sub>CYC8</sub> - t<sub>CCLR</sub> - t<sub>CCHR</sub>) are specified.

\*2 All timing is specified using 20% and 80% of V<sub>DD</sub> as the reference.

\*3 t<sub>CCLW</sub> and t<sub>CCLR</sub> are specified as the overlap between /CS1 being "L" (CS2 = "H") and /WR and /RD being at the "L" level.

## System Bus Read/Write Characteristics 2 (For the 6800 Series MPU)

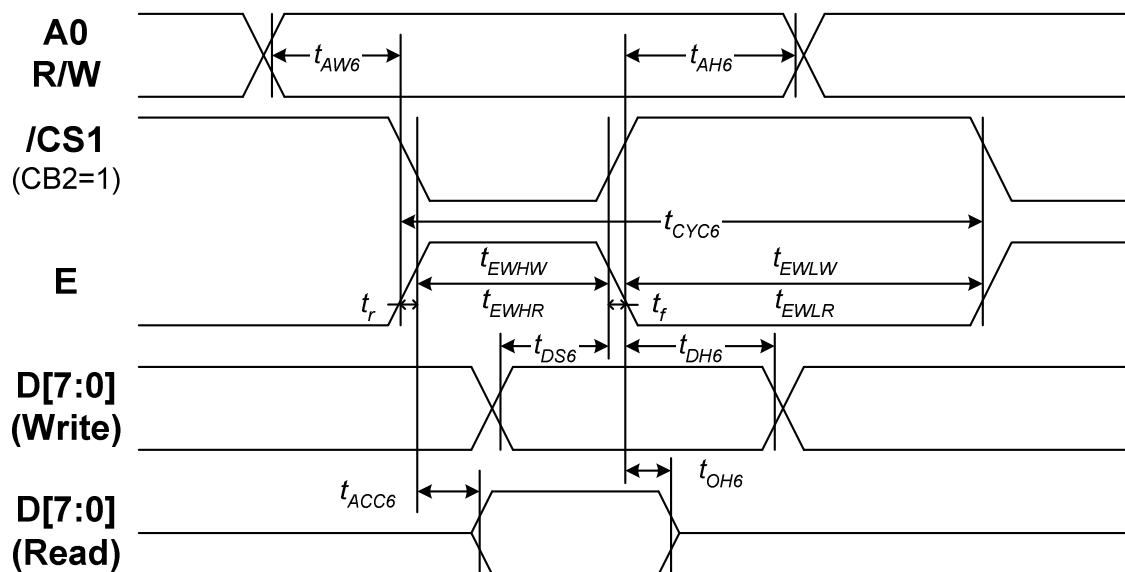


Figure 38

Table 27

(V<sub>DD</sub> = 3.3V, T<sub>a</sub> = -30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t <sub>AH6</sub>		0	—	ns
Address setup time		t <sub>AW6</sub>		0	—	
System cycle time		t <sub>CYC6</sub>		240	—	
Enable L pulse width (WRITE)	E	t <sub>EWLW</sub>		80	—	
Enable H pulse width (WRITE)		t <sub>EWHW</sub>		80	—	
Enable L pulse width (READ)		t <sub>EWLR</sub>		80	—	
Enable H pulse width (READ)		t <sub>EWHR</sub>		140	—	
WRITE Data setup time	D0 to D7	t <sub>DS6</sub>		40	—	
WRITE Address hold time		t <sub>DH6</sub>		0	—	
READ access time		t <sub>ACC6</sub>	CL = 100 pF	—	70	
READ Output disable time		t <sub>OH6</sub>	CL = 100 pF	5	50	

**Table 28**

(V<sub>DD</sub> = 2.7V, Ta = -30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t <sub>AH6</sub>		0	—	ns
Address setup time		t <sub>AW6</sub>		0	—	
System cycle time		t <sub>CYC6</sub>		400	—	
Enable L pulse width (WRITE)	E	t <sub>EWLW</sub>		220	—	
Enable H pulse width (WRITE)		t <sub>EWHW</sub>		180	—	
Enable L pulse width (READ)		t <sub>EWLR</sub>		220	—	
Enable H pulse width (READ)		t <sub>EWHR</sub>		180	—	
WRITE Data setup time	D0 to D7	t <sub>DS6</sub>		40	—	
WRITE Address hold time		t <sub>DH6</sub>		0	—	
READ access time		t <sub>ACC6</sub>	CL = 100 pF	—	140	
READ Output disable time		t <sub>OH6</sub>	CL = 100 pF	10	100	

**Table 29**

(V<sub>DD</sub> = 1.8V, Ta = -30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t <sub>AH6</sub>		0	—	ns
Address setup time		t <sub>AW6</sub>		0	—	
System cycle time		t <sub>CYC6</sub>		640	—	
Enable L pulse width (WRITE)	E	t <sub>EWLW</sub>		360	—	
Enable H pulse width (WRITE)		t <sub>EWHW</sub>		280	—	
Enable L pulse width (READ)		t <sub>EWLR</sub>		360	—	
Enable H pulse width (READ)		t <sub>EWHR</sub>		280	—	
WRITE Data setup time	D0 to D7	t <sub>DS6</sub>		80	—	
WRITE Address hold time		t <sub>DH6</sub>		0	—	
READ access time		t <sub>ACC6</sub>	CL = 100 pF	—	240	
READ Output disable time		t <sub>OH6</sub>	CL = 100 pF	10	200	

\*1 The input signal rise time and fall time (t<sub>r</sub>, t<sub>f</sub>) is specified at 15 ns or less. When the system cycle time is extremely fast, (t<sub>r</sub> + t<sub>f</sub>) ≤ (t<sub>CYC6</sub> - t<sub>EWLW</sub> - t<sub>EWHW</sub>) for (t<sub>r</sub> + t<sub>f</sub>) ≤ (t<sub>CYC6</sub> - t<sub>EWLR</sub> - t<sub>EWHR</sub>) are specified.

\*2 All timing is specified using 20% and 80% of V<sub>DD</sub> as the reference.

\*3 t<sub>EWLW</sub> and t<sub>EWLR</sub> are specified as the overlap between CS1 being "L" (CS2 = "H") and E.

## The Serial Interface

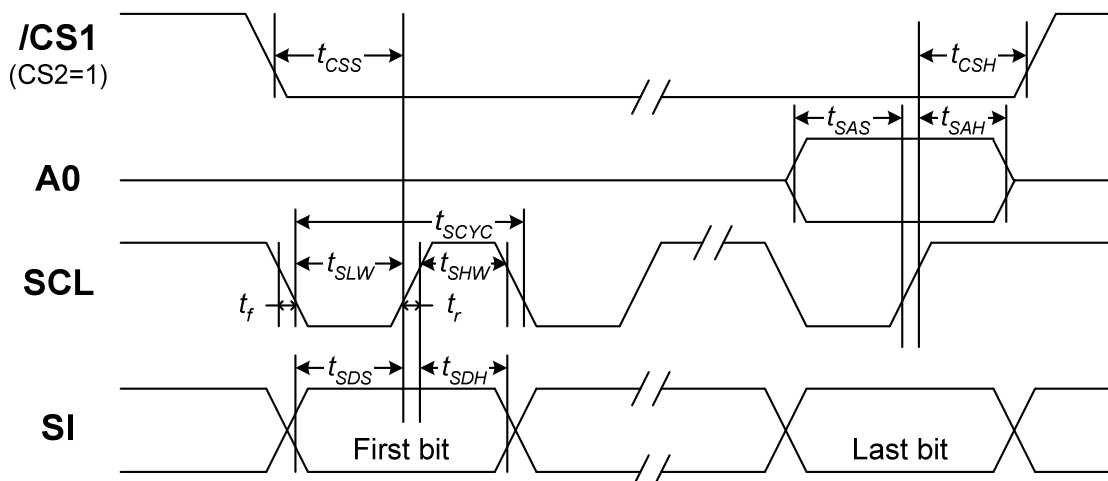


Figure 39

Table 30

( $V_{\text{DD}} = 3.3\text{V}$ ,  $T_a = -30$  to  $85^\circ\text{C}$ )

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	$t_{\text{SCYC}}$		50	—	ns
SCL "H" pulse width		$t_{\text{SHW}}$		25	—	
SCL "L" pulse width		$t_{\text{SLW}}$		25	—	
Address setup time	A0	$t_{\text{SAS}}$		20	—	
Address hold time		$t_{\text{SAH}}$		10	—	
Data setup time	SI	$t_{\text{SDS}}$		20	—	
Data hold time		$t_{\text{SDH}}$		10	—	
CS-SCL time	CS	$t_{\text{CSS}}$		20	—	
CS-SCL time		$t_{\text{CSH}}$		40	—	

Table 31

( $V_{\text{DD}} = 2.7\text{V}$ ,  $T_a = -30$  to  $85^\circ\text{C}$ )

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	$t_{\text{SCYC}}$		100	—	ns
SCL "H" pulse width		$t_{\text{SHW}}$		50	—	
SCL "L" pulse width		$t_{\text{SLW}}$		50	—	
Address setup time	A0	$t_{\text{SAS}}$		30	—	
Address hold time		$t_{\text{SAH}}$		20	—	
Data setup time	SI	$t_{\text{SDS}}$		30	—	
Data hold time		$t_{\text{SDH}}$		20	—	
CS-SCL time	CS	$t_{\text{CSS}}$		30	—	
CS-SCL time		$t_{\text{CSH}}$		60	—	

**Table 32**

(V<sub>DD</sub> = 1.8V, T<sub>a</sub> = -30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t <sub>SCYC</sub>		200	—	ns
SCL "H" pulse width		t <sub>SHW</sub>		80	—	
SCL "L" pulse width		t <sub>SLW</sub>		80	—	
Address setup time	A0	t <sub>SAS</sub>		60	—	
Address hold time		t <sub>SAH</sub>		30	—	
Data setup time	SI	t <sub>SDS</sub>		60	—	
Data hold time		t <sub>SDH</sub>		30	—	
CS-SCL time	CS	t <sub>CSS</sub>		40	—	
CS-SCL time		t <sub>CSH</sub>		100	—	

\*1 The input signal rise and fall time (t<sub>r</sub>, t<sub>f</sub>) are specified at 15 ns or less.

\*2 All timing is specified using 20% and 80% of V<sub>DD</sub> as the standard.

## Reset Timing

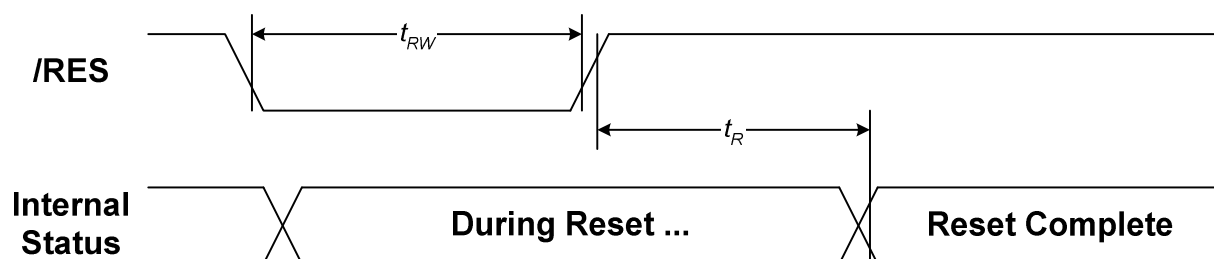


Figure 41

Table 36

(V<sub>DD</sub> = 3.3V, Ta = -30 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time	/RES	$t_R$		—	—	1.0	μs
Reset "L" pulse width		$t_{RW}$		1.0	—	—	μs

Table 37

(V<sub>DD</sub> = 2.7V, Ta = -30 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time	/RES	$t_R$		—	—	2.0	μs
Reset "L" pulse width		$t_{RW}$		2.0	—	—	μs

Table 38

(V<sub>DD</sub> = 1.8V, Ta = -30 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time	/RES	$t_R$		—	—	3.0	μs
Reset "L" pulse width		$t_{RW}$		3.0	—	—	μs

\*1 All timing is specified with 20% and 80% of V<sub>DD</sub> as the standard.



## THE MPU INTERFACE (REFERENCE EXAMPLES)

ST7565P can be connected to either 80X86 series MPUs or 68000 series MPU. Moreover, by using the serial interface, it is possible to operate ST7565P with fewer signal pins.

The display area can be extended horizontally by using two ST7565P chips. Two chip select signals can be used to select the individual ICs to access.

### (1) 8080 Series MPUs

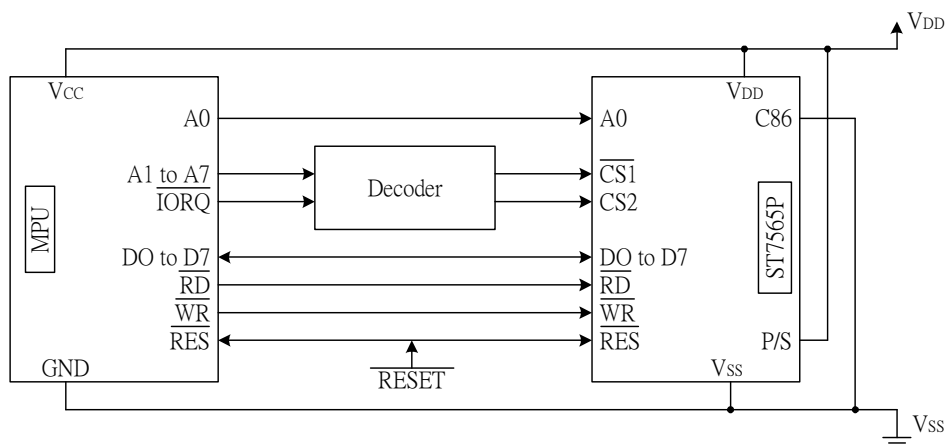


Figure 42-1

### (2) 6800 Series MPUs

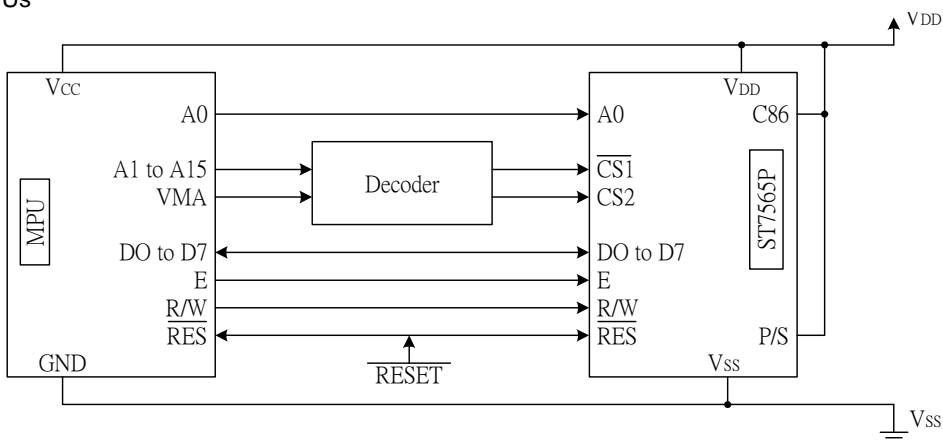


Figure 42-2

### (3) Using the Serial Interface

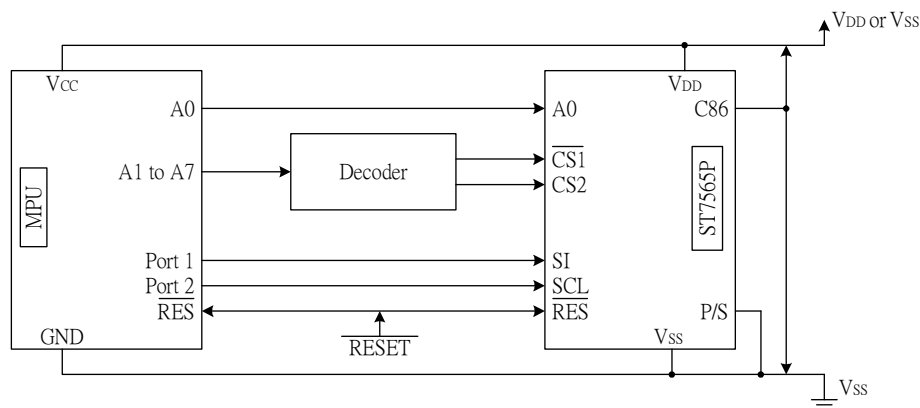


Figure 42-3

## CONNECTIONS BETWEEN LCD DRIVERS (REFERENCE EXAMPLE)

The display area of LCD panel can be extended horizontally by using two ST7565P chips. Use a same equipment type.

(1) ST7565P (master) → ST7565P (slave)

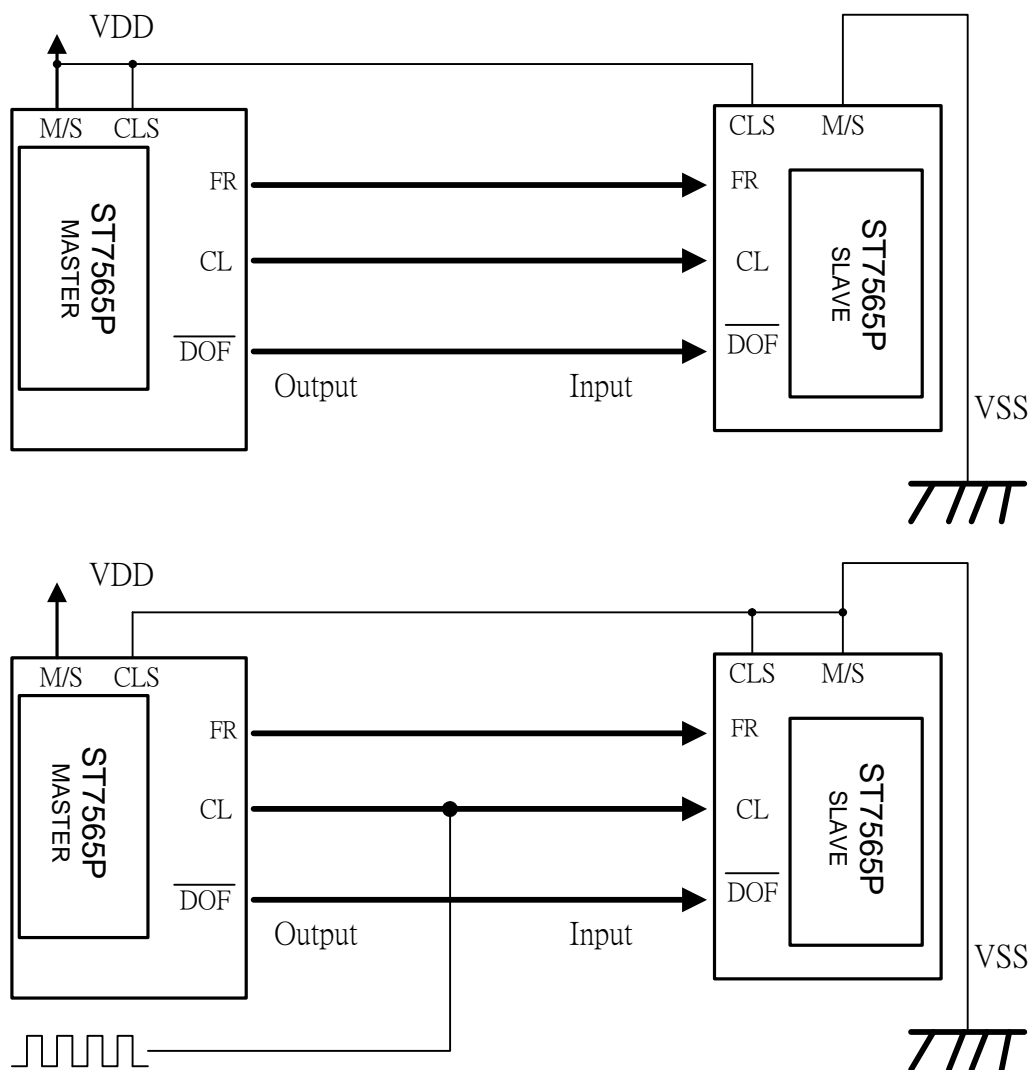


Figure 43-1

(2) Single-chip Structure

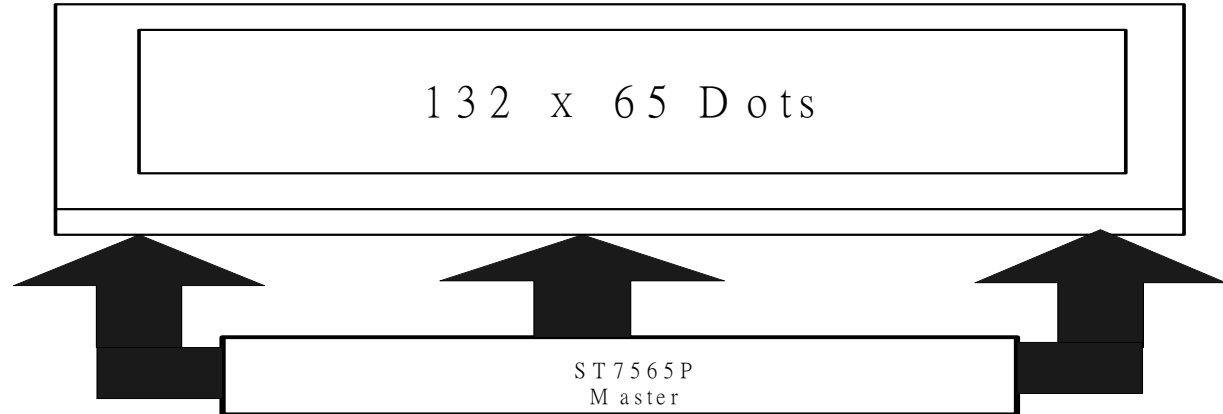


Figure 43-2

(3) Double-chip Structure

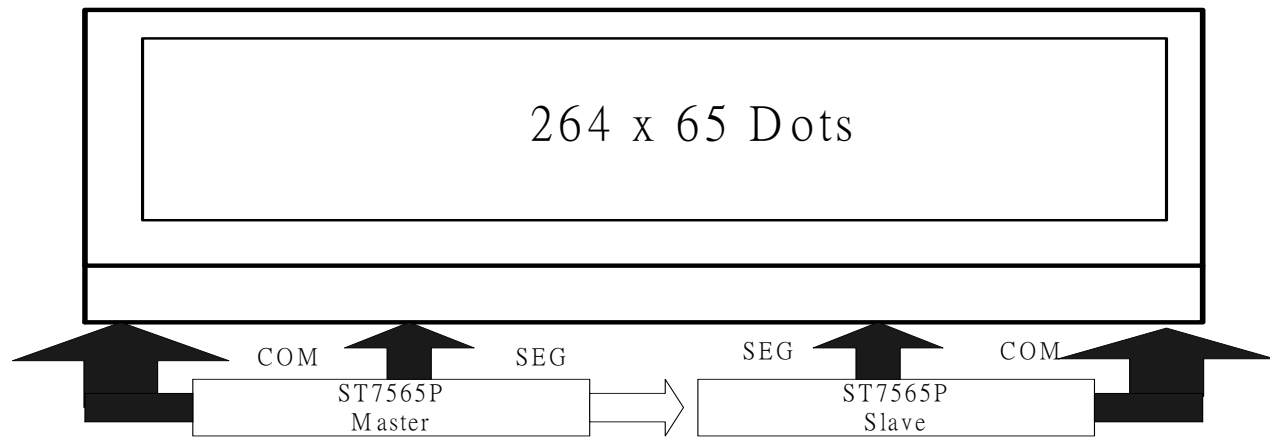


Figure 43-3

**Change Notes**

2004.04.05	Ver 1.2a	● Modify Serial interface Timing Character.
2004.05.18	Ver 1.3	● Change Temperature compensation rate to $-0.05\%/^{\circ}\text{C}$ .
2004.05.31	Ver 1.4	● Add I/O pin ITO resistor limitation.
2004.06.24	Ver 1.5	● Modify Page 2 PAD Diagram.
2004.07.14	Ver 1.6	● Modify Page 19 V1~V4 voltage setting with different bias set command.
2005.09.22	Ver 1.7	<ul style="list-style-type: none"><li>● Modify Feature Description;</li><li>● Modify operating temperature;</li><li>● Modify PIN Name: PAD 80~85 to TEST0~5;</li><li>● Modify Absolute Maximum Ratings;</li><li>● Modify Ta of DC Characteristics and Reset Timing;</li><li>● Remove redundant Page 28;</li><li>● Modify reference voltage to Vss (Page 58, 59).</li></ul>
2006.02.13	Ver 1.8	<ul style="list-style-type: none"><li>● Modify the description of DC characteristics.</li><li>● Modify function description.</li><li>● Redraw figures.</li><li>● Redraw the PAD DIAGRAM.</li><li>● Highlight the HPM (High Power Mode) description.</li><li>● Put emphasis on the power OFF procedure (Page 56-57).</li></ul>
2006/03/10	Ver 1.9	● Fix Ver. 1.8: Booster Circuit mistake (Booster X6, Page 32).
2007/11/06	Ver 1.9a	● Modify PAD pitch between COM[40] and alignment mark of PAD DIAGRAM. (Page 2).
2008/02/19	Ver 1.9b	<ul style="list-style-type: none"><li>● Modify Page 2 information: PAD 115, 290 and alignment mark drawing.</li><li>● Modify some description for easy understanding.</li></ul>
2008/03/14	Ver 1.9c	<ul style="list-style-type: none"><li>● Modify Ver 1.9c mistake: alignment mark coordinate.</li><li>● Add <math>V_{\text{IN}}</math> and <math>V_{\text{O}}</math> in Absolute Maximum Ratings.</li><li>● Modify description in Absolute Maximum Ratings.</li></ul>
2008/04/10	Ver 2.0	<ul style="list-style-type: none"><li>● Remove Static Indicator function and command.</li><li>● Reserved FRS pin function.</li><li>● Truncated Alignment mark coordinate.</li><li>● Rewrite some description.</li><li>● Update timing figures and naming.</li></ul>
2008/07/15	Ver 2.1	● Modify Page 2 information: bump size of PAD 115, 290.
2009/02/23	Ver 2.1a	● Modify mistake of Status Read.