ePAPER DISPLAY MODULE DATASHEET

Datasheet Release 2019-10-22
for
CFAP122250A0-0213

Revision 1v2

Crystalfontz America, Inc.

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TABLE OF CONTENTS

1. General Information

Datasheet Revision History
Datasheet Release Date: **2019-10-22** Datasheet for the CFAP122250A0-0213 ePaper display module.

Product Change Notifications
You can check for or subscribe to Part Change Notices for this display module on our website.

Variations
Slight variations between lots are normal (e.g., contrast, color, or intensity).

Volatility
This display module has volatile memory.

Disclaimer
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2. Description Overview

The CFAP122250A0-0213 is small monochrome ePaper / E-Ink has a 122x250 resolution in a 2.13" diagonal display with about 130 pixels per inch. This is an Active Matrix Electrophoretic Display (AMEPD), and is bi-stable. This display can perform both a full and a partial refresh, and can be used in either portrait or landscape orientation.

3. Features

- High contrast, over 8:1
- High reflectance, over 35%
- Ultra-wide viewing angle
- Ultra-low power consumption
- Pure reflective mode
- Bi-Stable Display
- Commercial temperature range
- Landscape, portrait mode
- Antiglare hard-coated front-surface
- Low current deep sleep mode
- On-chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating V_{COM}, Gate and source driving voltage
- I^2C Signal Master Interface to read external temperature sensor

4. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.13	in	
Display Resolution	122 × 250	pixel	ppi: 130.6
Active Area	48.55 (H) x 23.80 (W)	mm	
Pixel Pitch	0.194 × 0.194	mm	
Pixel Configuration	Rectangle		
Outline Dimension	59.2 (H) x 29.2 (W) × 1.05 (D)	mm	
Weight (Typical)	3±0.5	g	

5. Input/Output Terminals

5.1. Pin Out List

Pin #	Type	Single	Description
1		NC	No Connection and Do Not Connect with Other NC Pins
2	O	GDR	N-Channel MOSFET Gate Drive Control
3	O	RESE	Current Sense Input for the Control Loop
4	C	VGL	Negative Gate Driving Voltage
5	C	VGH	Positive Gate Driving Voltage
6	-	NC	No Connection and Do Not Connect with Other NC Pins
7	O	TOUT1	Serial Data Pin for Panel Break Detection
8	I	BS1	Bus Selection Pin – LOW for 4-wire SPI, HIGH for 3-wire SPI
9	O	BUSY	Busy State Output Pin - when BUSY is HIGH, the operation of chip should not be interrupted and no commands should be issued to the module.
10	I	RES #	Reset signal input. Active low
11	I	D/C #	Data /Command Control Pin connects to the MCU. When D/C# is HIGH data will be interpreted as data, when D/C is Low, data will be interpreted as command.
12	I	CS #	Chip Select Input Pin indicates chip is enabled for MCU communication when CS# is LOW.
13	I/O	D0 (SCLK)	Serial Clock Pin (SPI)
14	I/O	D1 (SDIN)	Serial Data Pin (SPI)
15	I	VDDIO	Power for Interface Logic Pins
16	I	VCI	Power Supply Pin for the Chip
17		VSS	Ground
18	C	VDD	Core Logic Power Pin
19	C	VPP	Power Supply for OTP Programming
20	C	VSH	Positive Source Driving Voltage
21	C	PREVGH	Power Supply Pin for VGH and VSH
22	C	VSL	Negative Source Driving Voltage
23	C	PREVGL	Power Supply Pin for VCOM, VGL, and VSL
24	C	VCOM	VCOM Driving Voltage

6. MCU Interface

6.1. MCU Serial Peripheral Interface (4-Wire SPI)

4-Wire SPI consists of serial clock SCLK (D0), serial data SDIN (D1), D/C#, and CS#. In SPI mode, D0 acts as SCLK and D1 acts as SDIN. The

Table 6-1: Control Pin Status for 4-Wire SPI

Function	D0 (SCLK) Pin	D1 (SDIN) Pin	D/C# Pin	CS# Pin
Write Command	↑	Command Bit	L	L
Write Data	↑	Data Bit	H	L

Notes:
(1) L is connected to V_{SS} and H is connected to V_{DDIO}
(2) ↑ indicates rising edge of signal
(3) SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.

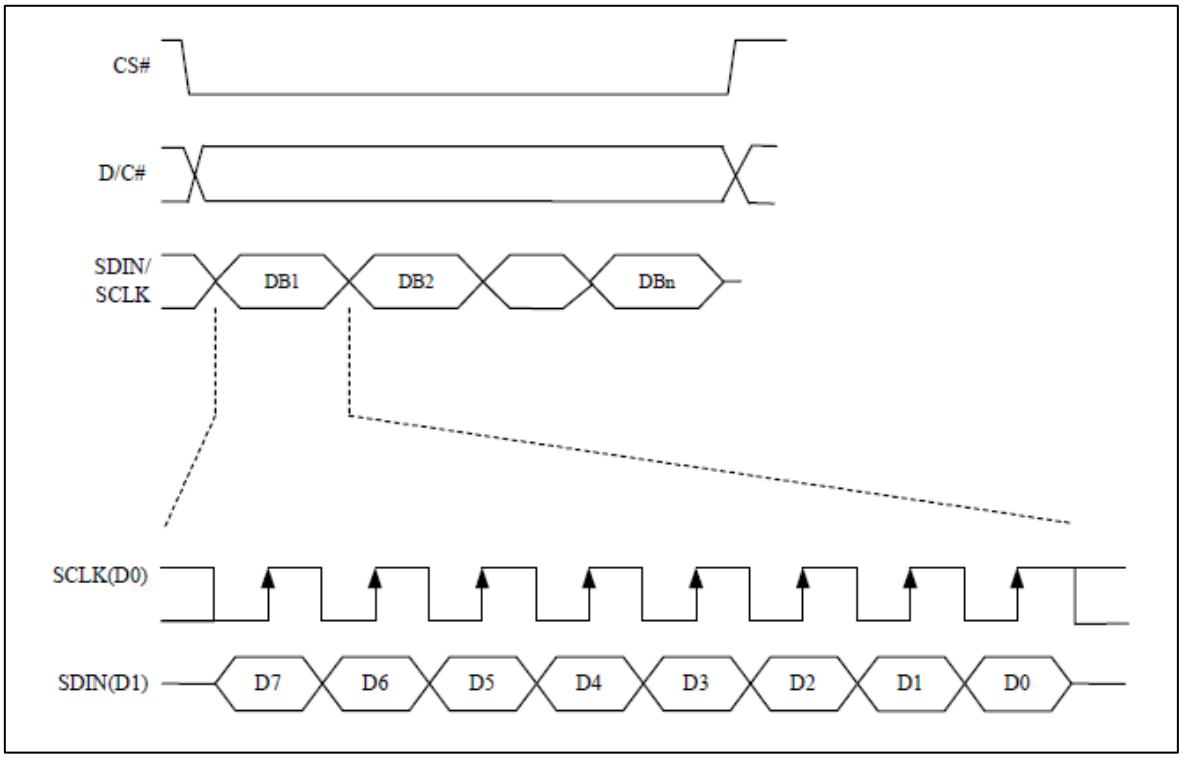


Figure 6-1: Write Procedure in 4-Wire SPI

6.2. MCU Serial Peripheral Interface (3-Wire SPI)

The 3-wire SPI consists of serial clock SCLK, serial data SDIN and CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN. The operation is similar to 4-wire SPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 6-3.

In the write operation, the 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is D/C# bit, D7, D6,… to D0 bit. The first bit is the D/C# bit which determines the following byte is command or data. When the D/C# bit is 0, the following byte is command. When the D/C# bit is 1, the following byte is data.

Table 6-2: Write Procedure in 3-Wire SPI

Function	SCLK Pin	SDIN Pin	D/C# Pin	CS# Pin
Write Command	↑	Command Bit	Tie LOW	L
Write Data	↑	Data Bit	Tie LOW	L

Note: "L" is connected to V_{SS}. "H" is connected to V_{DDIO}. "↑" stands for rising edge of signal.

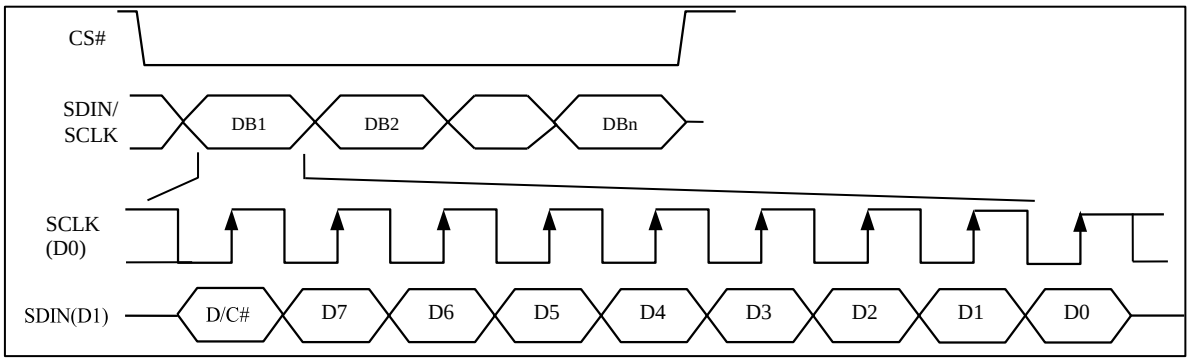


Figure 6-2: Control Pins Status of 3-Wire SPI

7. Temperature Register Mapping

If the temperature value MSByte bit D11 = 0, then the temperature is positive and the value is given by:

(DegC) = + (Temperature value) / 16

If the temperature value MSByte bit D11 = 1, then the temperature is negative and the value is given by:

(DegC) = - (2's complement of temperature value) / 16

12-bit binary (2's complement)	Hexadecimal Value	Decimal Value	Value [DegC]
0111 1111 0000	7F0	2032	127
0111 1110 1110	7EE	2030	126.875
0111 1110 0010	7E2	2018	126.125
0111 1101 0000	7D0	2000	125
0001 1001 0000	190	400	25
0000 0000 0010	002	2	0.125
0000 0000 0000	000	0	0
1111 1111 1110	FFE	-2	-0.125
1110 0111 0000	E70	-400	-25
1100 1001 0010	C92	-878	-54.875
1100 1001 0000	C90	-880	-55

8. Panel Break Detection

The panel break detection function is used to detect a breakage at the panel edge. When the panel break detection command is issued, the panel break detection will be executed. During the detection period, BUSY output is at high level. BUSY output is at low level when the detection is completed. Then, the user can issue the Status Bit Read command to check the status bit for the result of the panel break.

9. Command Table

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>01</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="3">Driver Output Control</td><td rowspan="3">Gate setting
Setting for 232 gates is:

Set A[7:0] = F9h
Set B[2:0] = 00h</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td>0</td><td>0</td><td>03</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td rowspan="3">Gate Driving Voltage Control</td><td rowspan="3">Set Gate driving voltage.

A[4:0] = 10h [POR], VGH at 22V
B[3:0] = 0Ah [POR], VGL at -20V</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td>0</td><td>0</td><td>04</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td rowspan="2">Source Driving Voltage Control</td><td rowspan="2">Set Source output voltage.

A[4:0] = 19h [POR],
VSH/VSL at +/-15V</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>10</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2">Deep Sleep Mode</td><td rowspan="2">Deep Sleep Mode Control<table><tr><th>A[0]</th><th>Description</th></tr><tr><td>0</td><td>Normal Mode [POR]</td></tr><tr><td>1</td><td>Enter Deep Sleep Mode</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>11</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="2">Data Entry Mode Setting</td><td rowspan="2">Define data entry sequence.
A[1:0] = ID[1:0]

Address automatic increment / decrement setting.

The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address.

00-Y decrement, X decrement,
01-Y decrement, X increment,
10-Y increment, X decrement,
11-Y increment, X increment [POR]

A[2] = AM
Set the direction in which the address counter is updated automatically after data is written to the RAM.

When AM = 0, the address counter is updated in the X direction. [POR]

When AM = 1, the address counter is updated in the Y direction.</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A2</td><td>A1</td><td>A0</td></tr>
</table>

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	12	0	0	0	1	0	0	1	0	SWRESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode. **Note**: RAM is unaffected by this command.
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to Temperature Register)	Write to Temperature Register. A[7:0] MSByte 01111111[POR] B[7:0] LSByte 11110000[POR]
0	1	-	A7	A6	A5	A4	A3	A2	A1	A0		
0	1	-	B7	B6	B5	B4	0	0	0	0		
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence. The Display Update Sequence Option is located at R22h. Do not interrupt this operation to avoid corruption of panel images.
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	Option for Display Update Bypass Option used for Pattern Display, which is used for displaying the RAM content on to the Display. OLD RAM Bypass option A[7] A[7] = 1: Enable bypass A[7] = 0: Disable bypass [POR] A[4] value will be used as New RAM for bypass. A[4] = 0 [POR] A[1:0] Initial Update Option - Source Control A[1:0] / GSA / GSB 01[POR] / GS0 / GS1
0	1	-	A7	A6	A5	A4	A3	A2	A1	A0		

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>22</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td rowspan="2">Display Update Control 2</td><td rowspan="2">Display Update Sequence Option:
Enable the stage for Master Activation

<table><tr><th colspan="2">Parameter (in Hex)</th></tr><tr><td>Enable Clock Signal,
Then Enable Analog
Then Load LUT
Then INIITIAL DISPLAY
Then PATTERN DISPLAY
Then Disable Analog
Then Disable OSC</td><td>FF [POR]</td></tr><tr><td>Setting for LUT from OTP
Enable Clock Signal,
Then Enable Analog
Then Load LUT
Then PATTERN DISPLAY
Then Disable Analog
Then Disable OSC</td><td>D7</td></tr><tr><td>Setting for LUT from MCU
Enable Clock Signal,
Then Enable Analog
Then PATTERN DISPLAY
Then Disable Analog
Then Disable OSC</td><td>C7</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>23</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>Panel Break Detection</td><td>After this command is issued, panel break detection will start. The status can be checked by Command 2Fh. During detection, BUSY will be high. The command required CLKEN=1.</td></tr>
<tr><td>0</td><td>0</td><td>24</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Write RAM</td><td>After this command, data entries will be written into the RAM until another command is written. Address pointers will advance accordingly.</td></tr>
</table>

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>2C</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Write VCOM Register</td><td>Write VCOM Register from MCU Interface
<table>
<tr><th>A[7:0]</th><th>VCOM (V)</th><th>A[7:0]</th><th>VCOM (V)</th></tr>
<tr><td>0Fh</td><td>-0.2</td><td>5Ah</td><td>-1.7</td></tr>
<tr><td>14h</td><td>-0.3</td><td>5Fh</td><td>-1.8</td></tr>
<tr><td>19h</td><td>-0.4</td><td>64h</td><td>-1.9</td></tr>
<tr><td>1Eh</td><td>-0.5</td><td>69h</td><td>-2</td></tr>
<tr><td>23h</td><td>-0.6</td><td>6Eh</td><td>-2.1</td></tr>
<tr><td>28h</td><td>-0.7</td><td>73h</td><td>-2.2</td></tr>
<tr><td>2Dh</td><td>-0.8</td><td>78h</td><td>-2.3</td></tr>
<tr><td>32h</td><td>-0.9</td><td>7Dh</td><td>-2.4</td></tr>
<tr><td>37h</td><td>-1</td><td>82h</td><td>-2.5</td></tr>
<tr><td>3Ch</td><td>-1.1</td><td>87h</td><td>-2.6</td></tr>
<tr><td>41h</td><td>-1.2</td><td>8Ch</td><td>-2.7</td></tr>
<tr><td>46h</td><td>-1.3</td><td>91h</td><td>-2.8</td></tr>
<tr><td>4Bh</td><td>-1.4</td><td>96h</td><td>-2.9</td></tr>
<tr><td>50h</td><td>-1.5</td><td>9Bh</td><td>-3</td></tr>
<tr><td>55h</td><td>-1.6</td><td></td><td></td></tr>
</table></td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>2F</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>Status Bit Read</td><td>A[3]: Panel-Break flag [POR=0]

0: Normal
1: Broken

A[1:0] : Chip ID [POR=01]</td></tr>
<tr><td>1</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A3</td><td>0</td><td>A1</td><td>A0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>32</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Write LUT Register</td><td>Write LUT register from MCU interface [30 bytes] (excluding the VSH/VSL and Dummy bit).</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>3A</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Set Dummy Line Period</td><td>Set A[7:0] = 06h</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>3B</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Set Gate Line Width</td><td>Set A[3:0] = 0Bh</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td></td><td></td></tr>
</table>

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>3C</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td rowspan="2">Border Waveform Control</td><td rowspan="2">Select border waveform for VBD

A[7] Follow Source at Initial Update Display
A[7]=0: [POR]
A[7]=1: Follow Source at Initial Update Display for VBD, A [6:0] settings are being overridden at Initial Display STAGE.
A[6] Select GS Transition/ Fix Level for VBD
A[6]=0: Select GS Transition A[3:0] for VBD
A[6]=1: Select FIX level Setting A[5:4] for VBD [POR]
A[5:4] Fix Level Setting for VBD

<table><tr><th>A[5:4]</th><th>VBD level</th></tr><tr><td>00</td><td>VSS</td></tr><tr><td>01</td><td>VSH</td></tr><tr><td>10</td><td>VSL</td></tr><tr><td>11[POR]</td><td>HiZ</td></tr></table>
A [1:0] GS transition setting for VBD (Select waveform like data A[3:2] to data A[1:0])

<table><tr><th>A[1:0]</th><th>GSC</th><th>GSD</th></tr><tr><td>01[POR]</td><td>GS0</td><td>GS1</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>0</td><td>0</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>44</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td rowspan="3">Set RAM X - Address Start / End position</td><td rowspan="3">Specify the start/end positions of the window address in the X direction by an address unit

A[4:0]: X-Start, POR = 00h
B[4:0]: X-End, POR = 12h</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td>0</td><td>0</td><td>45</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td rowspan="3">Set Ram Y- Address Start / End position</td><td rowspan="3">Specify the start/end positions of the window address in the Y direction by an address unit

A[7:0]: Y-Start, POR = 00h
B[7:0]: Y-End, POR = F9h</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td>0</td><td>0</td><td>4E</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td rowspan="2">Set RAM X - Address Counter</td><td rowspan="2">Make initial settings for the RAM X address in the address counter (AC) A[4:0] : POR is 00h</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>4F</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td rowspan="2">Set RAM Y - Address Counter</td><td rowspan="2">Make initial settings for the RAM Y address in the address counter (AC) A[7:0] : POR is 00h</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
</table>

10. Absolute Maximum Rating

Symbol	Parameter	Rating	Unit
V_{CI}	Logic Supply Voltage	-0.5 to +4.0	V
V_{IN}	Logic Input Voltage	-0.5 to V_{DDIO}+0.5	V
V_{OUT}	Logic Output Voltage	-0.5 to V_{DDIO}+0.5	V
T_{OPR}	Operation Temperature Range	0 to 40	°C
T_{STG}	Storage Temperature Range	-10 to 50	°C
RH	Humidity Range	40 to 70	%
IMPORTANT: It is recommended that you use a UV protective film when operating the module in direct sunlight.			

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the DC Characteristics tables or Pin Out List section.

IMPORTANT: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

- For proper operation, it is recommended that V_{CI} be constrained to the range $V_{SS} < V_{CI}$.
- Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DDIO}), unless noted to leave open.
- This device is not radiation protected.
- Unused outputs must be left open.
- This device is light sensitive.

11. DC Characteristics

The following specifications apply for V_{SS}=0V, V_{CI}=3.0V, T_{OPR}=25°C.

Symbol	Parameter	Test Condition	Applicable Pin	Min	Typ	Max	Unit
V_{CI}	V_{CI} Operation Voltage		V_{CI}	2.4	3.0	3.7	V
V_{IH}	High-Level Input Voltage		D1 (SDIN), D0 (SCLK), CS#, D/C#, RES#, BS1	0.8V_{DDIO}			V
V_{IL}	Low-Level Input Voltage					0.2V_{DDIO}	V
V_{OH}	High-Level Output Voltage	I_{OH} = -100uA	BUSY, TOUT1	0.9V_{DDIO}			V
V_{OL}	Low-Level Output Voltage	I_{OL} = 100uA				0.1V_{DDIO}	V

12. Serial Peripheral Interface Timing

The following specifications apply for V_{SS}=0V, V_{CI}=2.4V, T_{OPR}=25ɗ.

Symbol	Parameter	Min	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	ns
t_{AS}	Address Setup Time	150	-	ns
t_{AH}	Address Hold Time	150	-	ns
t_{CSS}	Chip Select Setup Time	120	-	ns
t_{CSH}	Chip Select Hold Time	60	-	ns
t_{DSW}	Write Data Setup Time	50	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	100	-	ns
t_{CLKH}	Clock High Time	100	-	ns
t_R	Rise Time (20%-80%)	-	15	ns
t_F	Fall Time (20%-80%)	-	15	ns

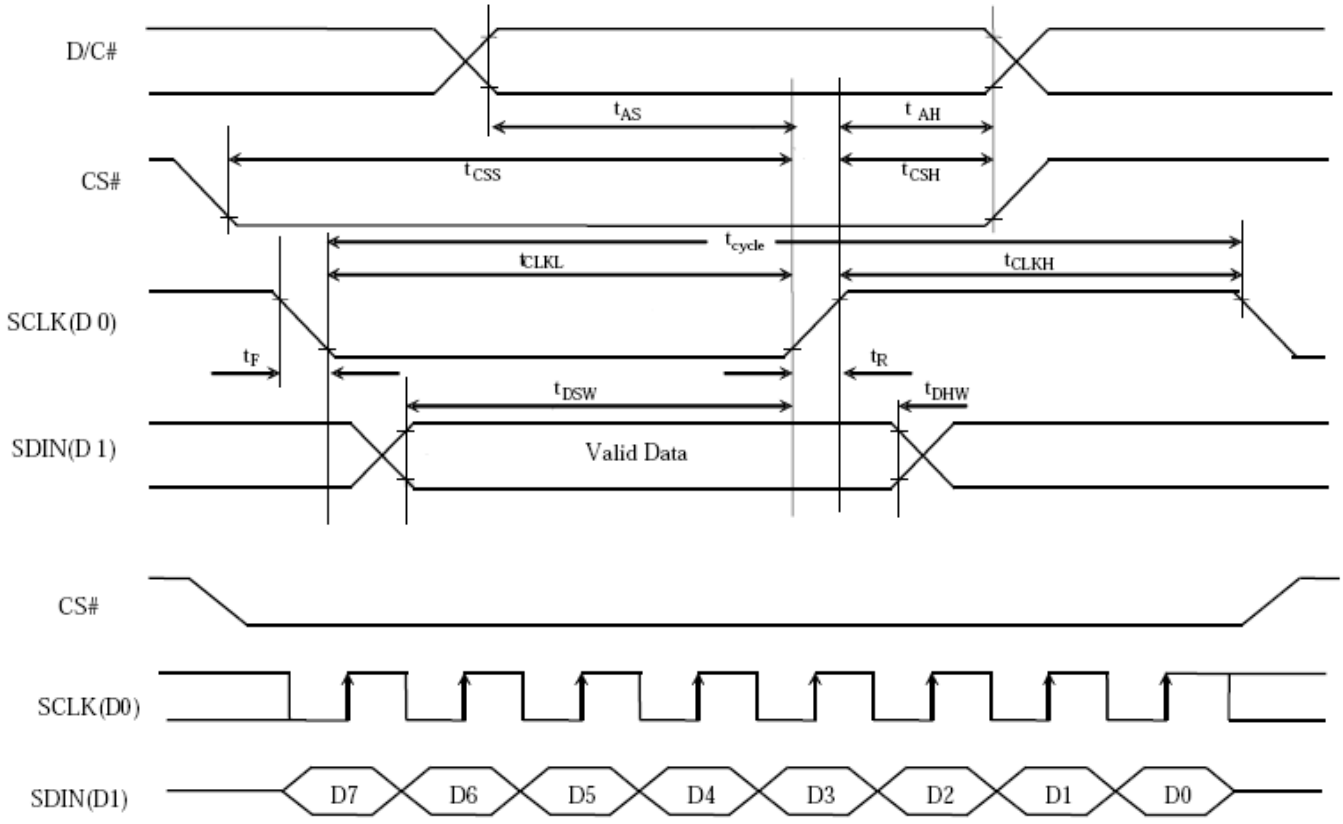
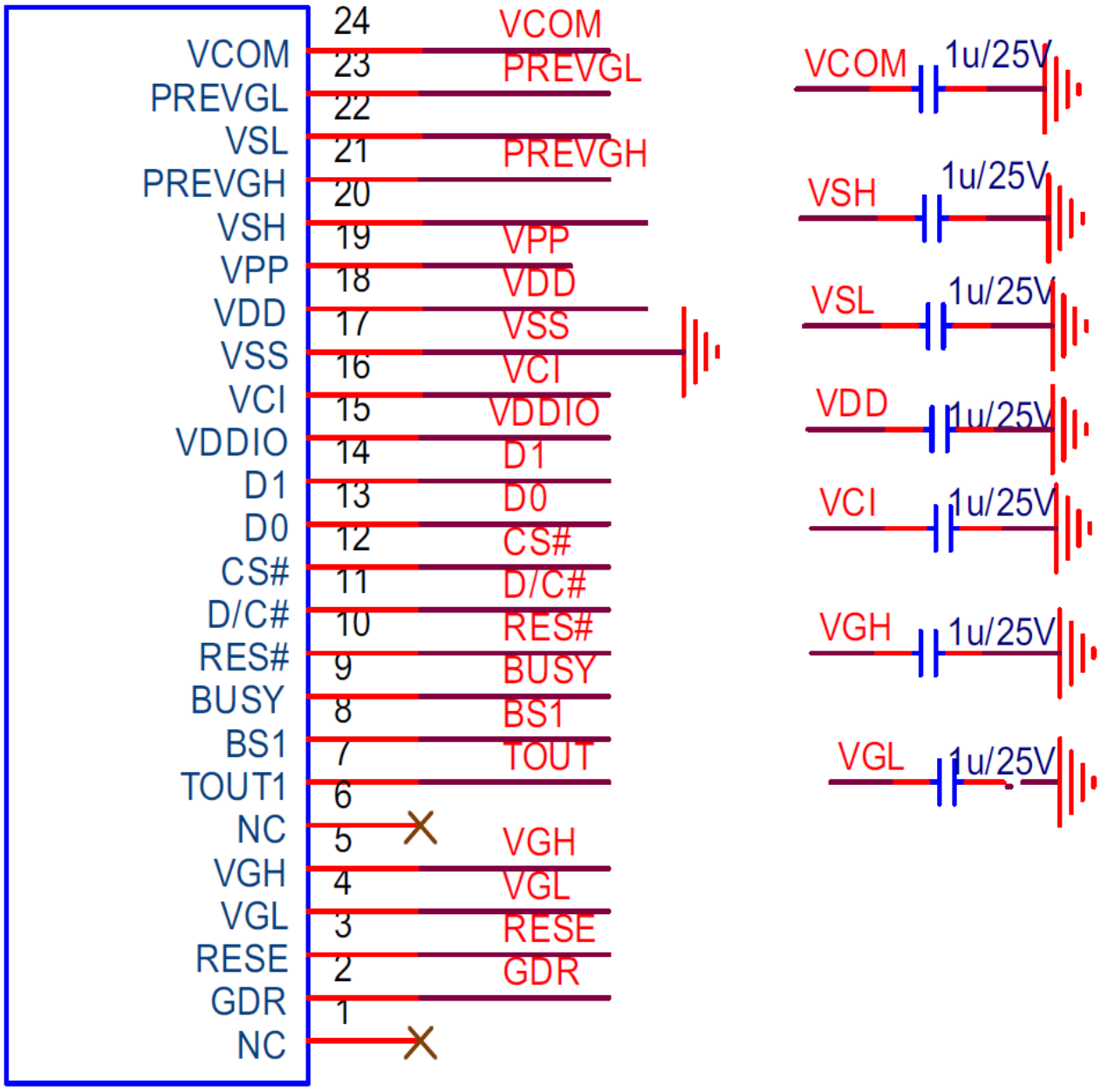


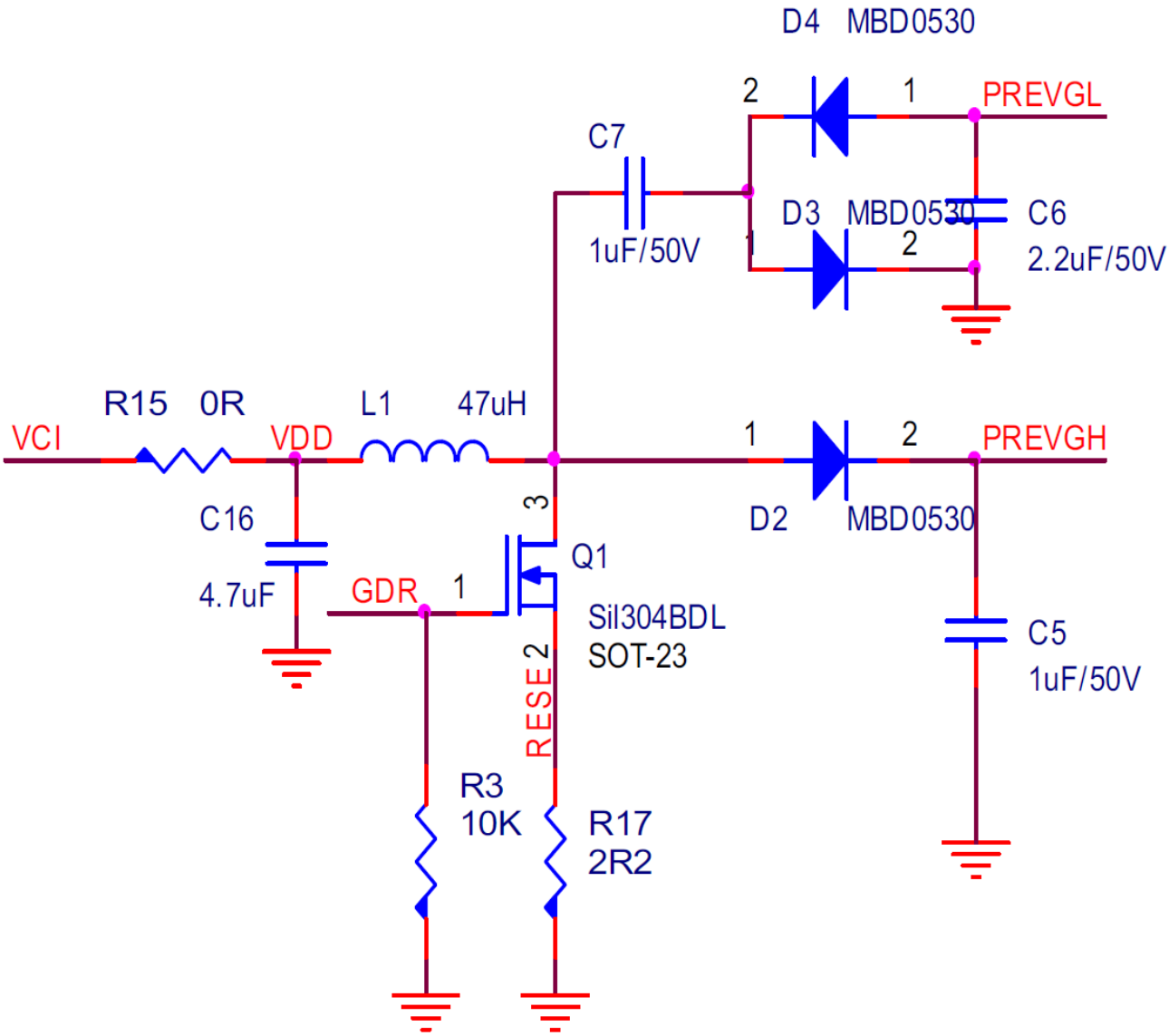
Figure 11-1: Serial Peripheral Interface Timing Characteristics

13. Power Consumption

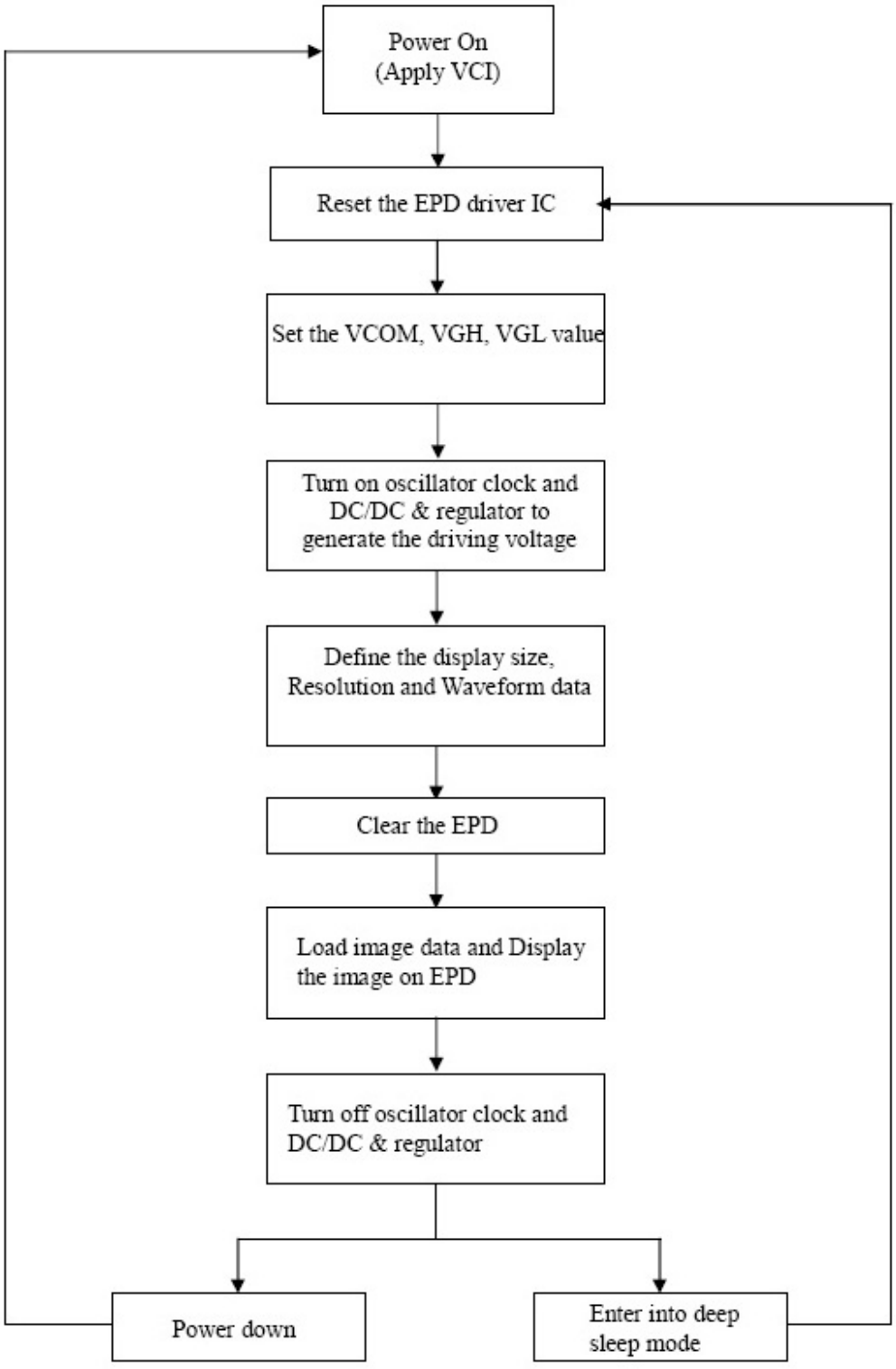
Parameter	Symbol	Conditions	Typical	Max	Unit
Panel Power Consumption During Update	-	-	26.4	40	mW
Power Consumption in Standby Mode	-	-	-	0.017	mW

14. Reference Circuit




D4 MBD0530
2
1
PREVGL
C7
1uF/50V
D3 MBD0530
1
2
C6
2.2uF/50V
R15 0R
L1 47uH
VCI
VDD
1
2
PREVGH
C16
4.7uF
3
Q1
D2 MBD0530
GDR
1
Sil304BDL
SOT-23
RESE2
C5
1uF/50V
R3
10K
R17
2R2

15. Typical Operating Sequence



16. Optical Characteristics

16.1. Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25°C

Symbol	Parameter	Conditions	Min	Typical	Max	Unit	Note
R	Reflectance	White	30	34	-	%	Note 15-1
Gn	2Gray Level	-	-	DS＋(WS-DS)×n(m-1)	-	L*	-
CR	Contrast Ratio	Indoor	7	-	-	-	-
T_{UPDATE}	Update Time	25°C	-	680	-	ms	-
Panel Life	-	0°C-40°C	-	1,000,000 times or 5 years	-	-	Note 15-2

WS: White State, DS: Dark State

Gray State from Dark to White: DS, WS

m: 2

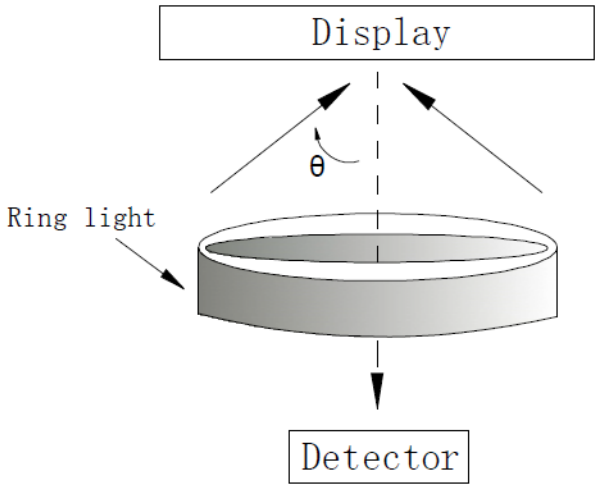
Note (15-1): Luminance Meter: Eye – One Pro Spectrophotometer
Note (15-2): Panel life is not guaranteed when working in temperatures below 0 degrees or above 40 degrees.

16.2. Definition of Contrast Ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd) ():

R1: White Reflectance Rd: Dark Reflectance

CR = R1/Rd

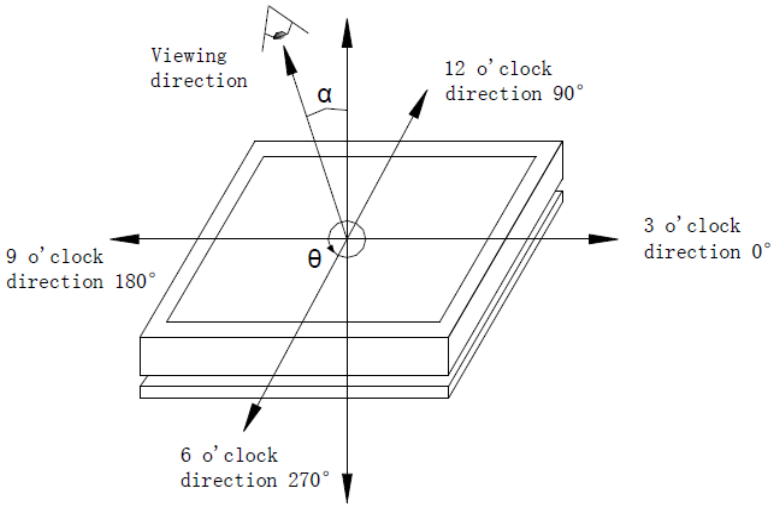


16.3. Reflection Ratio

The reflection ratio is expressed as:

$R = \text{Reflectance Factor}_{WHITE\ BOARD} \times (L_{CENTER} / L_{WHITE\ BOARD})$

L_{CENTER} is the luminance measured at center in a white area (R=G =B=1). $L_{WHITE\ BOARD}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.

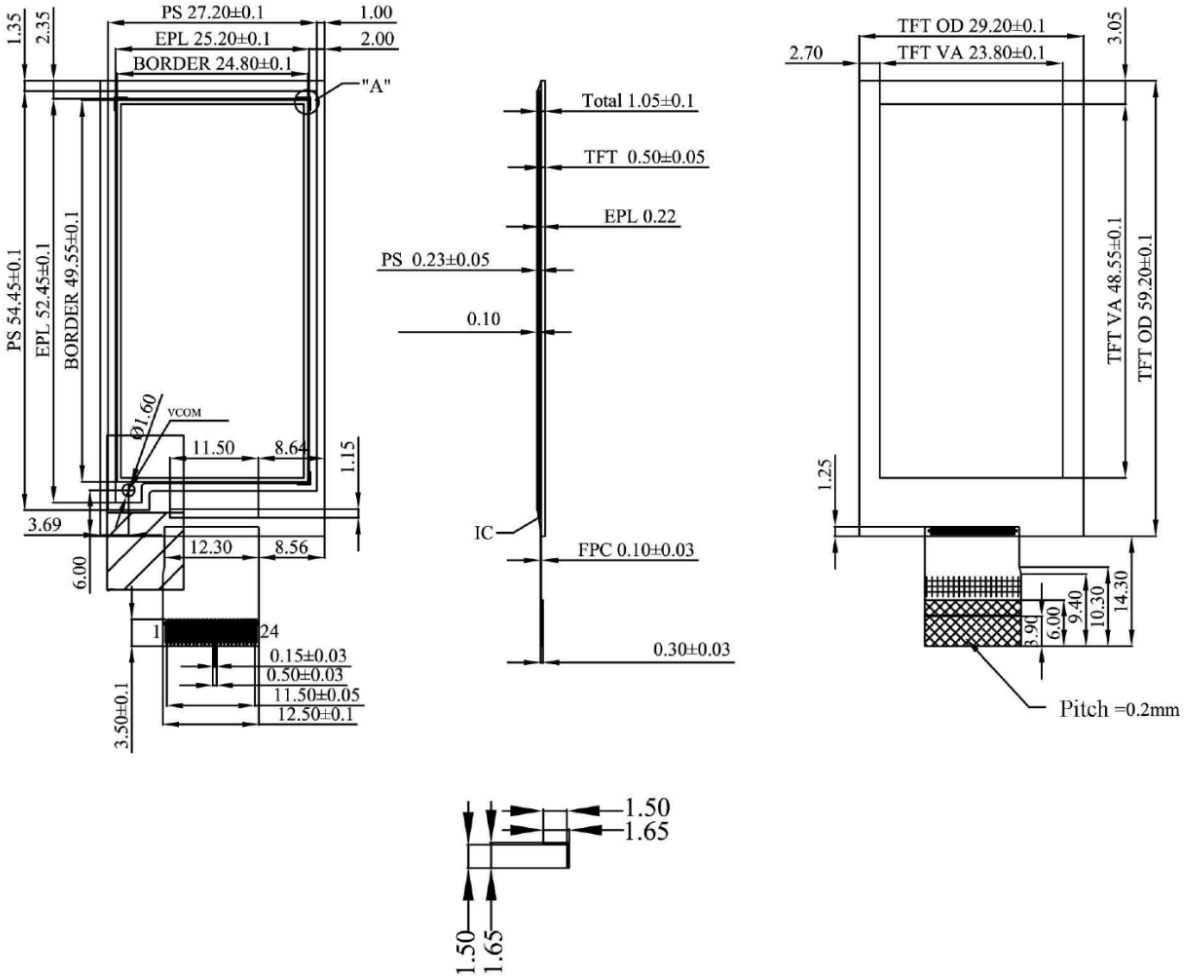


16.4. Bi-Stability

The Bi-Stability standard is as follows:

Bi-Stability	Result			
			AVG	MAX
24-Hour Luminance Drift	White State	△L*	-	3
	Black State	△L*	-	3

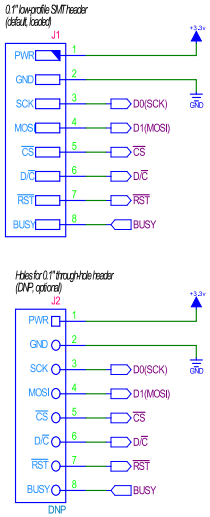
17. Mechanical Drawing

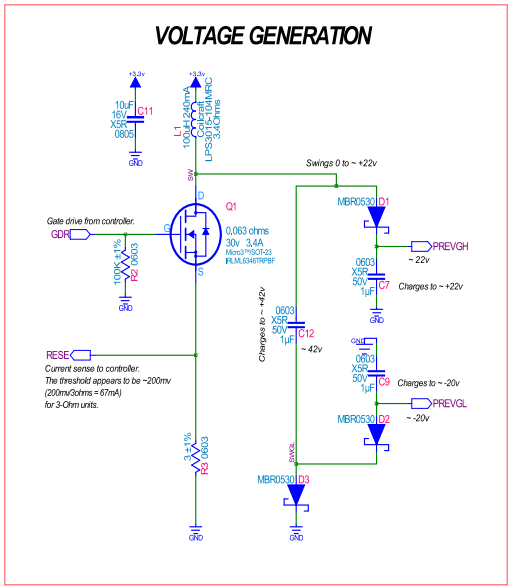


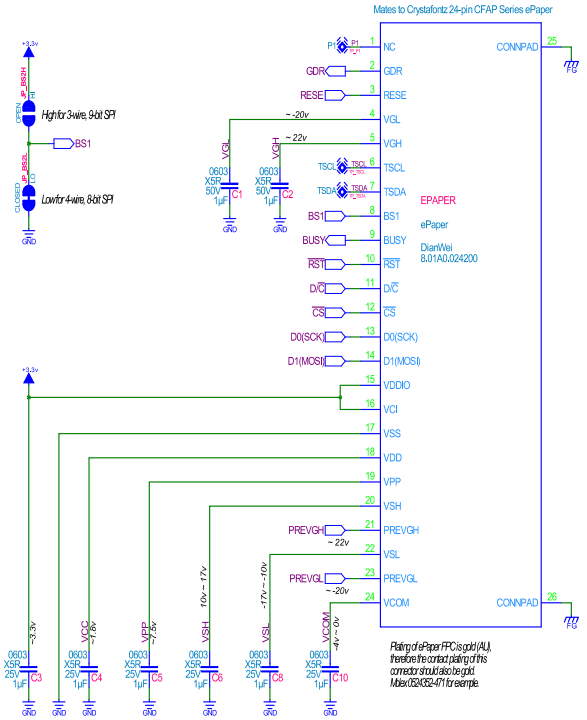
Part No.(s):	Scale:	Drawing Number:
CFAP122250A0-0213	Not to scale	CFAP122250A0-0213
	Units:	Date:
	Millimeters	2017-08-15

18. ePaper Breakout Board Schematic

REV	ENGINEER	DATE	REMARKS
0v0	BAC	2018-04-04	Initial Creation
0v1	BAC	2018-05-17	Ind val, C12 val, JP_0P47 open, CN FPC
-	-	-	-
-	-	-	-
-	-	-	-







Crystalfontz America, Inc

CFA-10084: ePaper Adapter Board 24-pin (3-ohm)

Page 1 / 1: Schematic

PRODUCT NAME:	PRODUCT REVISION:	PCB NUMBER:	PCB REVISION:
CFA-10084	0v1	PCB-10084	0v1