ePAPER DISPLAY MODULE DATASHEET

Datasheet Release 2017-08-15
for
CFAP122250A0-0213

Crystalfontz America, Inc.

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1. General Information

Datasheet Revision History
Datasheet Release Date: **2017-08-15** Datasheet for the CFAP122250A0-0213 ePaper display module.

Product Change Notifications
You can check for or subscribe to Part Change Notices for this display module on our website.

Variations
Slight variations between lots are normal (e.g., contrast, color, or intensity).

Volatility
This display module has volatile memory.

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2. Description Overview

This ePaper display is a TFT active matrix electrophoretic display with interface and a reference system design. The 2.13" active area contains 122×250 pixels and has 1-bit white/black full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM, and border are supplied with each panel.

3. Features

- High contrast
- High reflectance
- Ultra-wide viewing angle
- Ultra-low power consumption
- Pure reflective mode
- Bi-Stable Display
- Commercial temperature range
- Landscape, portrait mode
- Antiglare hard-coated front-surface
- Low current deep sleep mode
- On-chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating V_{COM}, Gate and source driving voltage
- I^2C Signal Master Interface to read external temperature sensor

4. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.13	inch	
Display Resolution	122 × 250	pixel	dpi: 112
Active Area	48.55 (H) x 23.71 (W)	mm	
Pixel Pitch	0.194 × 0.194	mm	
Pixel Configuration	Rectangle		
Outline Dimension	59.2 (H) x 29.2 (W) × 1.05 (D)	mm	
Weight (Typical)	3±0.5	g	

5. Input/Output Terminals

5.1. Pin Out List

Pin #	Type	Single	Description	Remark
1		NC	No Connection and Do Not Connect with Other NC Pins	Keep Open
2	O	GDR	N-Channel MOSFET Gate Drive Control	
3	O	RESE	Current Sense Input for the Control Loop	
4	C	VGL	Negative Gate Driving Voltage	
5	C	VGH	Positive Gate Driving Voltage	
6	-	NC	No Connection and Do Not Connect with Other NC Pins	
7	O	TOUT1	Serial Data Pin for Panel Break Detection	
8	I	BS1	Bus Selection Pin	Note 5-5
9	O	BUSY	Busy State Output Pin	Note 5-4
10	I	RES #	Reset	Note 5-3
11	I	D/C #	Data /Command Control Pin	Note 5-2
12	I	CS #	Chip Select Input Pin	Note 5-1
13	I/O	D0	Serial Clock Pin (SPI)	
14	I/O	D1	Serial Data Pin (SPI)	
15	I	VDDIO	Power for Interface Logic Pins	
16	I	VCI	Power Supply Pin for the Chip	
17		VSS	Ground	
18	C	VDD	Core Logic Power Pin	
19	C	VPP	Power Supply for OTP Programming	
20	C	VSH	Positive Source Driving Voltage	
21	C	PREVGH	Power Supply Pin for VGH and VSH	
22	C	VSL	Negative Source Driving Voltage	
23	C	PREVGL	Power Supply Pin for VCOM, VGL, and VSL	
24	C	VCOM	VCOM Driving Voltage	

Note (5-1): This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled Low.

Note (5-2): This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled Low, the data will be interpreted as command.

Note (5-3): This pin (RES#) is reset signal input. The Reset is active Low.

Note (5-4): This pin (BUSY) is Busy state output pin. When Busy is low, the operation of chip should not be interrupted and no commands should be issued to the module. The driver IC will put Busy pin low when the driver IC is working such as:

- Outputting Display Waveform; or
- Programming with OTP
- Communicating with Digital Temperature Sensor

Note (5-5): This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

6. MCU Interface

6.1. MCU Interface Selection

The IL3895 can support 3-wiUH/4-ZLUH VHULDO SHULSKHUDO LQWHUIDFH, Q WKH/3895, WKH 0&8 LQWHUIDFH L selectable by BS1 pins shown in.

MCU Interface Selection

BS1	MPU Interface
L	4-Lines Serial Peripheral Interface (SPI)
H	3-Lines Serial Peripheral Interface (SPI) – 9 bits

6.2. MCU Serial Peripheral Interface (4-Wire SPI)

The 4-Wire SPI consists of serial clock SCLK, serial data SDIN, D/C# and CS#. In SPI mode, D0 acts as SCLK and D1 acts as SDIN. The control pins status in 4-Wire SPI in writing command/data is shown in Table 6-2 and the Write Procedure 4-Wire SPI.

Table 6-2: Control Pins Status of 4-Wire SPI

Function	D0 (SCLK) Pin	D1 (SDIN) Pin	D/C# Pin	CS# Pin
Write Command	Ĺ	Command Bit	L	L
Write Data	Ĺ	Data Bit	H	L

Notes:
(1) L is connected to V_{SS} and H is connected to V_{DDIO}
(2) Ĺ stands for rising edge of signal
(3) SD_{IN} is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.

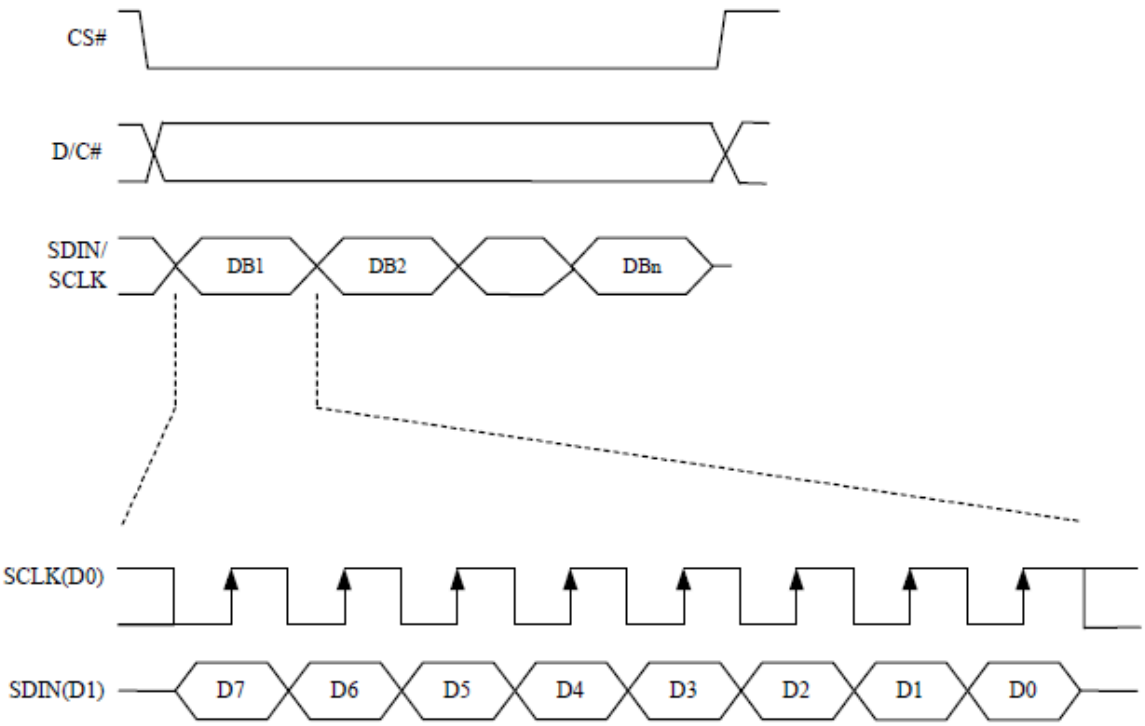


Figure 6-2: Write Procedure in 4-Wire SPI

6.3. MCU Serial Peripheral Interface (3-Wire SPI)

The 3-wire SPI consists of serial clock SCLK, serial data SDIN and CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN. The operation is similar to 4-wire SPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 6-3.

In the write operation, a 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is D/C# bit, D7 bit, D6 bit to D0 bit. The first bit is D/C# bit which determines the following byte is command or data. When D/C# bit is 0, the following byte is command. When D/C# bit is 1, the following byte is data.

Table 6-3 Shows the Write Procedure in 3-Wire SPI

Function	SCLK Pin	SDIN Pin	D/C# Pin	CS# Pin
Write Command	Ĺ	Command Bit	L	L
Write Data	Ĺ	Data Bit	H	L

Note: "L" is connected to V_{SS}. "H" is connected to V_{DDIO}. "Ĺ" stands for rising edge of signal.

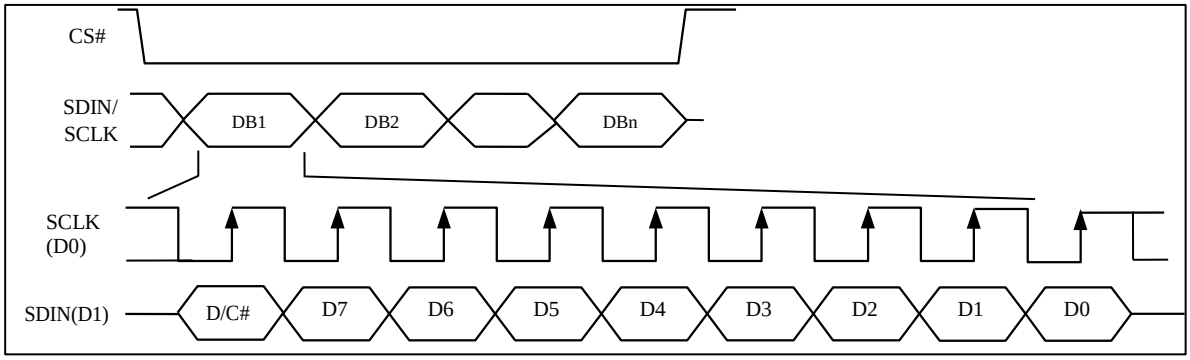


Figure 6-3: Control Pins Status of 3-Wire SPI

7. Temperature Register Mapping

If the temperature value MSByte bit D11 = 0, then

The temperature is positive and value (DegC) = + (Temperature value) / 16

If the temperature value MSByte bit D11 = 1, then

The temperature is negative and value (DegC) = ~ (2's complement of temperature value) / 16

12-bit binary (2's complement)	Hexadecimal Value	Decimal Value	Value [DegC]
0111 1111 0000	7F0	2032	127
0111 1110 1110	7EE	2030	126.875
0111 1110 0010	7E2	2018	126.125
0111 1101 0000	7D0	2000	125
0001 1001 0000	190	400	25
0000 0000 0010	002	2	0.125
0000 0000 0000	000	0	0
1111 1111 1110	FFE	-2	-0.125
1110 0111 0000	E70	-400	-25
1100 1001 0010	C92	-878	-54.875
1100 1001 0000	C90	-880	-55

8. Panel Break Detection

The panel break detection function is used to detect the breakage at panel edge. When the panel break detection command is issued, the panel break detection will be executed. During the detection period, BUSY output is at high level. BUSY output is at low level when the detection is completed. Then, the user can issue the Status Bit Read command to check the status bit for the result of the panel break.

9. Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	01	0	0	0	0	0	0	0	1	Driver Output Control	Set the number of gate. Setting for 232 gates is: Set A[7:0] = F9h Set B[7:0] = 00h
0	1	-	A7	A6	A5	A4	A3	A2	A1	A0		
0	1	-	0	0	0	0	0	B2	B1	B0		
0	0	03	0	0	0	0	0	0	1	1	Gate Driving Voltage Control	Set Gate driving voltage. A[4:0] = 10h [POR], VGH at 22V B[3:0] = 0Ah [POR], VGL at -20V
0	1	-	0	0	0	A4	A3	A2	A1	A0		
0	1	-	0	0	0	0	B3	B2	B1	B0		
0	0	04	0	0	0	0	0	1	0	0	Source Driving Voltage Control	Set Source output voltage. A[4:0] = 19h [POR], VSH/VSL at +/-15V
0	1	-	0	0	0	A4	A3	A2	A1	A0		
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep Mode	Deep Sleep Mode Control A[0] – Description 0 – Normal Mode [POR] 1 – Enter Deep Sleep Mode
0	1	-	0	0	0	0	0	0	0	A0		
0	0	11	0	0	0	1	0	0	0	1	Data Entry Mode Setting	Define data entry sequence. A[1:0] = ID[1:0] Address automatic increment / decrement setting. The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00-Y decrement, X decrement, 01-Y decrement, X increment, 10-Y increment, X decrement, 11-Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data is written to the RAM. When AM = 0, the address counter is updated in the X direction. [POR] When AM = 1, the address counter is updated in the Y direction.
0	1	-	0	0	0	0	0	A2	A1	A0		

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	12	0	0	0	1	0	0	1	0	SWRESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode. **Note**: RAM is unaffected by this command.
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to Temperature Register)	Write to Temperature Register. A[7:0] MSByte 01111111[POR] B[7:0] LSByte 11110000[POR]
0	1	-	A7	A6	A5	A4	A3	A2	A1	A0		
0	1	-	B7	B6	B5	B4	0	0	0	0		
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence. The Display Update Sequence Option is located at R22h. User should not interrupt this operation to avoid corruption of panel images.
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	Option for Display Update Bypass Option used for Pattern Display, which is used for display the RAM content into the Display. OLD RAM Bypass option A[7] A[7] = 1: Enable bypass A[7] = 0: Disable bypass [POR] A[4] value will be used as New RAM for bypass. A[4] = 0 [POR] A[1:0] Initial Update Option - Source Control A[1:0] | GSA | GSB 01[POR] | GS0 | GS1
0	1	-	A7	A6	A5	A4	A3	A2	A1	A0		

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation
0	1	-	A7	A6	A5	A4	A3	A2	A1	A0		

Parameter (in Hex)	
Enable Clock Signal, Then Enable Analog Then Load LUT Then INIITIAL DISPLAY Then PATTERN DISPLAY Then Disable Analog Then Disable OSC	FF [POR]
Setting for LUT from OTP Enable Clock Signal, Then Enable Analog Then Load LUT Then PATTERN DISPLAY Then Disable Analog Then Disable OSC	D7
Setting for LUT from MCU Enable Clock Signal, Then Enable Analog Then PATTERN DISPLAY Then Disable Analog Then Disable OSC	C7

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	23	0	0	1	0	0	0	1	1	Panel Break Detection	After this command is issued, panel break detection will start. The status can be checked by Command 2Fh. During detection, BUSY pad will output high. The command required CLKEN=1.
0	0	24	0	0	1	0	0	1	0	0	Write RAM	After this command, data entries will be written into the RAM until another command is written. Address pointers will advance accordingly.
0	0	2C	0	0	1	0	1	0	1	1	Write VCOM Register	Write VCOM Register from MCU Interface
0	1	-	A7	A6	A5	A4	A3	A2	A1	A0		

A[7:0]	VCOM (V)	A[7:0]	VCOM (V)
0Fh	-0.2	5Ah	-1.7
14h	-0.3	5Fh	-1.8
19h	-0.4	64h	-1.9
1Eh	-0.5	69h	-2
23h	-0.6	6Eh	-2.1
28h	-0.7	73h	-2.2
2Dh	-0.8	78h	-2.3
32h	-0.9	7Dh	-2.4
37h	-1	82h	-2.5
3Ch	-1.1	87h	-2.6
41h	-1.2	8Ch	-2.7
46h	-1.3	91h	-2.8
4Bh	-1.4	96h	-2.9
50h	-1.5	9Bh	-3
55h	-1.6		

0	0	2F	0	0	1	0	1	0	0	1	Status Bit Read	A[3]: Panel-Break flag (POR=0) 0: Normal 1: Broken A[1:0] : Chip ID (POR=01)
1	1	-	0	0	0	0	A3	0	A1	A0		
0	0	32	0	0	1	1	0	0	1	0	Write LUT Register	Write LUT register from MCU interface [30 bytes] (excluding the VSH/VSL and Dummy bit).
0	1	-	A7	A6	A5	A4	A3	A2	A1	A0		
0	1	-	B7	B6	B5	B4	B3	B2	B1	B0		
0	1	-	:	:	:	:	:	:	:	:		
0	1	-	.	.	.	.	.	.	.	.		

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - Address Start / End Position	Specify the start/end positions of the window address in the X direction by an address unit A[4:0]: X-Start, POR = 00h B[4:0]: X-End, POR = 12h
0	1	-	0	0	0	A4	A3	A2	A1	A0		
0	1	-	0	0	0	B4	B3	B2	B1	B0		
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- Address Start / End Position	Specify the start/end positions of the window address in the Y direction by an address unit A[7:0]: Y-Start, POR = 00h B[7:0]: Y-End, POR = F9h
0	1	-	A7	A6	A5	A4	A3	A2	A1	A0		
0	1	-	B7	B6	B5	B4	B3	B2	B1	B0		
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X - Address Counter	Make initial settings for the RAM X address in the address counter (AC) A[4:0] : POR is 00h
0	1	-	0	0	0	A4	A3	A2	A1	A0		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y - Address Counter	Make initial settings for the RAM Y address in the address counter (AC) A[7:0] : POR is 00h
0	1	-	A7	A6	A5	A4	A3	A2	A1	A0		
0	0	3A	0	0	1	1	1	0	1	0	Set Dummy Line Period	Set A[7:0] = 06h
0	1	-	0	A6	A5	A4	A3	A2	A1	A0		
0	0	3B	0	0	1	1	1	0	1	1	Set Gate Line Width	Set A[3:0] = 0Bh
0	1	-	0	0	0	0	A3	A2	A1	A0		

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>3C</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td rowspan="2">Border Waveform Control</td><td rowspan="2">Select border waveform for VBD

A[7] Follow Source at Initial Update Display
A[7]=0: [POR]
A[7]=1: Follow Source at Initial Update Display for VBD, A [6:0] settings are being overridden at Initial Display STAGE.
A[6] Select GS Transition/ Fix Level for VBD
A[6]=0: Select GS Transition A[3:0] for VBD
A[6]=1: Select FIX level Setting A[5:4] for VBD [POR]
A[5:4] Fix Level Setting for VBD

<table><tr><th>A[5:4]</th><th>VBD level</th></tr><tr><td>00</td><td>VSS</td></tr><tr><td>01</td><td>VSH</td></tr><tr><td>10</td><td>VSL</td></tr><tr><td>11[POR]</td><td>HiZ</td></tr></table>
A [1:0] GS transition setting for VBD (Select waveform like data A[3:2] to data A[1:0])

<table><tr><th>A[1:0]</th><th>GSC</th><th>GSD</th></tr><tr><td>01[POR]</td><td>GS0</td><td>GS1</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>0</td><td>0</td><td>A1</td><td>A0</td></tr>
</table>

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - Address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit A[4:0]: X-Start, POR = 00h B[4:0]: X-End, POR = 12h
0	1	-	0	0	0	A4	A3	A2	A1	A0		
0	1	-	0	0	0	B4	B3	B2	B1	B0		
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- Address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit A[7:0]: Y-Start, POR = 00h B[7:0]: Y-End, POR = F9h
0	1	-	A7	A6	A5	A4	A3	A2	A1	A0		
0	1	-	B7	B6	B5	B4	B3	B2	B1	B0		
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X - Address Counter	Make initial settings for the RAM X address in the address counter (AC) A[4:0] : POR is 00h
0	1	-	0	0	0	A4	A3	A2	A1	A0		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y - Address Counter	Make initial settings for the RAM Y address in the address counter (AC) A[7:0] : POR is 00h
0	1	-	A7	A6	A5	A4	A3	A2	A1	A0		

10. Absolute Maximum Rating

Symbol	Parameter	Rating	Unit
V_{CI}	Logic Supply Voltage	-0.5 to +4.0	V
V_{IN}	Logic Input Voltage	-0.5 to V_{DDIO}+0.5	V
V_{OUT}	Logic Output Voltage	-0.5 to V_{DDIO}+0.5	V
T_{OPR}	Operation Temperature Range	0 to 40	°C
T_{STG}	Storage Temperature Range	-10 to 50	°C
RH	Humidity Range	40~70	%
IMPORTANT: It is recommended that you use a UV protective film when operating the module in direct sunlight.			

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the DC Characteristics tables or Pin Out List section.

IMPORTANT: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

- For proper operation, it is recommended that V_{CI} be constrained to the range $V_{SS} < V_{CI}$.
- Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DDIO}).
- Caution should be taken to avoid exposure of this device to any light source during normal operation.
- This device is not radiation protected.
- Unused outputs must be left open.
- This device is light sensitive.

11. DC Characteristics

The following specifications apply for V_{SS}=0V, V_{CI}=3.0V, T_{OPR}=25ď.

Symbol	Parameter	Test Condition	Applicable Pin	Min	Typ	Max	Unit
V_{CI}	V_{CI} Operation Voltage		V_{CI}	2.4	3.0	3.7	V
V_{IH}	High-Level Input Voltage		D1 (SDIN), D0 (SCLK), CS#, D/C#, RES#, BS1	$0.8V_{DDIO}$			V
V_{IL}	Low-Level Input Voltage					$0.2V_{DDIO}$	V
V_{OH}	High-Level Output Voltage	I_{OH} = -100uA	BUSY, TOUT1	$0.9V_{DDIO}$			V
V_{OL}	Low-Level Output Voltage	I_{OL} = 100uA				$0.1V_{DDIO}$	V

12. Serial Peripheral Interface Timing

The following specifications apply for V_{SS}=0V, V_{CI}=2.4V, T_{OPR}=25ď.

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time (20%-80%)	-	-	15	ns
t_F	Fall Time (20%-80%)	-	-	15	ns

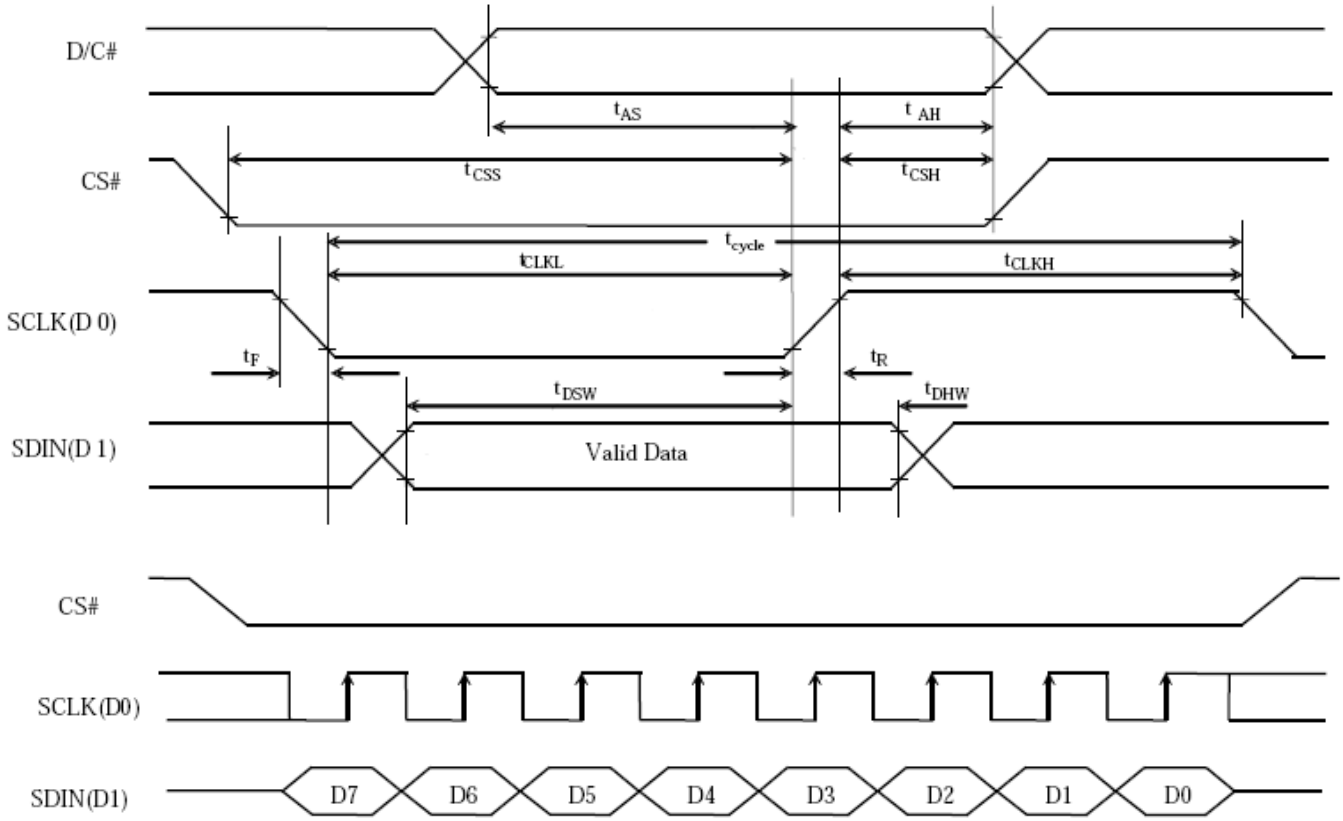
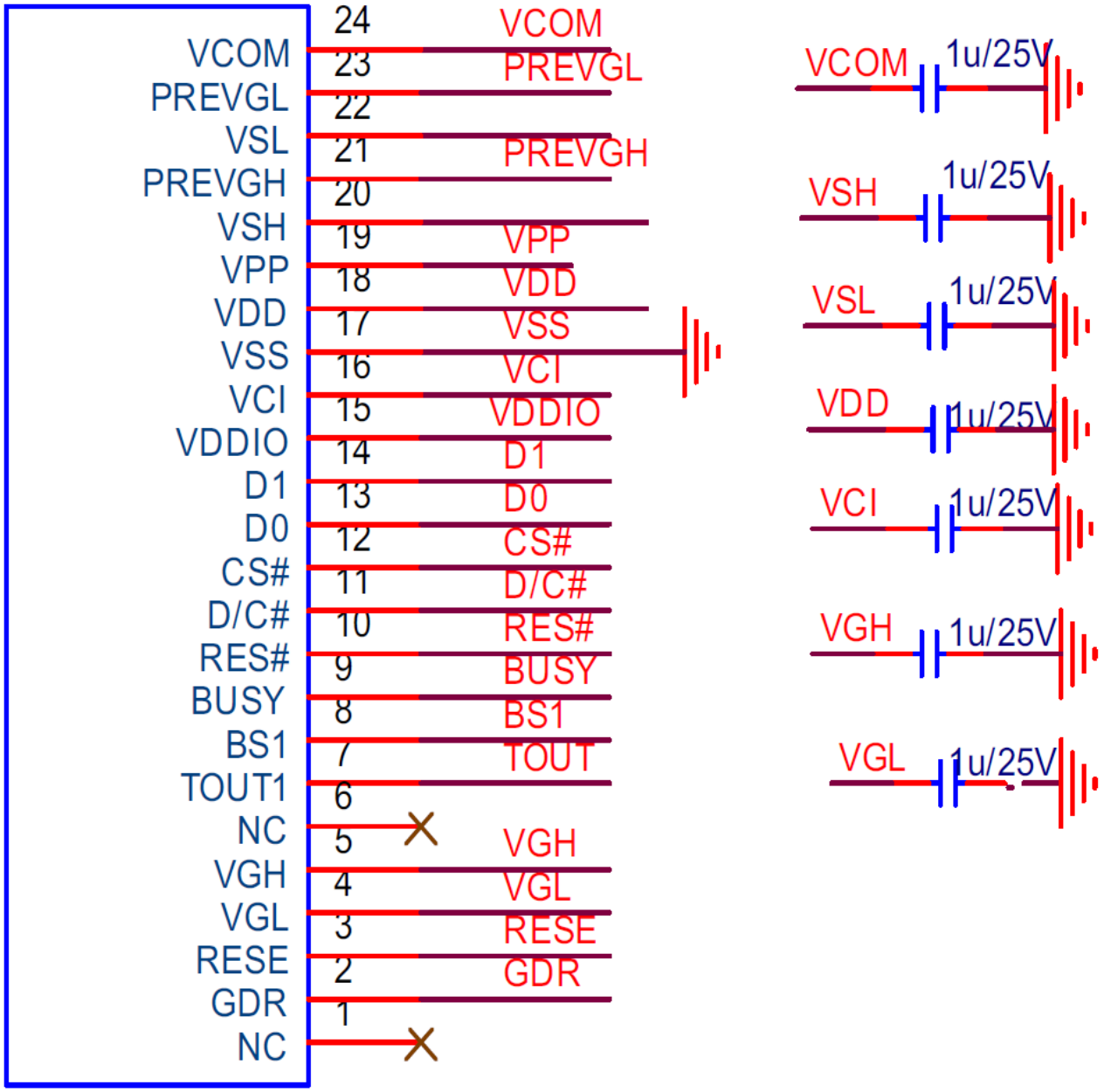


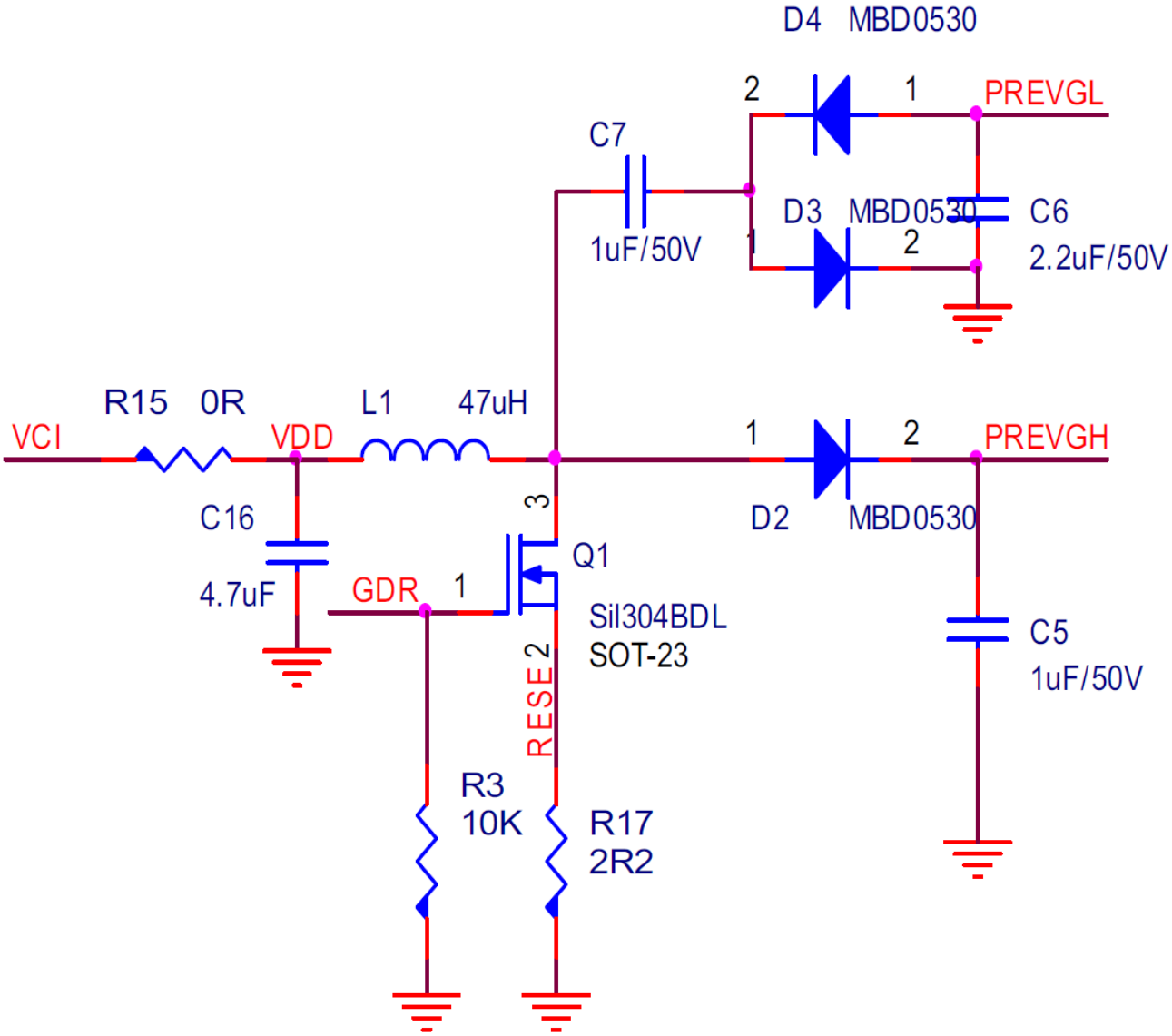
Figure 11-1: Serial Peripheral Interface Characteristics

12.1. Power Consumption

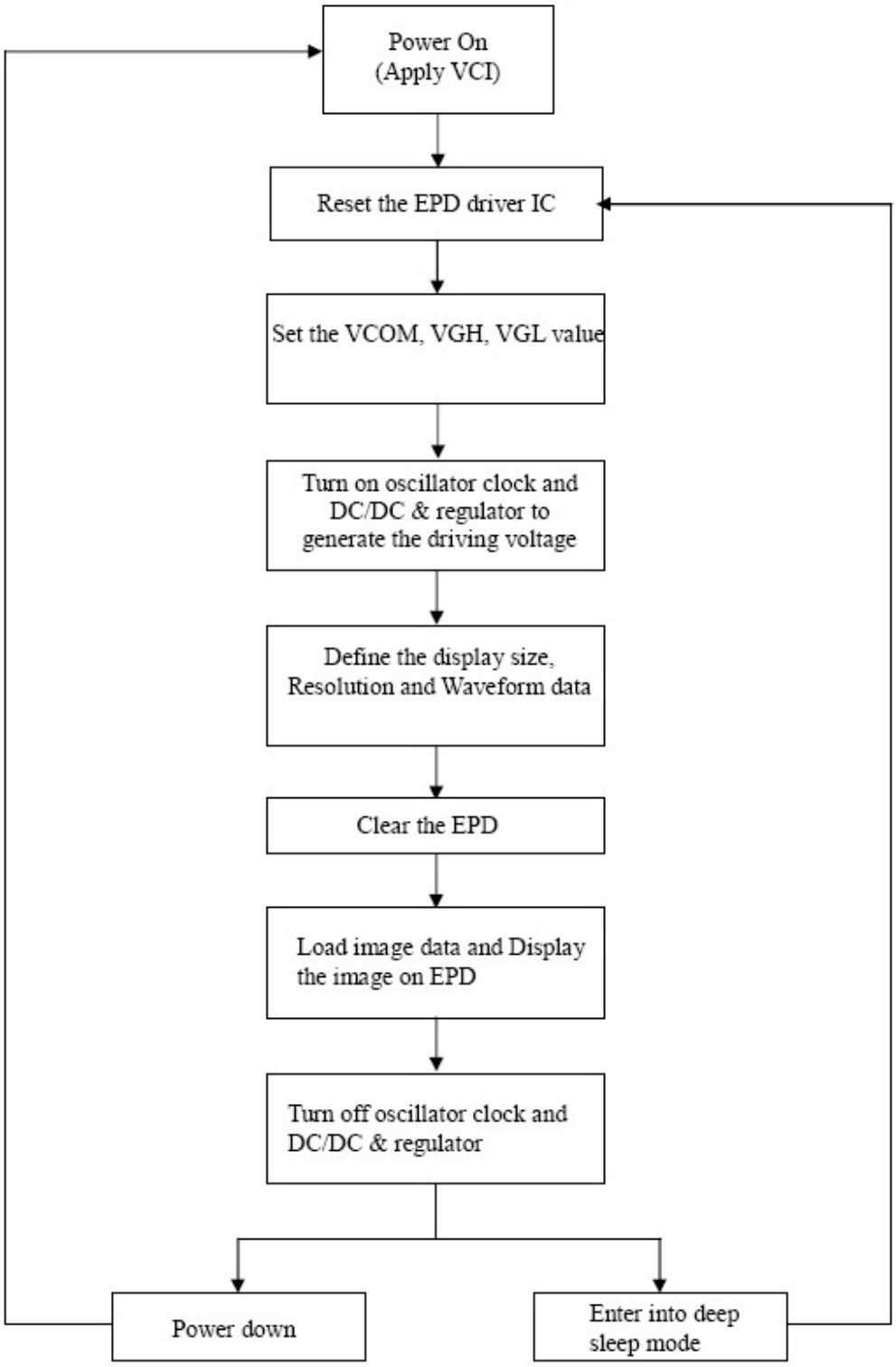
Parameter	Symbol	Conditions	Typical	Max	Unit
Panel Power Consumption During Update	-	-	26.4	40	mW
Power Consumption in Standby Mode	-	-	-	0.017	mW

13. Reference Circuit




D4 MBD0530
2
1
PREVGL
C7
1uF/50V
D3 MBD0530
C6
2.2uF/50V
1
2
R15 0R
L1 47uH
VCI
VDD
1
2
PREVGH
C16
4.7uF
3
Q1
D2 MBD0530
GDR
1
Sil304BDL
SOT-23
C5
1uF/50V
RESE2
R3
10K
R17
2R2

14. Typical Operating Sequence



15. Optical Characteristics

15.1. Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25°C

Symbol	Parameter	Conditions	Min	Typical	Max	Unit	Note
R	Reflectance	White	30	34	-	%	Note 15-1
Gn	2Gray Level	-	-	DS＋(WS-DS)×n(m-1)	-	L*	-
CR	Contrast Ratio	Indoor	7		-	-	-
T_{UPDATE}	Update Time	25℃	-	680 ms	-	sec	-
Panel Life	-	0°C~40°C	-	1,000,000 times or 5 years	-	-	Note 15-2

WS: White State, DS: Dark State

Gray State from Dark to White: DS, WS

m: 2

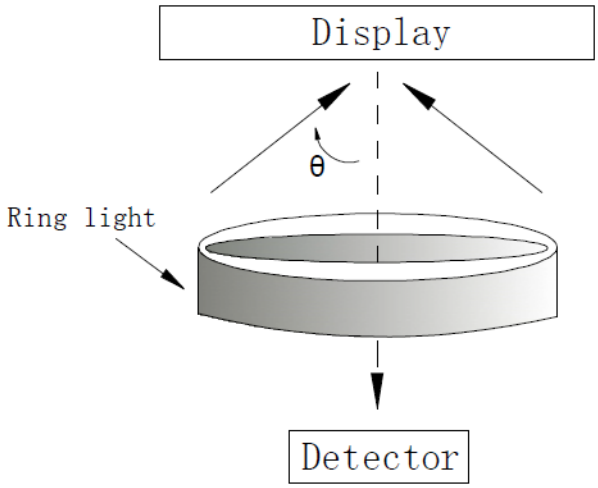
Note (15-1): Luminance Meter: Eye – One Pro Spectrophotometer
Note (15-2): Panel life is not guaranteed when working in temperatures below 0 degrees or above 40 degrees.

15.2. Definition of Contrast Ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd) ():

R1: White Reflectance Rd: Dark Reflectance

CR = R1/Rd

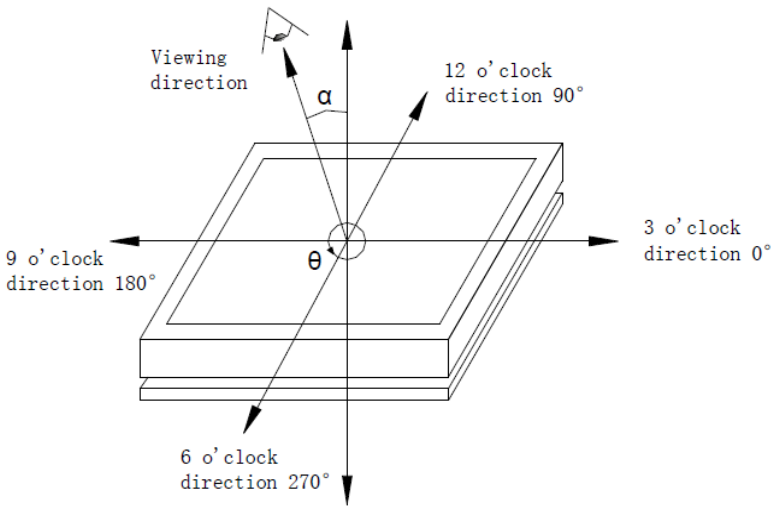


15.3. Reflection Ratio

The reflection ratio is expressed as:

R = Reflectance Factor $_{WHITE\ BOARD}$ x (L_{CENTER} / $L_{WHITE\ BOARD}$)

L_{CENTER} is the luminance measured at center in a white area (R=G =B=1). $L_{WHITE\ BOARD}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.

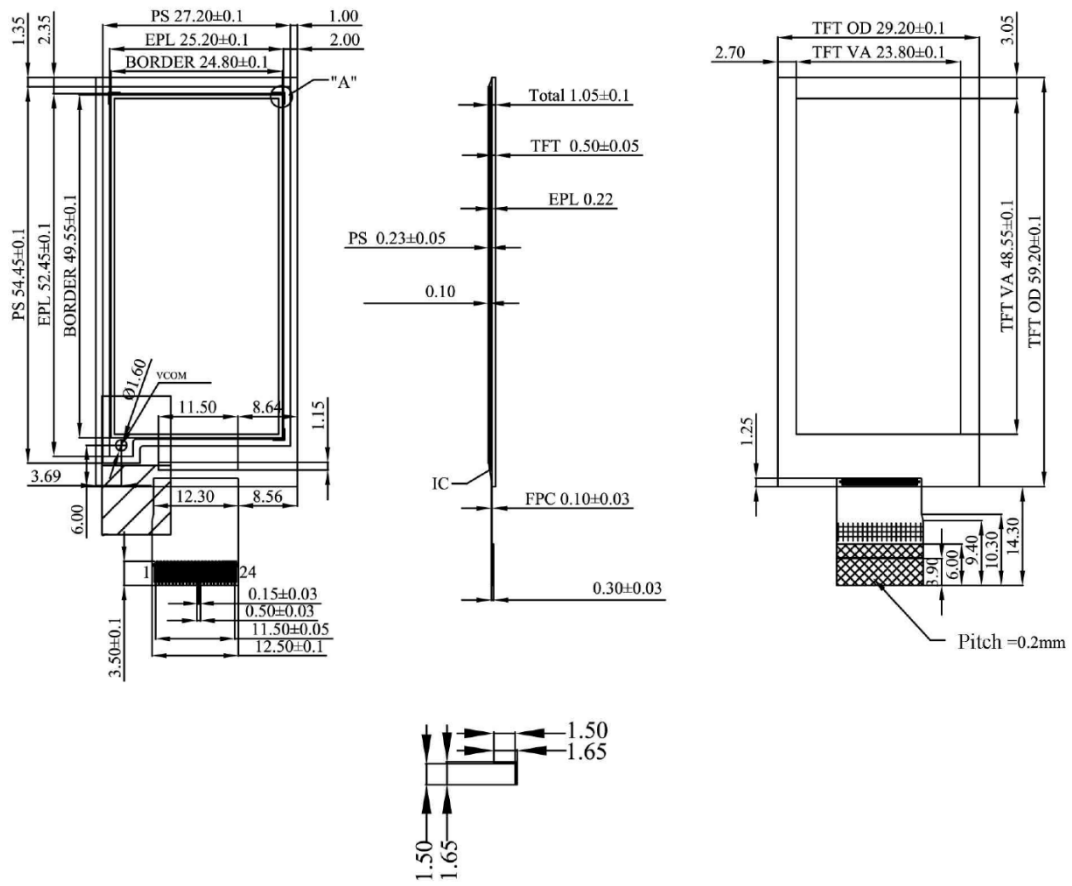


15.4. Bi-Stability

The Bi-Stability standard is as follows:

Bi-Stability	Result			
			AVG	MAX
24-Hour Luminance Drift	White State	△L*	-	3
	Black State	△L*	-	3

16. Mechanical Drawing



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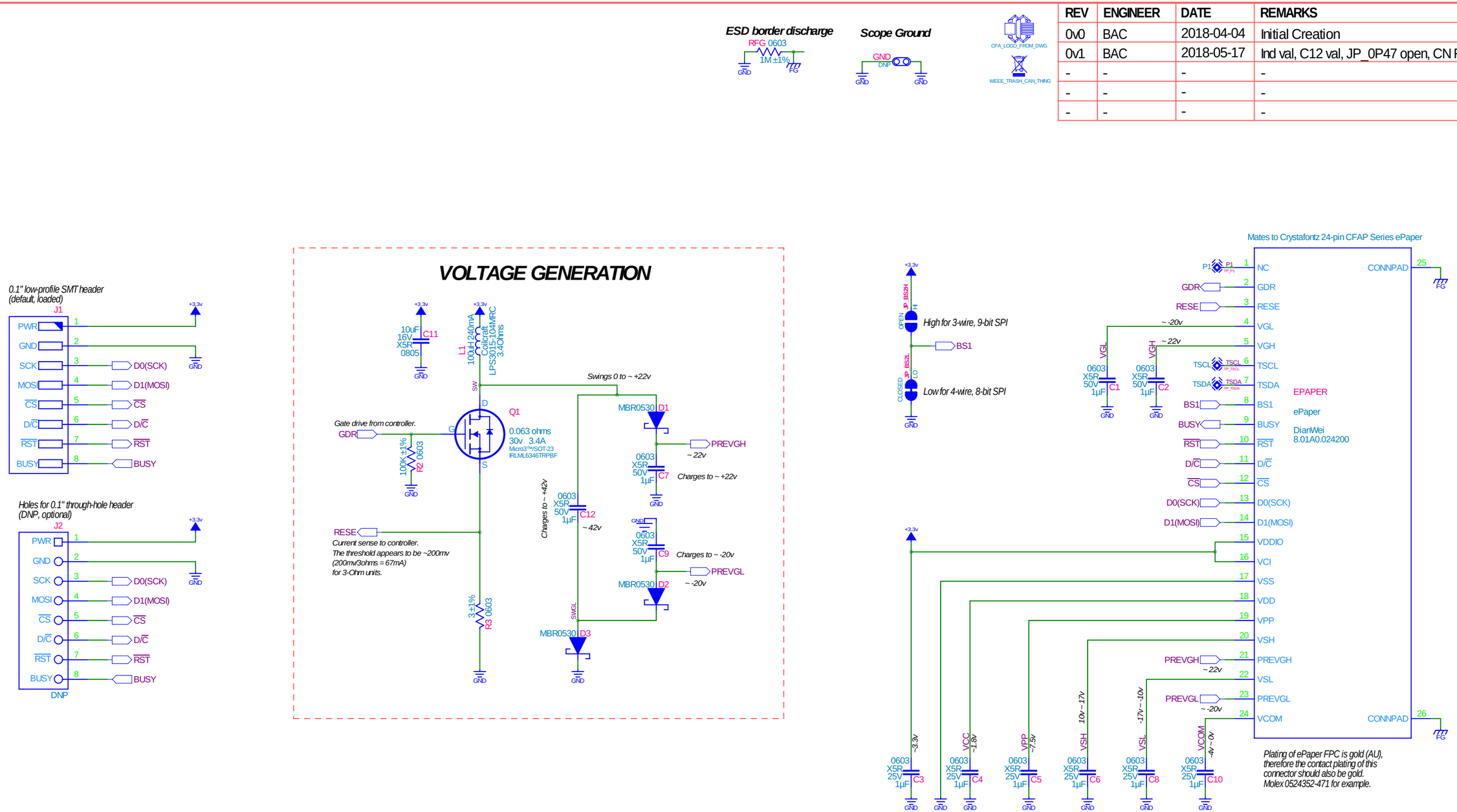
		Units: Millimeters	*Date:* 2017-08-15

REV	ENGINEER	DATE	REMARKS
0v0	BAC	2018-04-04	Initial Creation
0v1	BAC	2018-05-17	Ind val, C12 val, JP_0P47 open, CN FPC
-	-	-	-
-	-	-	-
-	-	-	-



Crystalfontz America, Inc.

CFA-10084: ePaper Adapter Board 24-pin (3-ohm)

Page 1/1: Schematic

PRODUCT NAME:	PRODUCT REVISION:	PCB NUMBER:	PCB REVISION:
CFA-10084	0v1	PCB-10084	0v1