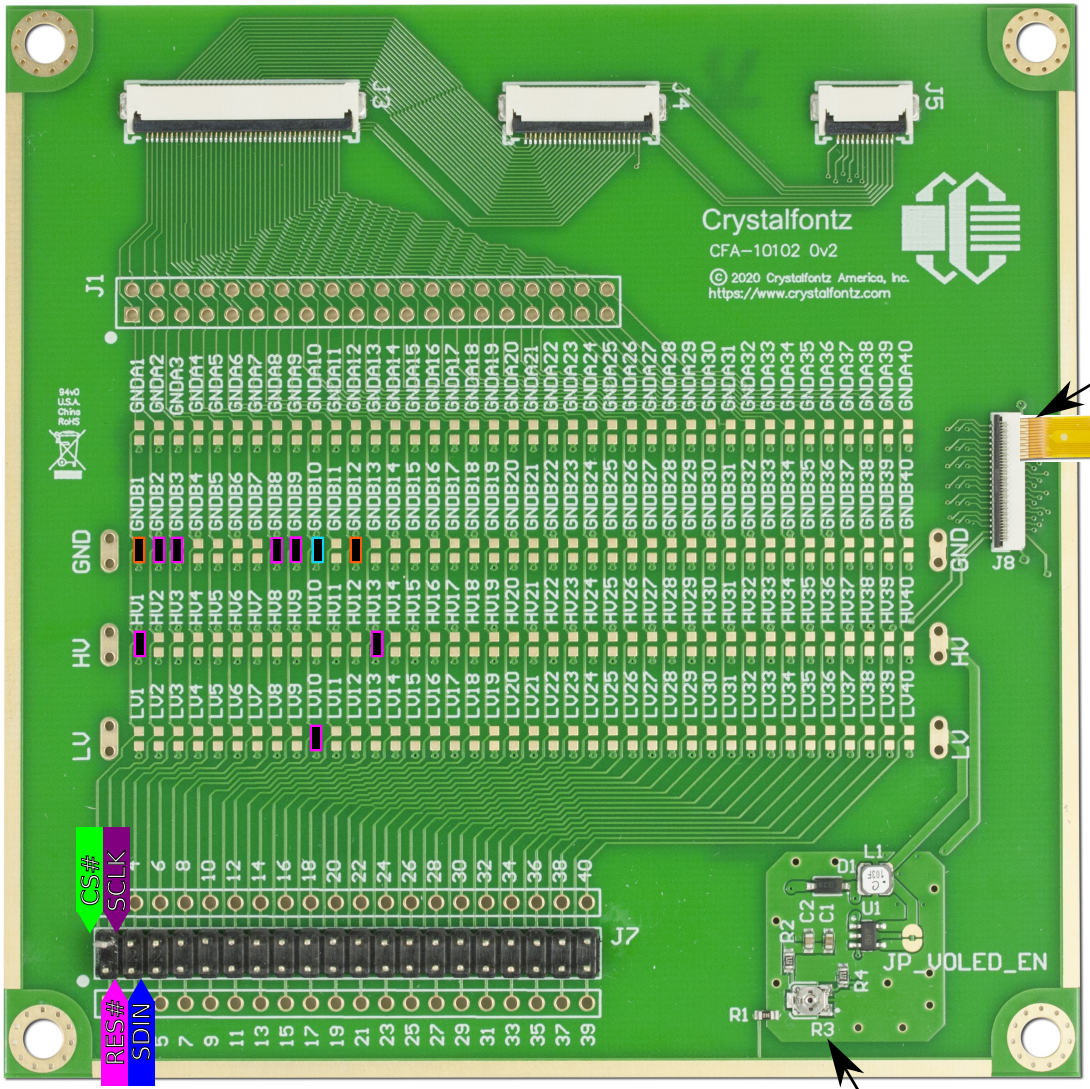
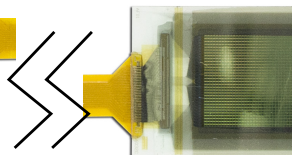
Getting Started Guide

Bring up the Flexible OLED CFAL16032A0-018P-W using the Generic Adapter Board CFA10102

The CFA10102 is a generic breakout board with three different electrical loops - low voltage, high voltage (controlled by the variable resistor),and ground (GNDA and GNDB are electrically connected). By soldering 0603 components on the land patterns as specified below, the required circuit the dispay can easily be created.



Carefully align the ZIF tail to the top of the ZIF connector and close the connector.



Color Guide

- 0Ω Resistor
- 2.2uF Capacitor
- 1uF Capacitor

Connect logic pins to a
3.3v logic level controller.
3.3v must be connected to the LV loop
GND must be connected to the GND loop

Adjust the high voltage using the potentiometer. The panel voltage should be set to 12 volts.

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Pin	Symbol	J7 on CFA10102	Function
1	VCC	0Ω to HV 2.2uF to GNDB	**Power Supply** Connect this pin the to high voltage loop using a solder blob or 0 ohm resistor. Check that the HV loop is set to 12v (adjust using R3). For reliability add capacitors between pin and ground.
2	VLSS	GNDB	**Ground of Analog Circuit** This is an analog ground pin. Connect to one of the ground circuits
3	VSS	GNDB	**Ground of Logic Circuit** This is a ground pin. It acts as a reference for the logic pins. Connect to one of the ground circuits
4	CS#	Connect to MCU	**Chip Select** This pin is the chip select input. The chip is enabled for communication only when CS# is pulled low. Connect to
5	RES#	Connect to MCU	**Power Reset for Controller and Driver** This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pulled high during normal operation.
6	SCLK	Connect to MCU	**Serial Clock Input Signal** The transmission of information in the bus is low, initialization of the chip is executed. Keep this pin pulled high during normal operation.
7	SDIN	Connect to MCU	**Serial Data Input Signal** This pin acts as a communication channel. The input data through SDIN are latched at the rising edge of SCLK in the sequence of MSB first and converted to 8-bit parallel data and handled at the rising edge of last serial clock. SDIN is identified to display data or command by D/C# bit data at the rising of the first SCLK.
8	VSS	GNDB	**Ground of Analog Circuit** This is an analog ground pin. Connect to one of the ground circuits
9	VLSS	GNDB	**Ground of Logic Circuit** This is a ground pin. It acts as a reference for the logic pins. Connect to one of the ground circuits
10	VDD	LV	**Power Supply for Logic** This is a voltage supply pin. Connect to LV loop.
11	N.C.	-	**Reserved Pin** The N.C. pins between function pins are reserved for compatible and flexible design.
12	VCOMH	2.2uF to GNDB	**Voltage Output High Level for COM Signal** This pin is the input pin for the voltage output high level for COM signals. Connect a 2.2uF capacitor to ground
13	VCC	HV	**Power Supply** Connect this pin the to high voltage loop using a solder blob or 0 ohm resistor. Check that the HV loop is set to 12v